



8K-Bit Microwire Serial EEPROM

FEATURES

- High speed operation: 3MHz @ $V_{CC} \geq 2.5V$
- Low power CMOS technology
- 1.8 to 5.5 volt operation
- Selectable x8 or x16 memory organization
- Self-timed write cycle with auto-clear
- Software write protection
- Power-up inadvertant write protection
- 1,000,000 Program/erase cycles
- 100 year data retention
- Industrial and extended temperature ranges
- Sequential read
- “Green” package option available

PIN CONFIGURATION

PDIP (L), SOIC (V)
 TSSOP (Y), TDFN (ZD4)

CS	1	8	V_{CC}
SK	2	7	NC
DI	3	6	ORG
DO	4	5	GND

PIN FUNCTION

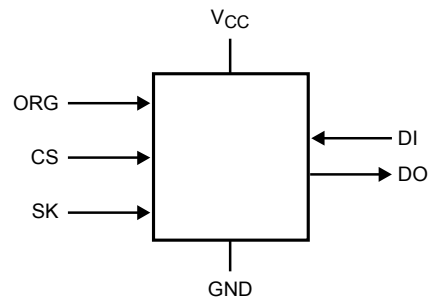
Pin Name	Function
CS	Chip Select
SK	Serial Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
ORG	Memory Organization
NC	No Connection

Note: When the ORG pin is connected to V_{CC} , x16 organization is selected. When it is connected to ground, x8 organization is selected. If the ORG pin is left unconnected, then an internal pull-up device will select x16 organization.

DESCRIPTION

The CAT93C76 is an 8K-bit Serial EEPROM memory device which is configured as either registers of 16 bits (ORG pin at V_{CC} or Not Connected) or 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C76 is manufactured using Catalyst’s advanced CMOS EEPROM floating gate technology. The device is designed to endure 1,000,000 program/erase cycles and has a data retention of 100 years. The device is available in 8-pin PDIP, SOIC, TSSOP and 8-pad TDFN packages.

FUNCTIONAL SYMBOL



For Ordering Information details, see page 12.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Parameters	Ratings	Units
Temperature Under Bias	-55 to +125	°C
Storage Temperature	-65 to 150	°C
Voltage on any Pin with Respect to Ground ⁽²⁾	-2.0 to +V _{CC} +2.0	V
V _{CC} with Respect to Ground	-2.0 to +7.0	V
Lead Soldering Temperature (10 seconds)	300	°C
Output Short Circuit Current ⁽³⁾	100	mA

RELIABILITY CHARACTERISTICS⁽³⁾

Symbol	Parameter	Reference Test Method	Min	Units
N _{END} ⁽⁴⁾	Endurance	MIL-STD-883, Test Method 1033	1,000,000	Cycles/Byte
T _{DR} ⁽⁴⁾	Data Retention	MIL-STD-883, Test Method 1008	100	Years
V _{ZAP} ⁽⁴⁾	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000	V
I _{LTH} ⁽⁴⁾⁽⁵⁾	Latch-Up	JEDEC Standard 17	100	mA

D.C. OPERATING CHARACTERISTICS

V_{CC} = +1.8V to +5.5V unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I _{CC1}	Power Supply Current (Write)	f _{SK} = 1MHz; V _{CC} = 5.0V		1	3	mA
I _{CC2}	Power Supply Current (Read)	f _{SK} = 1MHz; V _{CC} = 5.0V		300	500	μA
I _{SB1}	Power Supply Current (Standby) (x8 Mode)	CS = 0V ORG = GND		2	10	μA
I _{SB2}	Power Supply Current (Standby) (x16 Mode)	CS = 0V ORG = Float or V _{CC}		0 ⁽⁶⁾	10	μA
I _{LI}	Input Leakage Current	V _{IN} = 0V to V _{CC}		0 ⁽⁶⁾	10	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0V to V _{CC} , CS = 0V		0 ⁽⁶⁾	10	μA
I _{LORG}	ORG Pin Leakage Current	ORG = GND or ORG = V _{CC}		1	10	μA
V _{IL1}	Input Low Voltage	4.5V ≤ V _{CC} ≤ 5.5V	-0.1		0.8	V
V _{IH1}	Input High Voltage	4.5V ≤ V _{CC} ≤ 5.5V	2		V _{CC} + 1	V
V _{IL2}	Input Low Voltage	1.8V ≤ V _{CC} < 4.5V	0		V _{CC} x 0.2	V
V _{IH2}	Input High Voltage	1.8V ≤ V _{CC} < 4.5V	V _{CC} x 0.7		V _{CC} + 1	V
V _{OL1}	Output Low Voltage	4.5V ≤ V _{CC} ≤ 5.5V; I _{OL} = 2.1mA			0.4	V
V _{OH1}	Output High Voltage	4.5V ≤ V _{CC} ≤ 5.5V; I _{OH} = -400μA	2.4			V
V _{OL2}	Output Low Voltage	1.8V ≤ V _{CC} < 4.5V; I _{OL} = 100μA			0.1	V
V _{OH2}	Output High Voltage	1.8V ≤ V _{CC} < 4.5V; I _{OH} = -100μA	V _{CC} - 0.2			V

Notes:

- (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.
- (2) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20ns.
- (3) Output shorted for no more than one second.
- (4) These parameters are tested initially and after a design or process change that affects the parameter.
- (5) Latch-up protection is provided for stresses up to 100 mA on I/O pins from -1V to V_{CC} +1V.
- (6) 0μA is defined as less than 900nA.

PIN CAPACITANCE⁽¹⁾

Symbol	Test	Conditions	Min	Typ	Max	Units
C _{OUT}	Output Capacitance (DO)	V _{OUT} = 0V			5	pF
C _{IN}	Input Capacitance (CS, SK, DI, ORG)	V _{IN} = 0V			5	pF

INSTRUCTION SET⁽²⁾

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A10-A0	A9-A0			Read Address AN– A0
ERASE	1	11	A10-A0	A9-A0			Clear Address AN– A0
WRITE	1	01	A10-A0	A9-A0	D7-D0	D15-D0	Write Address AN– A0
EWEN	1	00	11XXXXXXXXXX	11XXXXXXXXXX			Write Enable
EWDS	1	00	00XXXXXXXXXX	00XXXXXXXXXX			Write Disable
ERAL	1	00	10XXXXXXXXXX	10XXXXXXXXXX			Clear All Addresses
WRAL	1	00	01XXXXXXXXXX	01XXXXXXXXXX	D7-D0	D15-D0	Write All Addresses

A.C. CHARACTERISTICS

Symbol	Parameter	Test Conditions	Limits				Units
			V _{CC} = 1.8V - 2.5V		V _{CC} = 2.5V - 5.5V		
			Min	Max	Min	Max	
t _{CSS}	CS Setup Time		100		50		ns
t _{CSH}	CS Hold Time		0		0		ns
t _{DIS}	DI Setup Time		100		50		ns
t _{DIH}	DI Hold Time		100		50		ns
t _{PD1}	Output Delay to 1			250		150	ns
t _{PD0}	Output Delay to 0	C _L = 100pF ⁽³⁾		250		150	ns
t _{HZ} ⁽¹⁾	Output Delay to High-Z			150		100	ns
t _{EW}	Program/Erase Pulse Width			5		5	ms
t _{CSMIN}	Minimum CS Low Time		200		150		ns
t _{SKHI}	Minimum SK High Time		250		150		ns
t _{SKLOW}	Minimum SK Low Time		250		150		ns
t _{SV}	Output Delay to Status Valid			250		100	ns
SK _{MAX}	Maximum Clock Frequency		DC	1000	DC	3000	kHz

POWER-UP TIMING⁽¹⁾⁽⁴⁾

Symbol	Parameter	Max	Units
t _{PUR}	Power-up to Read Operation	1	ms
t _{PUW}	Power-up to Write Operation	1	ms

Notes:

- (1) These parameters are tested initially and after a design or process change that affects the parameter.
- (2) Address bit A10 for the 1,024x8 org. and A9 for the 512x16 org. are "don't care" bits, but must be kept at either a "1" or "0" for READ, WRITE and ERASE commands.
- (3) The input levels and timing reference points are shown in the "AC Test Conditions" table.
- (4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

A.C. TEST CONDITIONS

Input Rise and Fall Times	≤ 50ns	
Input Pulse Voltages	0.4V to 2.4V	4.5V ≤ V _{CC} ≤ 5.5V
Timing Reference Voltages	0.8V, 2.0V	4.5V ≤ V _{CC} ≤ 5.5V
Input Pulse Voltages	0.2V _{CC} to 0.7V _{CC}	1.8V ≤ V _{CC} ≤ 4.5V
Timing Reference Voltages	0.5V _{CC}	1.8V ≤ V _{CC} ≤ 4.5V

DEVICE OPERATION

The CAT93C76 is a 8192-bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C76 can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 13-bit instructions control the read, write and erase operations of the device. When organized as X8, seven 14-bit instructions control the read, write and erase operations of the device. The CAT93C76 operates on a single power supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the device is a logical "1" start bit, a 2-bit (or 4-bit) opcode, 10-bit address (an additional bit when organized X8) and for write operations a 16-bit data field (8-bit for X8 organizations). The most significant bit of the address is "don't care" but it must be present.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C76 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

For the CAT93C76, after the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is preceded by a dummy zero bit. All subsequent data words will follow without a dummy zero bit.

Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN} . The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C76 can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

Figure 1. Synchronous Data Timing

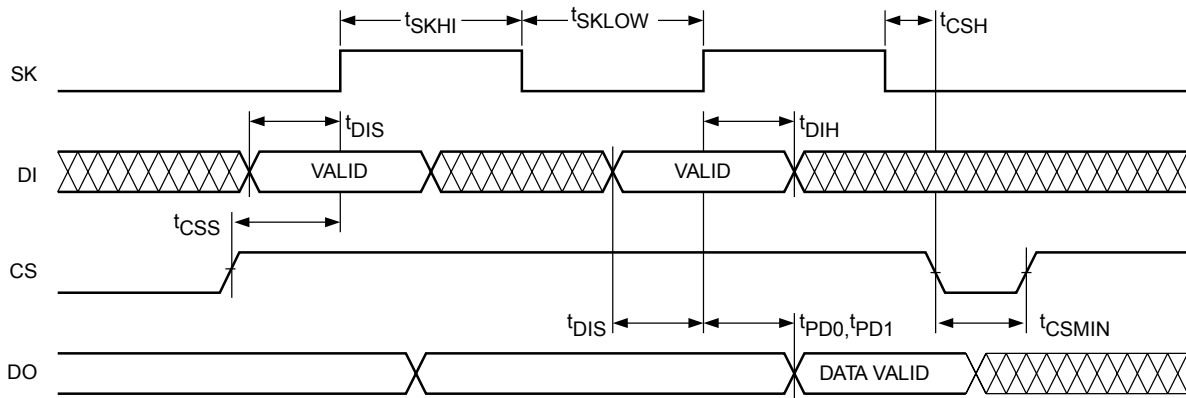


Figure 2. Read Instruction Timing

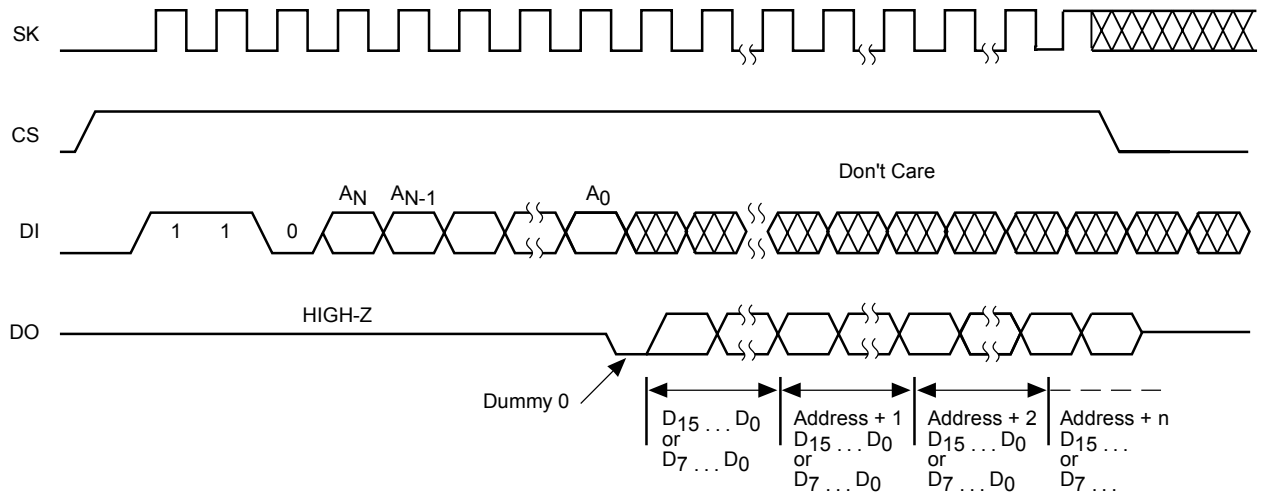
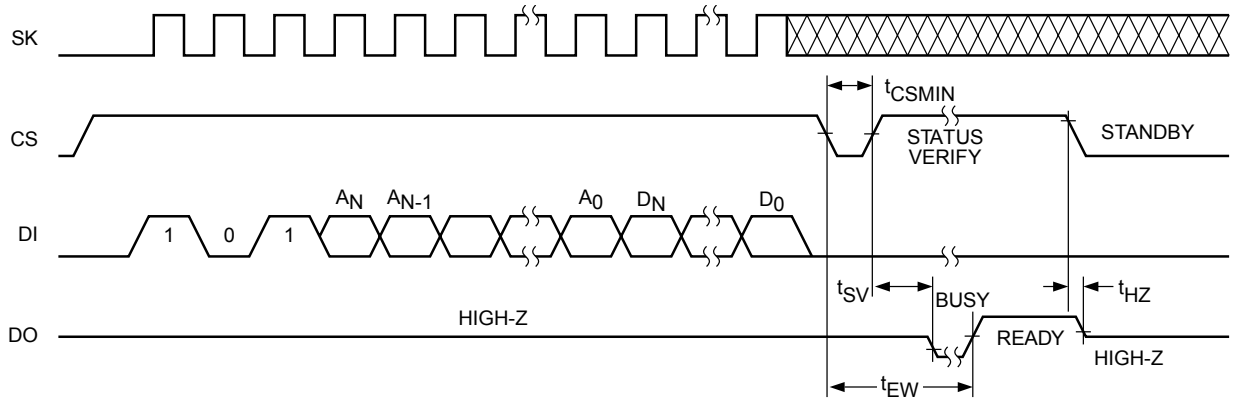


Figure 3. Write Instruction Timing



Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of t_{CSMIN} . The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C76 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical “1” state.

Erase/Write Enable and Disable

The CAT93C76 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C76 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN} . The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C76 can be

determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical “1” state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN} . The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C76 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

Note 1: After the last data bit has been sampled, Chip Select (CS) must be brought Low before the next rising edge of the clock (SK) in order to start the self-timed high voltage cycle. This is important because if CS is brought low before or after this specific frame window, the addressed location will not be programmed or erased.

Power-On Reset (POR)

The CAT93C76 incorporates Power-On Reset (POR) circuitry which protects the device against malfunctioning while V_{CC} is lower than the recommended operating voltage.

The device will power up into a read-only state and will power-down into a reset state when V_{CC} crosses the POR level of ~1.3 V.

Figure 4. Erase Instruction Timing

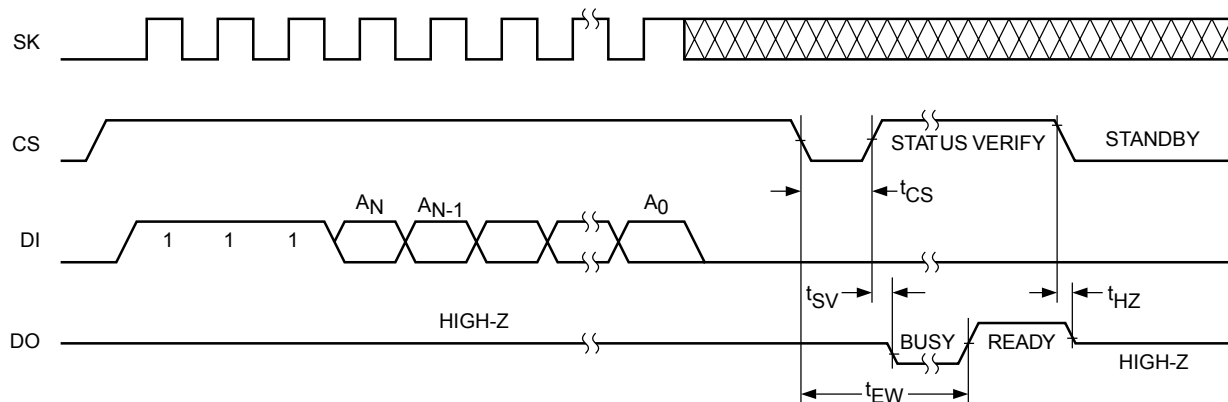


Figure 5. EWEN/EWDS Instruction Timing

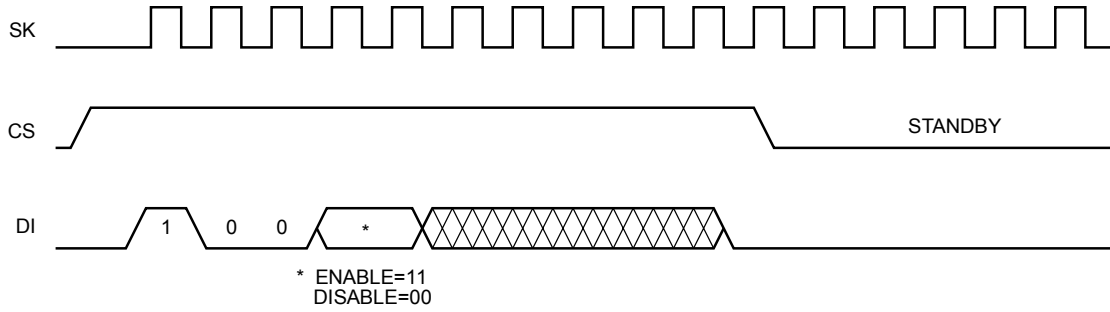


Figure 6. ERAL Instruction Timing

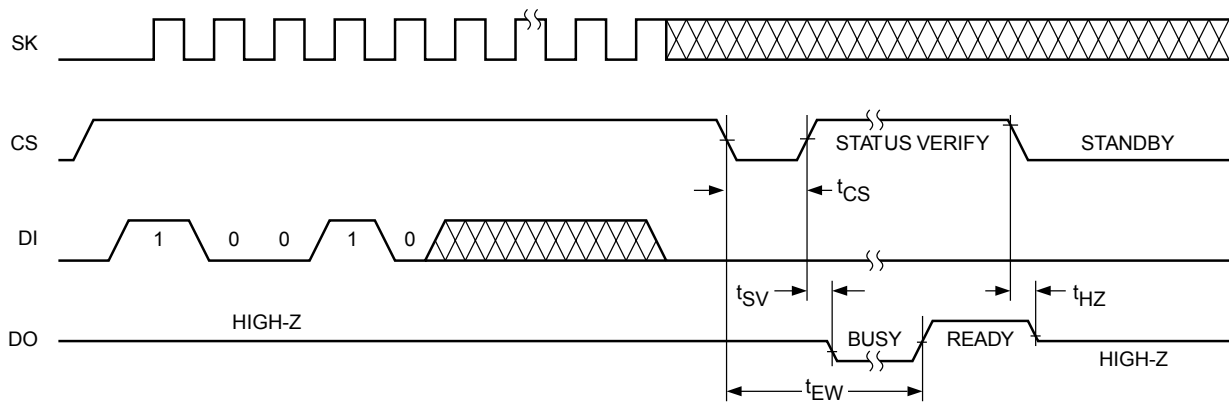
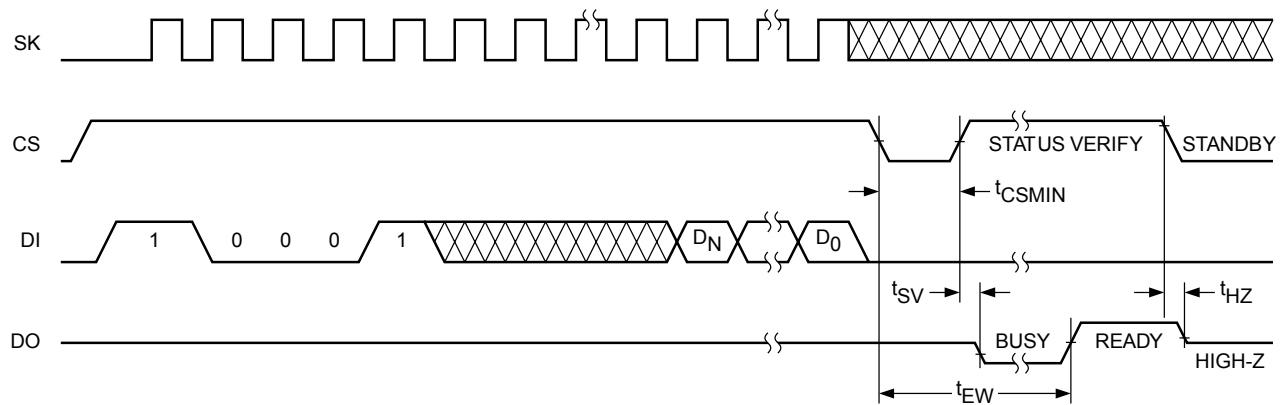
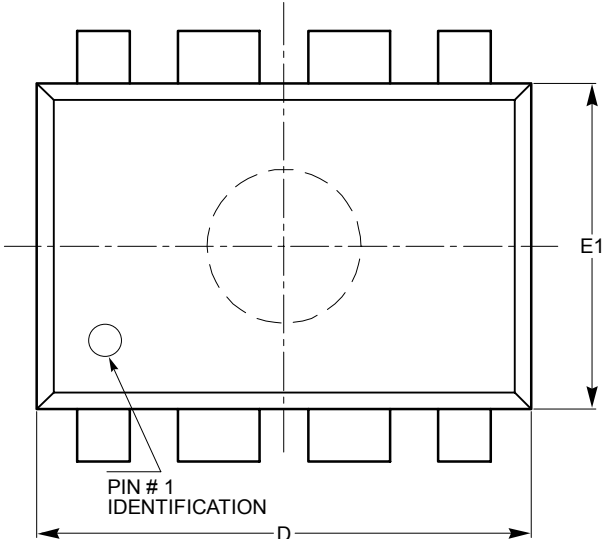


Figure 7. WRAL Instruction Timing



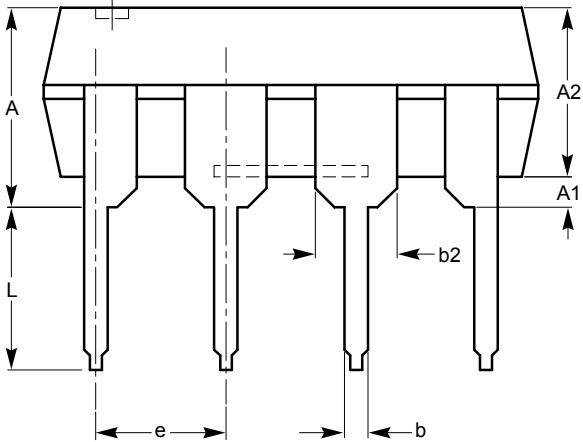
PACKAGE OUTLINE DRAWING

PDIP 8-Lead 300mils (L) ⁽¹⁾⁽²⁾

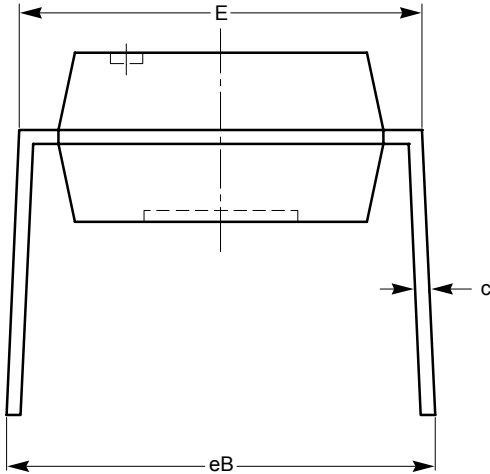


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
e	2.54 BSC		
E1	6.10	6.35	7.11
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW



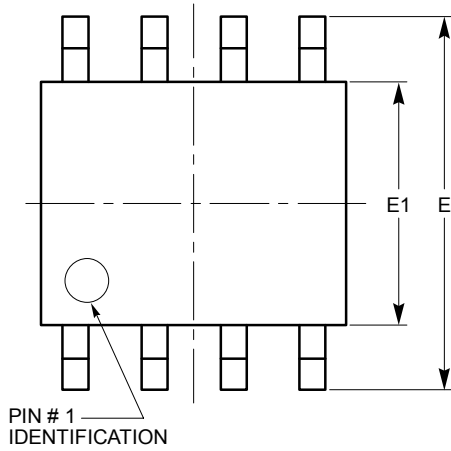
END VIEW

For current Tape and Reel information, download the PDF file from:
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Notes:

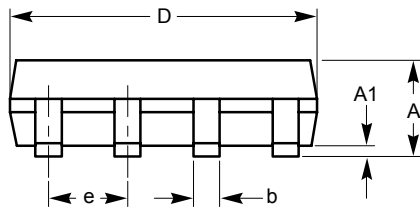
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-001.

SOIC 8-Lead 150mils (V) ⁽¹⁾⁽²⁾

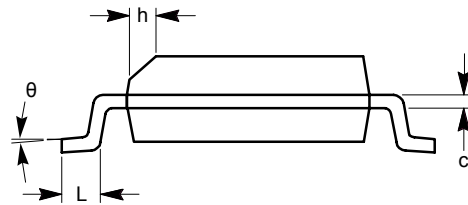


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW



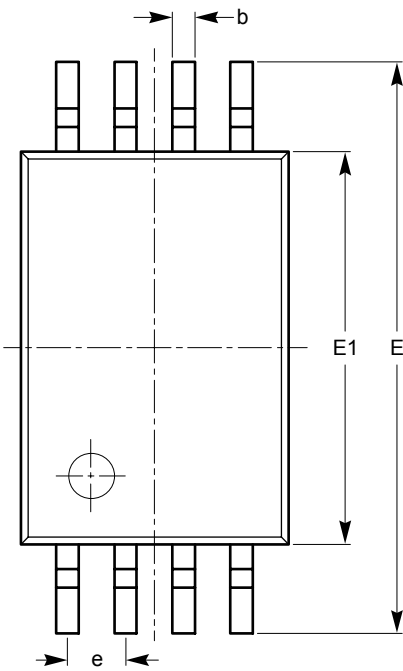
END VIEW

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Notes:

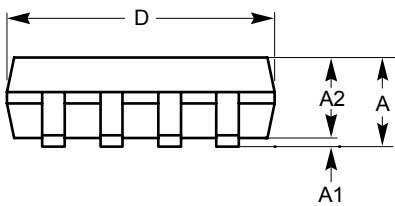
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

TSSOP 8-Lead (Y) ⁽¹⁾⁽²⁾

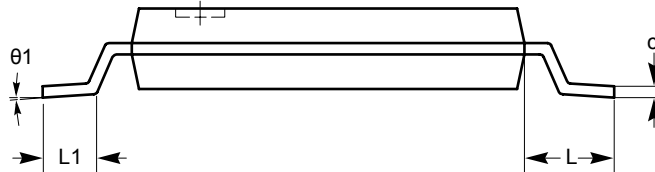


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
$\theta 1$	0°		8°



SIDE VIEW



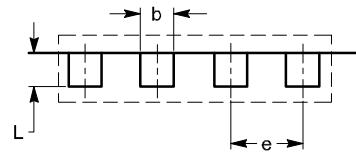
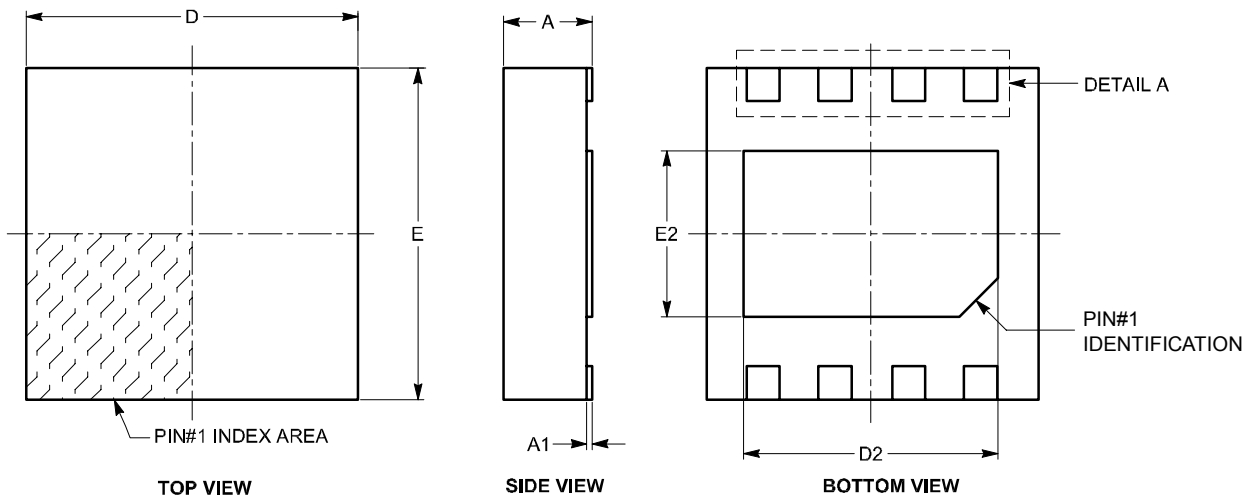
END VIEW

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<http://www.catsemi.com/documents/tapeandreel.pdf>

Notes:

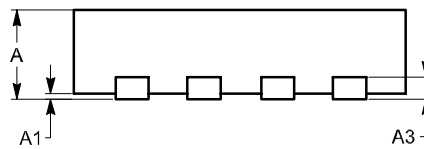
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

TDFN 8-Pad 3 x 3mm (ZD4) ⁽¹⁾⁽²⁾



DETAIL A

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20 REF		
b	0.23	0.30	0.37
D	2.90	3.00	3.10
D2	2.20	2.30	2.40
E	2.90	3.00	3.10
E2	1.40	1.50	1.60
e	0.65 TYP		
L	0.20	0.30	0.40



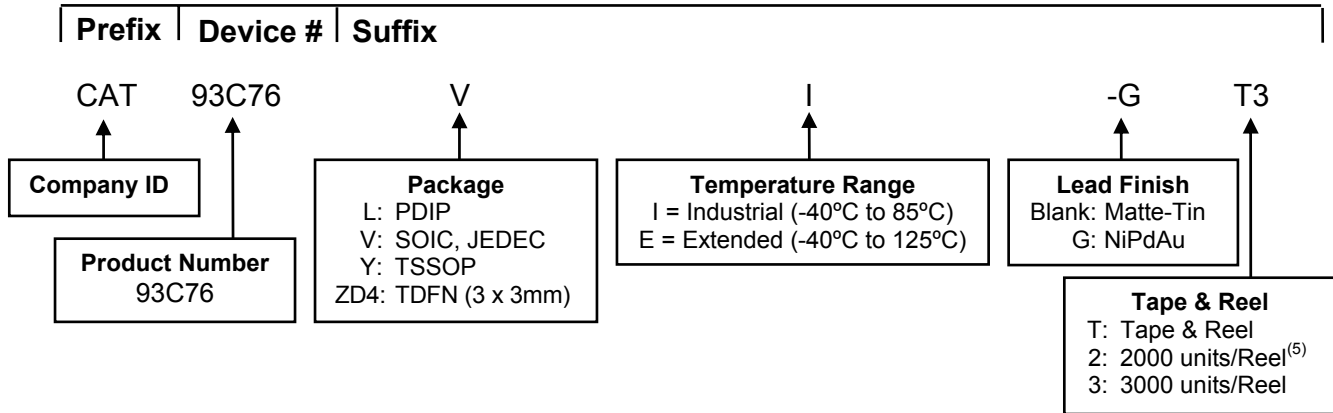
FRONT VIEW

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Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-229.

EXAMPLE OF ORDERING INFORMATION



Notes:

- (1) All packages are RoHS-compliant (Lead-free, Halogen-free).
- (2) The standard lead finish is NiPdAu.
- (3) The device used in the above example is a 93C76VI-GT3 (SOIC, Industrial Temperature, NiPdAu, Tape & Reel)
- (4) Product die revision letter is marked on top of the package as a suffix to the production date code (e.g., AYWWA.) For additional information, please contact your Catalyst sales office.
- (5) For TDFN 3 x 3mm package Tape and Reel = 2000 pcs/reel, all others = 3000 pcs/reel.
- (6) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

REVISION HISTORY

Date	Rev.	Comments
08/11/2004	A	Initial Issue
09/21/2007	B	Added Package Outline Drawings Updated the Example of Ordering Information

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