Spread Spectrum Frequency Timing Generator

Features

- **Maximized EMI suppression using Cypress's Spread Spectrum technology**
- **Generates a spread spectrum copy of the provided input**
- **Selectable spreading characteristics**
- **Integrated loop filter components**
- **Operates with a 3.3V or 5V supply**
- **SSON# pin enables frequency spreading**
- **Low power CMOS design**
- **Available in 8-pin SOIC (Small Outline Integrated Circuit)**

Overview

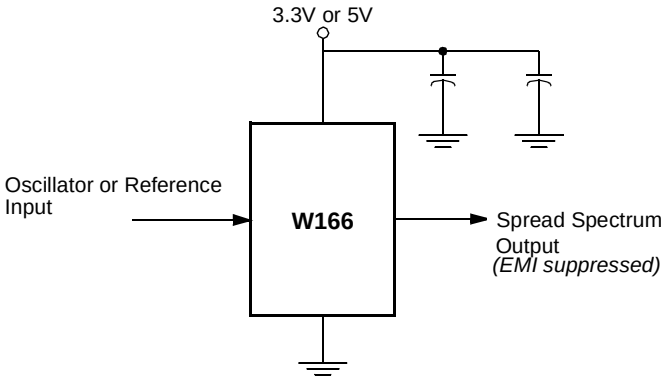
The W166 incorporates the latest advances in PLL spread spectrum frequency synthesizer techniques. By frequency modulating the output with a low-frequency carrier, peak EMI is greatly reduced. Use of this technology allows systems to pass increasingly difficult EMI testing without resorting to costly shielding or redesign.

In a system, not only is EMI reduced in the various clock lines, but also in all signals which are synchronized to the clock. Therefore, the benefits of using this technology increase with the number of address and data lines in the system. The Simplified Block Diagram shows a simple implementation.

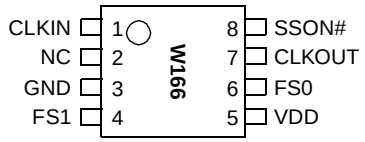
Table 1. Frequency Spread Selection

W166		Input Frequency (MHz)	Output Frequency (MHz)
FS1	FS0		
0	0	50 to 65	f_{IN} ±0.625%
0	1	50 to 65	f_{IN} ±1.25%
1	0	50 to 65	f_{IN} ±2.5%
1	1	50 to 65	f_{IN} –3.75%

Simplified Block Diagram



Pin Configuration



Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CLKOUT	7	O	***Output Modulated Frequency***: Frequency modulated copy of the reference input (SSON# asserted).
CLKIN	1	I	***External Reference Frequency Input:*** Clock input.
NC	2	NC	***No Connect:*** This pin must be left unconnected.
SSON#	8	I	***Spread Spectrum Control (Active LOW):*** Asserting this signal (active LOW) turns the internal modulation waveform on. This pin has an internal pull-down resistor.
FS0:1	6, 4	I	***Frequency Selection Bits 0,1:*** These pins select the frequency spreading characteristics. Refer to *Table 1*. These pins have internal pull-up resistors.
VDD	5	P	***Power Connection:*** Connected to 3.3V or 5V power supply.
GND	3	G	***Ground Connection:*** This should be connected to the common ground plane.

Functional Description

The W166 uses a Phase-Locked Loop (PLL) to frequency modulate an input clock. The result is an output clock whose frequency is slowly swept over a narrow band near the input signal. The basic circuit topology is shown in *Figure 1*. The input reference signal is divided by Q and fed to the phase detector. A signal from the VCO is divided by P and fed back to the phase detector also. The PLL will force the frequency of the VCO output signal to change until the divided output signal and the divided reference signal match at the phase detector input. The output frequency is then equal to the ratio of P/Q times the reference frequency. (Note: For the W166 the output frequency is equal to the input frequency.) The unique feature of the Spread Spectrum Frequency Timing Generator is that a modulating waveform is superimposed at the input to the VCO. This causes the VCO output to be slowly swept across a predetermined frequency band.

Because the modulating frequency is typically 1000 times slower than the fundamental clock, the spread spectrum process has little impact on system performance.

Frequency Selection With SSFTG

In Spread Spectrum Frequency Timing Generation, EMI reduction depends on the shape, modulation percentage, and frequency of the modulating waveform. While the shape and frequency of the modulating waveform are fixed, the modulation percentage may be varied.

A larger spreading percentage improves EMI reduction. However, large spread percentages may either exceed system maximum frequency ratings or lower the average frequency to a point where performance is affected. For these reasons, narrow and wide modulation selections are provided.

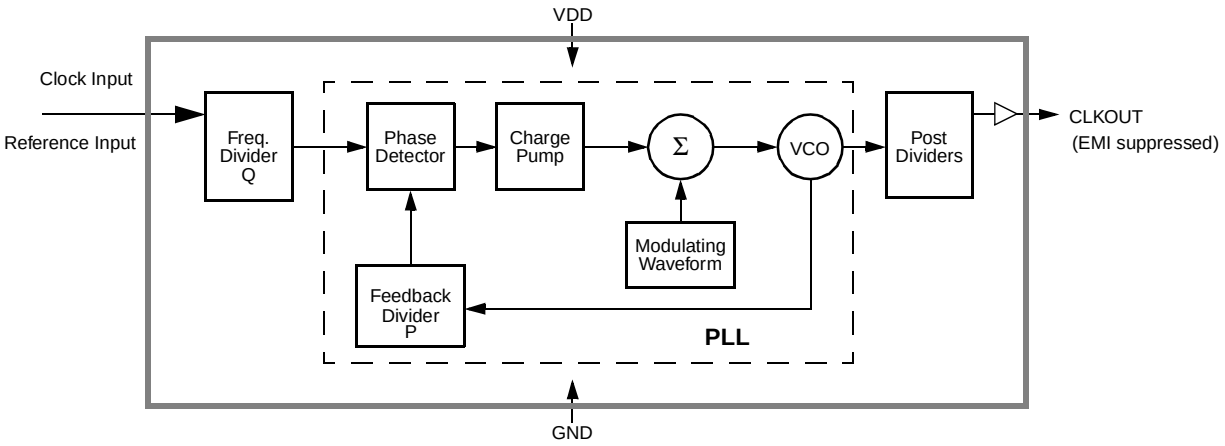


Figure 1. System Block Diagram

Spread Spectrum Frequency Timing Generator

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 2*.

As shown in *Figure 2*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is

$$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 3*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is ±0.45% or 0.6% of the selected frequency. *Figure 3* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

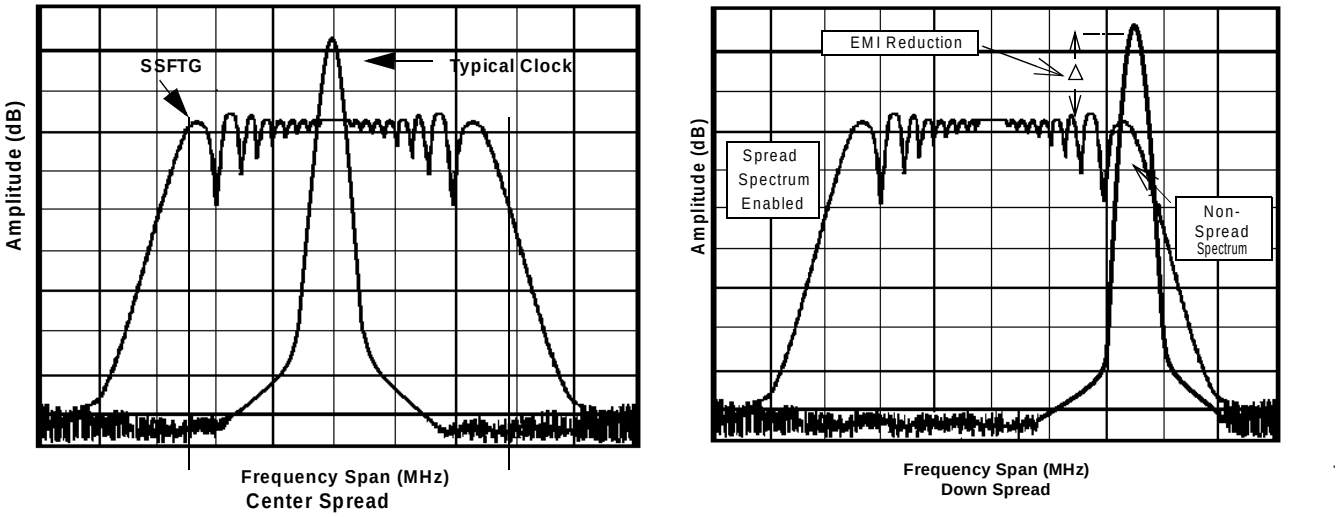


Figure 2. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

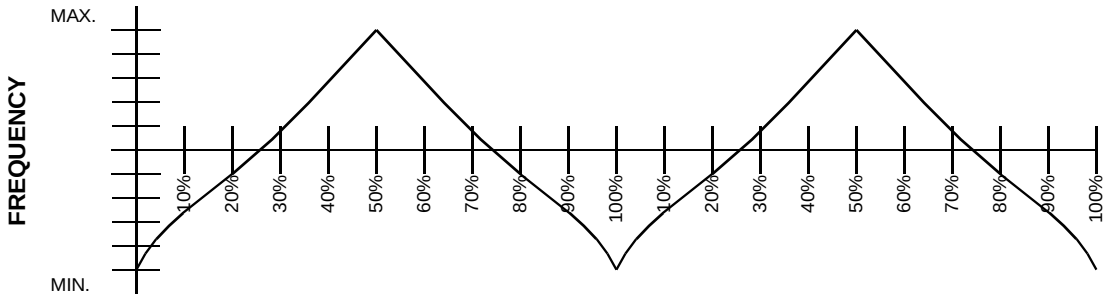


Figure 3. Typical Modulation Profile

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any Pin with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
P_D	Power Dissipation	0.5	W

DC Electrical Characteristics: $0°C < T_A < 70°C$, $V_{DD} = 3.3V \pm 5\%$

Parameter	Description	Test Condition	Min	Typ	Max	Unit
I_{DD}	Supply Current			18	32	mA
t_{ON}	Power Up Time	First locked clock cycle after Power Good			5	ms
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.4			V
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V
I_{IL}	Input Low Current	Note 1			–20	µA
I_{IH}	Input High Current	Note 1			20	µA
I_{OL}	Output Low Current	@ 0.4V, V_{DD} = 3.3V		15		mA
I_{OH}	Output High Current	@ 2.4V, V_{DD} = 3.3V		15		mA
C_I	Input Capacitance	All pins except CLKIN			7	pF
C_I	Input Capacitance	CLKIN pin only		6	5	pF
R_P	Input Pull-Up Resistor			500		kΩ
Z_{OUT}	Clock Output Impedance			25		Ω

Note:
1. Inputs FS1:0 have a pull-up resistor, Input SSON# has a pull-down resistor.

DC Electrical Characteristics: $0°C < T_A < 70°C$, $V_{DD} = 5V \pm 10\%$

Parameter	Description	Test Condition	Min	Typ	Max	Unit
I_{DD}	Supply Current			21	40	mA
t_{ON}	Power Up Time	First locked clock cycle after Power Good			5	ms
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		3.5			V
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V
I_{IL}	Input Low Current	Note 1			–20	µA
I_{IH}	Input High Current	Note 1			20	µA
I_{OL}	Output Low Current	@ 0.4V, V_{DD} = 5V		24		mA
I_{OH}	Output High Current	@ 2.4V, V_{DD} = 5V		24		mA
C_I	Input Capacitance	All pins except CLKIN			7	pF
C_I	Input Capacitance	CLKIN pin only			5	pF
R_P	Input Pull-Up Resistor			500		kΩ
Z_{OUT}	Clock Output Impedance			25		Ω

AC Electrical Characteristics: $T_A = 0°C$ to $+70°C$, $V_{DD} = 3.3V \pm 5\%$ or $5V \pm 10\%$

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
f_{IN}	Input Frequency	Input Clock	50		65	MHz
f_{OUT}	Output Frequency	Spread Off	50		65	MHz
t_R	Output Rise Time	15-pF load, 0.8V–2.4V		2	5	ns
t_F	Output Fall Time	15-pF load, 2.4V–0.8V		2	5	ns
t_{OD}	Output Duty Cycle	15-pF load, test at $V_{DD}/2$	40		60	%
t_{ID}	Input Duty Cycle		40		60	%
t_{JCYC}	Jitter, Cycle-to-Cycle			250	300	ps
	Harmonic Reduction	f_{out} = 50 MHz, third harmonic measured, reference board, 15-pF load	8			dB

Application Information

Recommended Circuit Configuration

For optimum performance in system applications the power supply decoupling scheme shown in *Figure 4* should be used.

VDD decoupling is important to both reduce phase jitter and EMI radiation. The 0.1-µF decoupling capacitor should be placed as close to the V_{DD} pin as possible, otherwise the increased trace inductance will negate its decoupling capability. The 10-µF decoupling capacitor shown should be a tantalum type. For further EMI protection, the V_{DD} connection can be made via a ferrite bead, as shown.

Recommended Board Layout

Figure 5 shows a recommended a 2-layer board layout.

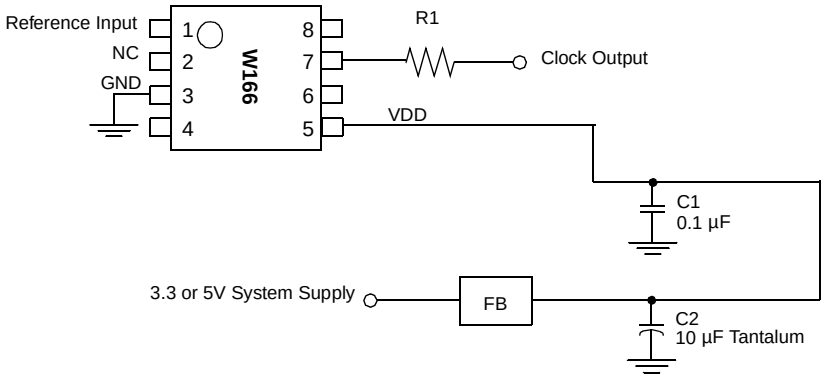


Figure 4. Recommended Circuit Configuration

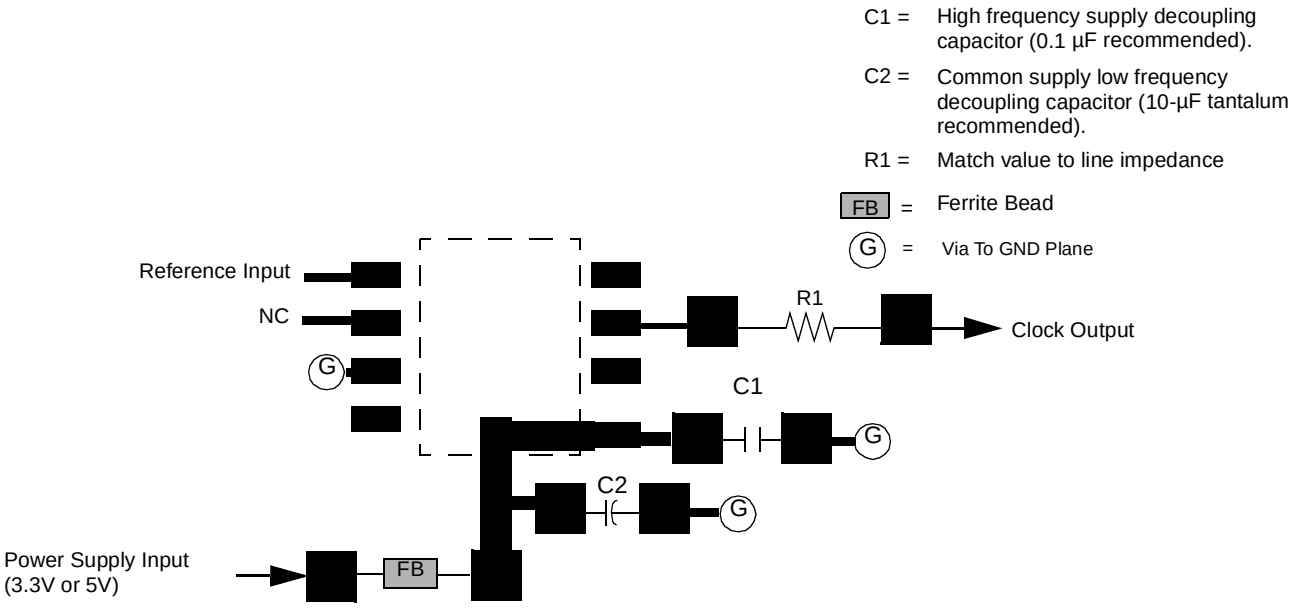


Figure 5. Recommended Board Layout (2-Layer Board)

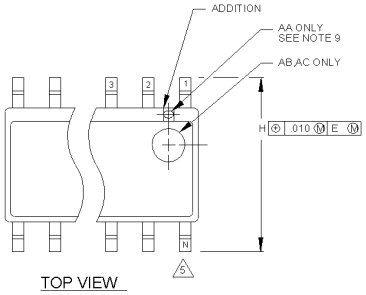
Ordering Information

Ordering Code	Package Name	Package Type
W166	G	8-pin Plastic SOIC (150-mil)

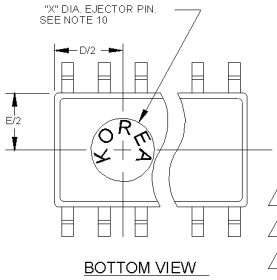
Document: #38-00878

Package Diagram

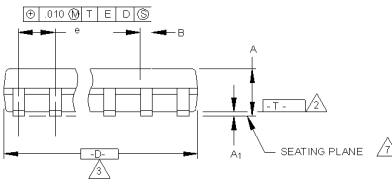
8-Pin Small Outlined Integrated Circuit (SOIC, 150-mil)



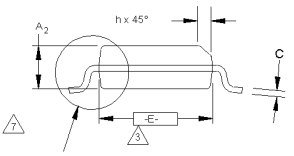
TOP VIEW



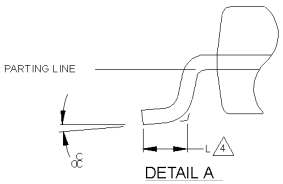
BOTTOM VIEW



SIDE VIEW



END VIEW



DETAIL A

NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. THE APPEARANCE OF PIN #1 I.D ON THE 8 LD IS OPTIONAL, ROUND TYPE ON SINGLE LEADFRAME AND RECTANGULAR TYPE ON MATRIX LEADFRAME.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
11. CONTROLLING DIMENSION: INCHES.

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	3			5
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	.061	.064	.068		AA	.189	.194	.196	8
A_1	.004	.006	.0098		AB	.337	.342	.344	14
A_2	.055	.058	.061		AC	.386	.391	.393	16
B	.0138	.016	.0192						
C	.0075	.008	.0098						
D	SEE VARIATIONS			3					
E	.150	.155	.157						
e	.050 BSC								
H	.230	.236	.244						
h	.010	.013	.016						
L	.016	.025	.035						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	3			5
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	1.55	1.63	1.73		AA	4.80	4.93	4.98	8
A_1	0.127	0.15	0.25		AB	8.58	8.69	8.74	14
A_2	1.40	1.47	1.55		AC	9.80	9.93	9.98	16
B	0.35	0.41	0.49						
C	0.19	0.20	0.25						
D	SEE VARIATIONS			3					
E	3.81	3.94	3.99						
e	1.27 BSC								
H	5.84	5.99	6.20						
h	0.25	0.33	0.41						
L	0.41	0.64	0.89						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	2.16	2.36	2.54						