

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ CE

500V CoolMOS™ CE Power Transistor
IPA50R190CE

Data Sheet

Rev. 2.2
Final

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE series combines the experience of the leading SJ MOSFET supplier with high class innovation while representing a cost appealing alternative compared to standard MOSFETs in target applications. The resulting devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter and cooler.



Features

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for standard grade applications

Applications

PFC stages, hard switching PWM stages and resonant switching PWM stages for e.g. PC Silverbox, LCD & PDP TV and Lighting.

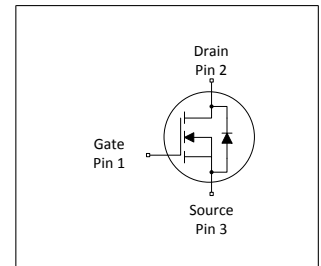


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	550	V
$R_{DS(on),max}$	0.19	Ω
$Q_{g,typ}$	47.2	nC
$I_{D,pulse}$	63	A
$E_{oss}@400V$	4.42	μJ
Body diode di/dt	500	A/ μs

Type / Ordering Code	Package	Marking	Related Links
IPA50R190CE	PG-TO 220 FullPAK	5R190CE	see Appendix A

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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	18.5 11.7	A	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	63	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	339	mJ	$I_D=7.7\text{A}; V_{DD} = 50\text{V}$
Avalanche energy, repetitive	E_{AR}	-	-	0.51	mJ	$I_D=7.7\text{A}; V_{DD} = 50\text{V}$
Avalanche current, repetitive	I_{AR}	-	-	7.7	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS} = 0\dots 400\text{V}$
Gate source voltage	V_{GS}	-20 -30	-	20 30	V	static; AC ($f > 1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	32	W	$T_C=25^\circ\text{C}$
Operating and storage temperature	T_j, T_{stg}	-40	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	I_S	-	-	16.0	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	63.0	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS} = 0\dots 400\text{V}, I_{SD} \leq I_S, T_j=25^\circ\text{C}, t_{cond} < 2\mu\text{s}$
Maximum diode commutation speed ³⁾	di/dt	-	-	500	A/ μs	$V_{DS} = 0\dots 400\text{V}, I_{SD} \leq I_S, T_j=25^\circ\text{C}, t_{cond} < 2\mu\text{s}$
Insulation withstand voltage for TO-220FP	V_{ISO}	-	-	2500	V	$V_{rms}, T_C=25^\circ\text{C}, t=1\text{min}$

3 Thermal characteristics

Table 3 Thermal characteristics TO-220 FullPAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.9	$^\circ\text{C/W}$	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	$^\circ\text{C/W}$	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	$^\circ\text{C}$	1.6mm (0.063 in.) from case for 10s

¹⁾ Limited by $T_{j,max} < 150^\circ\text{C}$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ $V_{DClink}=400\text{V}; V_{DS,peak} < V_{(BR)DSS}$; identical low side and high side switch with identical R_G

4 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	2.50	3	3.50	V	$V_{DS}=V_{GS}, I_D=0.51mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=500V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=500V, V_{GS}=0V, T_j=150^\circ C$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.17	0.19	Ω	$V_{GS}=13V, I_D=6.2A, T_j=25^\circ C$ $V_{GS}=13V, I_D=6.2A, T_j=150^\circ C$
Gate resistance	R_G	-	3	-	Ω	$f=1 MHz, \text{open drain}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1137	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Output capacitance	C_{oss}	-	68	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	56	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	251	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	9.5	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=7.7A,$ $R_G=3.4\Omega$
Rise time	t_r	-	8.5	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=7.7A,$ $R_G=3.4\Omega$
Turn-off delay time	$t_{d(off)}$	-	54	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=7.7A,$ $R_G=3.4\Omega$
Fall time	t_f	-	7.5	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=7.7A,$ $R_G=3.4\Omega$

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	6.1	-	nC	$V_{DD}=400V, I_D=7.7A, V_{GS}=0 \text{ to } 10V$
Gate to drain charge	Q_{gd}	-	24.5	-	nC	$V_{DD}=400V, I_D=7.7A, V_{GS}=0 \text{ to } 10V$
Gate charge total	Q_g	-	47.2	-	nC	$V_{DD}=400V, I_D=7.7A, V_{GS}=0 \text{ to } 10V$
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DD}=400V, I_D=7.7A, V_{GS}=0 \text{ to } 10V$

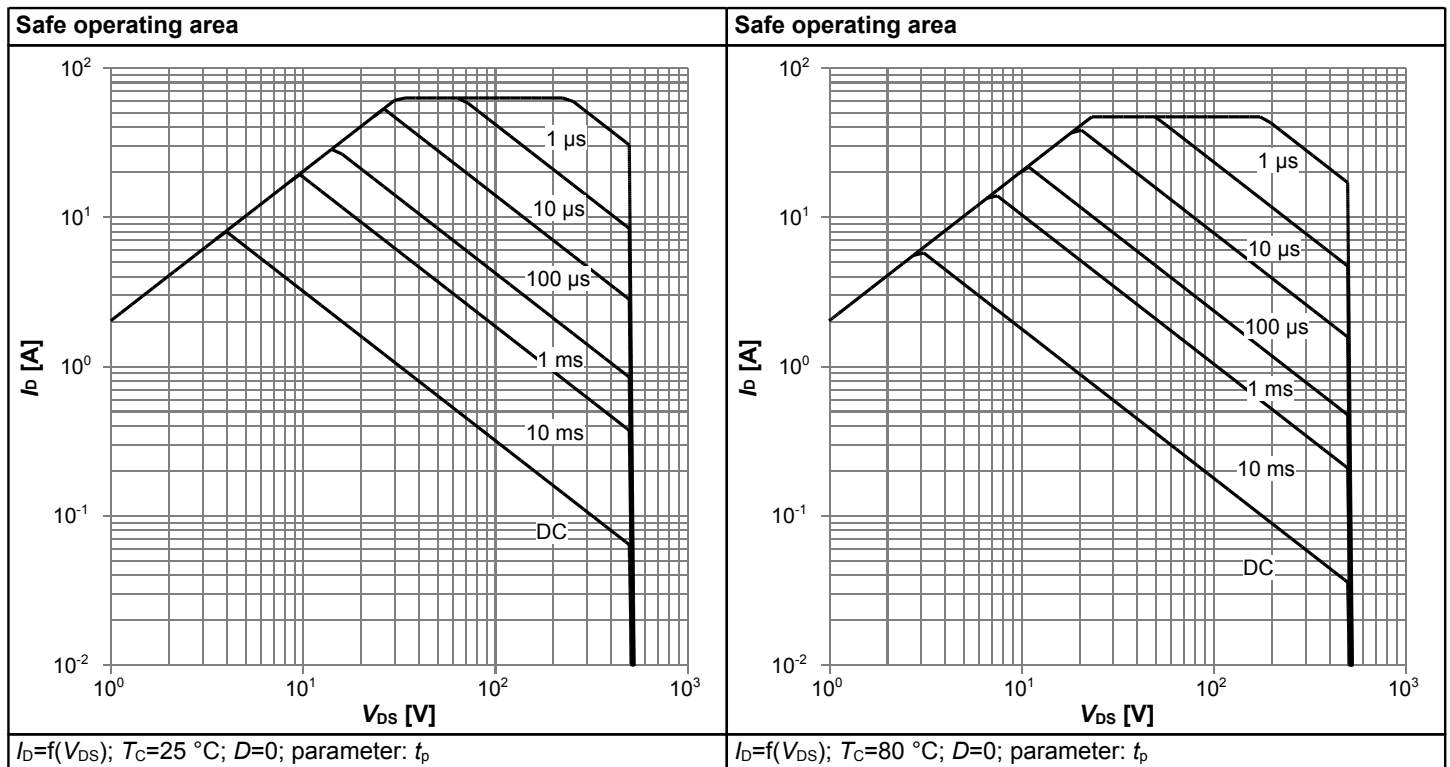
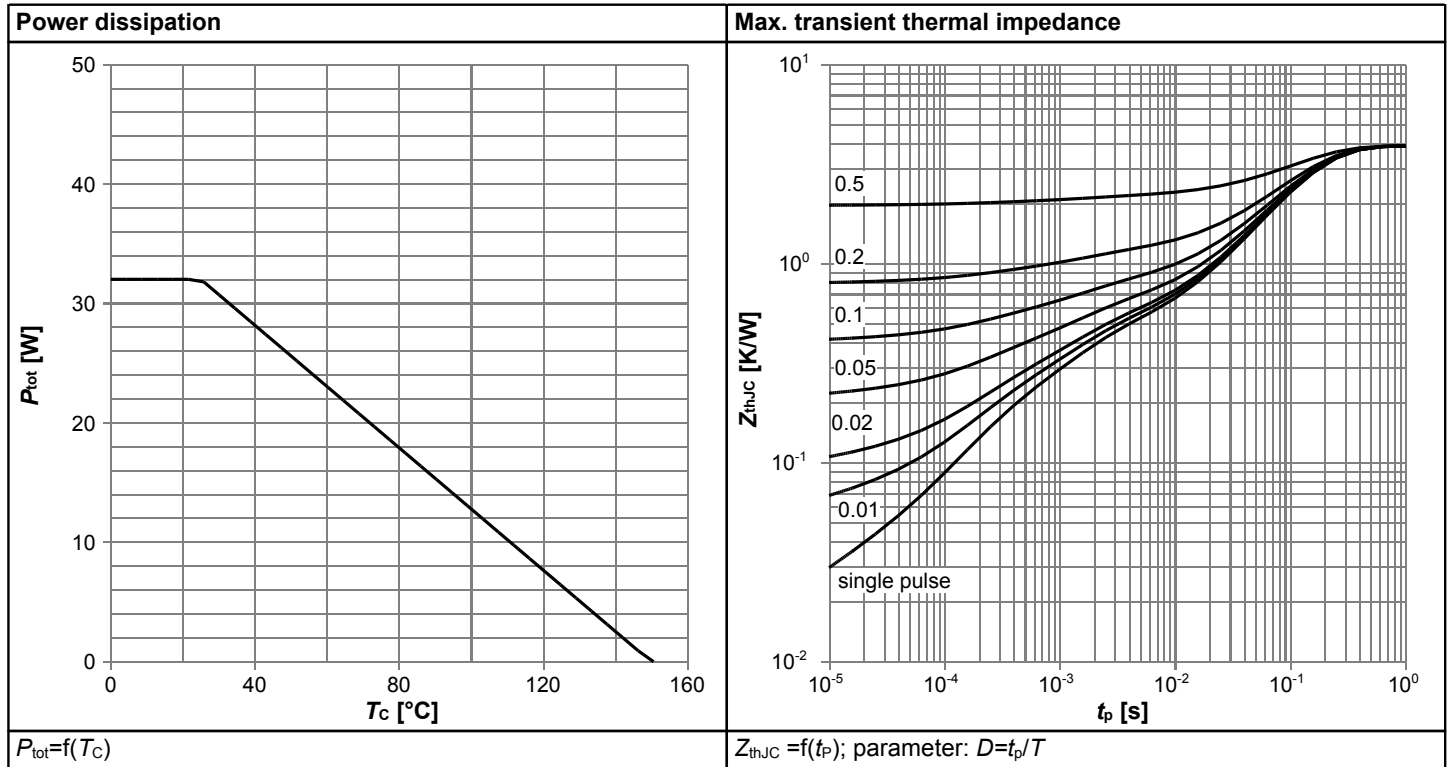
¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

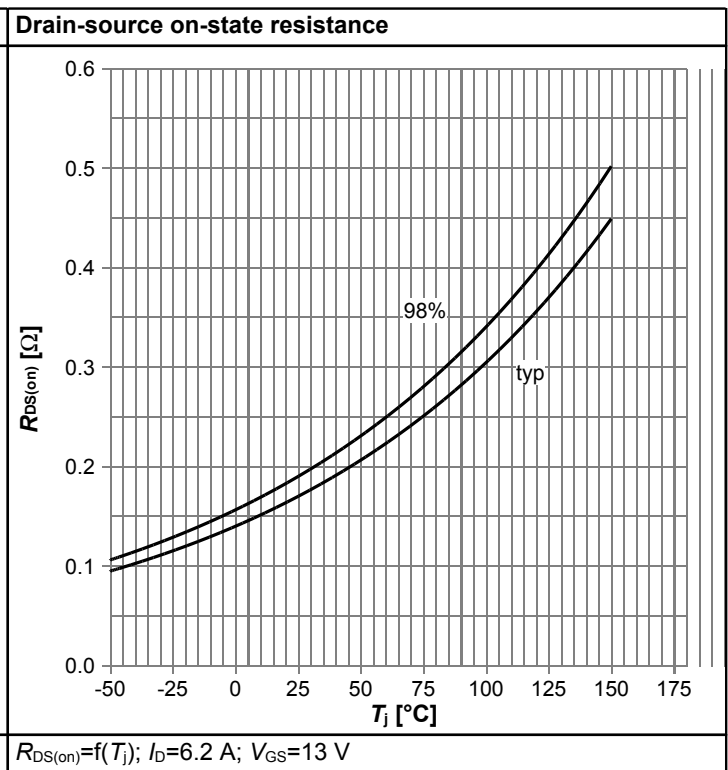
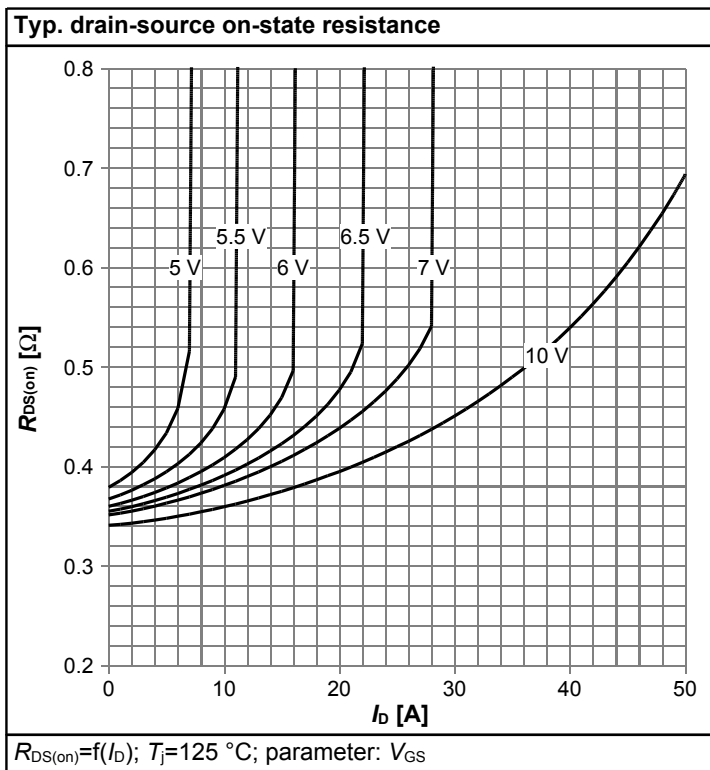
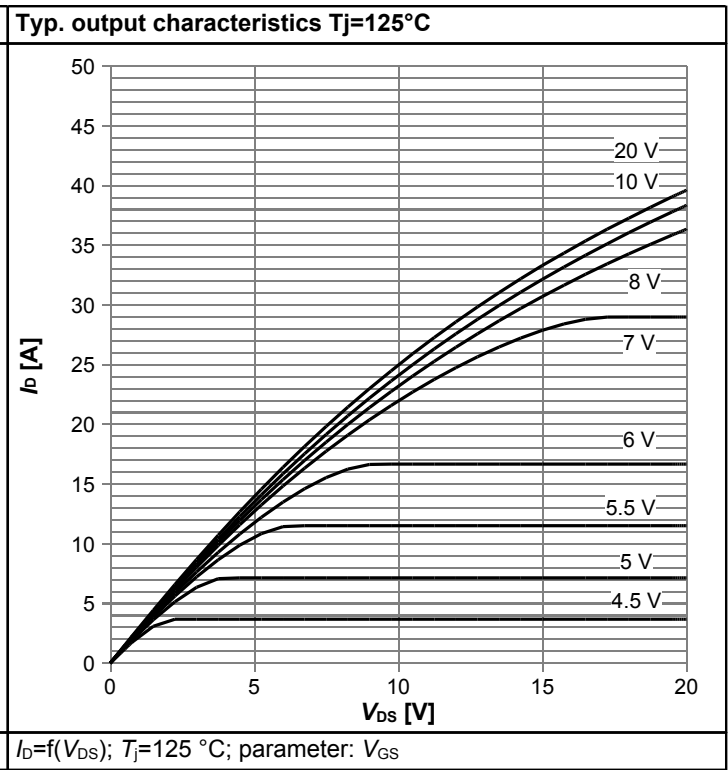
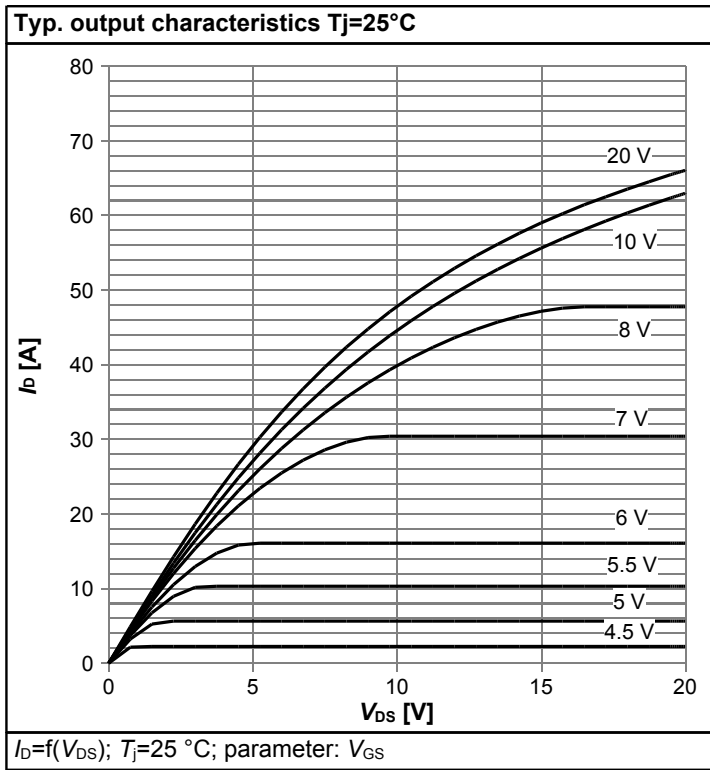
²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

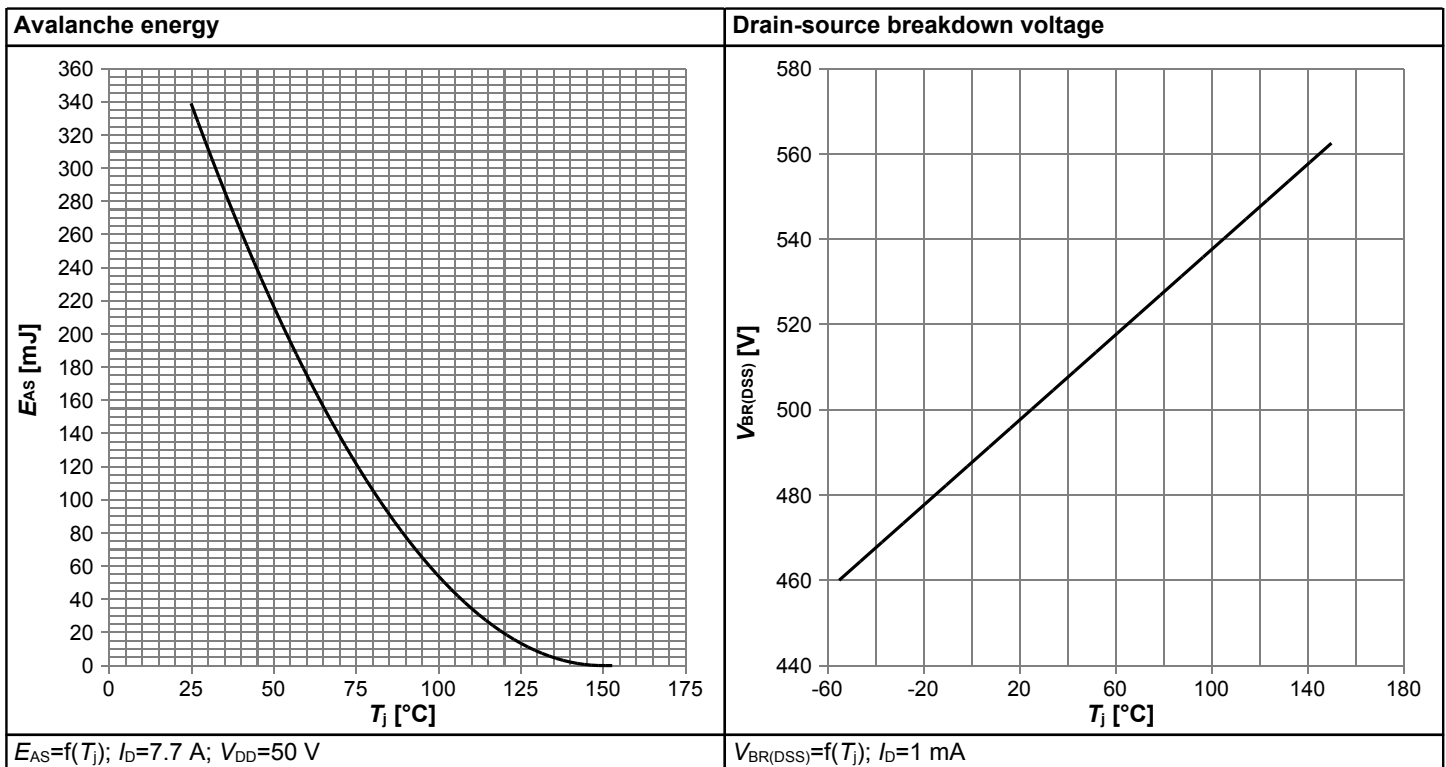
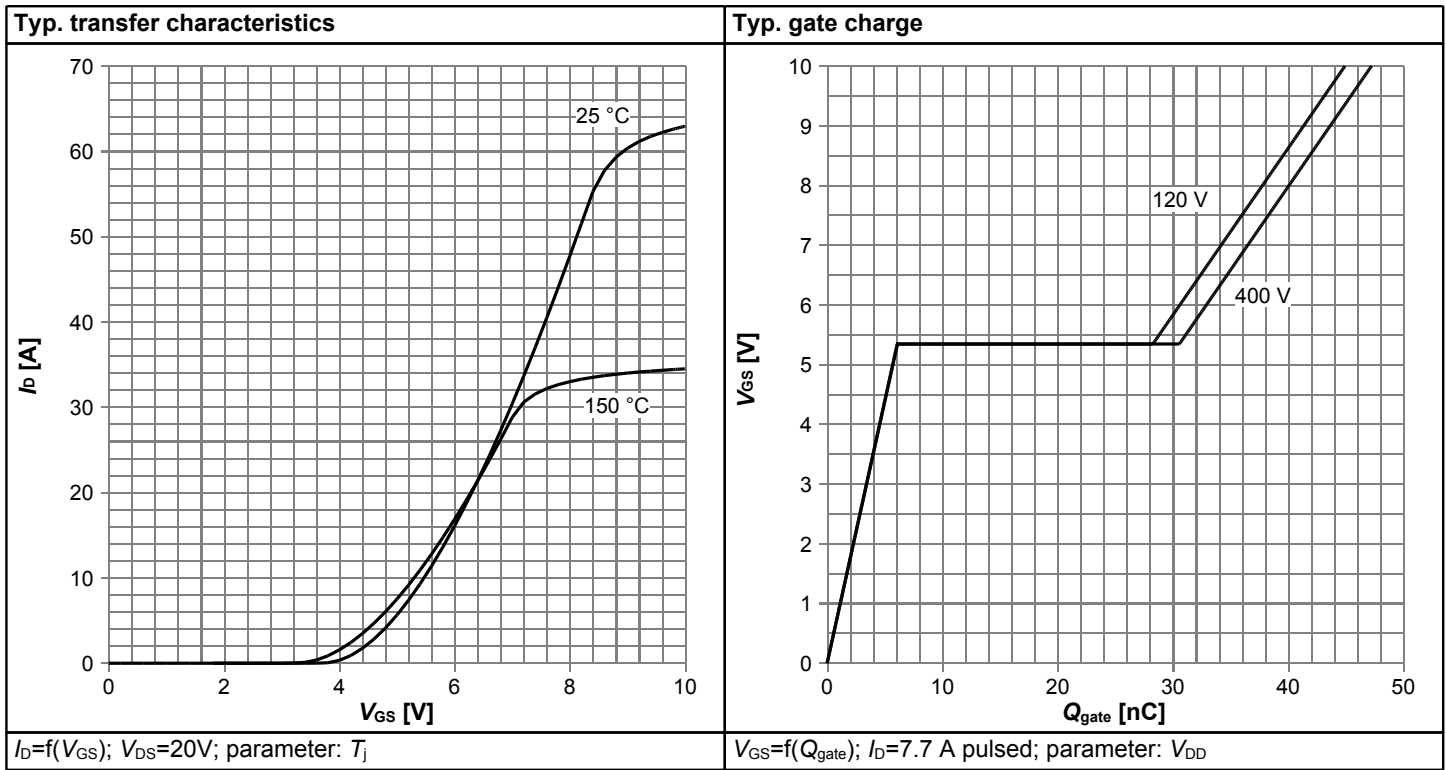
Table 7 Reverse diode characteristics

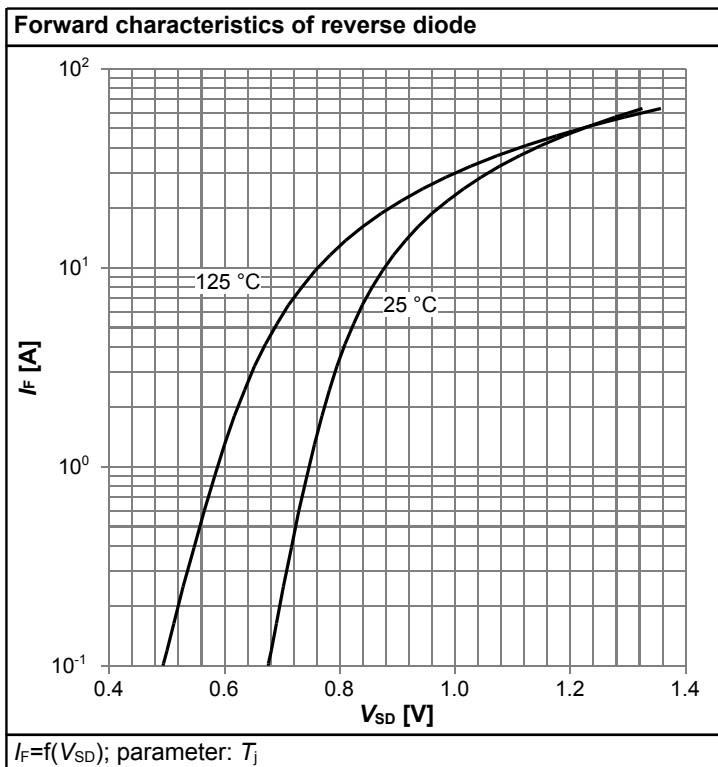
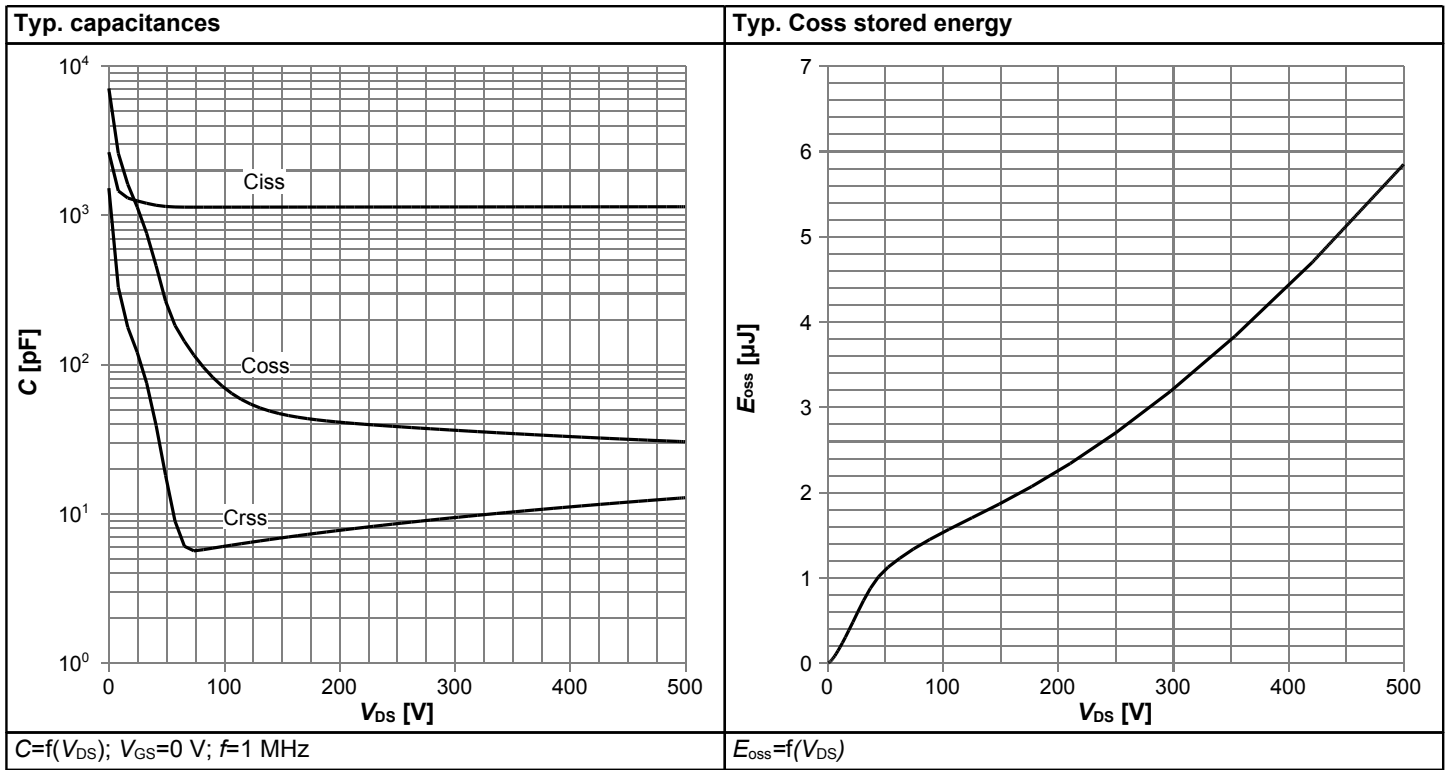
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.85	-	V	$V_{GS}=0V, I_F=7.7A, T_i=25^\circ C$
Reverse recovery time	t_{rr}	-	280	-	ns	$V_R=400V, I_F=7.7A, di_F/dt=100A/\mu s$
Reverse recovery charge	Q_{rr}	-	3.2	-	μC	$V_R=400V, I_F=7.7A, di_F/dt=100A/\mu s$
Peak reverse recovery current	I_{rrm}	-	21.5	-	A	$V_R=400V, I_F=7.7A, di_F/dt=100A/\mu s$

5 Electrical characteristics diagrams









6 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics	Diode recovery waveform

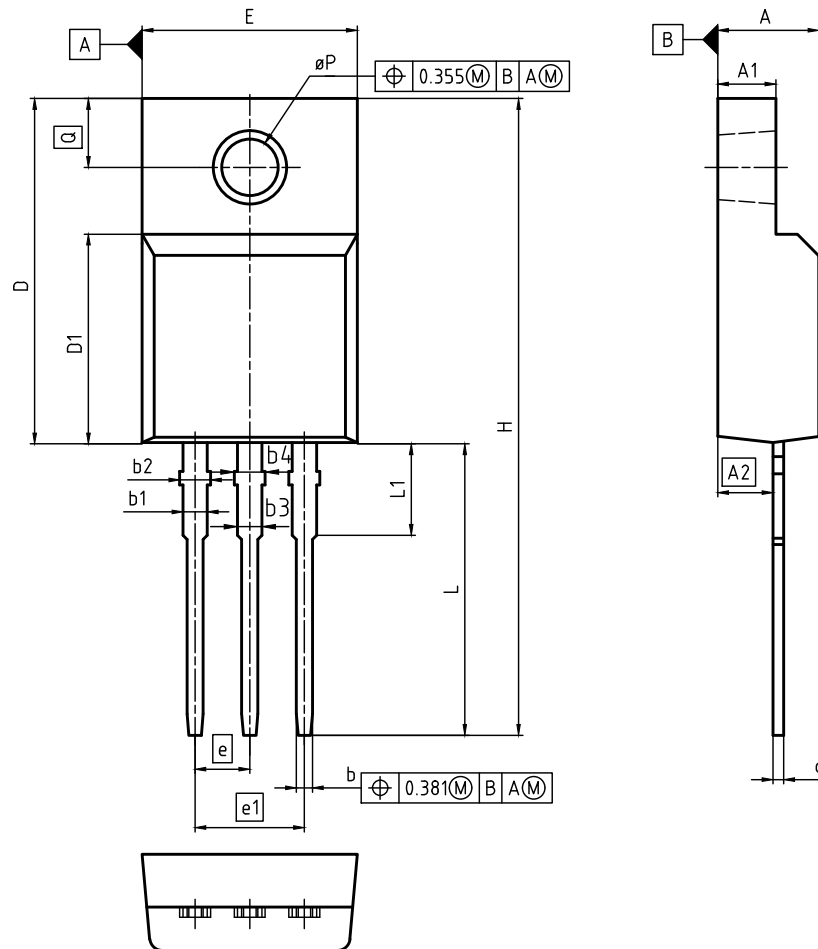
Table 9 Switching times

Switching times test circuit for inductive load	Switching times waveform

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform

7 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.85	0.092	0.112
A2	2.42	2.86	0.095	0.113
b	0.65	0.90	0.026	0.035
b1	0.95	1.38	0.037	0.054
b2	0.95	1.51	0.037	0.059
b3	0.65	1.38	0.026	0.054
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.67	16.15	0.617	0.636
D1	8.97	9.83	0.353	0.387
E	10.00	10.65	0.394	0.419
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	3		3	
H	28.70	29.75	1.130	1.171
L	12.78	13.75	0.503	0.541
L1	2.83	3.45	0.111	0.136
øP	2.95	3.38	0.116	0.133
Q	3.15	3.50	0.124	0.138

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EUROPEAN PROJECTION

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Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

8 Appendix A

Table 11 Related Links

- IFX CoolMOS Webpage: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPA50R190CE

Revision: 2015-08-21, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2011-06-07	Release of final Data sheet
2.0	2011-06-08	Release of final data sheet
2.1	2011-06-16	Release of final data sheet
2.2	2015-08-21	change to standard grade qualification

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