Data Sheet July 2000 File Number 2938.2

12-Bit, 3MSPS, Sampling A/D Converter

The HI5800 is a monolithic, 12-bit, sampling Analog-to-Digital Converter fabricated in the HBC10 BiCMOS process. It is a complete subsystem containing a sample and hold amplifier, voltage reference, two-step subranging A/D, error correction, control logic, and timing generator. The HI5800 is designed for high speed applications where wide bandwidth, accuracy and low distortion are essential.

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

Ordering Information

PART NUMBER	LINEARITY	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HI5800BID	±1 LSB	-40 to 85	40 Ld SBDIP	D40.6
HI5800JCD HI5800KCD	±2 LSB ±1 LSB	0 to 70	40 Ld SBDIP	D40.6
HI5800-EV		25	Evaluation Board	

Features

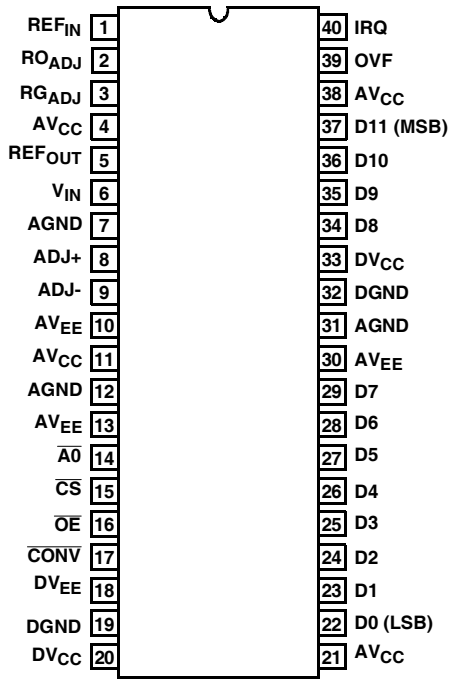
- Throughput Rate 3MSPS
- 12-Bit, No Missing Codes Over Temperature
- Integral Linearity Error . . . . . 1.0 LSB
- Buffered Sample and Hold Amplifier
- Precision Voltage Reference
- Input Signal Range. . . . . ±2.5V
- 20MHz Input BW Allows Sampling Beyond Nyquist
- Zero Latency/No Pipeline Delay

Applications

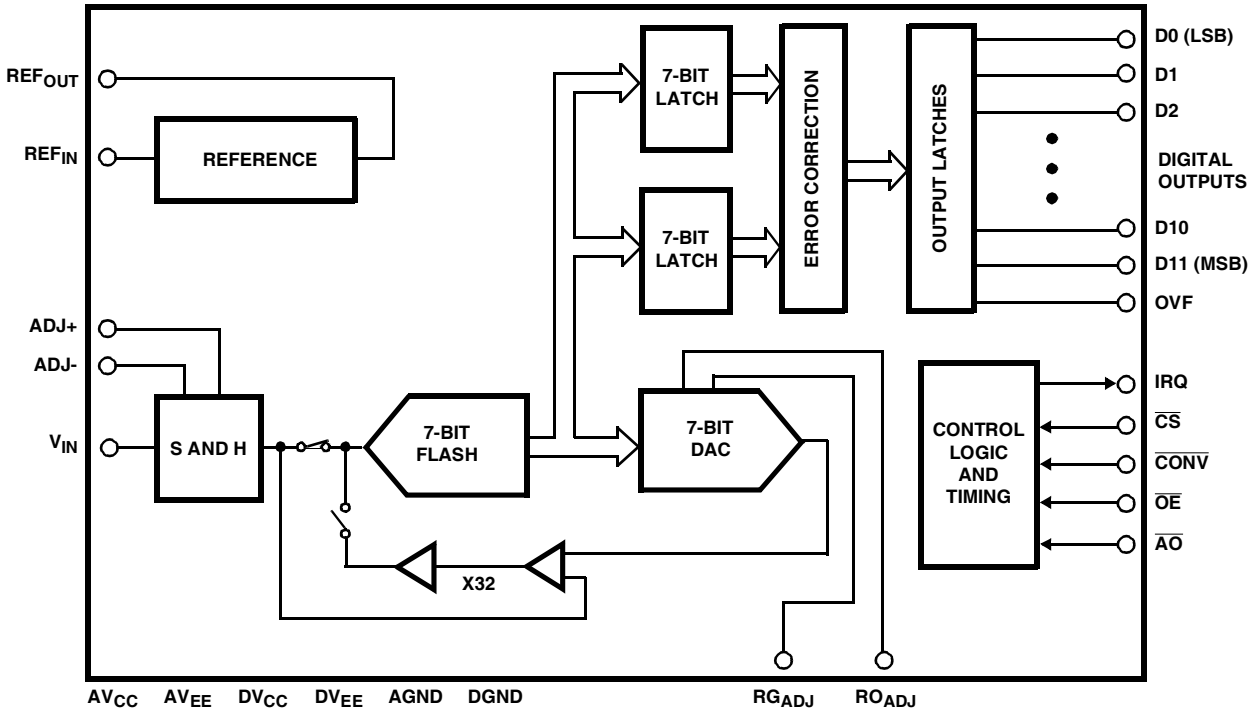
- High Speed Data Acquisition Systems
- Medical Imaging
- Radar Signal Analysis
- Document and Film Scanners
- Vibration/Waveform Spectrum Analysis
- Digital Servo Control

Pinout

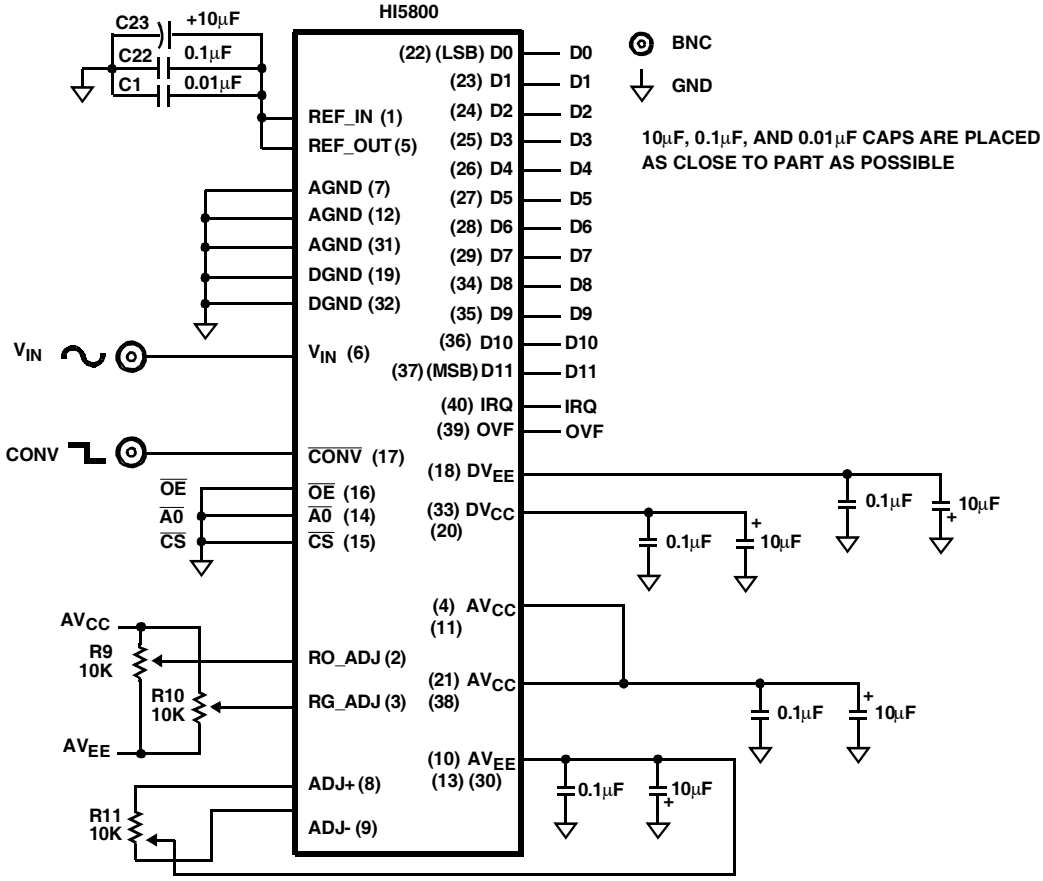
HI5800
(SBDIP)
TOP VIEW



Functional Block Diagram



Typical Application Schematic



Absolute Maximum Ratings

Supply Voltages
- AV_{CC} or DV_{CC} to GND . . . . . +5.5V
- AV_{EE} or DV_{EE} to GND. . . . . -5.5V
- DGND to AGND . . . . . ±0.3V

Analog Input Pins
- Reference Input REF_{IN} . . . . . +2.75V
- Signal Input V_{IN} . . . . . ±(REF_{IN} +0.2V)

RO_{ADJ}, RG_{ADJ}, ADJ+, ADJ- . . . . . V_{EE} to V_{CC}

Digital I/O Pins . . . . . GND to V_{CC}

Operating Conditions

Temperature Range
- HI5800JCD/KCD . . . . . 0°C to 70°C
- HI5800BID . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SBDIP Package	40	15

Maximum Junction Temperature
- SBDIP Package . . . . . 175°C

Maximum Storage Temperature Range . . . . . -65°C to 150°C

Maximum Lead Temperature (Soldering, 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

AV_{CC} = +5V, DV_{CC} = +5V, AV_{EE} = -5V, DV_{EE} = -5V; Internal Reference Used, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS		HI5800JCD 0°C TO 70°C MIN	HI5800JCD 0°C TO 70°C TYP	HI5800JCD 0°C TO 70°C MAX	HI5800KCD, HI5800BID 0°C TO 70°C -40°C TO 85°C MIN	HI5800KCD, HI5800BID 0°C TO 70°C -40°C TO 85°C TYP	HI5800KCD, HI5800BID 0°C TO 70°C -40°C TO 85°C MAX	UNITS
SYSTEM PERFORMANCE									
Resolution			12	-	-	12	-	-	Bits
Integral Linearity Error, INL	f_S = 3MHz, f_{IN} = 45Hz Ramp		-	±0.7	±2	-	±0.5	±1	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_S = 3MHz, f_{IN} = 45Hz Ramp		-	±0.5	±1	-	±0.3	±1	LSB
Offset Error, V_{OS} (Adjustable to Zero)	(Note 8)	JCD, KCD	-	±2	±15	-	±2	±15	LSB
		BID	-	-	-	-	±3	±15	LSB
Full Scale Error, FSE (Adjustable to Zero)	(Note 8)	JCD, KCD	-	±2	±15	-	±2	±15	LSB
		BID	-	-	-	-	±3	±15	LSB
DYNAMIC CHARACTERISTICS (Input Signal Level 0.5dB Below Full Scale)									
Throughput Rate	No Missing Codes		3.0	-	-	3.0	-	-	MSPS
Signal to Noise Ratio (SNR)	f_S = 3MHz, f_{IN} = 20kHz		66	69	-	68	71	-	dB
$= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_S = 3MHz, f_{IN} = 1MHz		65	67	-	67	69	-	dB
Signal to Noise Ratio (SINAD)	f_S = 3MHz, f_{IN} = 20kHz		66	68	-	68	71	-	dB
$= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_S = 3MHz, f_{IN} = 1MHz		65	67	-	67	68	-	dB
Total Harmonic Distortion, THD	f_S = 3MHz, f_{IN} = 20kHz		-	-74	-70	-	-85	-74	dBc
	f_S = 3MHz, f_{IN} = 1MHz		-	-70	-68	-	-77	-70	dBc
Spurious Free Dynamic Range, SFDR	f_S = 3MHz, f_{IN} = 20kHz		71	76	-	76	86	-	dBc
	f_S = 3MHz, f_{IN} = 1MHz		68	72	-	71	77	-	dBc
Intermodulation Distortion, IMD	f_S = 3MHz, f_1 = 49kHz, f_2 = 50kHz (Note 3)		-	-74	-66	-	-79	-70	dBc
Differential Gain	f_S = 1MHz		-	0.9	-	-	0.9	-	%
Differential Phase	f_S = 1MHz		-	0.05	-	-	0.05	-	Degrees
Aperture Delay, t_{AD}	(Note 3)		-	12	20	-	12	20	ns

Electrical Specifications AV_{CC} = +5V, DV_{CC} = +5V, AV_{EE} = -5V, DV_{EE} = -5V; Internal Reference Used, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS		HI5800JCD 0°C TO 70°C MIN	HI5800JCD 0°C TO 70°C TYP	HI5800JCD 0°C TO 70°C MAX	HI5800KCD, HI5800BID 0°C TO 70°C -40°C TO 85°C MIN	HI5800KCD, HI5800BID 0°C TO 70°C -40°C TO 85°C TYP	HI5800KCD, HI5800BID 0°C TO 70°C -40°C TO 85°C MAX	UNITS
Aperture Jitter, t_{AJ}	(Note 3)		-	10	20	-	10	20	ps
ANALOG INPUT									
Input Voltage Range			-	±2.5	±2.7	-	±2.5	±2.7	V
Input Resistance			1	3	-	1	3	-	MΩ
Input Capacitance			-	5	-	-	5	-	pF
Input Current			-	±1	±10	-	±1	±10	µA
Input Bandwidth			-	20	-	-	20	-	MHz
INTERNAL VOLTAGE REFERENCE									
Reference Output Voltage, REF_{OUT} (Loaded)			2.450	2.500	2.550	2.470	2.500	2.530	V
Reference Output Current	(Note 5)		2	-	-	2	-	-	mA
Reference Temperature Coefficient			-	20	-	-	13	-	ppm/°C
REFERENCE INPUT									
Reference Input Range			-	2.5	2.6	-	2.5	2.6	V
Reference Input Resistance			-	200	-	-	200	-	Ω
DIGITAL INPUTS									
Input Logic High Voltage, V_{IH}	(Note 6)		2.0	-	-	2.0	-	-	V
Input Logic Low Voltage, V_{IL}			-	-	0.8	-	-	0.8	V
Input Logic Current, I_{IL}	V_{IN} = 0V, 5V		-	±±1	±10	-	±1	±10	µA
Digital Input Capacitance, C_{IN}	V_{IN} = 0V		-	5	-	-	5	-	pF
DIGITAL OUTPUTS									
Output Logic High Voltage, V_{OH}	I_{OUT} = -160µA		2.4	4.3	-	2.4	4.3	-	V
Output Logic Low Voltage, V_{OL}	I_{OUT} = 3.2mA		-	0.22	0.4	-	0.22	0.4	V
Output Logic High Current, I_{OH}			-0.160	-6	-	-0.160	-6	-	mA
Output Logic Low Current, I_{OL}			3.2	6	-	3.2	6	-	mA
Output Three-State Leakage Current, I_{OZ}	V_{OUT} = 0V, 5V		-	±±1	±10	-	±1	±10	µA
Digital Output Capacitance, C_{OUT}			-	10	-	-	10	-	pF
TIMING CHARACTERISTICS									
Minimum $\overline{CONV}$ Pulse, t_1	(Notes 3, 4)		10	-	-	10	-	-	ns
$\overline{CS}$ to $\overline{CONV}$ Setup Time, t_2	(Note 3)		10	-	-	10	-	-	ns
$\overline{CONV}$ to $\overline{CS}$ Setup Time, t_3	(Note 3)		0	-	-	0	-	-	ns
Minimum $\overline{OE}$ Pulse, t_4	(Notes 3, 5)		15	-	-	15	-	-	ns
$\overline{CS}$ to $\overline{OE}$ Setup Time, t_5	(Note 3)		0	-	-	0	-	-	ns
$\overline{OE}$ to $\overline{CS}$ Setup Time, t_6	(Note 3)		0	-	-	0	-	-	ns
IRQ Delay from Start Convert, t_7	(Note 3)		10	20	25	10	20	25	ns
IRQ Pulse Width, t_8		JCD, KCD	190	200	230	190	200	230	ns
		BID	-	-	-	180	195	230	ns
Minimum Cycle Time for Conversion, t_9			-	325	333	-	325	333	ns
IRQ to Data Valid Delay, t_{10}	(Note 3)		-5	0	+5	-5	0	+5	ns
Minimum $\overline{A0}$ Pulse, t_{11}	(Notes 3, 5)		10	-	-	10	-	-	ns

Electrical Specifications AV_{CC} = +5V, DV_{CC} = +5V, AV_{EE} = -5V, DV_{EE} = -5V; Internal Reference Used, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	HI5800JCD 0°C TO 70°C			HI5800KCD, HI5800BID 0°C TO 70°C -40°C TO 85°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Data Access from $\overline{OE}$ Low, t_{12}	(Note 3)	10	18	25	10	18	25	ns
LSB, Nibble Delay from $\overline{A0}$ High, t_{13}	(Note 3)	-	10	20	-	10	20	ns
MSB Delay from $\overline{A0}$ Low, t_{14}	(Note 3)	-	14	20	-	14	20	ns
$\overline{CS}$ to Float Delay, t_{15}	(Note 3)	10	18	25	10	18	25	ns
Minimum $\overline{CS}$ Pulse, t_{16}	(Notes 3, 5)	15	-	-	15	-	-	ns
$\overline{CS}$ to Data Valid Delay, t_{17}	(Note 3)	10	18	25	10	18	25	ns
Output Fall 2 Time, t_f	(Note 3)	-	5	20	-	5	20	ns
Output Rise Time, t_r	(Note 3)	-	5	20	-	5	20	ns
POWER SUPPLY CHARACTERISTICS								
IV_{CC}		-	170	220	-	170	220	mA
IV_{EE}		-	150	190	-	150	190	mA
IDV_{CC}		-	24	40	-	24	40	mA
IDV_{EE}		-	2	5	-	2	5	mA
Power Dissipation		-	1.7	2.2	-	1.7	2.2	W
PSRR	V_{CC}, V_{EE} ±5%	-	0.01	-	-	±0.01	-	%/%

NOTES:

2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Parameter guaranteed by design or characterization and not production tested.
4. Recommended pulse width for $\overline{CONV}$ is 60ns.
5. Recommended minimum pulse width is 25ns.
6. This is the additional current available from the REF_{OUT} pin with the REF_{OUT} pin driving the REF_{IN} pin.
7. The $\overline{A0}$ pin V_{IH} at -40°C may exceed 2.0V by up to 0.4V at initial power up.
8. Excludes error due to internal reference temperature drift.

Timing Diagrams

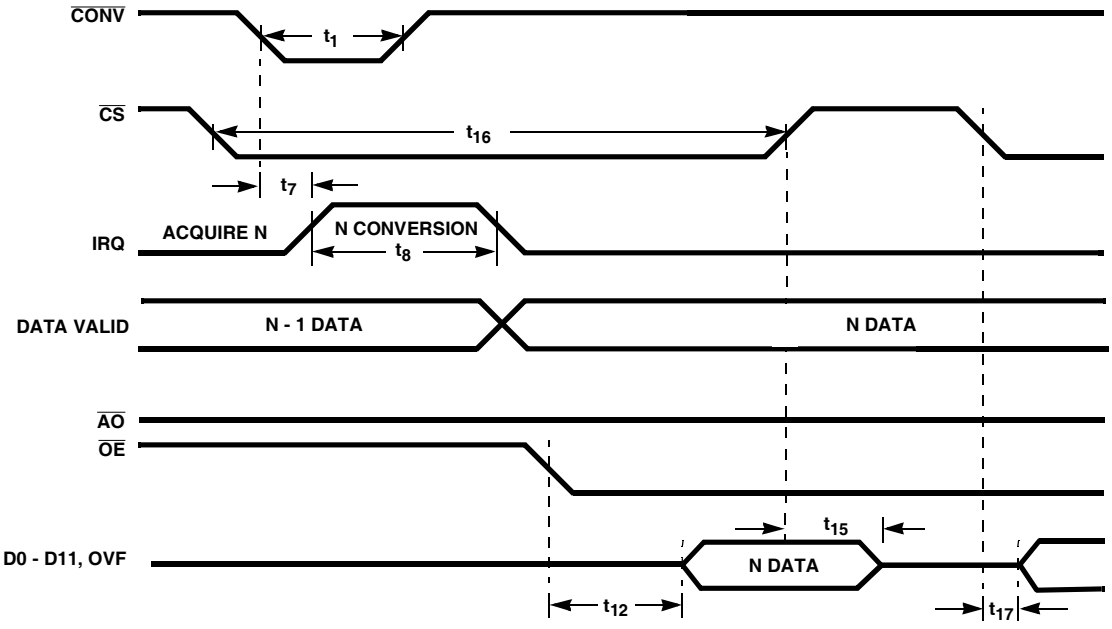


FIGURE 1. SINGLE SHOT TIMING

Timing Diagrams (Continued)

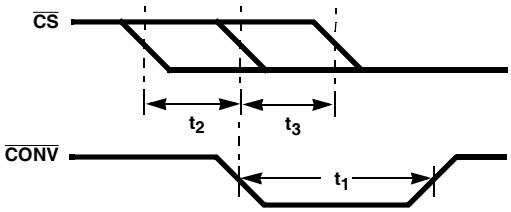


FIGURE 2A. START CONVERSION SETUP TIME

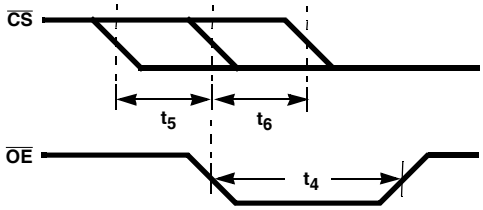


FIGURE 2B. OUTPUT ENABLE SETUP TIME

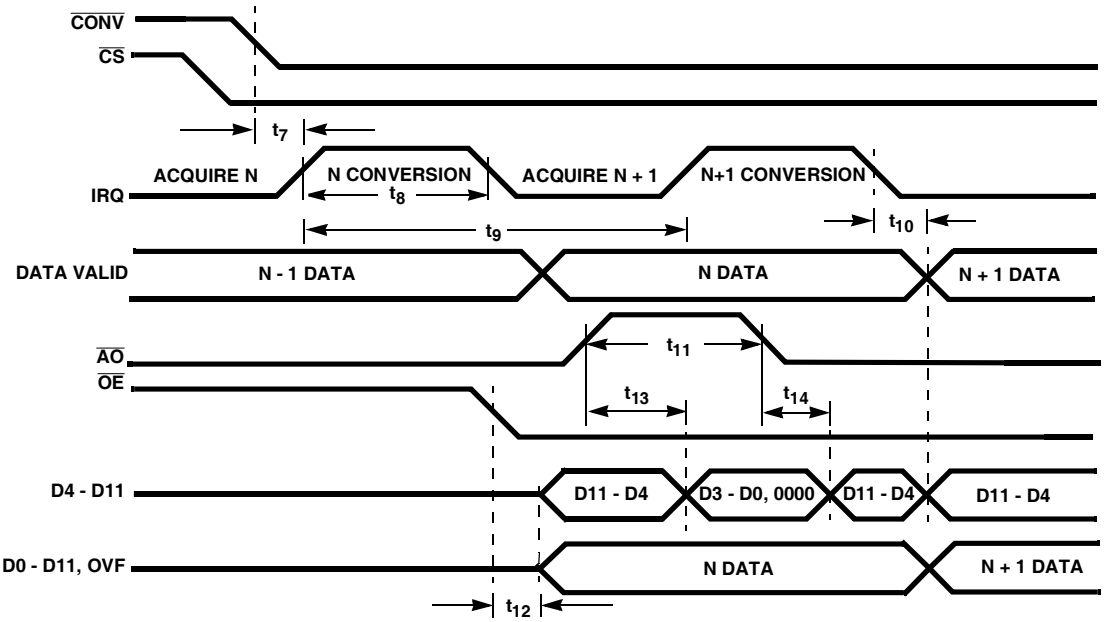


FIGURE 3. CONTINUOUS CONVERSION TIMING

Typical Performance Curves

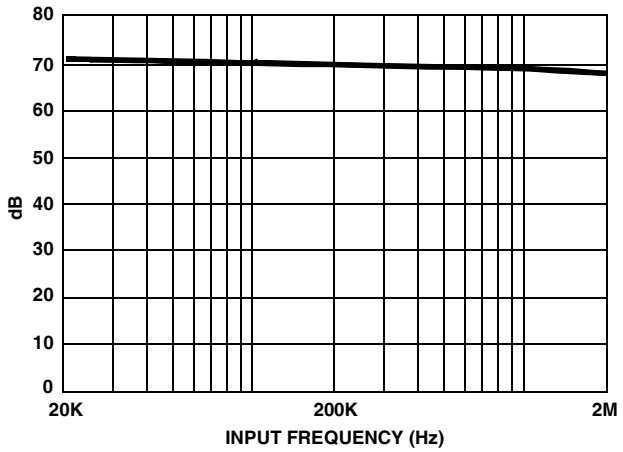


FIGURE 4. TYPICAL SNR vs INPUT FREQUENCY

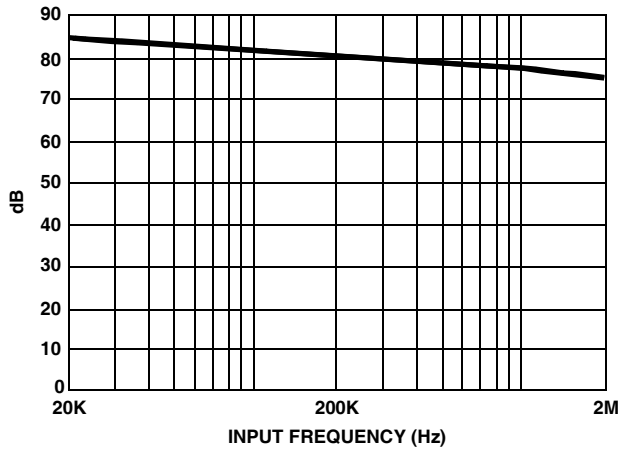


FIGURE 5. TYPICAL THD vs INPUT FREQUENCY

Typical Performance Curves (Continued)

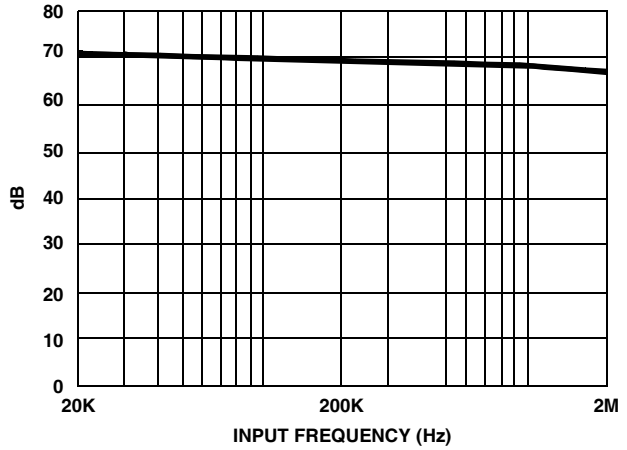


FIGURE 6. TYPICAL SINAD vs INPUT FREQUENCY

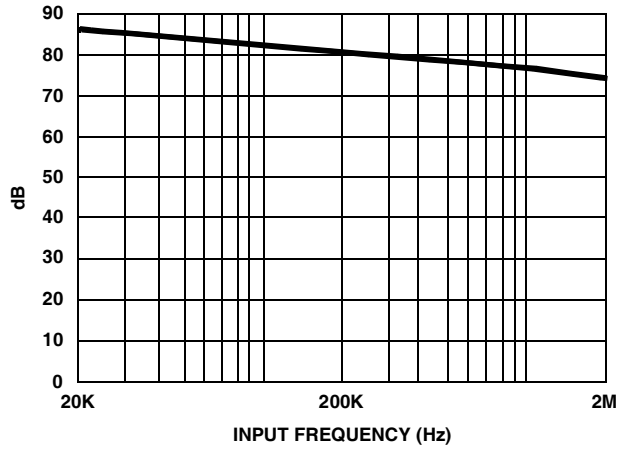


FIGURE 7. TYPICAL SFDR vs INPUT FREQUENCY

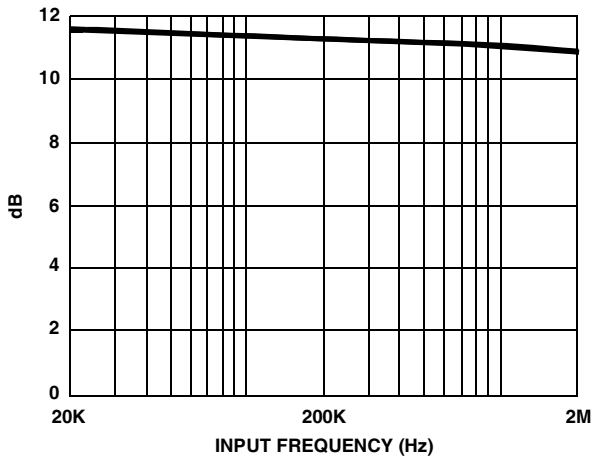


FIGURE 8. TYPICAL EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY

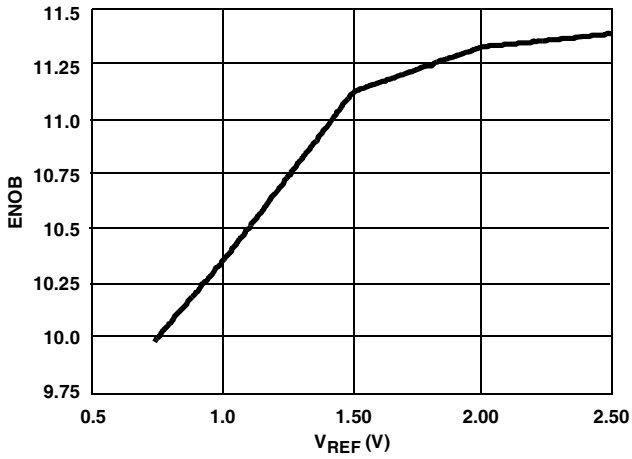


FIGURE 9. EFFECTIVE NUMBER OF BITS vs REFERENCE VOLTAGE (f_S = 3MHz, f_{IN} = 20kHz)

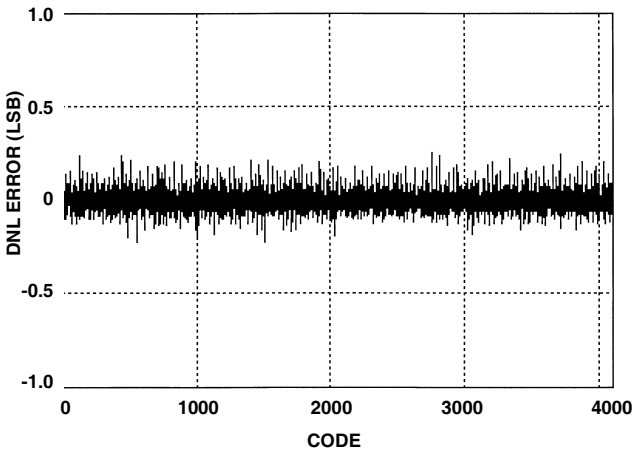


FIGURE 10. DIFFERENTIAL NON-LINEARITY

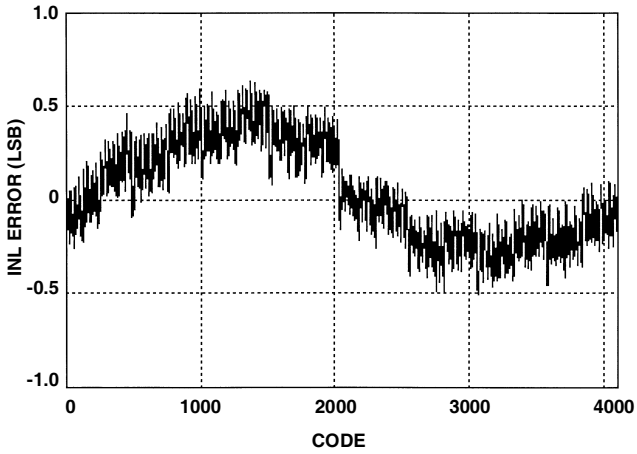


FIGURE 11. INTEGRAL NON-LINEARITY

Typical Performance Curves (Continued)

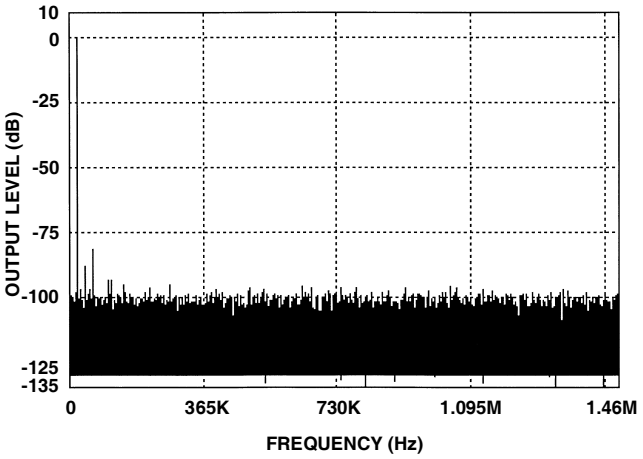


FIGURE 12. FFT SPECTRAL PLOT FOR f_{IN} = 20kHz, f_S = 3MHz

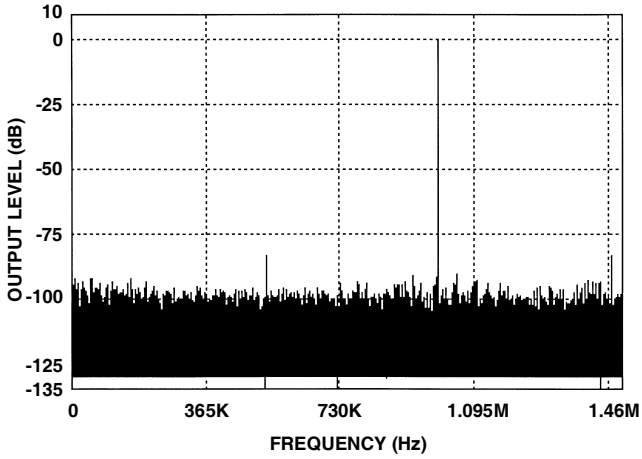


FIGURE 13. FFT SPECTRAL PLOT FOR f_{IN} = 1MHz, f_S = 3MHz

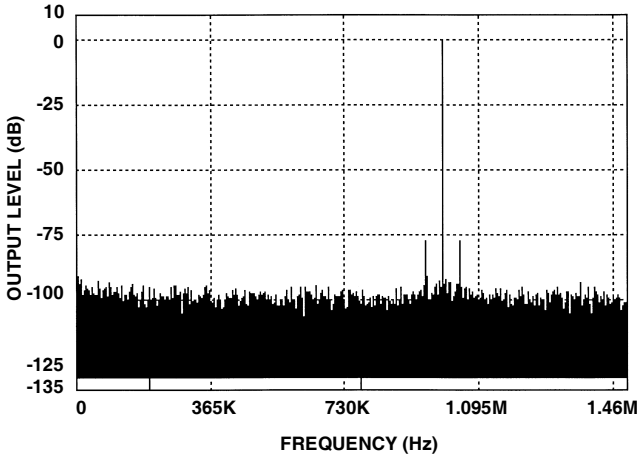


FIGURE 14. FFT SPECTRAL PLOT FOR f_{IN} = 2MHz, f_S = 3MHz

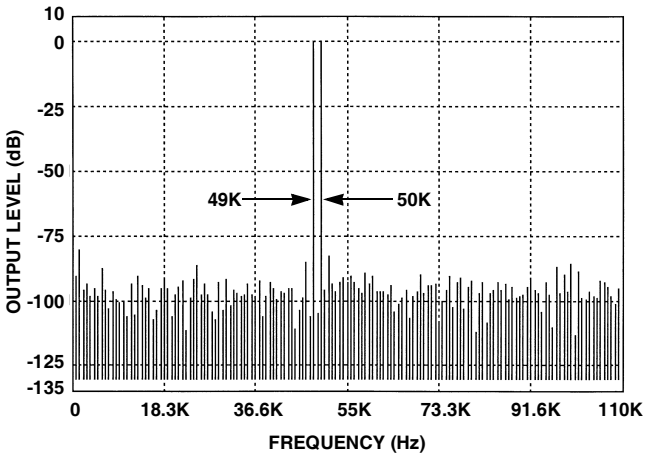


FIGURE 15. INTERMODULATION DISTORTION PLOT FOR f_{IN} = 49kHz, 50kHz at f_S = 3MHz

Pin Descriptions

PIN #	SYMBOL	PIN DESCRIPTION
1	REF_{IN}	External Reference Input.
2	RO_{ADJ}	DAC Offset Adjust (Connect to AGND If Not Used).
3	RG_{ADJ}	DAC Gain Adjust (Connect to AGND If Not Used).
4	AV_{CC}	Analog Positive Power Supply, +5V.
5	REF_{OUT}	Internal Reference Output, +2.5V.
-	NC	No Connection.
6	V_{IN}	Analog Input Voltage.
7	AGND	Analog Ground.
8	ADJ+	Sample/Hold Offset Adjust (Connect to AGND If Not Used).
9	ADJ-	Sample/Hold Offset Adjust (Connect to AGND If Not Used).

Pin Descriptions (Continued)

PIN #	SYMBOL	PIN DESCRIPTION
10	AV_{EE}	Analog Negative Power Supply, -5V.
11	AV_{CC}	Analog Positive Power Supply, +5V.
12	AGND	Analog Ground.
13	AV_{EE}	Analog Negative Power Supply, -5V.
14	$\overline{A0}$	Output Byte Control Input, active low. When low, data is presented as a 12-bit word or the upper byte (D11 - D4) in 8-bit mode. When high, the second byte contains the lower LSBs (D3 - D0) with 4 trailing zeroes. See Text.
15	$\overline{CS}$	Chip Select Input, active low. Dominates all control inputs.
-	NC	No Connection.
16	$\overline{OE}$	Output Enable Input, active low.
17	$\overline{CONV}$	Convert Start Input. Initiates conversion on the falling edge. If held low, continuous conversion mode overrides and remains in effect until the input goes high.
18	DV_{EE}	Digital Negative Power Supply, -5V.
19	DGND	Digital Ground.
20	DV_{CC}	Digital Positive Power Supply, +5V.
21	AV_{CC}	Analog Positive Power Supply, +5V.
22	D0	Data Bit 0, (LSB).
23	D1	Data Bit 1.
24	D2	Data Bit 2.
25	D3	Data Bit 3.
-	NC	No Connection
26	D4	Data Bit 4.
27	D5	Data Bit 5.
28	D6	Data Bit 6.
29	D7	Data Bit 7.
30	AV_{EE}	Analog Negative Power Supply, -5V.
31	AGND	Analog Ground.
32	DGND	Digital Ground.
33	DV_{CC}	Digital Positive Power Supply, +5V.
34	D8	Data Bit 8.
35	D9	Data Bit 9.
-	NC	No Connection.
36	D10	Data Bit 10.
37	D11	Data Bit 11 (MSB).
38	AV_{CC}	Analog Positive Power Supply, +5V.
39	OVF	Overflow Output. Active high when either an overrange or underrange analog input condition is detected.
40	IRQ	Interrupt ReQuest Output. Goes low when a conversion is complete.

Description

The HI5800 is a 12-bit, two-step, sampling analog-to-digital converter which uses a subranging technique with digital error correction. As illustrated in the block diagram, it uses a sample and hold front end, 7-bit, R-2R D/A converter which is laser trimmed to 14 bits accuracy, a 7-bit BiCMOS flash converter, precision bandgap reference, digital controller and timing generator, error correction logic, output latches and BiCMOS output drivers.

The falling edge of the convert command signal puts the sample and hold (S/H) in the hold mode and the conversion process begins. At this point the Interrupt Request (IRQ) line is set high indicating that a conversion is in progress. The output of the S/H circuit drives the input of the 7-bit flash converter through a switch. After allowing the flash to settle, the intermediate output of the flash is stored in the latches which feed the D/A and error correction logic. The D/A reconstructs the analog signal and feeds the gain amplifier whose summing node subtracts the held signal of the S/H and amplifies the residue by 32. This signal is then switched to the flash for a second pass using the input switch. The output of the second flash conversion is fed directly to the error correction which reconstructs the twelve bit word from the fourteen bit input. The logic also decodes the overflow bit and the polarity of the overflow. The output of the error correction is then gated through the read controller to the output drivers. The data is ready on the bus as soon as the IRQ line goes low.

I/O Control Inputs

The converter has four active low inputs ($\overline{CS}$, $\overline{CONV}$, $\overline{OE}$ and $\overline{A0}$) and fourteen outputs (D0 - D11, IRQ and OVF). All inputs and outputs are TTL compatible and will also interface to the newer TTL compatible families. All four inputs are CMOS high input impedance stages and all outputs are BiMOS drivers capable of driving 100pF loads.

In order to initiate a conversion or read the data bus, $\overline{CS}$ should be held low. The conversion is initiated by the falling edge of the $\overline{CONV}$ command. The $\overline{OE}$ input controls the output bus directly and is independent of the conversion process. The data on the bus changes just before the IRQ goes low. Therefore if the $\overline{OE}$ line is held low all the time, the data on the bus will change just before the IRQ line goes low. The byte control signal $\overline{A0}$ is also independent of the conversion process and the byte can be manipulated anytime. When $\overline{A0}$ is low the 12-bits and overflow word is read on the bus. The bus can also be hooked up such that the upper byte (D11 - D4) is read when $\overline{A0}$ is low. When $\overline{A0}$ is high, the lower byte (D3 - D0) is output on the same eight pins with trailing zeros.

In order to minimize switching noise during a conversion, byte manipulations done using the $\overline{A0}$ signal should be done in the single shot mode and $\overline{A0}$ should be changed during the acquisition phase. For accuracy, allow sufficient time for settling from any glitches before the next conversion.

Once a conversion is started, the converter will complete the conversion and acquisition periods irrespective of the input states. If during these cycles another convert command is issued, it will be ignored until the acquire phase is complete.

Stand Alone Operation

The converter can be operated in a stand alone configuration with bus inputs controlling the converter. The conversion will be started on the negative edge of the convert ($\overline{CONV}$) pulse as long as this pulse is less than the converter throughput rate. If the converter is given multiple convert commands, it will ignore all but the first command until such time when the acquisition period of the next cycle is complete. At this point it will start a new conversion on the first negative edge of the input command. This allows the converter to be synchronized to a multiple of a faster external clock. The new output data of the conversion is available on the same cycle at the negative edge of the IRQ pulse and is valid until the next negative edge of the IRQ pulse. Data may be accessed at any time during these cycles. It should be noted that if the data bus is kept enabled all the time ($\overline{OE}$ is low), then the data will be updating just before the IRQ goes low. During this time, the data may not be valid for a few nanoseconds.

Continuous Convert Mode

The converter can be operated at its maximum rate by taking the $\overline{CONV}$ line low (supplying the first negative edge) and holding it low. This enables the continuous convert mode. During this time, at the end of the internal acquisition period, the converter automatically starts a new conversion. The data will be valid between the IRQ negative edges.

Note that there is no pipeline delay on the data. The output data is available during the same cycle as the conversion and is valid until the next conversion ends. This allows data access to both previous and present conversions in the same cycle.

When initiating a conversion or a series of conversions, the last signal ($\overline{CS}$ and $\overline{CONV}$) to arrive dominates the function. The same condition holds true for enabling the bus to read the data ($\overline{CS}$ and $\overline{OE}$). To terminate the bus operations, the first signal ($\overline{CS}$ and $\overline{OE}$) to arrive dominates the function.

Interrupt Request Output

The interrupt request line (IRQ) goes high at the start of each conversion and goes low to indicate the start of the acquisition. During the time that IRQ is high, the internal sample and hold is in hold mode. At the termination of IRQ, the sample and hold switches to acquire mode which lasts approximately 100ns. If no convert command is issued for a period of time, the sample and hold simply remains in acquire mode tracking the analog input signal until the next conversion cycle is initiated. The IRQ line is the only output that is not three-stateable.

Analog Input, V_{IN}

The analog input of the HI5800 is coupled into the input stage of the Sample and Hold amplifier. The input is a high impedance bipolar differential pair complete with an ESD protection circuit. Typically it has >3MΩ input impedance. With this high input impedance circuit, the HI5800 is easily

interfaced to any type of op amp without a requirement for a high drive capability. Adequate precautions should be taken while driving the input from high voltage output op amps to ensure that the analog input pin is not overdriven above the specified maximum limits. For a +2.5V reference, the analog input range is ±2.5V. This input range scales with the value of the external reference voltage if the internal reference is not used. For best performance, the analog ground pin next to the analog input should be utilized for signal return.

Figures 16 and 17 illustrate the use of an input buffer as a level shifter to convert a unipolar signal to the bipolar input used by the HI5800. Figure 16 is an example of a non-inverting buffer that takes a 0 to 2.5V input and shifts it to ±2.5V. The gain can be calculated from:

$$V_{OUT} = \left[1 + \frac{R2}{(R1 \| R3)}\right] \times V_{IN} - \left[\frac{R1}{R1 + R3}\right] \times V_{OFFSET}$$

$$R1 \| R_3 = \frac{R1R3}{R1 + R3}$$

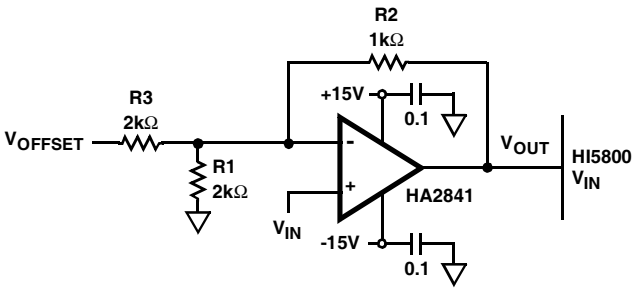


FIGURE 16. NON-INVERTING BUFFER

Figure 17 is an example of an inverting buffer that level shifts a 0V to 5V input to ±2.5V. Its gain can be calculated from:

$$V_{OUT} = (-R2/R1) \times V_{IN} - (R2/R3) \times V_{OFFSET}.$$

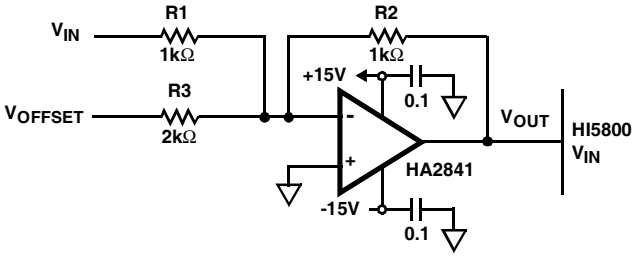


FIGURE 17. INVERTING BUFFER

Note that the correct op amp must be chosen in order to not degrade the overall dynamic performance of the circuit. Recommended op amps are called out in the figures.

Voltage Reference, REF_{OUT}

The HI5800 has a curvature corrected internal band-gap reference generator with a buffer amplifier capable of driving up to 15mA. The band-gap and amplifier are trimmed to give +2.50V. When connected to the reference input pin REF_{IN}, the reference is capable of driving up to 2mA externally. Further loading may degrade the performance of the output voltage. It is recommended that the output of the reference be decoupled with good quality capacitors to reduce the high frequency noise.

Reference Input, REF_{IN}

The converter requires a voltage reference connected to the REF_{IN} pin. This can be the above internal reference or it can be an external reference. It is recommended that adequate high frequency decoupling is provided at the reference input pin in order to minimize overall converter noise.

A user trying to provide an external reference to a HI5800 is faced with two problems. First, the drift of the reference over temperature must be very low. Second, it must be capable of driving the 200Ω input impedance seen at the REF_{IN} pin of the HI5800. Figure 18 is a recommended circuit for doing this that is capable of 2ppm/^{O}C drift over temperature.

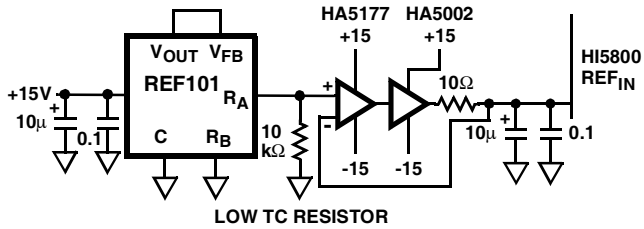


FIGURE 18. EXTERNAL REFERENCE

Supply and Ground Considerations

The HI5800 has separate analog and digital supply and ground pins to help keep digital noise out of the analog signal path. For the best performance, the part should be mounted on a board that provides separate low impedance planes for the analog and digital supplies and grounds. Only connect the two grounds together at one place preferably as close as possible to the part. The supplies should be driven by clean linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the HI5800.

If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Also, it is recommended that the turn-on power supply sequencing be such that the analog positive supply, AI_{CC}, come up first, followed by the remaining supplies.

Refer to the Application Note “Using Intersil High Speed A/D Converters” (AN9214) for additional suggestions to consider when using the HI5800.

Error Adjustments

For most applications the accuracy of the HI5800 is sufficient without any adjustments. In applications where accuracy is of utmost importance three external adjustments are possible: S/H offset, D/A offset and D/A gain. Figure 19 illustrates the use of external potentiometers to reduce the HI5800 errors to zero.

The D/A offset (RO_{ADJ}) and S/H offset (ADJ+ and ADJ-) trims adjust the voltage offset of the transfer curve while the

D/A gain trim (RG_{ADJ}) adjusts the tilt of the transfer curve around the curve midpoint (code 2048). The 10kΩ potentiometers can be installed to achieve the desired adjustment in the following manner.

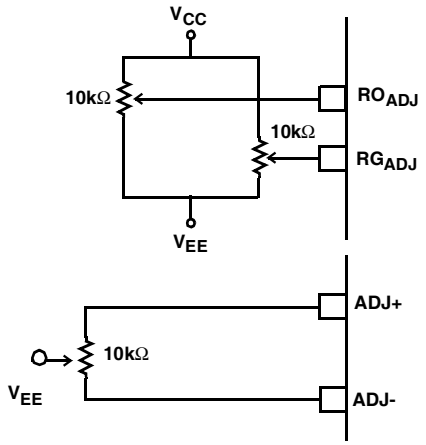


FIGURE 19. D/A OFFSET, D/A GAIN AND S/H OFFSET ADJUSTMENTS

Typically only one of the offset trimpots needs to be used. The offset should first be adjusted to get code 2048 centered at a desired DC input voltage such as 0V. Next the gain trim can be adjusted by trimming the gain pot until the 4094 to 4095 code transition occurs at the desired voltage (2.500V - 1.5 LSBs for a 2.5V reference). The gain trim can also be done by adjusting the gain pot until the code 0 to 1 transition occurs at a particular voltage (-2.5V + 0.5 LSBs for a 2.5V reference). If a nonzero offset is needed, then the offset pot can be adjusted after the gain trim is finished. The gain trim is simplified if an offset trim to zero is done first with a nonzero offset trim done after the gain trim is finished. The D/A offset and S/H offset trimpots have an identical effect on the converter except that the S/H offset is a finer resolution trim. The D/A offset and D/A gain typically have an adjustment range of ±30 LSBs and the S/H offset typically has an adjustment range of ±20 LSBs.

TABLE 1. I/O TRUTH TABLE

INPUTS				OUTPUT	
CS	**CONV**	**OE**	**A0**	**IRQ**	**FUNCTION**
1	X	X	X	X	No operation.
0	0	X	X	X	Continuous convert mode.
0	X	0	0	X	Outputs all 12-bits and OVF or upper byte D11 - D4 in 8 bit mode.
0	X	0	1	X	In 8-bit mode, outputs lower LSBs D3 - D0 followed by 4 trailing zeroes and OVF (See text).
0	1	X	X	0	Converter is in acquisition mode.
0	X	X	X	1	Converter is busy doing a conversion.
0	X	1	X	X	Data outputs and OVF in high impedance state.

X's = Don't Care

TABLE 2. A/D OUTPUT CODE TABLE

CODE DESCRIPTION $LSB = \frac{2(REF_{IN})}{4096}$	(NOTE) INPUT VOLTAGE REF_{IN} = 2.5V (V)	OUTPUT DATA (OFFSET BINARY) MSB												LSB
		OVF	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
≥+FS (Full Scale)	≥ +2.5000	1	1	1	1	1	1	1	1	1	1	1	1	1
+FS - 1 LSB	+2.49878	0	1	1	1	1	1	1	1	1	1	1	1	1
$+^3/_4$ FS	+1.8750	0	1	1	1	0	0	0	0	0	0	0	0	0
$+^1/_2$ FS	+1.2500	0	1	1	0	0	0	0	0	0	0	0	0	0
+1 LSB	+0.00122	0	1	0	0	0	0	0	0	0	0	0	0	1
0	0.0000	0	1	0	0	0	0	0	0	0	0	0	0	0
-1 LSB	-0.00122	0	0	1	1	1	1	1	1	1	1	1	1	1
$-^1/_2$ FS	-1.2500	0	0	1	0	0	0	0	0	0	0	0	0	0
$-^3/_4$ FS	-1.8750	0	0	0	1	0	0	0	0	0	0	0	0	0
-FS + 1 LSB	-2.49878	0	0	0	0	0	0	0	0	0	0	0	0	1
≤-FS	≤ -2.5000	1	0	0	0	0	0	0	0	0	0	0	0	0

NOTE: The voltages listed above represent the ideal center of each output code shown as a function of the reference voltage.

If no external adjustments are required the following pins should be connected to analog ground (AGND) for optimum performance: RO_{ADJ}, RG_{ADJ}, ADJ+, and ADJ-.

Typical Application Schematic

A typical application schematic diagram for the HI5800 is shown with the block diagram. The adjust pins are shown with 10kΩ potentiometers used for gain and offset adjustments. These potentiometers may be left out and the respective pins should be connected to ground for best untrimmed performance.

Definitions

Static Performance Definitions

Offset, Full scale, and gain all use a measured value of the internal voltage reference to determine the ideal plus and minus full scale values. The results are all displayed in LSBs.

Offset Error (V_{OS})

The first code transition should occur at a level $^1/_2$ LSB above the negative full scale. Offset is defined as the deviation of the actual code transition from this point. Note that this is adjustable to zero.

Full Scale Error (FSE)

The last code transition should occur for a analog input that is $1^1/_2$ LSBs below positive full scale. Full scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB. The converter is guaranteed for no missing codes over all temperature ranges.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Rejection (PSRR)

Each of the power supplies are moved plus and minus 5% and the shift in the offset and full scale error is noted. The number reported is the percent change in these parameters versus full scale divided by the percent change in the supply.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5800. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full scale for all these tests. Distortion results are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02,$$

where: $V_{CORR} = 0.5dB$.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component. If the harmonics are buried in the noise floor it is the largest peak.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present on the inputs. The ratio of the measured signal to the distortion terms is calculated. The IMD products used to calculate the total distortion are (f_2-f_1), (f_2+f_1), $(2f_1-f_2)$, $(2f_1+f_2)$, $(2f_2-f_1)$, $(2f_2+f_1)$, $(3f_1-f_2)$, $(3f_1+f_2)$, $(3f_2-f_1)$, $(3f_2+f_1)$, $(2f_2-2f_1)$, $(2f_2+2f_1)$, $(2f_1)$, $(2f_2)$, $(2f_1)$, $(2f_2)$, $(4f_1)$, $(4f_2)$. The data reflects the sum of all the IMD products.

Full Power Input Bandwidth

Full power input bandwidth is the frequency at which the amplitude of the fundamental of the digital output word has decreased 3dB below the amplitude of an input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Die Characteristics

DIE DIMENSIONS:

202 mils x 283 mils x 19 mils

METALLIZATION:

Metal 1: Type: AlSiCu, Thickness: 6kÅ +1500A/-750Å
Metal 2: Type: AlSiCu, Thickness: 16kÅ +2500A/-1100Å

PASSIVATION:

Type: Sandwich Passivation - Nitride + Undoped Si Glass (USG)
Thickness: Nitride - 4KÅ, USG - 8KÅ, Total - 12kÅ ±2kÅ

TRANSISTOR COUNT:

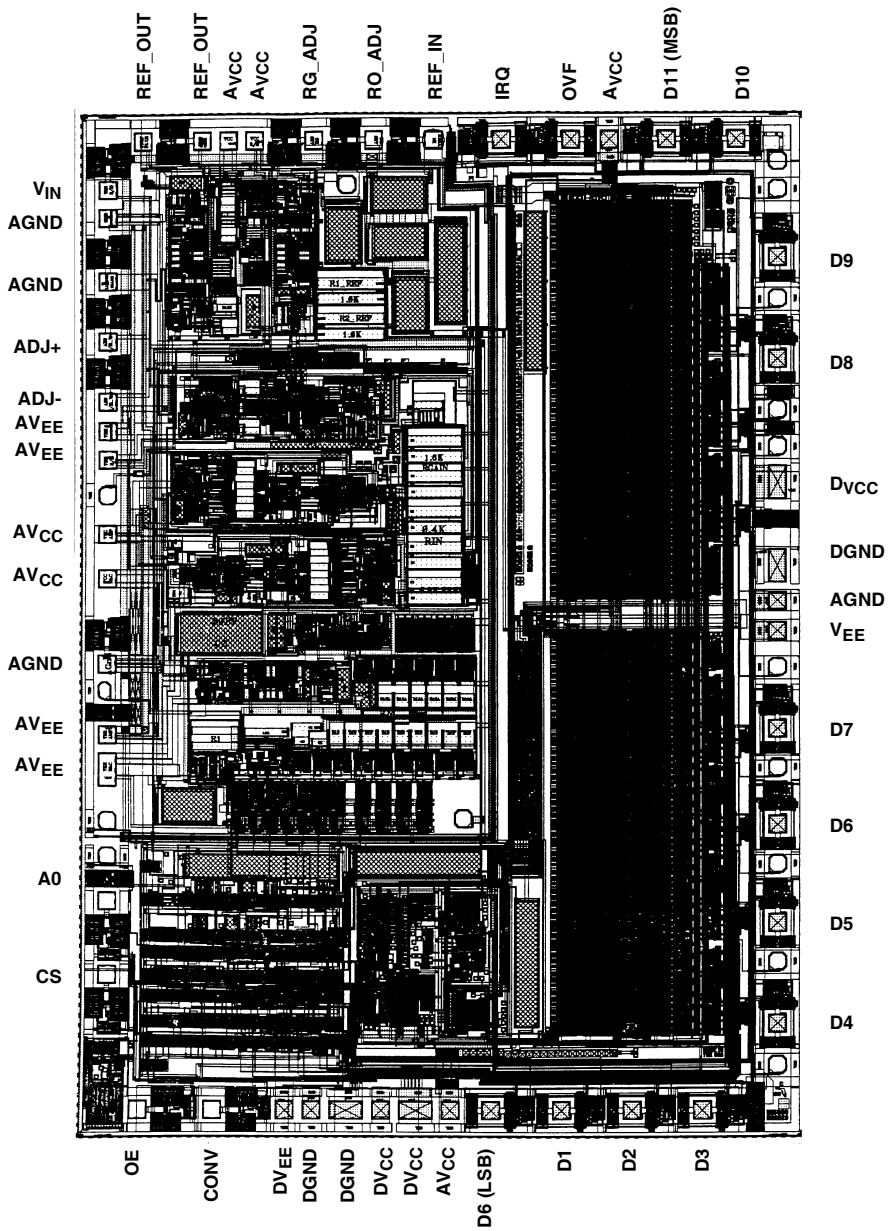
10K

SUBSTRATE POTENTIAL (POWERED UP):

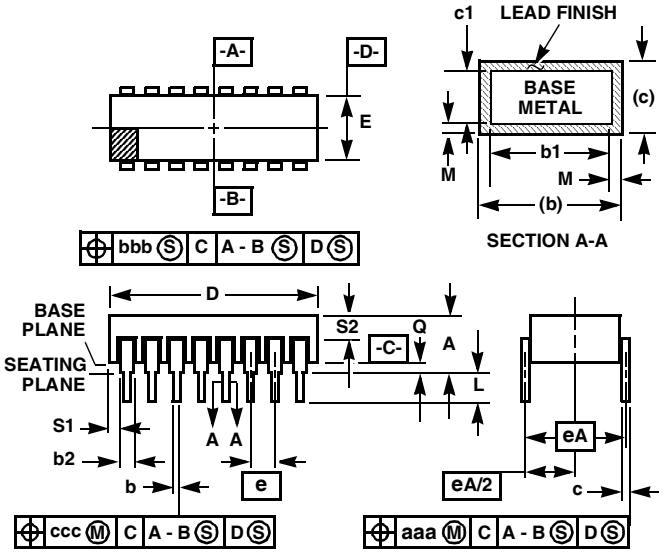
V_{EE}

Metallization Mask Layout

HI5800



Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D40.6 MIL-STD-1835 CDIP2-T40 (D-5, CONFIGURATION C)
40 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	2.096	-	53.24	4
E	0.510	0.620	12.95	15.75	4
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	40		40		8

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