19-4584; Rev 1; 6/10

EVALUATION KIT AVAILABLE

12-Channel, High-Voltage Battery-Pack Fault Monitors

General Description

The MAX11080/MAX11081 are battery-pack fault-monitor ICs capable of monitoring up to 12 lithium-ion (Li+) battery cells. This device is designed to provide an overvoltage or undervoltage fault indication when any of the cells cross the user-selectable threshold for longer than the set program-delay interval. The overvoltage levels are pin selectable from +3.3V to +4.8V in 100mV increments, and have a guaranteed accuracy of ±25mV over the entire temperature range. The undervoltage level is also user selectable from +1.6V to +2.8V in 200mV increments. These levels are guaranteed to ±100mV over the entire temperature range. Undervoltage detection can be disabled as one of the user-configuration options.

The MAX11080/MAX11081 have a built-in level-shifter that allows up to 31 MAX11080/MAX11081 devices to be connected in a daisy-chain fashion to reduce the number of interface signals needed for large stacks of series batteries. Each cell is monitored differentially and compared to the overvoltage and undervoltage thresholds. When any of the cells exceed this threshold for longer than the set program delay interval, the MAX11080/MAX11081 inhibit the heartbeat signal from being passed down the daisy-chain. Built-in comparator hysteresis prevents threshold chattering.

The MAX11080/MAX11081 are designed to be the perfect complement to the MAX11068 high-voltage measurement IC for redundant fault-monitoring applications. This device is offered in a 9.7mm x 4.4mm, 38-pin TSSOP package with 0.5mm pin spacing. The package is lead-free and RoHS compliant with an extended operating temperature range of -40°C to +105°C.

Applications

High-Voltage, Multicell-Series-Stacked Battery Systems

Electric Vehicles

Hybrid Electric Vehicles

Electric Bikes

High-Power Battery Backup

Solar Cell Battery Backup

Super-Cap Battery Backup

Features

- **Up to 12-Cell Li+ Battery Voltage Fault Detection**
- **Operation from 6.0V to 72V**
- **Pin-Selectable Overvoltage Threshold from +3.3V to +4.8V in 100mV Increments**
  - **±25mV Overvoltage-Detection Accuracy**
- **Pin-Selectable Undervoltage Threshold from +1.6V to +2.8V in 200mV Increments**
  - **±100mV Undervoltage-Detection Accuracy**
- **Overvoltage/Undervoltage-Threshold Detection Hysteresis**
  - **MAX11080: 300mV**
  - **MAX11081: 37.5mV**
- **Programmable Delay Time of Alarm Detection from 3.0ms to 3.32s with an External Capacitor**
- **Daisy-Chained Alarm and Shutdown Functions with Heartbeat Status Signal**
  - **Up to 31 Devices Can Be Connected**
- **Ultra-Low-Power Dissipation**
  - **Operating-Mode Current Drain: 80µA**
  - **Shutdown-Mode Current: 2µA**
- **Wide Operating Temperature Range from -40°C to +105°C (AEC-Q100, Type 2)**
- **9.7mm x 4.4mm, 38-Pin TSSOP Package**
- **Lead(Pb)-Free and RoHS Compliant**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX11080GUU/V+	-40°C to +105°C	38 TSSOP
MAX11081GUU/V+	-40°C to +105°C	38 TSSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part.

Pin Configuration appears at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

HV, VDD_U, GND_U, DCIN to AGND........................-0.3V to +80V
HV to DCIN and C12 ....-0.3V to +6V
Cn+1 to Cn, where n = 1 to 11 ....-0.3V to +80V
C1 to C0 ....-0.3V to +20V (Note 1)
C1 to AGND ....-0.3V to (V_{DCIN} + 0.6V) (Note 2)
C0 to AGND...-0.3V to +0.9V
C2–C12 to AGND ....-0.3V to (V_{DCIN} + 0.6V)
$\overline{SHDN}$, V_{AA} to AGND ....-0.3V to +4V
VDD_U to GND_U..-0.3V to +6V
OVSEL_, UVSEL_, TOPSEL to AGND ....-0.3V to (V_{AA} + 0.3V)
CD, $ALRM_L$ to AGND..................................-0.3V to (V_{AA} + 0.3V)
$ALRM_U$ to GND_U ....-0.3V to (+VDD_U + 0.3V)
CP+ to AGND ....(GND_U - 0.3V) to (VDD_U + 0.3V)
CP- to AGND...-0.3V to (GND_U + 0.3V)
CP- to VDD_U ....+0.3V

ESD Rating
C_, REF, V_{AA}, VDD_U, GND_U,
DCIN, $\overline{SHDN}$, CP+, CP-, HV,
OVSEL_, UVSEL_, TOPSEL,
$ALRM_U$, $ALRM_L$,
AGND, CD ....±2kV (Human Body Model, Note 3)
Continuous Power Dissipation (T_A = +70°C)
38-Pin TSSOP (derate 15.9mW/°C above +70°C) 1095.9mW
Operating Temperature Range ....-40°C to +105°C
Storage Temperature Range ....-55°C to +150°C
Junction Temperature (continuous)................................+150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Note 1: The C1 to C0 differential input path is tolerant to 80V as long as the $\overline{SHDN}$ pin is deasserted.
Note 2: The C1 input is tolerant to a maximum V_{DCIN} + 0.6V with $\overline{SHDN}$ = 1. If $\overline{SHDN}$ = 0, 20V is the maximum rating.
Note 3: Human Body Model to Specification MIL-STD-883 Method 3015.7.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}, unless otherwise noted. V_{DCIN} = V_{GND_U} = +6.0V to +72V, typical values are at T_A = +25°C, unless otherwise specified from -40°C to +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
C_ INPUTS						
Differential Input Range	$VCELL_{XIN}$	Any two inputs Cn to Cn+1, where n = 1 to 11 (Note 4)	1.5		72	V
		C1 to C0 with $\overline{SHDN}$ = 1	1.5		72	
		C1 to C0 with $\overline{SHDN}$ = 0	1.5		16	
Input Current	IC_{XIN}	V_{CELL} = 3.0V	-1	0.05	+1	µA
Overvoltage Threshold	V_{OV}		+3.3		+4.8	V
Overvoltage-Threshold Accuracy				±5	±25	mV
Undervoltage Threshold	V_{UV}		+1.6		+2.8	V
Undervoltage-Threshold Accuracy				±20	±100	mV
Comparator Hysteresis (Note 4)	V_{HYS}	MAX11080		300		mV
		MAX11081	12	37.5	77	
CD PIN						
CD Current	I_{CD}	V_{CD} = 0.4V	4.35	6.1	7.65	µA
CD Trip Voltage	V_{CD}	Internal at comparator		1.23		V
Delay-Time Accuracy		Excluding C_{DLY} variation		±20		%
STATUS/CONTROL PORT						
Shutdown Disable ($\overline{SHDN}$ High Voltage)	$\overline{SHDN}/V_{IH}$		2.1			V
Shutdown Asserted ($\overline{SHDN}$ Low Voltage)	$\overline{SHDN}/V_{IL}$				0.6	V

ELECTRICAL CHARACTERISTICS (continued)

($T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. $V_{DCIN} = V_{GND_U}$ = +6.0V to +72V, typical values are at T_A = +25°C, unless otherwise specified from -40°C to +105°C.)

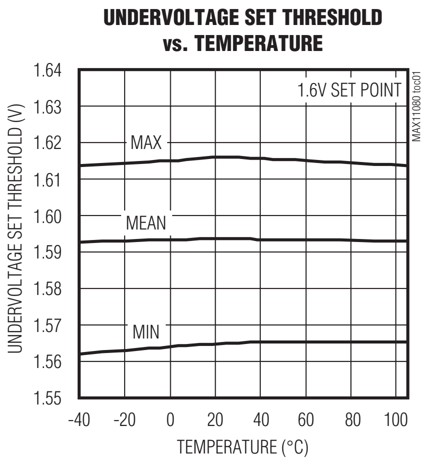
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VDD_U Output High	VDD_U V_{OH}		V_{GND_U} + 2.4			V
VDD_U Output Low	VDD_U V_{OL}				V_{GND_U} + 0.3	V
$ALRM_L$ Output Voltage High	$ALRM_L$ V_{OH}	I_{SOURCE} = 150µA	2.4			V
$ALRM_L$ Output Voltage Low	$ALRM_L$ V_{OL}	I_{SINK} = 150µA			0.6	V
$ALRM_U$ Input Voltage High	$ALRM_U$ V_{IH}	Daisy-chained $ALRM_U$ signal as coupled through a 3.3nF high-voltage capacitor and a 150kΩ resistor as referred to GND_U	V_{GND_U} + 2.1			V
$ALRM_U$ Input Voltage Low	$ALRM_U$ V_{IL}	Daisy-chained $ALRM_U$ signal as coupled through a 3.3nF high-voltage capacitor and a 150kΩ resistor as referred to GND_U			V_{GND_U} + 0.9	V
Alarm Voltage Output "Heartbeat" Frequency	$ALRM_L$ f_{OUT}	Heartbeat clock rate with no alarm condition	4032	4096	4157	Hz
Alarm Voltage Output Duty Cycle		Heartbeat clock rate with no alarm condition	49.0		51.0	%
LINEAR REGULATOR (V_{AA})						
Input-Voltage Range	V_{DCIN}		6		72	V
Output Voltage	V_{AAOUT}	6V < V_{DCIN} < 72V, I_{LOAD} = 0A	3.0	3.3	3.6	V
Short-Circuit Current	$I_{AASHORTCIRCUIT}$	V_{AA} = 0V, 6V < V_{DCIN} < 36V			50	mA
Power-On-Reset Trip Level (Note 5)	$V_{AARESET}$	Falling V_{AA}		2.8		V
	$V_{AAVALID}$	Rising V_{AA}		3.0		
	V_{AAHYS}	Hysteresis on rising V_{AA}		37		mV
Thermal Shutdown	T_{SHUT}	Rising temperature		+145		°C
POWER-SUPPLY REQUIREMENTS (DCIN)						
Current Consumption	I_{DCIN}	Operating mode, $\overline{SHDN}$ = 1, 12 battery cells, alarm inactive, $V_{DCIN} = V_{GND_U}$ = 36V		35	40	µA
		Shutdown mode, $\overline{SHDN}$ = 0, 12 battery cells, $V_{DCIN} = V_{GND_U}$ = 36V		1.3	2	
I_{GND_U} Operating Mode		$\overline{SHDN}$ = 1, battery cells, alarm inactive, $V_{DCIN} = V_{GND_U}$ = 36V		35	40	µA
LOGIC INPUTS AND OUTPUTS						
Threshold Setting	V_{IH}	UVSEL0/UVSEL1/UVSEL2, TOPSEL	V_{AA} - 0.1			V
	V_{IL}	OVSELO/OVSEL1/OVSEL2/OVSEL3			0.1	

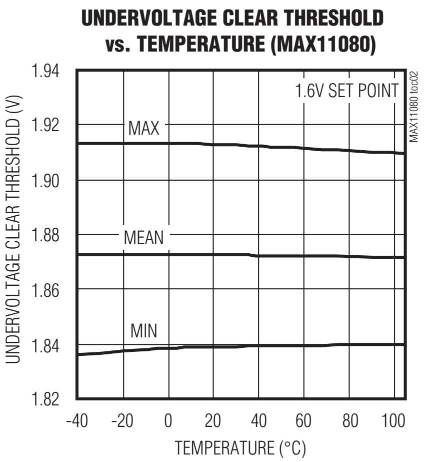
Note 4: Limits guaranteed by design and characterization statistical analysis, not production tested.

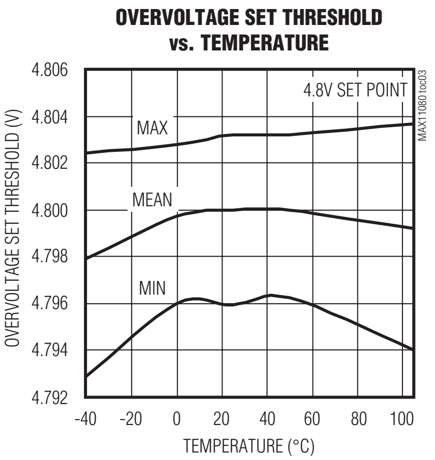
Note 5: Guaranteed by design and not production tested.

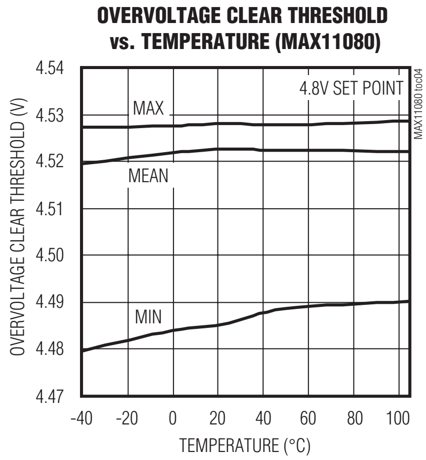
Typical Operating Characteristics

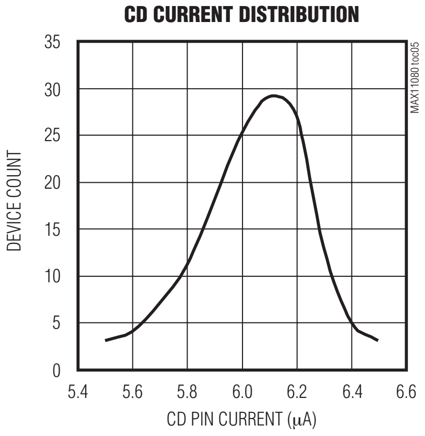
(T$_A$ = +25°C, unless otherwise noted.)

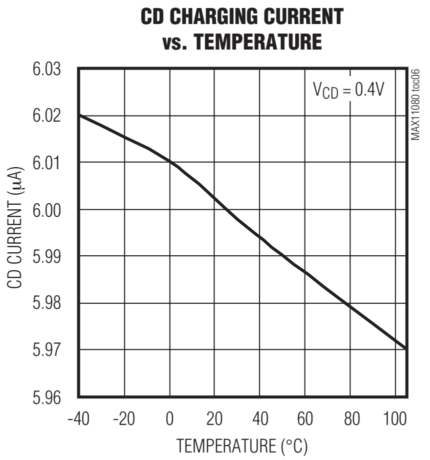

UNDERVOLTAGE SET THRESHOLD vs. TEMPERATURE

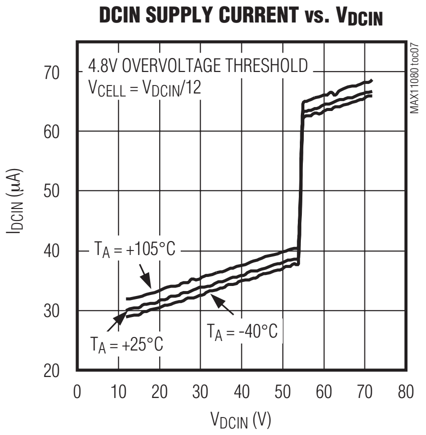

UNDERVOLTAGE CLEAR THRESHOLD vs. TEMPERATURE (MAX11080)

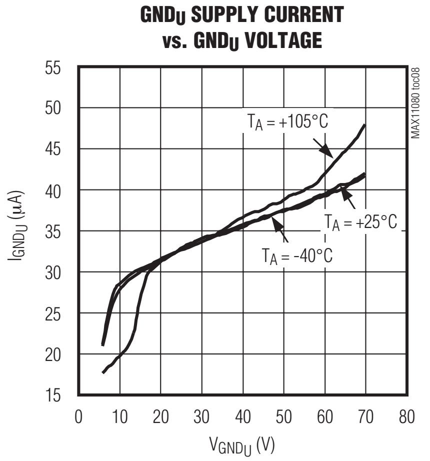

OVERVOLTAGE SET THRESHOLD vs. TEMPERATURE


OVERVOLTAGE CLEAR THRESHOLD vs. TEMPERATURE (MAX11080)


CD CURRENT DISTRIBUTION


CD CHARGING CURRENT vs. TEMPERATURE


DCIN SUPPLY CURRENT vs. V$_{DCIN}$


GND$_U$ SUPPLY CURRENT vs. GND$_U$ VOLTAGE

Pin Description

PIN	NAME	FUNCTION
1	DCIN	DC Power-Supply Input. DCIN supplies the internal 3.3V regulator. This pin should be connected as shown in the application diagrams.
2	HV	High-Voltage Bias. HV is biased by the output of the charge pump to provide a DC supply above the DCIN level. It is used internally to bias the cell-comparator circuitry. Bypass to DCIN with a 1µF capacitor.
3, 33	N.C.	No Connection. Not internally connected.
4	C12	Cell 12 Plus Connection. Top of battery module stack.
5	C11	Cell 12 Minus Connection and Cell 11 Plus Connection
6	C10	Cell 11 Minus Connection and Cell 10 Plus Connection
7	C9	Cell 10 Minus Connection and Cell 9 Plus Connection
8	C8	Cell 9 Minus Connection and Cell 8 Plus Connection
9	C7	Cell 8 Minus Connection and Cell 7 Plus Connection
10	C6	Cell 7 Minus Connection and Cell 6 Plus Connection
11	C5	Cell 6 Minus Connection and Cell 5 Plus Connection
12	C4	Cell 5 Minus Connection and Cell 4 Plus Connection
13	C3	Cell 4 Minus Connection and Cell 3 Plus Connection
14	C2	Cell 3 Minus Connection and Cell 2 Plus Connection
15	C1	Cell 2 Minus Connection and Cell 1 Plus Connection
16	C0	Cell 1 Minus Connection. Connect to AGND.
17	UVSEL0	Undervoltage Threshold Select 0 to 2. Used to select one of eight undervoltage alarm threshold settings. The parts have internal pulldown; these pins should only be tied to V_{AA} or AGND to set the logic state.
18	UVSEL1	
19	UVSEL2	
20	OVSEL0	Overvoltage Threshold Select 0 to 3. Used to select one of 16 overvoltage alarm threshold settings. The parts have internal pulldown; these pins should only be tied to V_{AA} or AGND to set the logic state.
21	OVSEL1	
22	OVSEL2	
23	OVSEL3	

Pin Description (continued)

PIN	NAME	FUNCTION
24	V_{AA}	+3.3V Analog Supply Output. Bypass with a 1µF capacitor to AGND.
25	AGND	Analog Ground. Should be connected to the negative terminal of cell 1.
26	$\overline{\text{SHDN}}$	Active-Low Shutdown Input. This pin completely shuts down the MAX11080/MAX11081 internal regulators and oscillators when the pin is less than 0.6V as referenced to AGND. The host controller should drive $\overline{\text{SHDN}}$ for the first pack. See Figure 2 for the $\overline{\text{SHDN}}$ daisy-chained module connection.
27	$ALRM_L$	Lower Port Alarm Output. This output is an alarm indicator for overvoltage, undervoltage, and setup faults. The alarm signal is daisy-chained and driven from the highest module down to the lowest. The alarm output is nominally a clocked “heartbeat” signal that provides a 4kHz clock when no alarm is present. The $ALRM_L$ can also be configured as level signal and set to “low” for no alarm and “high” for alarm state. See the *TOPSEL Function* section for details. This signal swings between V_{AA} and AGND, and is active high in the alarm state.
28	CD	Programmable Delay Time. Connect a capacitor from this pin to AGND to set the hold time required for a fault condition before the alarm is set. The capacitor should be a ceramic capacitor in the 15nF to 16.5µF range.
29, 30, 32	TST1, TST2, TST3	Production Test Pins. Connect to AGND.
31	TOPSEL	Input to Indicate Topmost Device in the Daisy-Chain. This pin should be connected to AGND for all devices except the topmost. For the top device, this pin should be connected to V_{AA}.
34	$ALRM_U$	Upper Port Alarm Input. This input receives the $ALRM_L$ output signal from an upper neighboring module. It swings between VDD_U and GND_U.
35	GND_U	Level-Shifted Upper Port Ground. Upper port-supply return and supply input for the charge-pump supply. This pin should be connected to the DCIN takeoff point on the battery stack as shown in the application diagrams.
36	VDD_U	Level-Shifted Upper Port Supply. Upper port-supply output for the daisy-chained bus. This is a regulated output voltage from the internal charge pump that is level-shifted above the DCIN pin voltage level. It should be bypassed with a 1µF capacitor to GND_U.
37, 38	CP-, CP+	Charge-Pump Capacitor. Negative/positive input for the internal charge pump. Connect a 0.01µF high-voltage capacitor between CP+ and CP-.

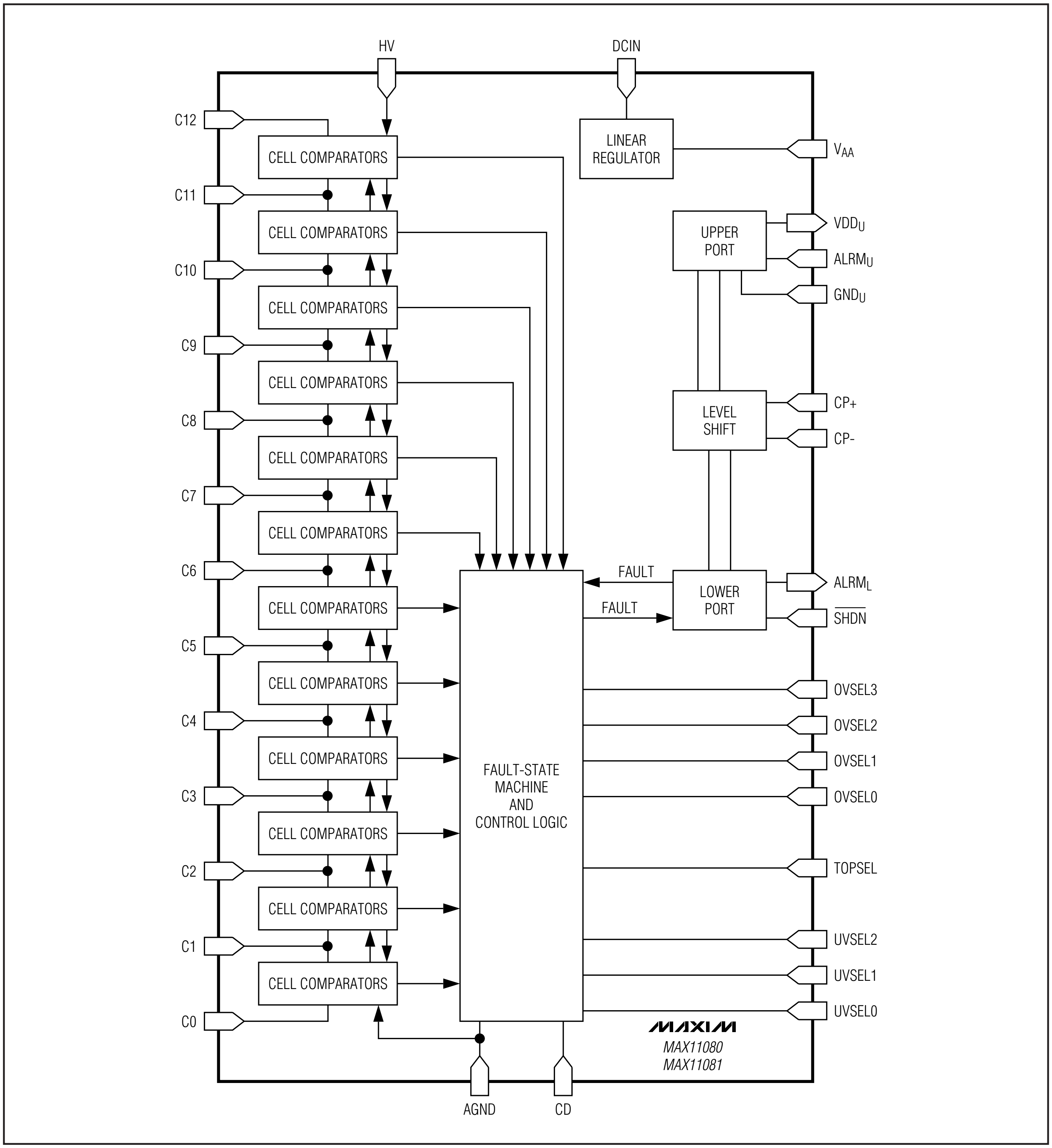


Figure 1. Functional Diagram

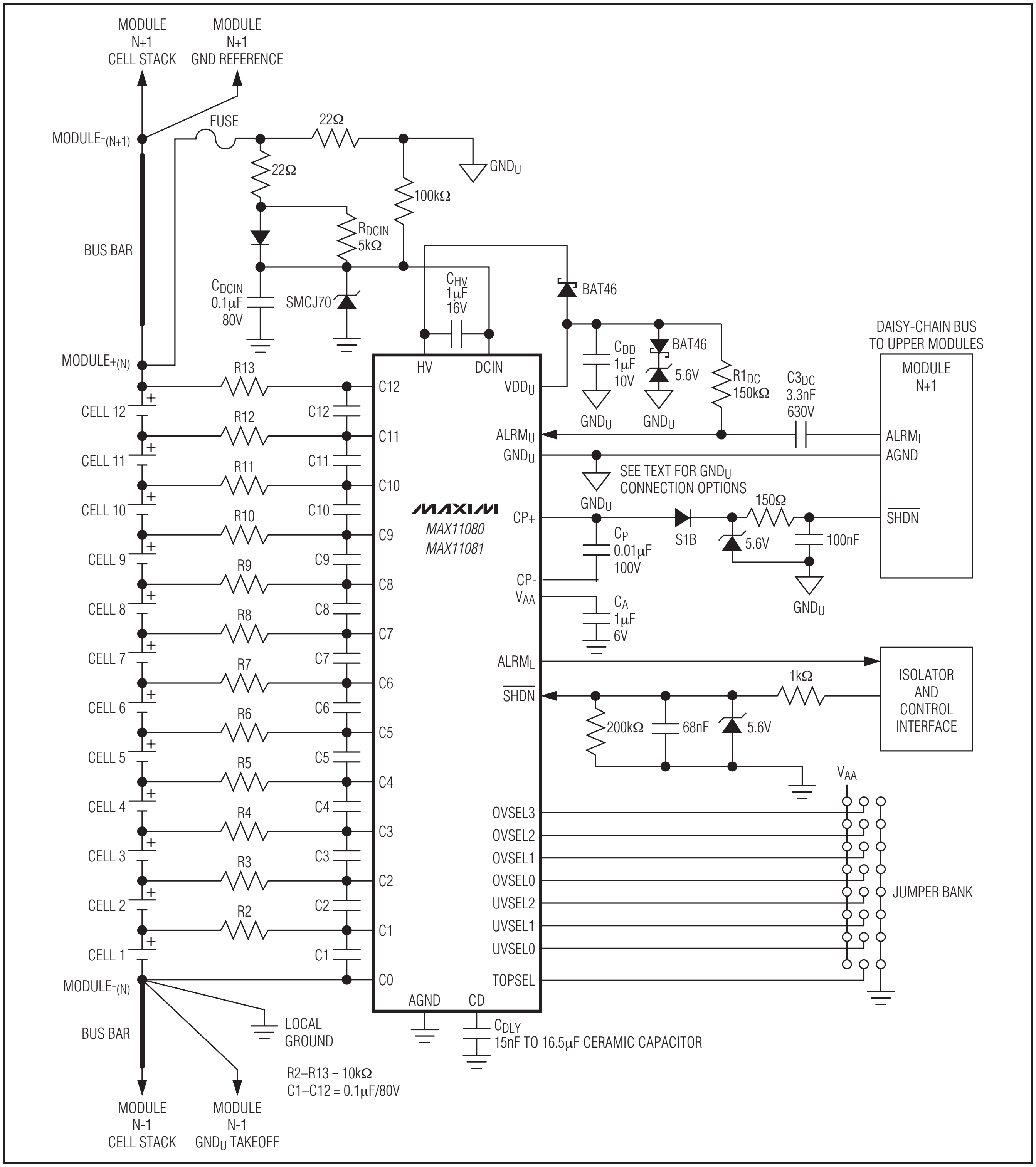


Figure 2. Application Circuit Diagram for a 12-Cell System

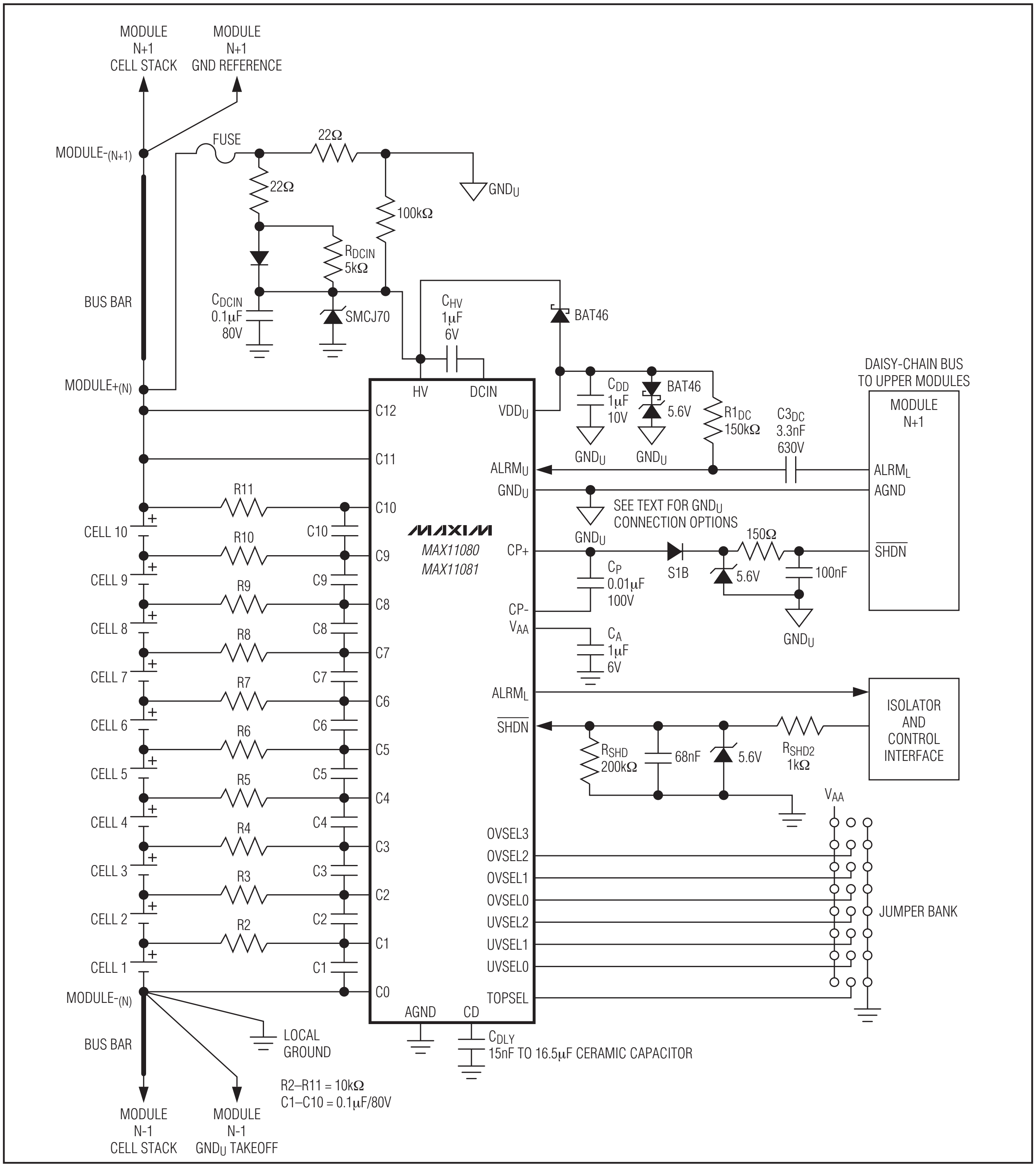


Figure 3. Application Circuit Diagram for a 10-Cell System

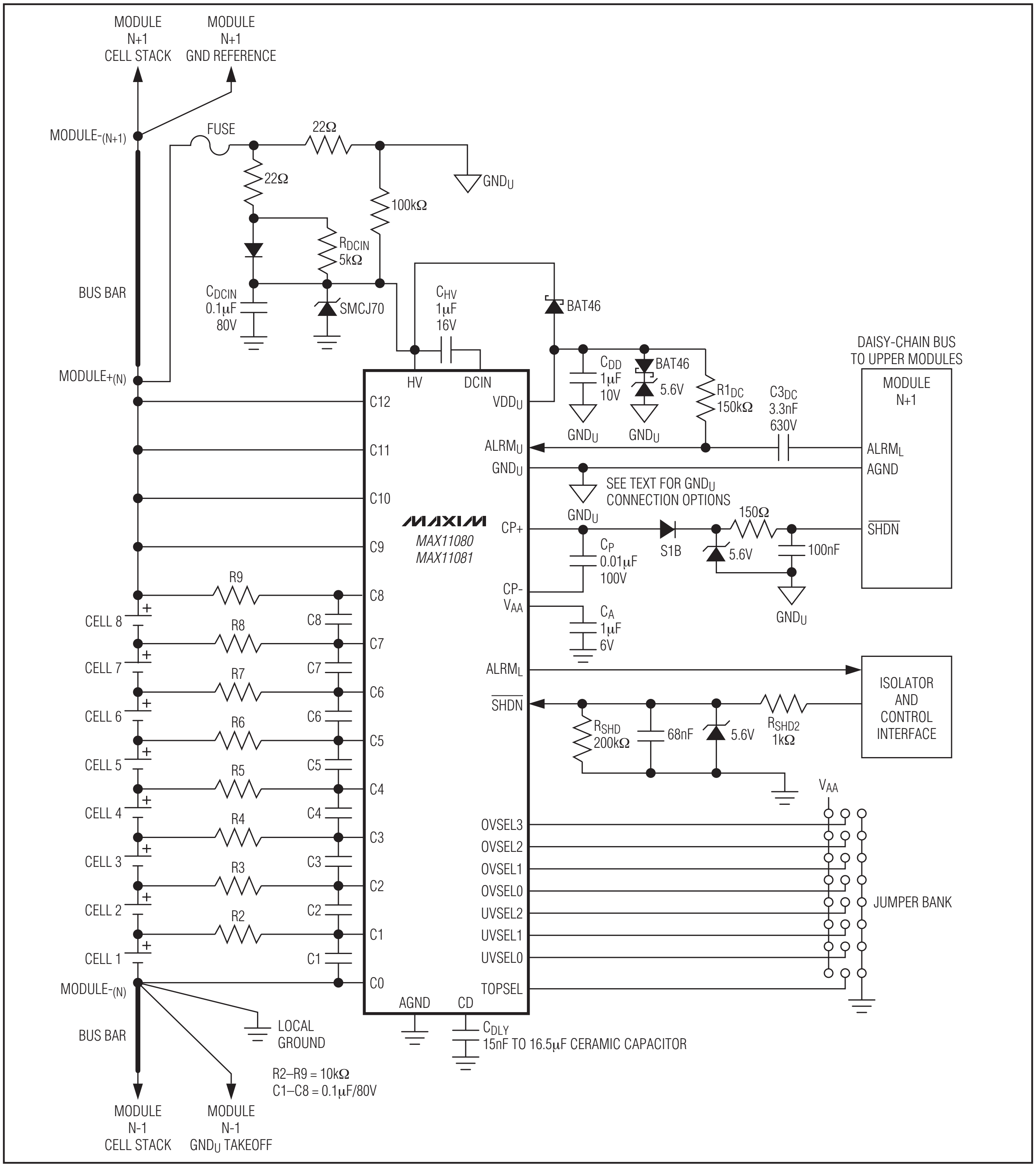


Figure 4. Application Circuit Diagram for an 8-Cell System

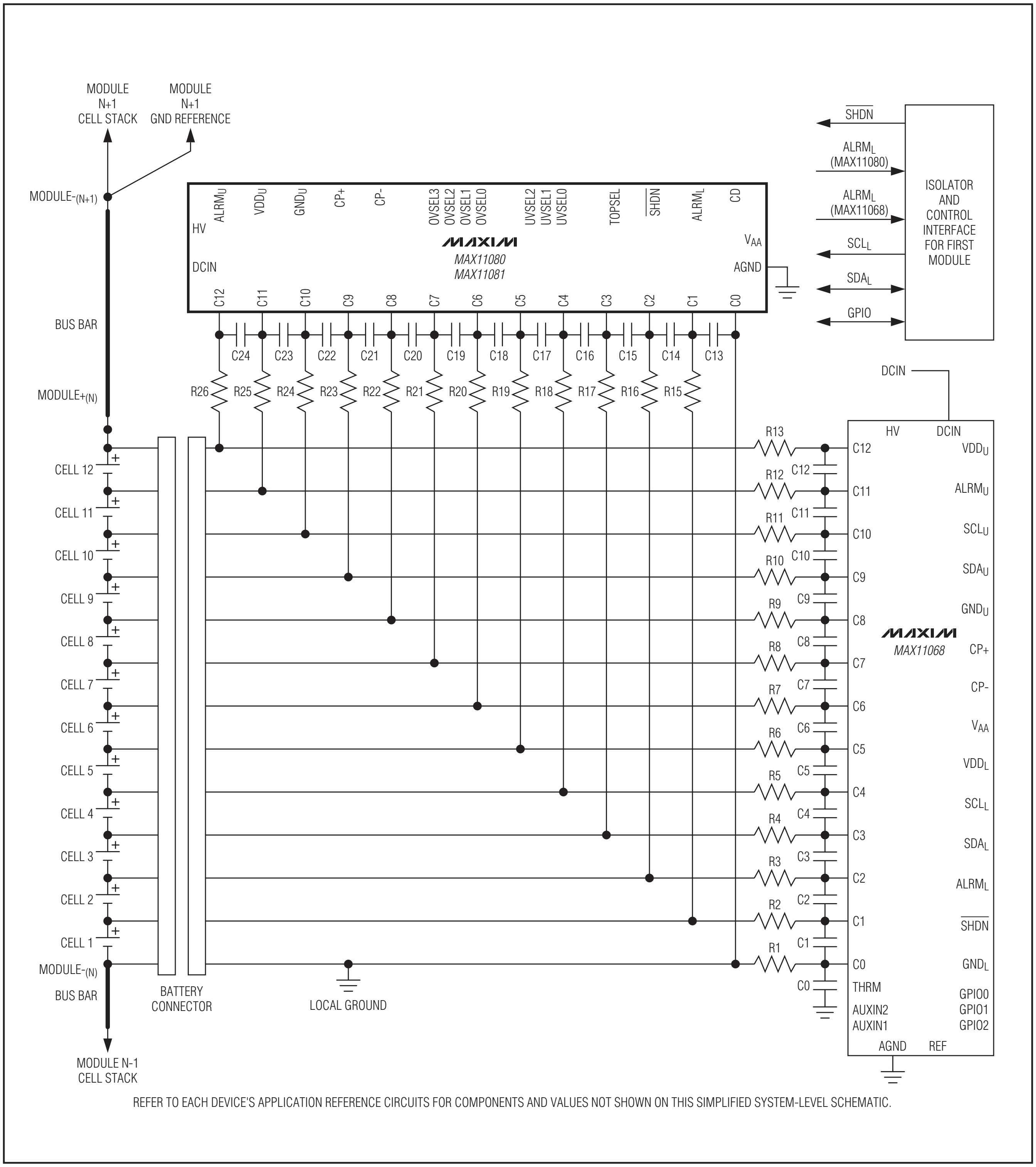


Figure 5. Battery Module System with Redundant Fault-Detection Application Schematic

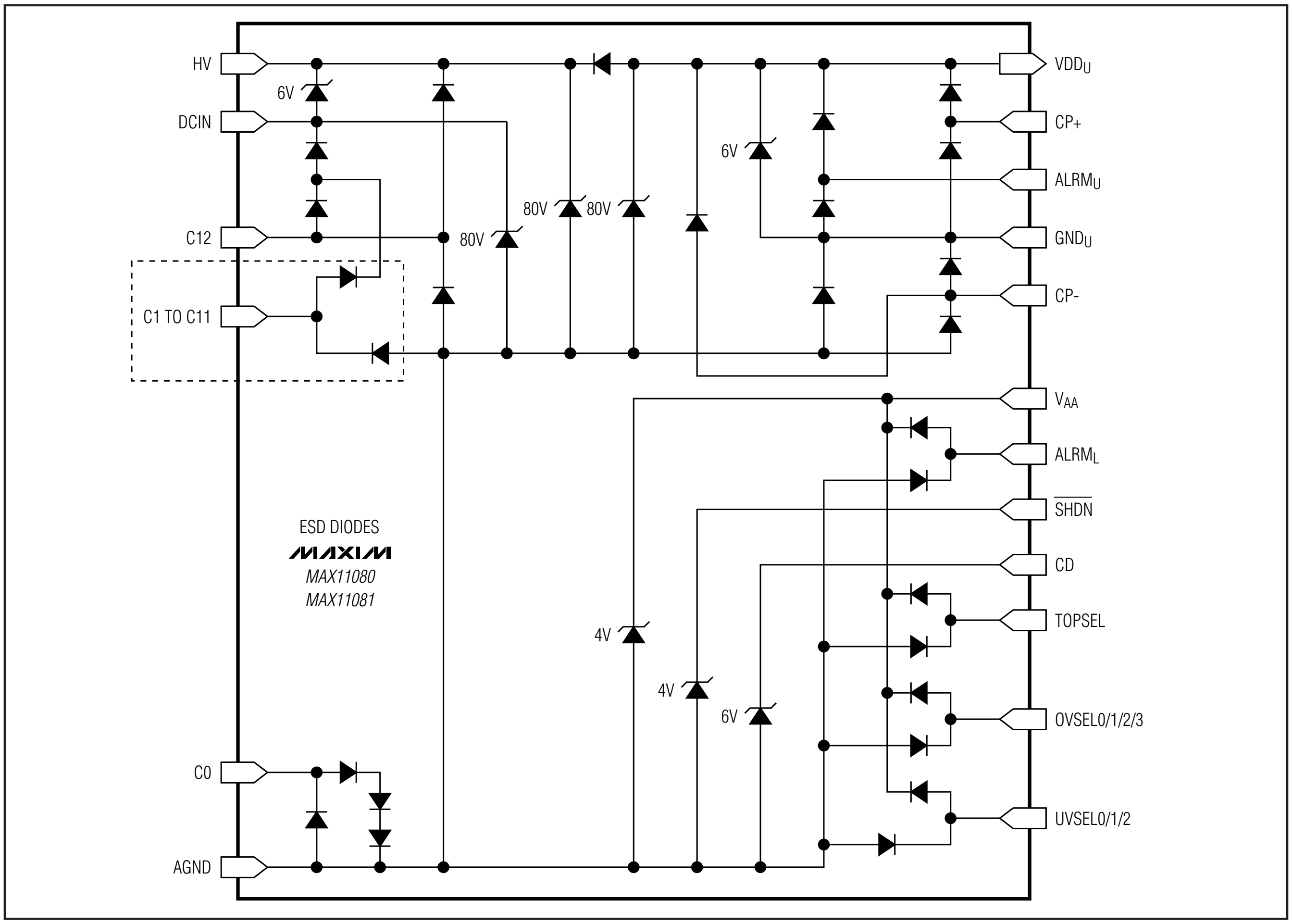


Figure 6. ESD Diode Diagram

Detailed Description

Figure 1 shows the functional diagram; Figure 2 shows the application circuit diagram for a 12-cell system while Figure 3 shows the application circuit design for a 10-cell system and Figure 4 for an 8-cell system. Figure 5 is the application schematic for the battery module system with redundant fault detection and Figure 6 is the ESD diode diagram.

Architectural Overview

The MAX11080/MAX11081 are battery-pack fault-monitor ICs capable of monitoring up to 12 Li+ battery cells. These devices are designed to provide an overvoltage or undervoltage alarm indicator when any of the cells cross the user-selectable threshold for longer than the configured decision delay interval. The MAX11080/MAX11081 also incorporates daisy-chain bus for use in high-voltage stacked-battery operation. The daisy-chain bus relays shutdown and alarm communication across up to 31 stacked modules without the need for isolation between each module. This results in a simplified system with reduced cost. The MAX11080/MAX11081 are ideal as an ultra-low-power, redundant cell-fault monitor that is the perfect complement to the MAX11068 high-voltage battery measurement IC. Both ICs in concert form a powerful Li+ battery system monitor with redundant overvoltage and undervoltage fault detection.

Overvoltage and Undervoltage Fault Detection

Figure 7 summarizes the fault-detection mechanism for a set of differential cell inputs in the MAX11080/MAX11081.

First, the differential cell inputs are attenuated by a factor of four while being level shifted and converted to a single-ended voltage referenced to AGND. The ground-referenced voltage is then connected to a set of overvoltage and undervoltage comparators. The threshold references for the comparators are set by the UVSEL_ and OVSEL_ input pins. When one of the cell voltages exceeds V_{OV} or is below V_{UV} when V_{UV} is enabled, the internal cell out-of-range signal for the given cell is set and logically ORed with the same signal for the other cell positions to create an overall out-of-range signal.

When any cells are out-of-range as indicated by the internal out-of-range signal, an internal current source begins to charge the capacitor C_{DLY} connected to the CD pin. If the voltage at the CD pin reaches V_{CD}, the $ALRM_L$ line is set to V_{AA} (+2.4V minimum as referred to AGND). Normally, the $ALRM_L$ line is a heartbeat signal with pulses occurring every 250µs. If all cell voltages transition from out-of-range to in-range before the voltage at pin CD reaches V_{CD}, an internal switch clamps the CD pin to GND. This action discharges C_{DLY} and, because the delay had not yet expired, no alarm occurs. Discharging C_{DLY} ensures that the full delay time occurs for the next overvoltage or undervoltage

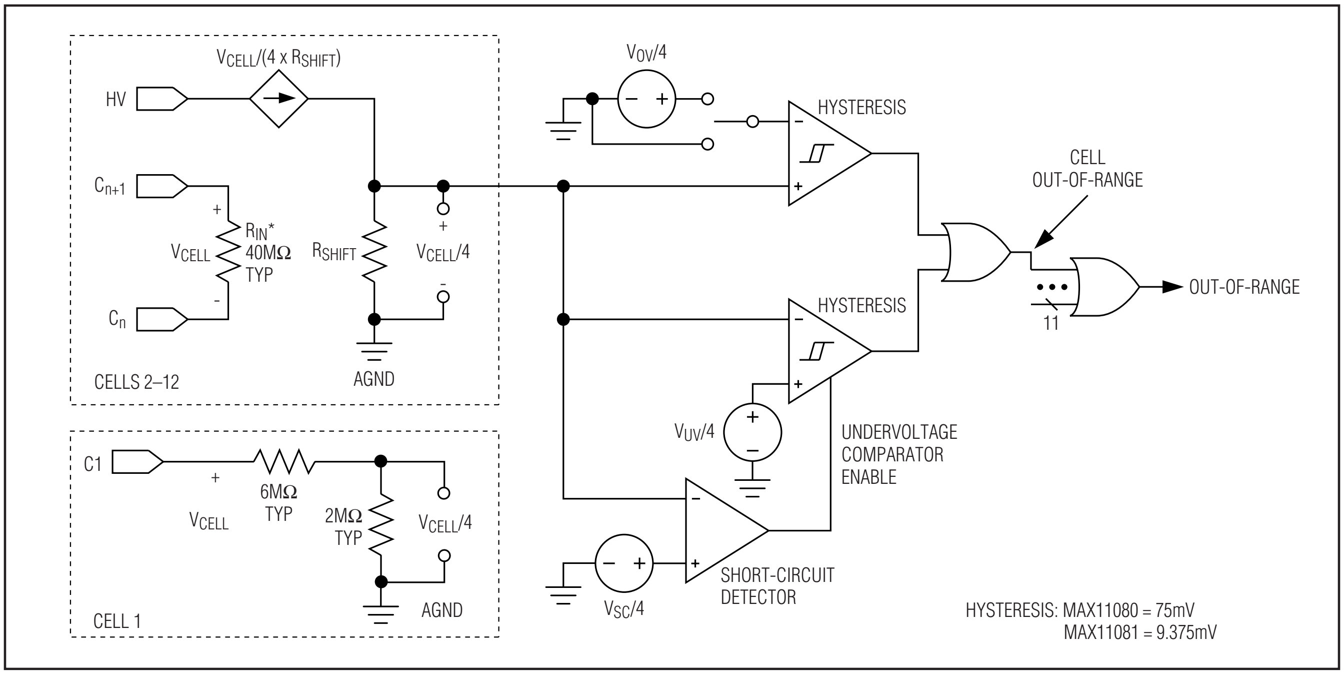


Figure 7. Cell Differential Input and Comparator Block Diagram

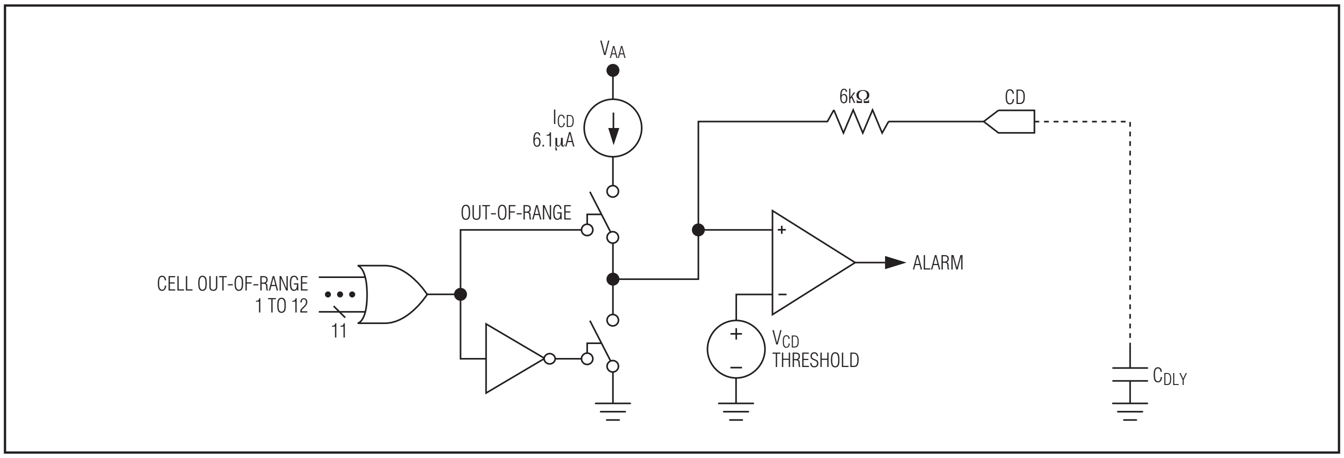


Figure 8. C_{DLY} Circuit Block Diagram

event. Figure 8 summarizes the C_{DLY} circuit.

Once the $ALRM_L$ pin is forced high due to an alarm (+2.4V minimum as referred to AGND), it transitions back to a heartbeat signal only after all battery cells meet the following condition:

$$(V_{OV} - V_{HYS}) > V_{CELL(ALL)} > (V_{UV} + V_{HYS})$$

Examples of cell-voltage readings and their effect on the alarm status are shown in Figures 9 and 10 for single- and multiple-cell systems. In the case where an upper module is forwarding an active alarm condition down the daisy-chain, that condition continues to be propagated toward the host regardless of the alarm state of any lower module. Furthermore, to circumvent the possibility of a short-circuited capacitor connected to CD preempting the fault-time validation process, a redundant built-in delay of 4s nominal is asserted as a backup. If the V_{CD} threshold is not reached within 4s of an out-of-range event, the alarm becomes active.

Programmable Delay Time

The alarm trigger delay time is calculated according to the following equations:

$$t_{DLY} = (V_{CD} \times C_{DLY})/I_{CD}$$

$$C_{DLY} = (t_{DLY} \times I_{CD})/V_{CD}$$

The effective I_{CD} value of the current source is 6.1µA typical and the threshold voltage, V_{CD}, is 1.23V typical. The V_{CD} threshold is specified at an internal node prior to the resistor in series with the CD pin as shown in Figure 8. The threshold voltage seen at the pin is approximately 1.18V due to the drop associated with the typical I_{CD} value and the 6kΩ resistor. The MAX11080/MAX11081 can operate with capacitor values from 15nF (3.0ms) to 16.5µF (3.32s). Each capacitor should have a voltage tolerance of 5V minimum.

Cell-Voltage Threshold Selection

The overvoltage and undervoltage threshold selection is configured through the OVSEL_ and UVSEL_ inputs. The overvoltage selection can be configured from 3.3V to 4.8V in 100mV increments. The undervoltage threshold can be configured from 1.6V to 2.8V in 200mV increments. The undervoltage detection can also be disabled. See Tables 1 and 2 for the proper configuration settings.

Immunity to unintended changes in the threshold voltage setting (due to accidental pin-to-pin short circuits, for example) is provided. The customer-programmed

Table 1. Overvoltage Threshold Selection

THRESHOLD (V)	OVERVOLTAGE SELECTION			
	OVSEL3	OVSEL2	OVSEL1	OVSEL0
3.3	0	0	0	0
3.4	0	0	0	1
3.5	0	0	1	0
3.6	0	0	1	1
3.7	0	1	0	0
3.8	0	1	0	1
3.9	0	1	1	0
4.0	0	1	1	1
4.1	1	0	0	0
4.2	1	0	0	1
4.3	1	0	1	0
4.4	1	0	1	1
4.5	1	1	0	0
4.6	1	1	0	1
4.7	1	1	1	0
4.8	1	1	1	1

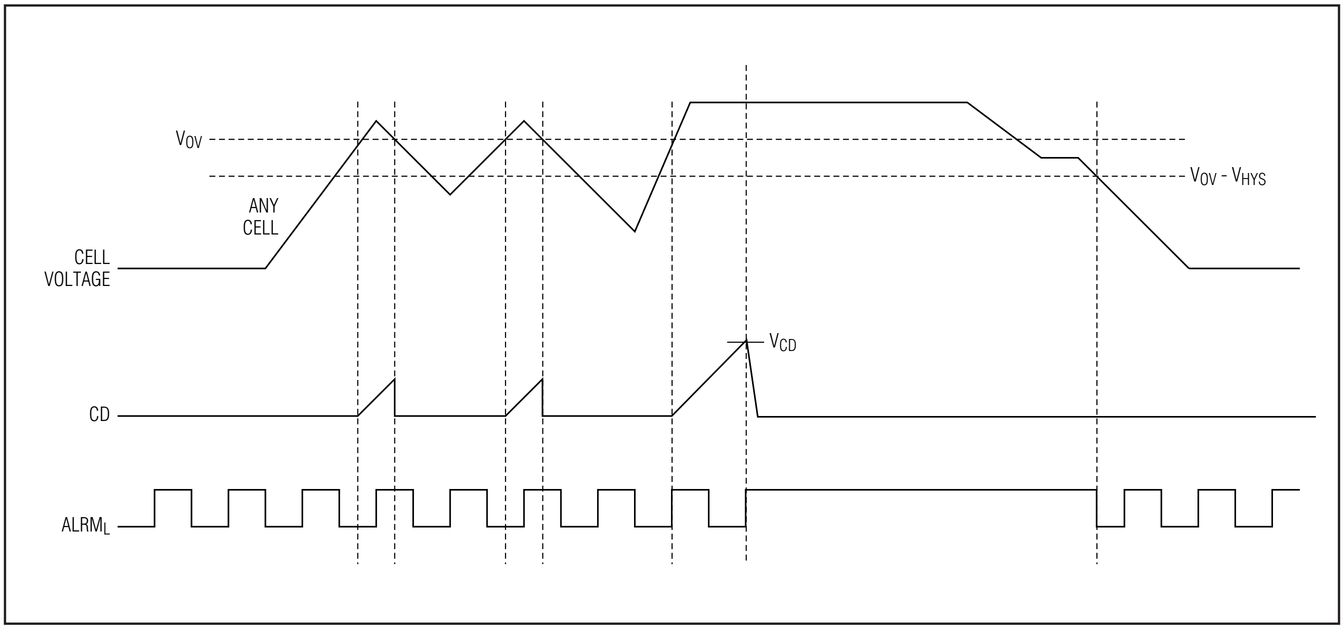


Figure 9. Single-Cell Overvoltage Detection Example

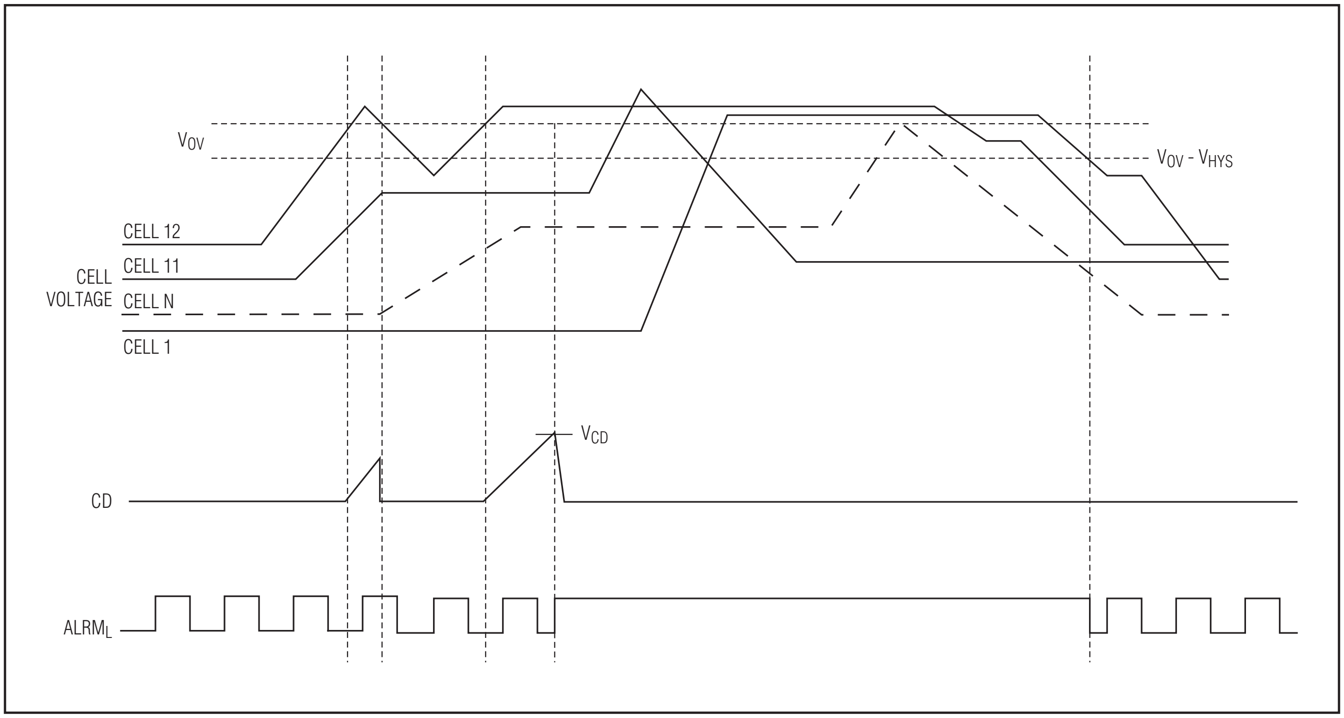


Figure 10. Multiple-Cell Overvoltage Detection Example

Table 2. Undervoltage Threshold Selection

THRESHOLD (V)	UNDERVOLTAGE SELECTION		
	UVSEL2	UVSEL1	UVSEL0
Disabled	0	0	0
1.6	0	0	1
1.8	0	1	0
2.0	0	1	1
2.2	1	0	0
2.4	1	0	1
2.6	1	1	0
2.8	1	1	1

selection is sensed and stored at power-up and any subsequent change to the input pin status is ignored.

Internal Linear Regulator

The MAX11080/MAX11081 have an internal linear regulator for generating the internal supply from DCIN (Figure 11). The regulator can accept a supply voltage on the DCIN pin from +6.0V to +72V, which it regulates to 3.3V to run the voltage-detection system, control logic, and low-side alarm-pulse interface. When the SHDN pin is not active and a sufficient voltage is applied to DCIN, the output of the regulator becomes active. The regulator is paired with a power-on-reset (POR) circuit that senses its output voltage and holds the MAX11080/MAX11081 in a reset state until the internal supply has reached a sustainable threshold of +3.0V (±5%). The internal comparators have built-in hysteresis that can reject noise on the supply line. Because secondary metal batteries are never fully discharged to 0V, the MAX11080/MAX11081 are designed for a hot-swap insertion of the battery cells. Once the POR threshold is reached, approximately 1ms later the internal reset signal disables, the internal oscillator starts, and the charge pump begins operating. The charge pump reaches regulation in approximately 3ms. The MAX11080/MAX11081 associated with the top module in the battery pack are identified as detailed in the *TOPSEL Function* section. This is followed by a self-test of the overvoltage comparators and detection of the number of cells connected. At this time in the power-on sequence, the MAX11080/MAX11081 are ready for operation. When the charge pump achieves regulation of 3.3V between VDD_U and GND_U, it switches to a standby mode until the voltage drops by about 35mV. The specified accuracy and full operation of the MAX11080/MAX11081

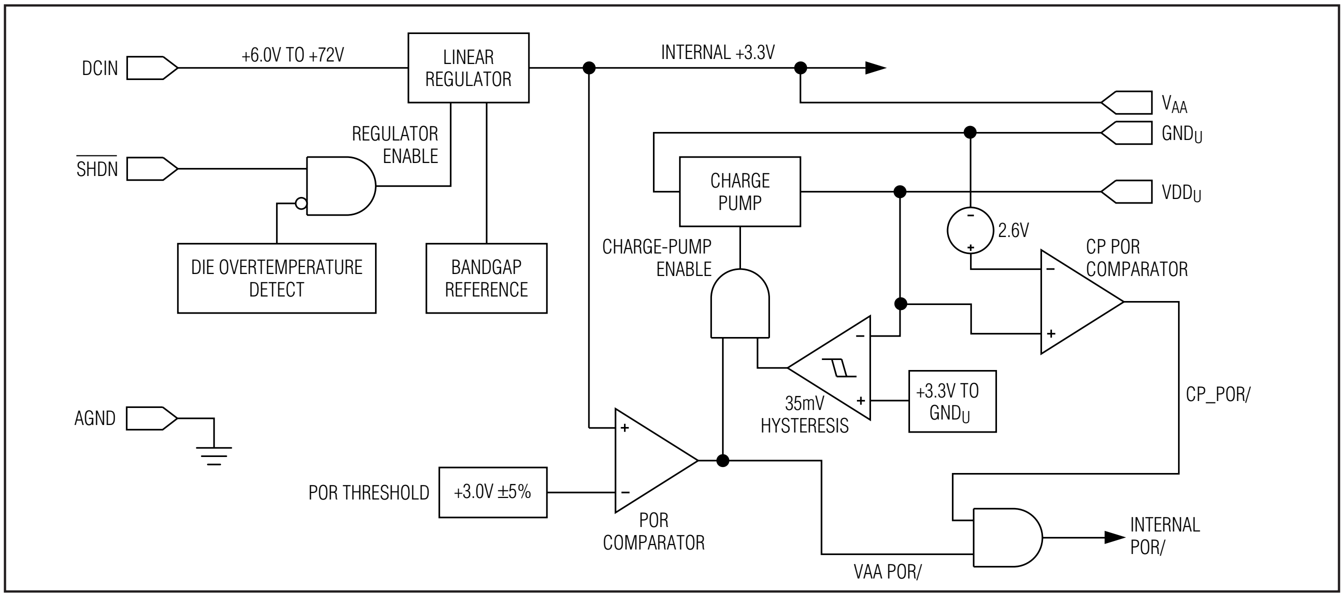


Figure 11. Internal Linear Regulator Block Diagram

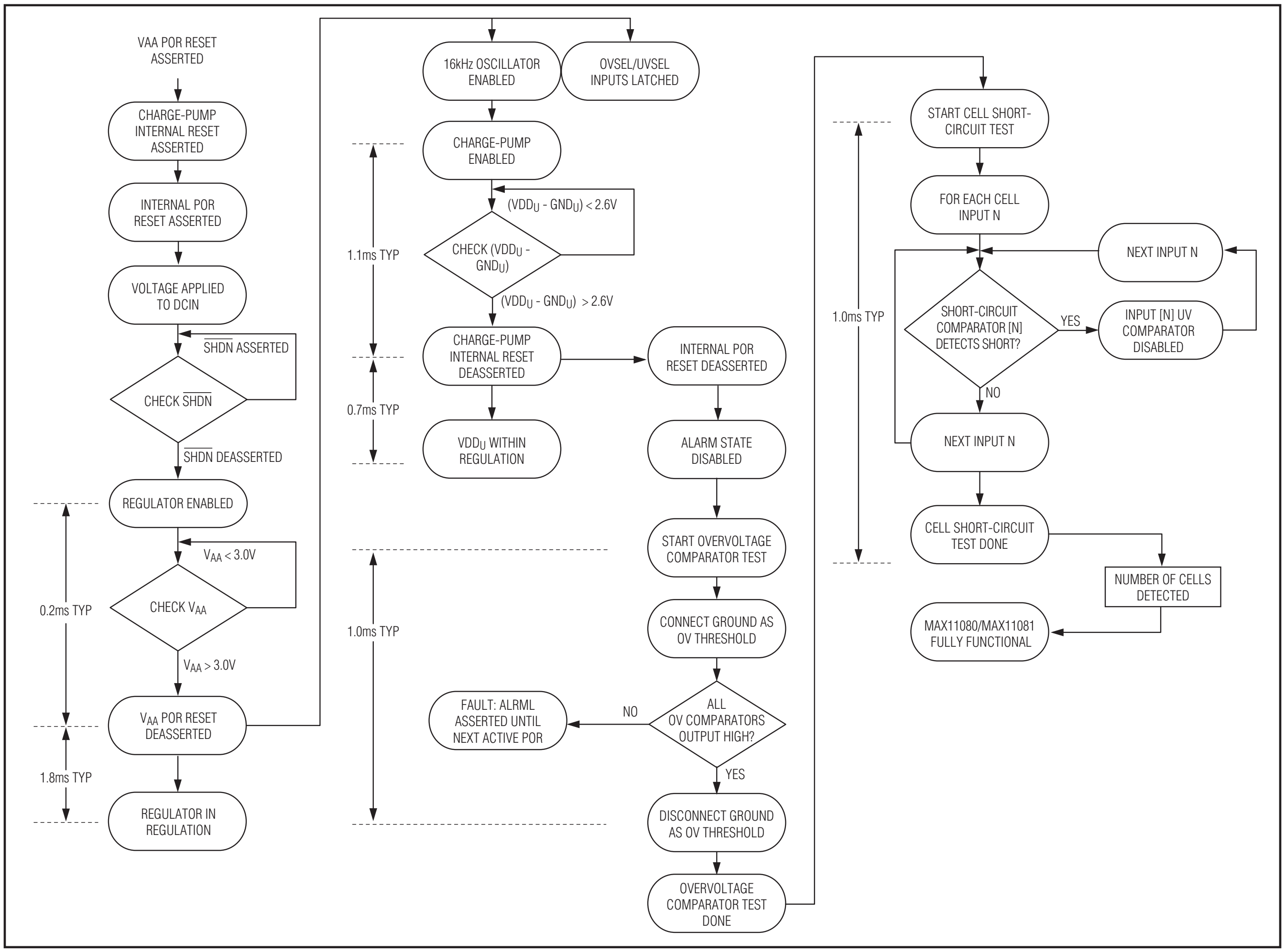


Figure 12. Linear Regulator Power-Up Sequence

are not guaranteed until a minimum of 6.0V is applied to the DCIN pin.

The linear regulator also incorporates a thermal shutdown feature. If the MAX11080/MAX11081 die temperature rises above +145°C, the device shuts down. After a thermal shutdown, the die temperature must cool 15°C below the shutdown temperature before the device restarts.

Figure 12 shows the linear regulator power-up sequence and Figure 13 shows the low DCIN POR event.

DCIN and GND_U Supply Connections

A surge voltage is produced by the electric motor during regenerative braking conditions. The MAX11080/MAX11081 are designed to tolerate an absolute maximum of 80V under this condition. The MAX11080/MAX11081 should be protected against higher voltages with an external voltage suppressor such as

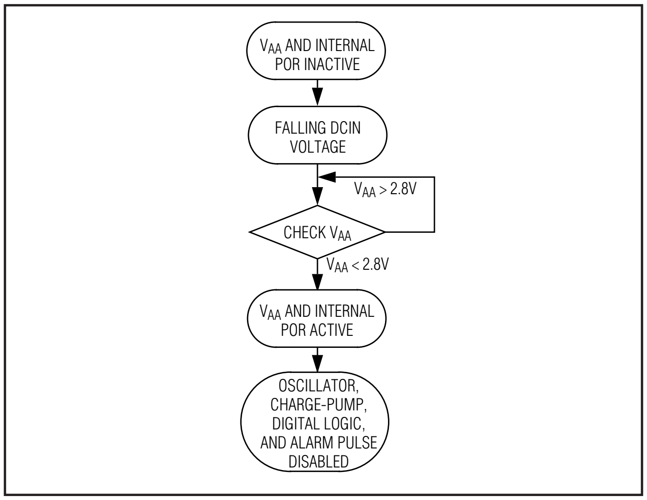


Figure 13. Low DCIN POR Event

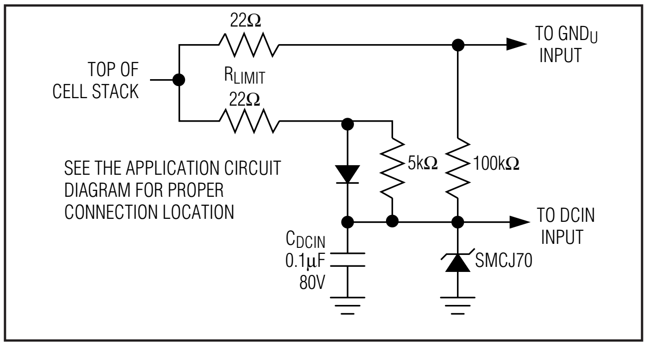


Figure 14. Battery Module Surge and Overvoltage Protection Circuit

the SMCJ70 on the DCIN connection point. This protection circuit also helps to reduce power spikes that can occur during the insertion of the battery cells. During negative voltage excursions, the protection circuit stores enough charge to power the regulator through the transient. Figure 14 shows the clamp configuration to protect the DCIN supply input.

The DCIN input contains a comparator circuit to detect an open circuit on this pin for fault-management purposes. Whenever a nominal voltage of two silicon diode drops appears between C12 and DCIN following the power-up sequence, the ALRM$_L$ output is asserted as a fault indication. This voltage drop must appear for at least the delay time set by C$_{DLY}$ to result in a fault. The voltage drop from C12 to DCIN during normal operation should be kept at no more than 0.5V to prevent erroneous tripping of the DCIN open-circuit comparator under worst-case circumstances (lowest silicon diode forward bias voltage). The diode D$_{DCIN}$ is used to supply the transient current demanded at startup by the decoupling circuit. In parallel with this diode, R$_{DCIN}$ provides the supply path during normal operation. It is selected to be 5kΩ so that the maximum voltage drop between C12 and DCIN is about 0.25V with nominal supply currents.

High-power batteries are often used in noisy environments subject to high dV/dt or dI/dt supply noise and EMI noise. For example, the supply noise of a power inverter driving a high horse-power motor produces a large square wave at the battery terminals, even though the battery is also a high-power battery. Typically, the battery dominates the task of absorbing this noise, since it is impractical to put hundreds of farads at the inverter.

The MAX11080/MAX11081 are designed with several mechanisms to deal with extremely noisy environments. First, the major power-supply inputs that see the full battery-stack voltage are 80V tolerant. This is high enough to handle the large voltage changes on the battery stack that can occur when the batteries transition between charge and discharge conditions. Next, the linear regulator has high PSRR to produce a clean low-voltage power supply for the internal circuitry. This allows DCIN to be connected directly to the stack voltage. Finally, GND$_U$ serves two purposes. It supplies the internal charge pump with its power and acts as the reference ground for the upper alarm communication port. The charge pump creates a secondary low-voltage supply that is referenced to GND$_U$. Because the level-shifted supply VDD$_U$ is referenced to GND$_U$, the entire upper alarm communication port glides smoothly on GND$_U$ and it is effectively immune to noise on GND$_U$. The upper alarm signal is internally shifted down to AGND level where it is processed by the digital logic. There are two connection methods that can be used for GND$_U$ depending on application requirements.

For the top module in a system, or where GND$_U$ cannot be DC-coupled to the next higher module for other reasons, GND$_U$ should be connected to the same location as DCIN. This connection is valid as long as the voltage difference between the top of Stack(n) and the bottom of Stack(n+1) during worst-case conditions does not exceed the margin of the alarm pin signaling levels. When GND$_U$ is not DC-coupled to the far side of the bus bar, it can be AC-coupled to the far side to maintain alarm communication when the bus bar is open-circuit. In that case, the two sides of the AC-coupling capacitor can be at different DC potentials, but the alarm communication signal continues to be passed across the capacitor connection. It is recommended that an AC- or DC-coupled version of GND$_U$ is paired with the alarm signal through the communication bus wiring, possibly by twisted pair wire, for maximum noise immunity and minimum emissions.

The preferred connection to reject noise between modules is when a DC connection can be made from GND$_U$ to AGND of the next module. It is again recommended that the DC-coupled GND$_U$ signal is routed adjacent to the alarm signal as part of the communication bus for maximum noise immunity and minimum emissions.

Shutdown Control

The $\overline{SHDN}$ pin connections of the MAX11080/MAX11081 operate in a manner that allows the shutdown/wake-up command to trickle up through the series of daisy-chained packs. Because the internal linear regulator is powered down during shutdown, the shutdown function must operate when V$_{AA}$ is absent and, therefore, it cannot depend on a Schmitt trigger input. A special low-current, high-voltage circuit is used to detect the state of the $\overline{SHDN}$ pin. The shutdown pin has a +2.1V minimum threshold for the inactive state. When $\overline{SHDN}$ > 2.1V, the MAX11080/MAX11081 turn on and begin regulating V$_{AA}$,

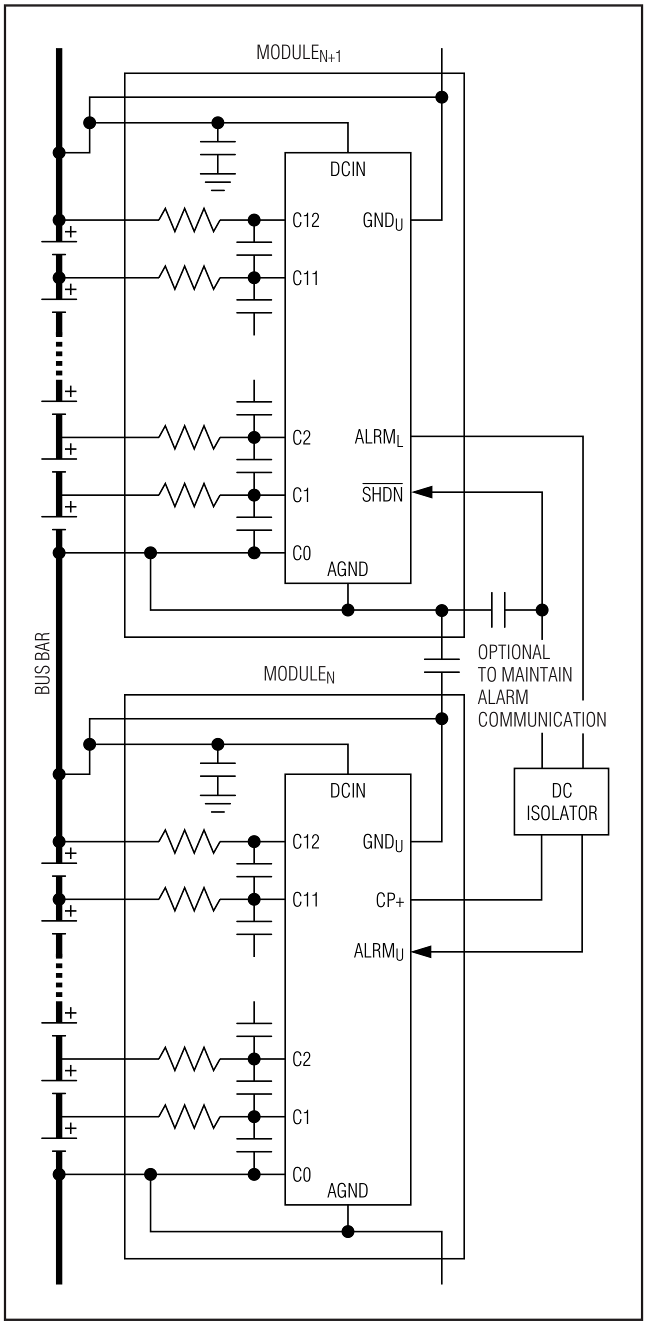


Figure 15. GND_U Connection: AC-Coupled to Next Module, DC-Coupled to Present Module

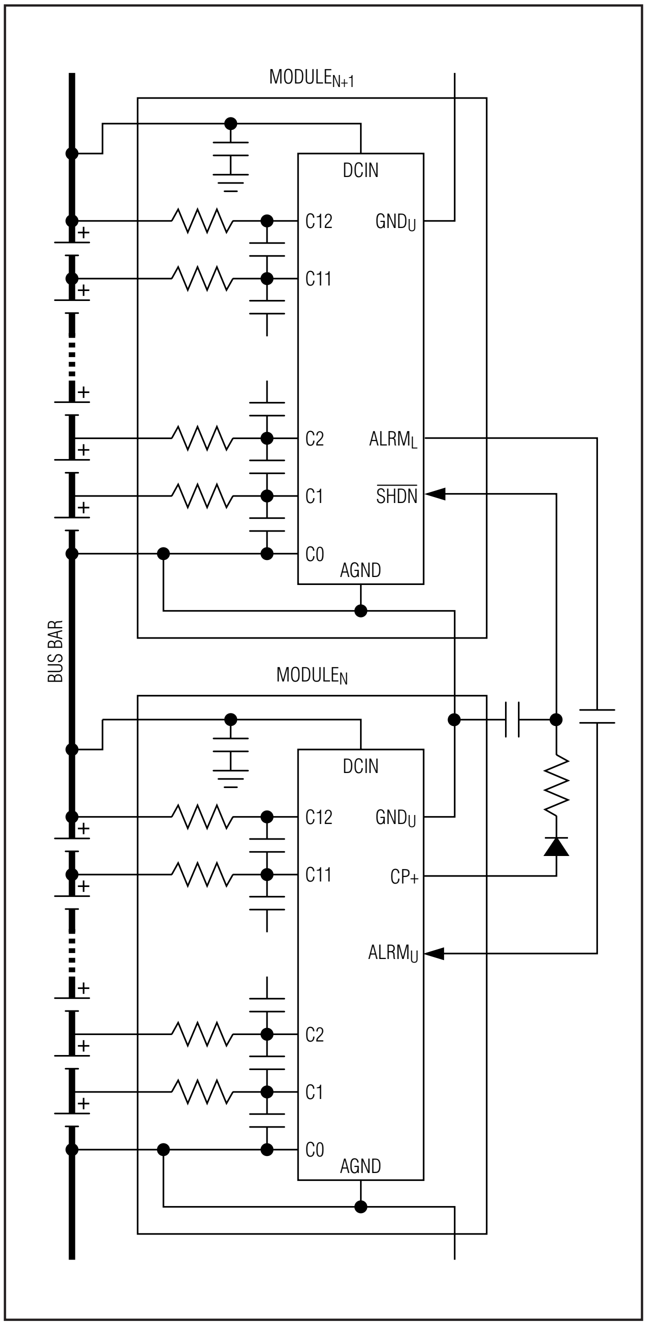


Figure 16. GND_U Connection: DC-Coupled with the Communication Bus

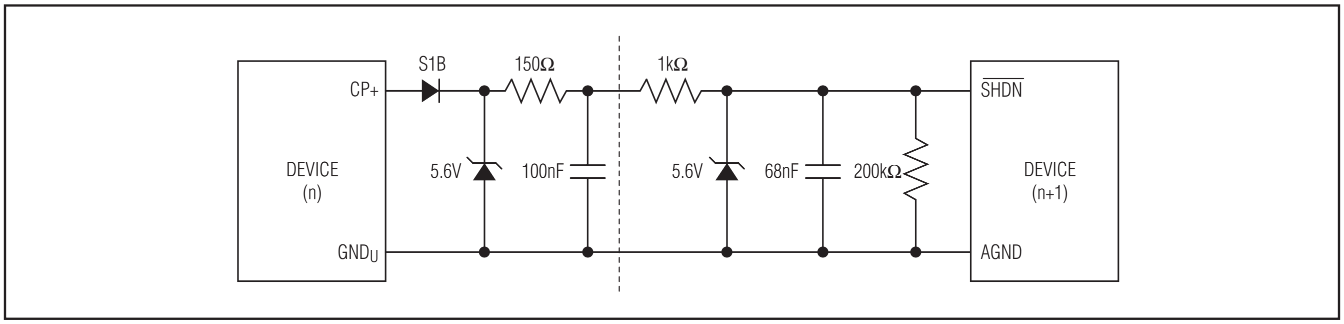


Figure 17. Shutdown Circuit Interface

and then VDD_U. If $\overline{\text{SHDN}}$ < 0.6V, the MAX11080/MAX11081 shut down.

Figure 17 shows the shutdown circuit interface of two daisy-chain devices.

When $\overline{\text{SHDN}}$ is high for device n, the charge pump is enabled and begins to charge the capacitors in the interface circuit. When the voltage of the $\overline{\text{SHDN}}$ pin for device (n+1) rises above the VIH threshold, that device begins its power-up sequence. This action propagates up the daisy-chain until the last battery module is enabled. Conversely, pulling $\overline{\text{SHDN}}$ to AGND powers down a module and thus propagates the power-down to all higher daisy-chained modules as the charge on their $\overline{\text{SHDN}}$ capacitors is dissipated. The zener diodes provide additional ESD protection. The filter capacitors and resistors are sized to provide robust noise immunity. The diode from the CP+ pin should be S1B or a similar low-leakage type for high-temperature stability.

The $\overline{\text{SHDN}}$ pin has a weak internal pulldown resistor on the order of 12MΩ. A 200kΩ or similar resistor from $\overline{\text{SHDN}}$ to AGND should be installed to ensure that the $\overline{\text{SHDN}}$ pin is pulled low when the active $\overline{\text{SHDN}}$ signal is propagated up the daisy-chain bus. The resistor is not needed for applications that tie $\overline{\text{SHDN}}$ high at all times. The typical $\overline{\text{SHDN}}$ rising edge propagation time from one daisy-chained module to the next is 1.5ms.

For FMEA detectability, the $\overline{\text{SHDN}}$ pin is designed to detect logic transitions that could be indicative of a short circuit to the $ALRM_L$ pin. The $\overline{\text{SHDN}}$ pin circuit shown in Figure 18 provides some immunity for rare glitches at the $\overline{\text{SHDN}}$ pin, such as those during power-up, that are not a result of a short to $ALRM_L$. The $\overline{\text{SHDN}}$ pin signal is fed as a clock to a 5-bit counter. When the counter reaches the maximum count of 32, the full flag is set and acts as a clock to a D flip-flop. When the D flip-flop is clocked, its output goes high to signal the FMEA fault condition and trigger the alarm. In this way, the device goes into the alarm state only after 32 pulses on the $\overline{\text{SHDN}}$ pin have occurred. To clear the FMEA fault state, a POR of the device must be activated. The application circuit should ensure that the $\overline{\text{SHDN}}$ pin is glitch free and only toggles when a shutdown or power-down event is intended. This FMEA detection circuit should not be considered as a provision to filter out noise or glitches on the $\overline{\text{SHDN}}$ pin.

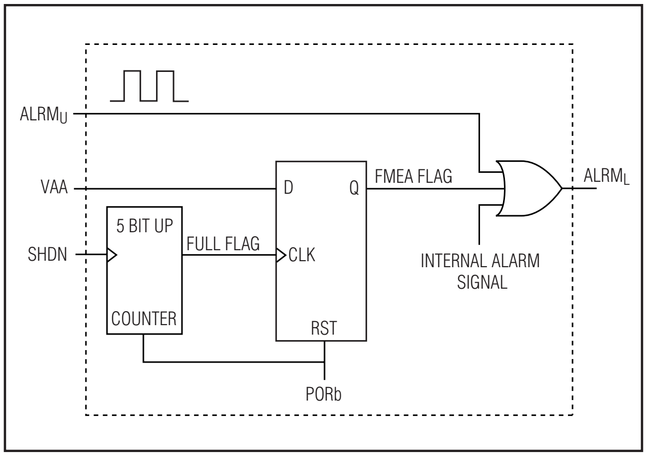


Figure 18. Internal FMEA $\overline{\text{SHDN}}$ Pin Functionality Circuit

C1 Input Absolute Maximum Rating

The C1 input is limited to V_{DCIN} - 0.6V above AGND or a maximum of 20V if the $\overline{\text{SHDN}}$ pin is asserted. If an application requires that the 20V restriction be removed during active shutdown, then a 4.0V zener diode can be added from V_{AA} to AGND. This protects V_{AA} and allows the C1 input to go to V_{DCIN} - 0.6V regardless of the $\overline{\text{SHDN}}$ state. It also allows the differential C1 to C0 voltage to range from -0.3V to +80V.

Cell-Connection and Detection

An individual MAX11080/MAX11081 can be connected to as many as 12 series-connected cells. To accommodate configurations with fewer cells, unused cell inputs must be shorted together, but Cell 1 must always be populated. The designer can choose which cell inputs to leave unused. The example application circuits recommended are the most efficient configurations.

At power-up, the part compares the voltage applied to each cell input with a nominal cell-detection threshold voltage of 0.7V. If the cell voltage is less than the cell-detection threshold, undervoltage detection is disabled for that cell input. If the voltage at the input is 0.7V or greater, undervoltage detection is specified by the state of the UVSEL_ inputs. Overvoltage detection is always enabled for all cell-voltage inputs. The cell-connection detection occurs just before the MAX11080/MAX11081 are fully functional as shown in Figure 12 under NUMBER OF CELLS DETECTED.

TOPSEL Function

The TOPSEL pin is used to indicate to a device whether it is the top device in the daisy-chain stack. The top daisy-chain device is responsible for generating the heartbeat signal at the top of the ALRM_ pin bus. This heartbeat propagates along the chain toward the host. To designate a device as the top device, the TOPSEL pin should be connected to V_{AA}. For all other devices in a daisy-chain, this pin should be connected to AGND. The TOPSEL pin has a weak internal pulldown resistor, but this resistor should not be relied upon as the sole means of setting the TOPSEL logic level. The logic level of the TOPSEL pin is not latched internally at startup and is continuously sampled during operation. The $ALRM_U$ input should be connected to GND_U for the top module as good design practice to prevent noise pickup even though the input logic level is ignored.

For a single device or DC-coupled daisy-chain application, the device can be operated in an alarm level mode instead of heartbeat mode by tying TOPSEL to AGND for all devices. In this mode of operation, $ALRM_L$ passes the signal of $ALRM_U$ when the device is not in the alarm state. $ALRM_L$ drives high when the device is in the alarm state. $ALRM_U$ must be tied to GND_U for the topmost device for this application. The following table summarizes the operation of TOPSEL and $ALRM_L$ for level mode:

TOPSEL	**$ALRM_U$**	**$ALRM_L$**	
		No alarm	Alarm
0	0	$ALRM_U$	1
1	X	Heartbeat	1

Internal Self-Test

The MAX11080/MAX11081 perform an internal self-test during power-up according to the linear regulator power-up flowchart (Figure 12). Each overvoltage comparator is tested for the ability to detect an internally generated overvoltage test condition. This is done by using the ground voltage level as the threshold reference in place of the usual threshold level. Figure 8 shows the connection for this test-mode compare level. If all comparators can detect the internally generated overvoltage test event, part operation continues. If any comparator fails to detect the internally generated overvoltage test event, a fault is signaled using the $ALRM_L$ pin. The device must be power cycled to retest the comparators and attempt to clear this fault condition.

Failure Mode and Effects Analysis

High-voltage battery-pack systems can be subjected to severe stresses during in-service fault conditions and could experience similar conditions during the manufacturing and assembly process. The MAX11080/MAX11081 are designed with high regard to these potential states.

Open and short circuits at the package level must be readily detected for fault diagnosis and should be tolerated whenever possible. A number of circuits are employed within the MAX11080/MAX11081 specifically to detect such conditions and progress to a known device state. Table 3 summarizes other conditions typical in a normal manufacturing process along with their effect on the MAX11080/MAX11081 devices.

See Table 4 for the FMEA analysis of the MAX11080/MAX11081. If the cell voltage is within the monitor range, the heartbeat signal on $ALRM_L$ resumes once the fault condition (either open or short) is removed, unless otherwise specified.

Table 3. System Fault Modes

CONDITION	EFFECT	DESIGN RECOMMENDATION
PCB or IC package open or short circuit—no stack load	Refer to the pin-level FMEA analysis spreadsheet available from the factory	The built-in features of the MAX11080/MAX11081, should ensure low FMEA risk in most cases.
Random connection of cells to IC—no stack load	No effect	The series resistors on the cell inputs of the MAX11080/MAX11081, as well as the internal design, ensure protection against random power-supply or ground connections.
Random connection of modules—no stack load	No effect	Each module is referenced to its neighbor, so no special connection order is necessary.
Random connect/disconnect of communication bus—no stack load; AC- or DC-coupled	Communication from host to the first break in the daisy-chain bus	The level-shifted interface design of the MAX11080/MAX11081 ensures that the $\overline{\text{SHDN}}$, GND_U, and ALRM_ communication bus can be connected at any time with no load.
Random connect/disconnect of communication bus—with stack load; AC- or DC-coupled	Communication from host to the first break in the daisy-chain bus	The level-shifted interface design of the MAX11080/MAX11081 ensures that the $\overline{\text{SHDN}}$, GND_U, ALRM_ communication bus can be connected at any time as long as the power bus is properly connected.
Connect/disconnect module interconnect (bus bar)—no stack load	No effect for DC- or AC-coupled communication bus	A break in the power bus does not cause a problem as long as there is no load on the stack.
Removal/fault of module interconnect (bus bar)—with stack load	No effect for AC-coupled communication bus; device damage for DC-coupled bus	An AC-coupled bus with isolation on the $\overline{\text{SHDN}}$ pin or a redundant bus-bar connection should be used to protect against this case.
Removal/fault of module interconnect (bus bar)—with stack under charge	No effect for AC-coupled communication bus; device damage for DC-coupled bus	An AC-coupled bus with isolation on the $\overline{\text{SHDN}}$ pin or a redundant bus-bar connection should be used to protect against this case.

Table 4. FMEA Analysis (Note 6)

PIN NUMBER	NAME	ACTION	EFFECT
1	DCIN	Open (or Disconnected)	$ALRM_L$ goes high (see Note 7).
		Short to Pin 2	$ALRM_L$ goes high.
2	HV	Open (or Disconnected)	$ALRM_L$ goes high.
		Short to Pin 3	No effect.
3	N.C.	Open (or Disconnected)	No effect.
		Short to Pin 4	No effect.
4	C12	Open (or Disconnected)	• If open occurs before power-up, the part works as if C12 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C12 to C11 is disabled and is not enabled even if the pin is reconnected. • If open occurs after power-up, it is considered a zero voltage input. $ALRM_L$ goes high when the undervoltage is enabled.
		Short to Pin 5	• If short occurs before power-up, the part works as if C12 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C12 to C11 is disabled and is not enabled even if the short is removed. • If short occurs after power-up, the situation is treated as a zero voltage input for C12 to C11. $ALRM_L$ goes high when the undervoltage is enabled.
5	C11	Open (or Disconnected)	$ALRM_L$ goes high because it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 6	• If short occurs before power-up, the part works as if C11 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C11 to C10 is disabled and is not enabled even if the short is removed. • If short occurs after power-up, the situation is treated as a zero voltage input for C11 to C10. $ALRM_L$ goes high when the undervoltage is enabled.
6	C10	Open (or Disconnected)	$ALRM_L$ goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 7	• If short occurs before power-up, the part works as if C10 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C10 to C9 is disabled and is not enabled even if the short is removed. • If short occurs after power-up, the situation is treated as a zero voltage input for C10 to C9. $ALRM_L$ goes high when the undervoltage is enabled.
7	C9	Open (or Disconnected)	$ALRM_L$ goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 8	• If short occurs before power-up, the part works as if C9 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C9 to C8 is disabled and is not enabled even if the short is removed. • If short occurs after power-up, the situation is treated as a zero voltage input for C9 to C8. $ALRM_L$ goes high when the undervoltage is enabled.

Table 4. FMEA Analysis (Note 6) (continued)

PIN NUMBER	NAME	ACTION	EFFECT
8	C8	Open (or Disconnected)	$ALRM_L$ goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 9	• If short occurs before power-up, the part works as if C8 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C8 to C7 is disabled and is not enabled even if the short is removed. • If short occurs after power-up, the situation is treated as a zero voltage input for C8 to C7. $ALRM_L$ goes high when the undervoltage is enabled.
9	C7	Open (or Disconnected)	$ALRM_L$ goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 10	• If short occurs before power-up, the part works as if C7 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C7 to C6 is disabled and is not enabled even if the short is removed. • If short occurs after power-up, the situation is treated as a zero voltage input for C7 to C6. $ALRM_L$ goes high when the undervoltage is enabled.
10	C6	Open (or Disconnected)	$ALRM_L$ goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 11	• If short occurs before power-up, the part works as if C6 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C6 to C5 is disabled and is not enabled even if the short is removed. • If short occurs after power-up, the situation is treated as a zero voltage input for C6 to C5. $ALRM_L$ goes high when the undervoltage is enabled.
11	C5	Open (or Disconnected)	$ALRM_L$ goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 12	• If short occurs before power-up, the part works as if C5 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C5 to C4 is disabled and is not enabled even if the short is removed. • If short occurs after power-up, the situation is treated as a zero voltage input for C5 to C4. $ALRM_L$ goes high when the undervoltage is enabled.
12	C4	Open (or Disconnected)	$ALRM_L$ goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 13	• If short occurs before power-up, the part works as if C4 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C4 to C3 is disabled and is not enabled even if the short is removed. • If short occurs after power-up, the situation is treated as a zero voltage input for C4 to C3. $ALRM_L$ goes high when the undervoltage is enabled.

Table 4. FMEA Analysis (Note 6) (continued)

PIN NUMBER	NAME	ACTION	EFFECT
13	C3	Open (or Disconnected)	$ALRM_L$ goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 14	• If short occurs before power-up, the part works as if C3 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C3 to C2 is disabled and is not enabled even if the short is removed. • If short occurs after power-up, the situation is treated as a zero voltage input for C5 to C4. $ALRM_L$ goes high when the undervoltage is enabled.
14	C2	Open (or Disconnected)	$ALRM_L$ goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 15	• If short occurs before power-up, the part works as if C2 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C2 to C1 is disabled and is not enabled even if the short is removed. • If short occurs after power-up, the situation is treated as a zero voltage input for C2 to C1. $ALRM_L$ goes high when the undervoltage is enabled.
15	C1	Open (or Disconnected)	$ALRM_L$ goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 16	$ALRM_L$ goes high irrespective of whether undervoltage is enabled/disabled and before *and* after power-up.
16	C0	Open (or Disconnected)	No effect.
		Short to Pin 17	• If pin 17 is tied to V_{AA}, then V_{AA} is shorted to AGND and ALRML goes low. • If pin 17 is tied to AGND, there is no effect.
17	UVSEL0	Open (or Disconnected)	The pin defaults to low due to the internal pulldown (see Note 8). The effect depends on the intended undervoltage setting.
		Short to Pin 18	• If pin 17 and pin 18 have the same intended value, there is no effect for the short. • If pin 17 and pin 18 have a different setting, the V_{AA} is shorted to AGND. $ALRM_L$ goes low.
18	UVSEL1	Open (or Disconnected)	The pin defaults to low due to the internal pulldown (see Note 8). The effect depends on the intended undervoltage setting.
		Short to Pin 19	• If pin 18 and pin 19 have the same intended value, there is no effect for the short. • If pin 18 and pin 19 have a different setting, the V_{AA} is shorted to AGND. $ALRM_L$ goes low.
19	UVSEL2	Open (or Disconnected)	The pin defaults to low due to the internal pulldown (see Note 8). The effect depends on the intended undervoltage setting.
		Short to Pin 20	• If pin 19 and pin 20 have the same intended value, there is no effect for the short. • If pin 19 and pin 20 have the different setting, the V_{AA} is shorted to. AGND $ALRM_L$ goes low.

Table 4. FMEA Analysis (Note 6) (continued)

PIN NUMBER	NAME	ACTION	EFFECT
20	OVSEL0	Open (or Disconnected)	The pin defaults to low due to the internal pulldown (see Note 8). The effect depends on the intended overvoltage setting.
		Short to Pin 21	• If pin 20 and pin 21 have the same intended value, there is no effect for the short. • If pin 20 and pin 21 have a different setting, the V_{AA} is shorted to AGND. $ALRM_L$ goes low.
21	OVSEL1	Open (or Disconnected)	The pin defaults to low due to the internal pulldown (see Note 8). The effect depends on the intended overvoltage setting.
		Short to Pin 22	• If pin 21 and pin 22 have the same intended value, there is no effect for the short. • If pin 21 and pin 22 have a different setting, the V_{AA} is shorted to AGND. $ALRM_L$ goes low.
22	OVSEL2	Open (or Disconnected)	The pin defaults to low due to the internal pulldown (see Note 8). The effect depends on the intended overvoltage setting.
		Short to Pin 23	• If pin 22 and pin 23 have the same intended value, there is no effect for the short. • If pin 22 and pin 23 have a different setting, the V_{AA} is shorted to AGND. $ALRM_L$ goes low.
23	OVSEL3	Open (or Disconnected)	The pin defaults to low due to the internal pulldown (see Note 8). The effect depends on the intended overvoltage setting.
		Short to Pin 24	• If pin 23 is set high, there is no effect for the short. • If pin 23 is set low, the V_{AA} is shorted to AGND. $ALRM_L$ goes low.
24	V_{AA}	Open (or Disconnected)	$ALRM_L$ goes high.
		Short to Pin 25	$ALRM_L$ goes low.
25	AGND	Open (or Disconnected)	V_{AA} goes to approximately 100mV and $ALRM_L$ is approximately 0.5V. There is no heartbeat if there is a one before the opening.
		Short to Pin 26	The device is in shutdown mode. $ALRM_L$ is low.
26	$\overline{\text{SHDN}}$	Open (or Disconnected)	The pin is internally pulled down and the device goes to the shutdown mode. $ALRM_L$ is low.
		Short to Pin 27	$ALRM_L$ goes high and stays high even if the short is removed. The internal detect circuit considers this a major failure and the part has to be repowered up to come out of this state.
27	$ALRM_L$	Open (or Disconnected)	The signal at the $ALRM_L$ cannot be seen by the host.
		Short to Pin 28	$ALRM_L$ goes high and stays high even if the short is removed. The internal detect circuit considers this a major failure and the part has to be repowered up to come out of this state.
28	CD	Open (or Disconnected)	The delay between the fault condition and alarm setting ($ALRM_L$ goes high) goes to the minimum. This means there is almost no delay.
		Short to Pin 29	The delay between the fault condition and alarm setting ($ALRM_L$ goes high) is approximately 4s, which is set by the internal watchdog.

Table 4. FMEA Analysis (Note 6) (continued)

PIN NUMBER	NAME	ACTION	EFFECT
29	TST1	Open (or Disconnected)	No effect.
		Short to Pin 30	No effect.
30	TST2	Open (or Disconnected)	No effect.
		Short to Pin 31	If pin TOPSEL is set high (V_{AA}), it causes the short between V_{AA} and AGND. $ALRM_L$ is low. There is no effect if TOPSEL is set low.
31	TOPSEL	Open (or Disconnected)	If the part is the topmost device in the daisy chain, the $ALRM_L$ is set high as the state of TOPSEL is low (internally pulled down). There are no other effects as the state of the pin stays the same (both low).
		Short to Pin 32	No effect if TOPSEL is set low. If TOPSEL is set high, it causes the short between V_{AA} and AGND and $ALRM_L$ is low.
32	TST3	Open (or Disconnected)	No effect.
		Short to Pin 33	No effect.
33	N.C.	Open (or Disconnected)	No effect.
		Short to Pin 34	No effect.
34	$ALRM_U$	Open (or Disconnected)	$ALRM_U$ is internally pulled up to VDD_U. There is no effect to the topmost device. Otherwise, the communication of the chain is broken and the alarm signal from the parts close to the topmost device are not passed through. Since $ALRM_L$ is a reflection of $ALRM_U$, the state of $ALRM_L$ is high for the no-alarm state.
		Short to Pin 35	No effect for the topmost device. Otherwise, the communication of the chain is broken and the alarm signal from the parts close to the topmost are not passed through. Since $ALRM_L$ is a reflection of $ALRM_U$, the state of $ALRM_L$ is low for the no-alarm state.
35	GND_U	Open (or Disconnected)	The $ALRM_L$ goes high.
		Short to Pin 36	The $ALRM_L$ is high. (See Note 9.)
36	VDD_U	Open (or Disconnected)	$ALRM_L$ goes high. HV is approximately 0.4V below DCIN. (See Note 9.)
		Short to Pin 37	$ALRM_L$ goes high. VDD_U is approximately 0.5V lower than GND_U. (See Note 9.)
37	CP-	Open (or Disconnected)	$ALRM_L$ goes high. VDD_U and HV collapse.
		Short to Pin 38	$ALRM_L$ goes high. VDD_U is approximately 0.5V lower than GND_U. (See Note 9.)
38	CP+	Open (or Disconnected)	$ALRM_L$ goes high. VDD_U and HV collapse. (See Note 9.)

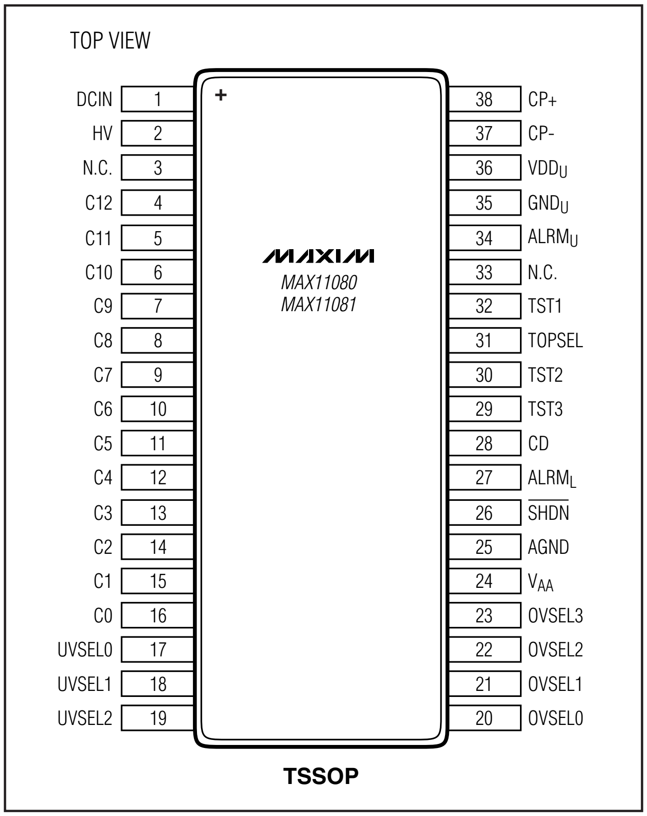
Note 6: If the cell voltage is within the monitor range, the heartbeat signal on $ALRM_L$ resumes once the fault condition is removed.

Note 7: The voltage level of high is equal to V_{AA} and low is equal to AGND.

Note 8: Even if the pin has internal pulldown, the pulldown is very weak and the pin should be tied to AGND for logic 0 setting.

Note 9: VDD_U - GND_U = 3.3V and HV - DCIN = 3.6V for the typical configuration. When VDD_U and HV collapse, $VDD_U - GND_U \approx 0V$ and HV - DCIN ≈ -0.4V.

Pin Configuration



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
38 TSSOP	U38-1	**21-0081**	**90-0140**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/09	Initial release	—
1	6/10	Added the MAX11081; corrected bugs found in application; new derivative of C015 featuring timed fault hysteresis in the order of 50mV or less	1–29