MAX44264

nanoPower Op Amp in a Tiny 6-Bump WLP

General Description

The MAX44264 is an ultra-small (6-bump WLP) op amp that draws only 750nA of supply current. It operates from a single +1.8V to +5.5V supply and features ground-sensing inputs and rail-to-rail output. The ultralow supply current, low-operating voltage, and rail-to-rail output capabilities make these operational amplifiers ideal for use in single lithium ion (Li+), or two-cell NiCd or alkaline battery systems. The rail-to-rail output stage of the MAX44264 is capable of driving the output voltage to within 4mV of the rail with a 100kΩ load, and can sink and source 11mA with a +5V supply. The IC is unity-gain stable and available in a space-saving 0.9mm x 1.3mm, 6-bump WLP package.

Applications

- Cell Phones
- Tablet/Notebook Computers
- Mobile Accessories
- Battery-Powered Devices

Benefits and Features

- Ultra-Low 750nA Supply Current per Amplifier
- Ultra-Low +1.8V Supply Voltage Operation
- Ground-Sensing Input Common-Mode Range
- Outputs Swing Rail-to-Rail
- Outputs Source and Sink 11mA of Load Current
- No Phase Reversal for Overdriven Inputs
- High 120dB Open-Loop Voltage Gain
- Low 500µV Input Offset Voltage
- 9kHz Gain-Bandwidth Product
- 250pF (min) Capacitive Load Capability
- Available in a Tiny, 0.9mm x 1.3mm, 6-Bump WLP Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX44264EWT+	-40°C to +85°C	6 WLP	+CB

+Denotes a lead(Pb)-free/RoHS-compliant package.

19-5708; Rev 1; 3/17

maxim integrated™

Absolute Maximum Ratings

V_{DD} to V_{SS} ..... -0.3V to +6V
IN_+ or IN_- ..... (V_{SS} - 0.3V) to (V_{DD} + 0.3V)
OUT_ Shorted to V_{SS} or V_{DD} ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
6-Bump WLP (derate 10.5mW/°C above +70°C) 840mW

Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = 0V, V_{OUT} = V_{DD}/2, R_L = ∞ to V_{DD}/2, **T_A = +25°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by PSRR tests		1.8		5.5	V
Supply Current (per Amplifier)	I_{DD}	V_{DD} = +1.8V			0.6		µA
		V_{DD} = +5.0V			0.75	1.2	
Input Offset Voltage	V_{OS}				±0.5	±7.0	mV
Input Bias Current	I_B				±200	±1500	pA
Input Offset Current	I_{OS}				±12.5		pA
Input Common-Mode Voltage Range	V_{CM}	Guaranteed by the CMRR test		V_{SS}		V_{DD} - 1.1	V
Common-Mode Rejection Ratio	CMRR	Specified with V_{SS} ≤ V_{CM} ≤ (V_{DD} - 1.1V)		70	95		dB
Power-Supply Rejection Ratio	PSRR	+1.8V ≤ V_{DD} ≤ +5.5V		70	90		dB
Large-Signal Voltage Gain	A_{VOL}	R_L = 1MΩ, V_{OUT} = 50mV to V_{DD} - 50mV		90	120		dB
		R_L = 100kΩ, V_{OUT} = 200mV to V_{DD} - 200mV		90	112		
		R_L = 10kΩ, V_{OUT} = 200mV to V_{DD} - 200mV			100		
Output Voltage Swing	V_{OH}	Swing high specified as V_{DD} - V_{OH}	R_L = 1MΩ		1	4	mV
			R_L = 100kΩ		4	10	
			R_L = 10kΩ		40		
	V_{OL}	Swing low specified as V_{OL} - V_{SS}	R_L = 1MΩ		0.5	5	
			R_L = 100kΩ		1	5	
			R_L = 10kΩ		10		
Gain-Bandwidth Product	GBW				9		kHz
Phase Margin	Φ_M				90		degrees

Electrical Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = 0V, V_{OUT} = V_{DD}/2, R_L = ∞ to V_{DD}/2, **T_A = +25°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Slew Rate	SR	V_{OUT} = 4V step		2		V/ms
Input Voltage Noise	e_n	f = 1kHz		150		nV/√Hz
		f = 10kHz		120		
Output Short-Circuit Current		Shorted to V_{SS} (sourcing)		11		mA
		Shorted to V_{DD} (sinking)		36		
Power-On Time	t_{ON}			2		µs
Power-Off Time	t_{OFF}			2		µs
Capacitive Load	C_{LOAD}	No sustained oscillations	250			pF

Electrical Characteristics

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = 0V, V_{OUT} = V_{DD}/2, R_L = ∞ to V_{DD}/2, **T_A = T_{MIN} to T_{MAX}**, unless otherwise noted.) (Note 1)

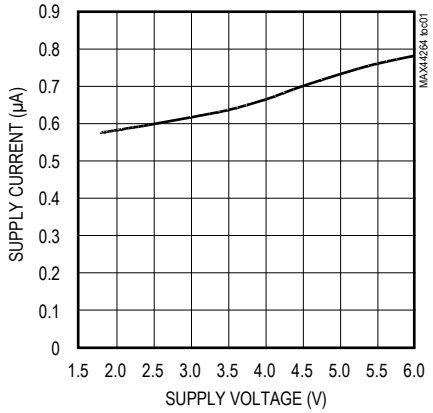
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by PSRR tests		1.8		5.5	V
Supply Current (per Amplifier)	I_{DD}	V_{DD} = +5.0V				1.5	µA
Input Offset Voltage	V_{OS}					±15	mV
Input Offset Voltage Temperature Coefficient	TCV_{OS}				8		µV/°C
Input Bias Current	I_B					4.25	nA
Input Common-Mode Voltage Range	V_{CM}	Guaranteed by the CMRR test		V_{SS}		V_{DD} -1.1	V
Common-Mode Rejection Ratio	CMRR	V_{SS} ≤ V_{CM} ≤ (V_{DD} - 1.1V)		56			dB
Power-Supply Rejection Ratio	PSRR	+1.8V ≤ V_{DD} ≤ +5.5V, 0°C ≤ T_A ≤ +85°C		65			dB
		+2V ≤ V_{DD} ≤ +5.5V, -40°C ≤ T_A ≤ +85°C		65			
Large-Signal Voltage Gain	A_{VOL}	V_{OUT} = 50mV to V_{DD} - 50mV, R_L = 1MΩ		75			dB
		V_{OUT} = 200mV to V_{DD} - 200mV, R_L = 100kΩ		75			
Output Voltage Swing	V_{OH}	Swing high specified as V_{DD} - V_{OH}	R_L = 1MΩ			5	mV
			R_L = 100kΩ			15	
	V_{OL}	Swing low specified as V_{OL} - V_{SS}	R_L = 1MΩ			5	
			R_L = 100kΩ			5	

Note 1: All devices are production tested at T_A = +25°C. All temperature limits are guaranteed by design.

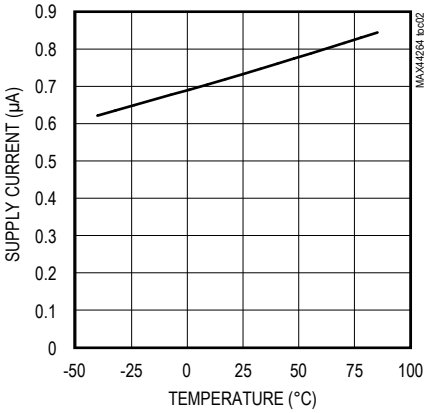
Typical Operating Characteristics

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = 0V, R_L = 100kΩ to V_{DD}/2, T_A = +25°C, unless otherwise noted.)

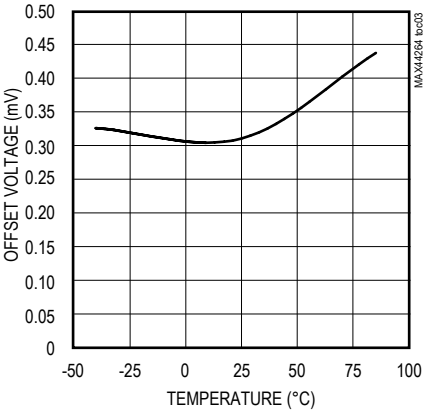
SUPPLY CURRENT vs. SUPPLY VOLTAGE



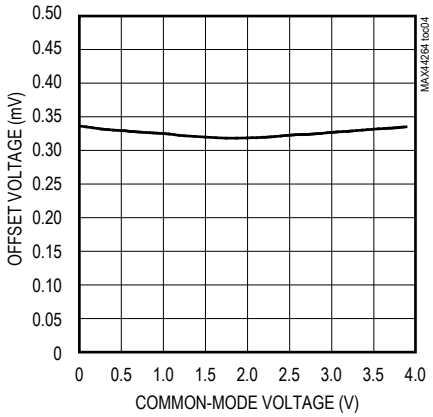
SUPPLY CURRENT vs. TEMPERATURE



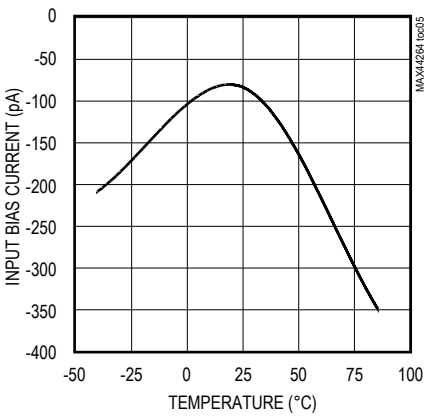
OFFSET VOLTAGE vs. TEMPERATURE



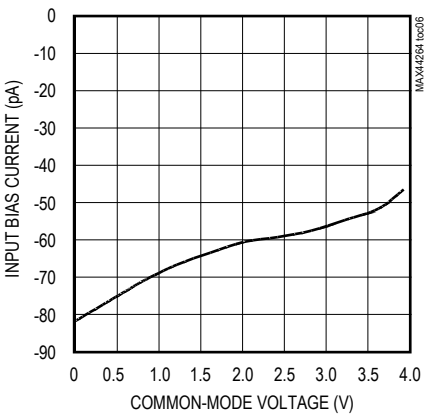
OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



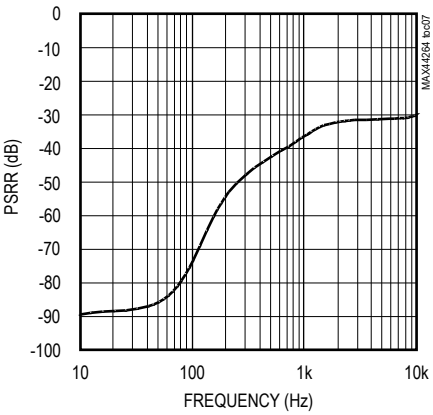
INPUT BIAS CURRENT vs. TEMPERATURE



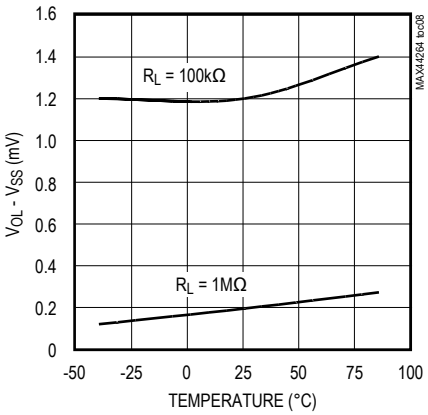
INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



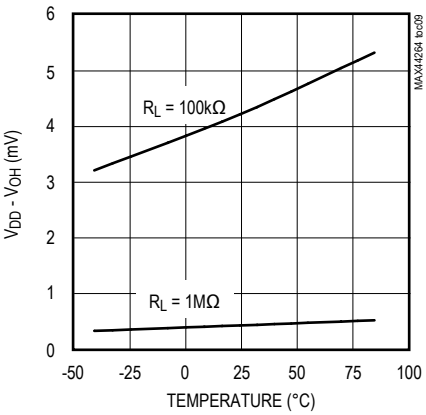
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



OUTPUT VOLTAGE SWING LOW vs. TEMPERATURE



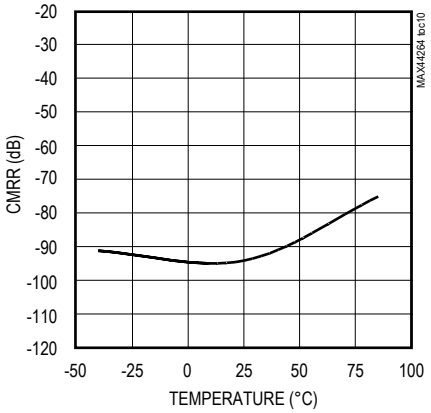
OUTPUT VOLTAGE SWING HIGH vs. TEMPERATURE



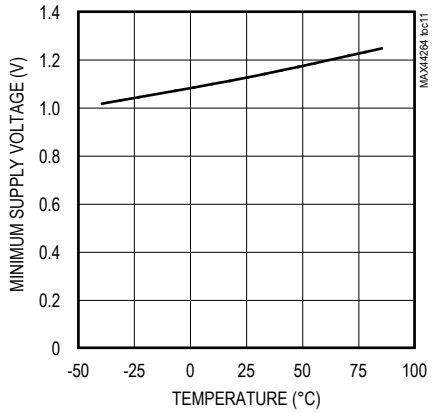
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = 0V, R_L = 100kΩ to V_{DD}/2, T_A = +25°C, unless otherwise noted.)

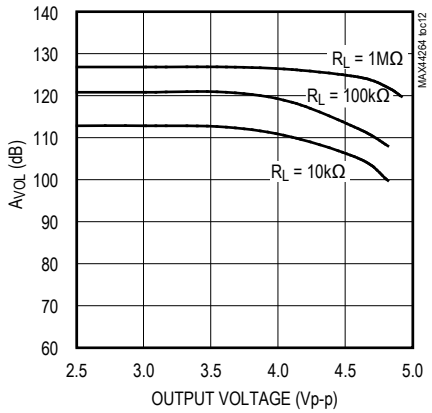
COMMON-MODE REJECTION RATIO vs. TEMPERATURE



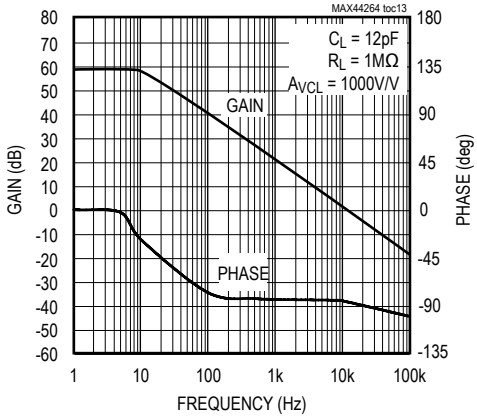
MINIMUM SUPPLY VOLTAGE vs. TEMPERATURE



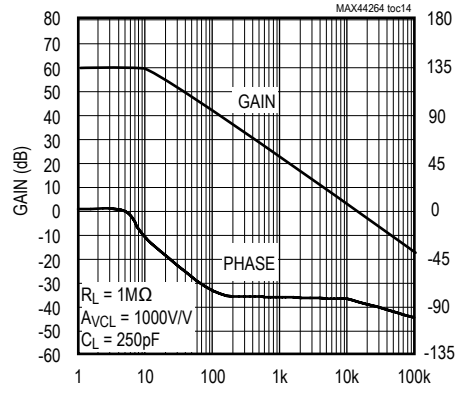
AVOL vs. OUTPUT VOLTAGE SWING



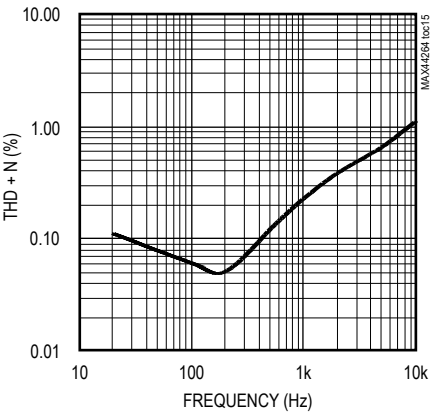
GAIN AND PHASE vs. FREQUENCY



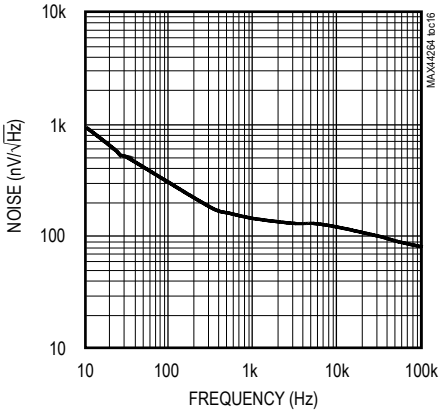
GAIN AND PHASE vs. FREQUENCY



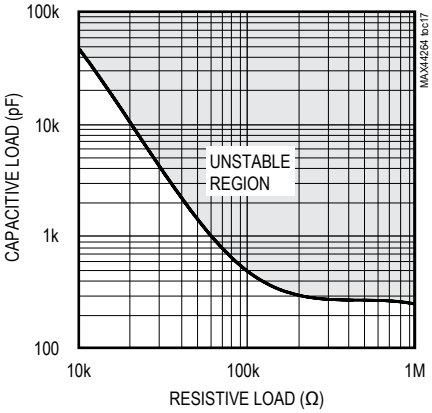
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



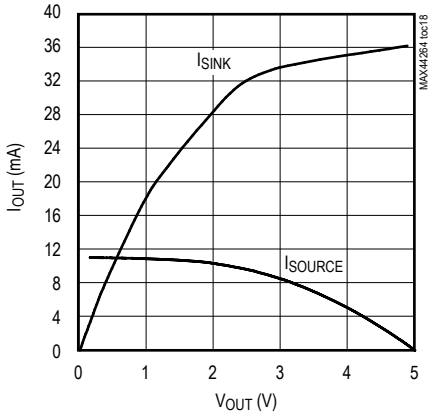
VOLTAGE NOISE DENSITY vs. FREQUENCY



STABILITY vs. CAPACITIVE AND RESISTIVE LOADS



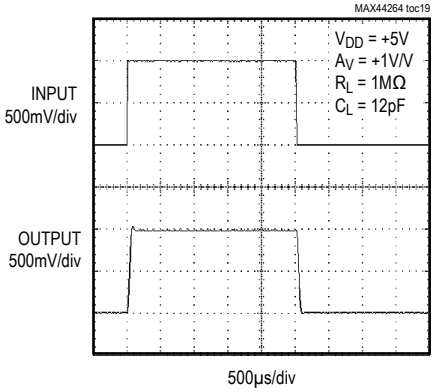
IOUT vs. VOUT



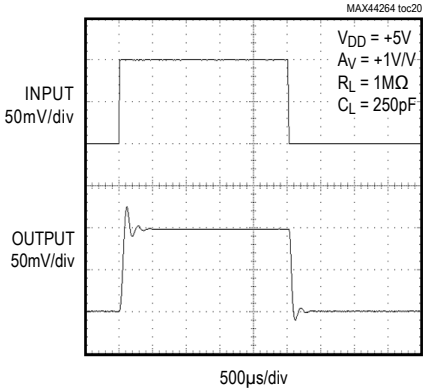
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = 0V, R_L = 100kΩ to V_{DD}/2, T_A = +25°C, unless otherwise noted.)

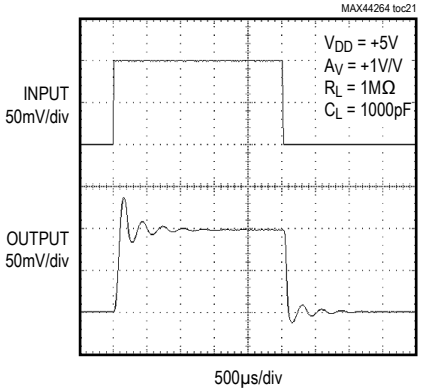
SMALL-SIGNAL STEP RESPONSE



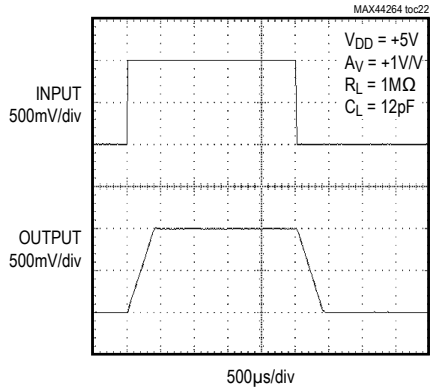
SMALL-SIGNAL STEP RESPONSE



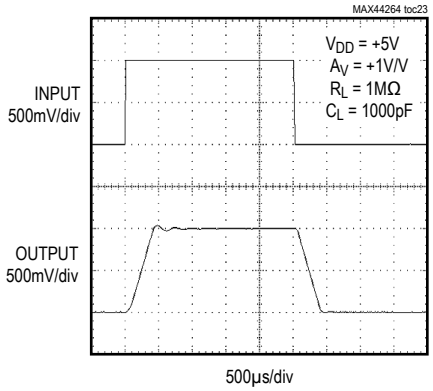
SMALL-SIGNAL STEP RESPONSE



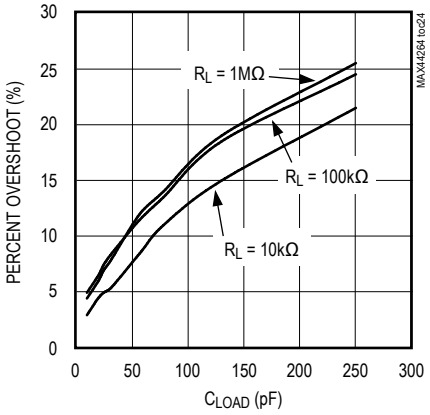
LARGE-SIGNAL STEP RESPONSE



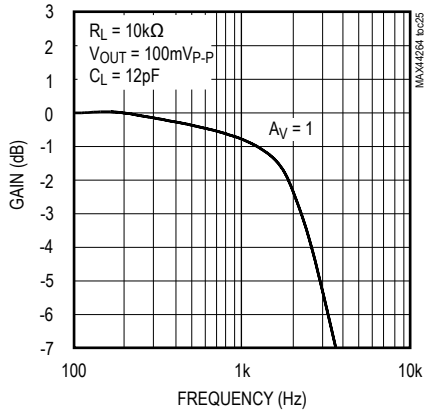
LARGE-SIGNAL STEP RESPONSE



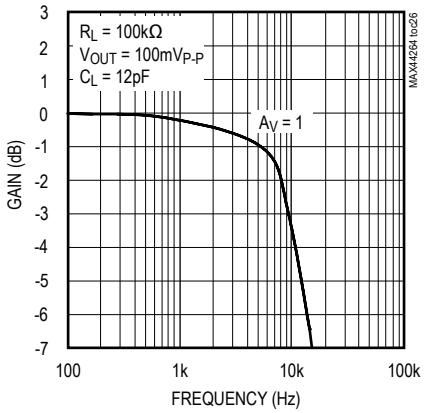
PERCENT OVERSHOOT vs. CAPACITIVE LOAD



SMALL-SIGNAL GAIN vs. FREQUENCY



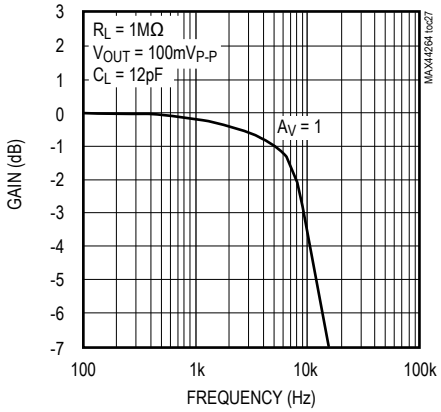
SMALL-SIGNAL GAIN vs. FREQUENCY



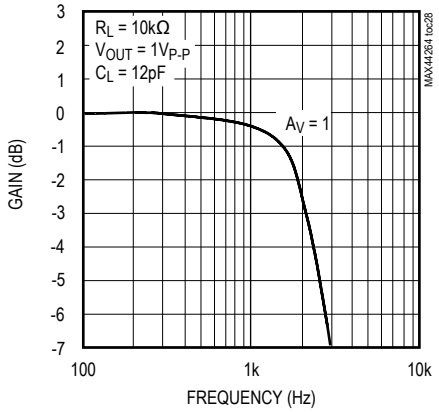
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = 0V, R_L = 100kΩ to V_{DD}/2, T_A = +25°C, unless otherwise noted.)

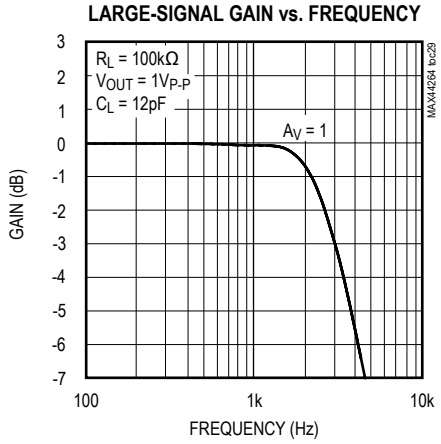
SMALL-SIGNAL GAIN vs. FREQUENCY



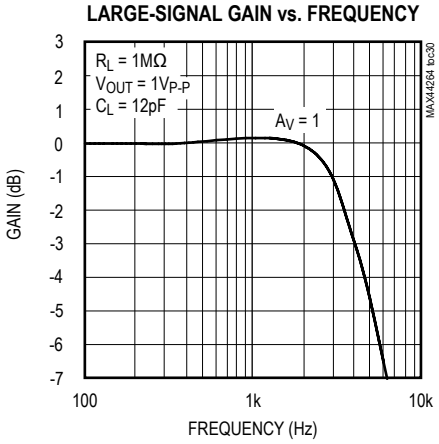
LARGE-SIGNAL GAIN vs. FREQUENCY



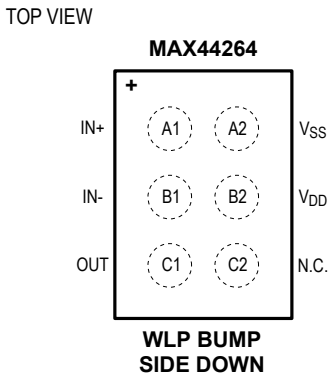
LARGE-SIGNAL GAIN vs. FREQUENCY



LARGE-SIGNAL GAIN vs. FREQUENCY



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
A1	IN+	Noninverting Amplifier Input
A2	V_{SS}	Negative Power-Supply Voltage
B1	IN-	Inverting Amplifier Input
B2	V_{DD}	Positive Power-Supply Voltage
C1	OUT	Amplifier Output
C2	N.C.	No Connection. Not internally connected.

Applications Information

Ground Sensing

The common-mode input range of the MAX44264 extends down to ground, and offers excellent common-mode rejection. These devices are guaranteed not to undergo phase reversal when the input is overdriven.

Power Supplies and Layout

The IC operates from a single +1.8V to +5.5V power supply. Bypass power supplies with a 0.1µF ceramic capacitor placed close to the V_{DD} pin.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the op amp's inputs and outputs. To decrease stray capacitance, minimize PCB lengths and resistor leads, and place external components close to the op amps' pins.

Bandwidth

The IC is internally compensated for unity-gain stability and has a typical gain-bandwidth of 9kHz.

Stability

The IC maintains stability in their minimum gain configuration while driving capacitive loads. Although this product family is primarily designed for low-frequency applications, good layout is extremely important because low-power requirements demand high-impedance circuits. The layout should also minimize stray capacitance at the amplifier inputs. However some stray capacitance may be unavoidable, and it may be necessary to add a 2pF to 10pF capacitor across the feedback resistor as shown in Figure 1. Select the smallest capacitor value that ensures stability.

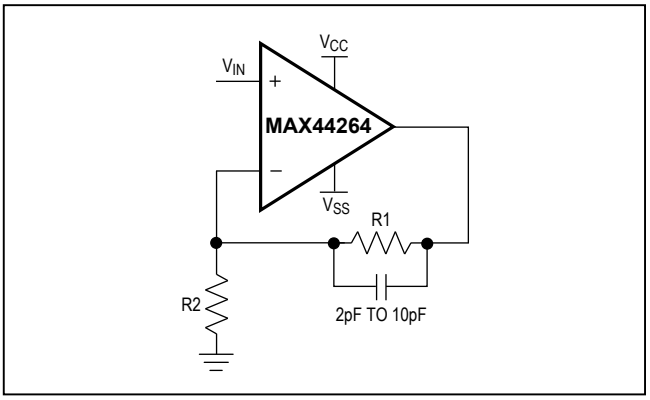


Figure 1. Compensation for Feedback Node Capacitance

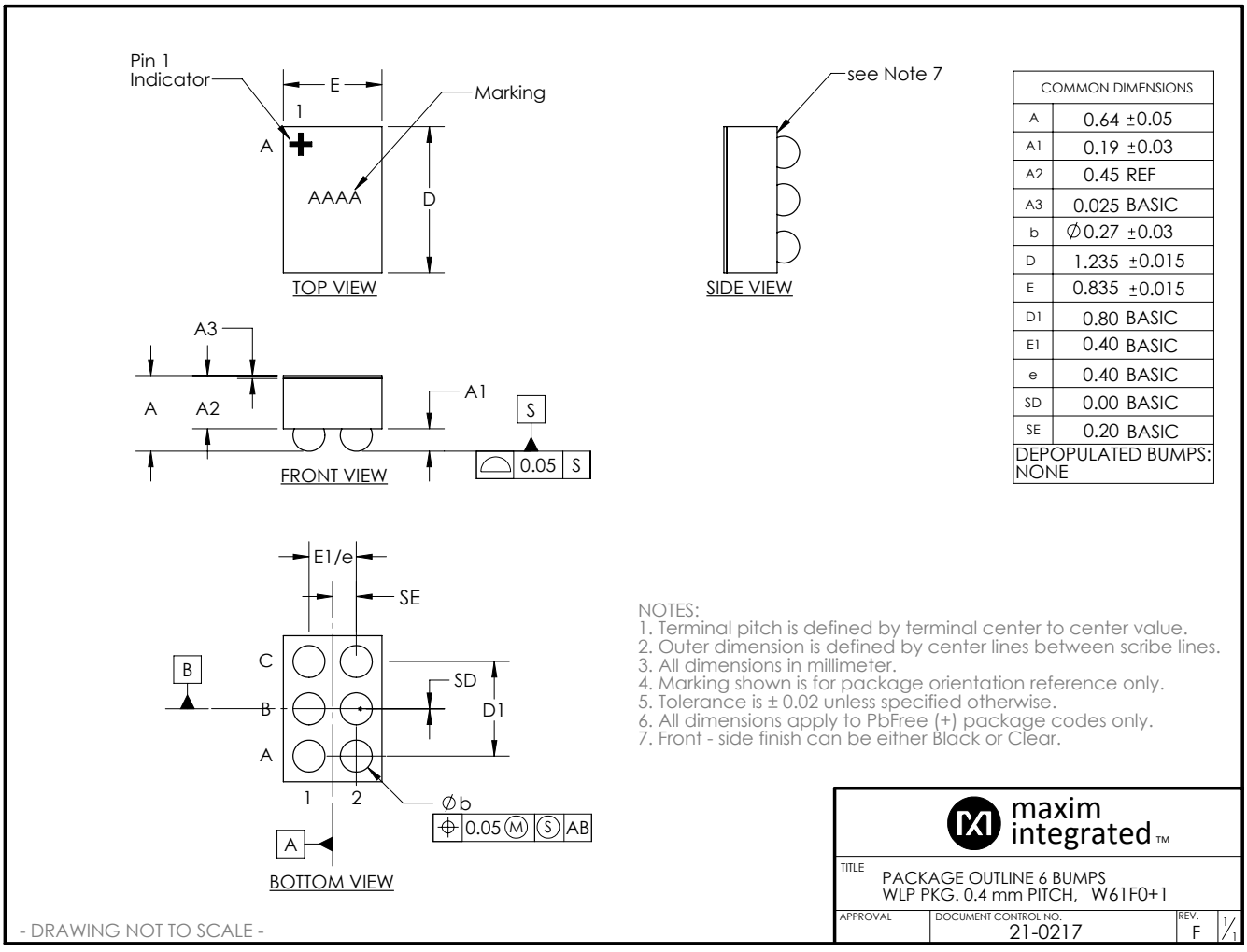
Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 WLP	W61B1+1	21-0217	—



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.19 ±0.03
A2	0.45 REF
A3	0.025 BASIC
b	∅0.27 ±0.03
D	1.235 ±0.015
E	0.835 ±0.015
D1	0.80 BASIC
E1	0.40 BASIC
e	0.40 BASIC
SD	0.00 BASIC
SE	0.20 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

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TITLE: PACKAGE OUTLINE 6 BUMPS
WLP PKG. 0.4 mm PITCH, W61F0+1

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0217	F	1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/10	Initial release	—
1	3/17	Updated title to include “nanoPower”	1–10

