

**SCHOTTKY BARRIER DIODES – LEADLESS PACKAGE FOR SURFACE MOUNT**  
**– METALLURGICALLY BONDED**  
**– DOUBLE PLUG CONSTRUCTION**

*Qualified per MIL-PRF-19500/444*

**DEVICES**

<b>1N5711UR-1</b>	<b>1N6857UR-1</b>	<b>CDLL2810</b>	<b>CDLL6263</b>
<b>1N5712UR-1</b>	<b>1N6858UR-1</b>	<b>CDLL5711</b>	<b>CDLL6857</b>
		<b>CDLL5712</b>	<b>CDLL6858</b>

**QUALIFIED LEVELS**

**JAN**  
**JANTX**  
**JANTXV**

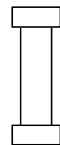
**MAXIMUM RATING AT 25°C**

Operating Temperature:	-65°C to +150°C		
Storage Temperature:	5711 & 6263 types	:33mA dc @ T <sub>EC</sub> = +140°C	
Operating Current:	2810, 5712 & 6858 types	:75mA dc @ T <sub>EC</sub> = +130°C	
	6857 type	:150mA dc @ T <sub>EC</sub> = +110°C	
	all types	:Derate to 0 (zero) mA dc @ +150°C	

Derating:

**ELECTRICAL CHARACTERISTICS (TA = 25°C, unless otherwise specified)**

TYPE NUMBER	MINIMUM BEAKDOWN VOLTAAGE	MAXIMUM FORWARD VOLTAGE	MAXIMUM FORWARD VOLTAGE	MAXIMUM REVERSE LEAKAGE CURRENT		MAXIMUM CAPACITANCE @ V <sub>R</sub> = 0 VOLTS f = 1.0MHz	ESDS CLASS
	V <sub>BR</sub> @ 10µA	V <sub>F</sub> @ 1mA	V <sub>F</sub> @ I <sub>F</sub>	I <sub>R</sub> @ V <sub>R</sub>		C <sub>T</sub>	
	VOLTS	VOLTS	VOLTS @ mA	nA	VOLTS	PICO FARADS	
1N5711UR-1	70	0.41	1.0 @ 15	200	50	2.0	1
1N5712UR-1	20	0.41	1.0 @ 35	150	16	2.0	1
1N6857UR-1	20	0.35	0.75 @ 35	150	16	4.5	2
1N6858UR-1	70	0.36	0.65 @ 15	200	50	4.5	2
CDLL2810	20	0.41	1.0 @ 35	100	15	2.0	1
CDLL5711	70	0.41	1.0 @ 15	200	50	2.0	1
CDLL5712	20	0.41	1.0 @ 35	150	16	2.0	1
CDLL6263	60	0.41	1.0 @ 15	200	50	2.2	1
CDLL6857	20	0.35	0.75 @ 35	150	16	4.5	2
CDLL6858	70	0.36	0.65 @ 15	200	50	4.5	2



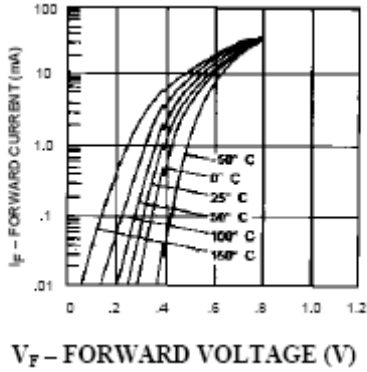
**FIGURE 1**

**NOTE:**

1. Effective Minority Carrier Lifetime ( $\tau$ ) is 100 Pico Seconds
2. Qualification testing to J, JX, JV and JS levels for 6857 and 6858 types is underway. Contact the factory for qualification completion dates. These two part numbers are being introduced by CDI as “drop-in” replacements for the 5711 and 5712. They provide a more robust mechanical design and a higher ESDS class with the only trade-off being an increase in capacitance.

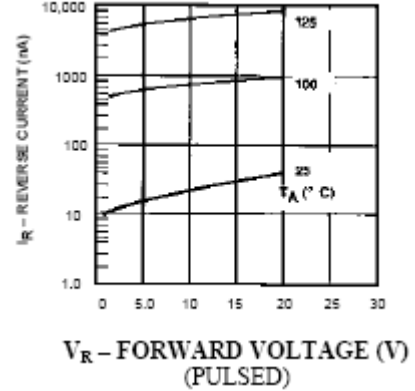
## GRAPHS

**FIGURE 1**



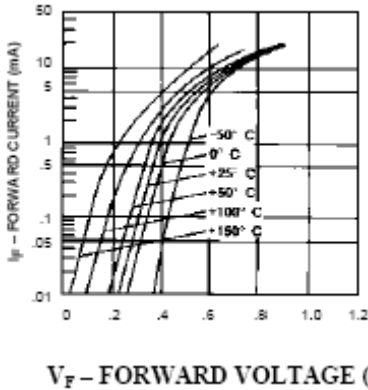
I – V Curve Showing Typical Forward Voltage Variation with Temperature for the CDLL2810 and CDLL5712 Schottky Diodes.

**FIGURE 2**



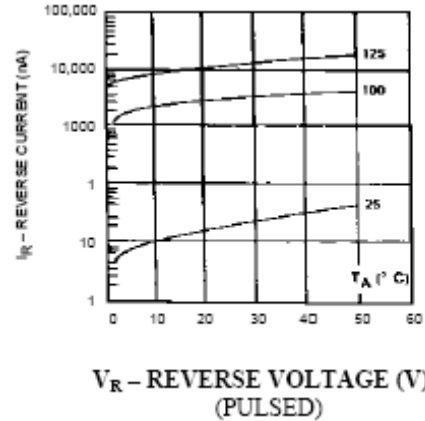
CDLL2810 and CDLL5712 Typical Variation of Reverse Current ( $I_R$ ) vs. Reverse Voltage ( $V_R$ ) at Various Temperatures

**FIGURE 3**



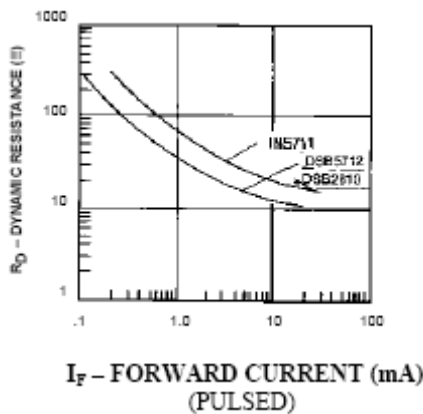
I – V Curve Showing Typical Forward Voltage Variation with Temperature for Schottky Diode CDLL5711.

**FIGURE 4**



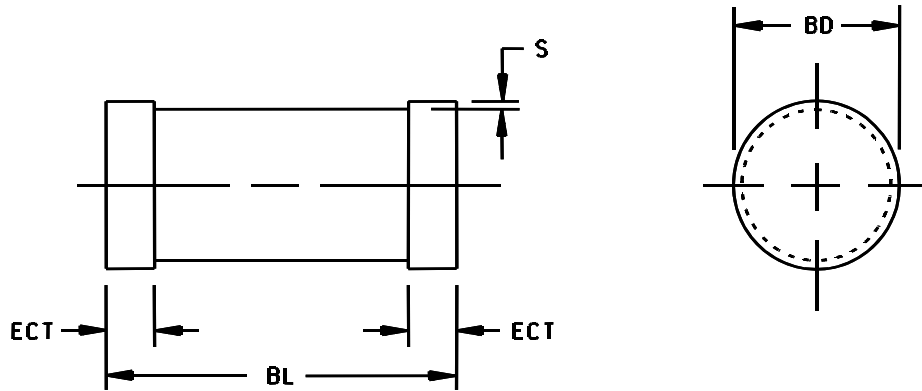
CDLL5711 Typical; Variation of Reverse Current ( $I_R$ ); vs. Reverse Voltage ( $V_R$ ) at Various Temperatures.

**FIGURE 5**



Typical Dynamic Resistance ( $R_D$ ) vs. Forward Current ( $I_F$ )

▶ **PACKAGE DIMENSIONS**



**NOTE:**

1. Dimensions are in inches. Millimeters are given for general information only.
2. In accordance with ASME Y14.5M, diameters are equivalent to  $\Phi x$  symbology.

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BD	.063	.067	1.60	1.70	
BL	.130	.146	3.30	3.71	
ECT	.016	.022	0.41	0.55	
S	.001 Min				

**DESIGN DATA**

**CASE:** DO-213AA, Hermetically sealed glass case. (MELF, SOD-80, LL34)

**LEAD FINISH:** Tin / Lead

**THERMAL RESISTANCE:** ( $R_{\theta EC}$ ): 100°C/W maximum at L = 0 inch

**THERMAL IMPEDANCE:** ( $Z_{\theta IX}$ ): 40°C/W maximum.

**POLARITY:** Cathode end is banded.

**MOUNTING POSITION SURFACE SELECTION:** The Axial Coefficient of Expansion (COE) of this device is approximately +6PPM/°C. The COE of the Mounting Surface System should be selected to provide a suitable match with this device.