



IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

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Thank you for your cooperation and understanding,

WeEn Semiconductors



1. General description

Planar passivated very sensitive gate four quadrant triac in a SOT54 (TO-92) plastic package intended for use in applications requiring direct interfacing to logic ICs and low power gate drivers.

2. Features and benefits

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drive circuits
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate in four quadrants

3. Applications

- General purpose low power motor control
- Home appliances
- Industrial process control
- Low power AC Fan controllers

4. Quick reference data

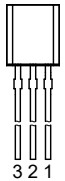
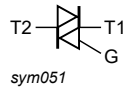
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------------|-------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| V_{DRM} | repetitive peak off-state voltage | | - | - | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{lead} \leq 45\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | - | 1 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | - | 8 | A |
| | | full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$ | - | - | 8.5 | A |
| T_j | junction temperature | | - | - | 125 | °C |
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 7 | - | - | 3 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 7 | - | - | 3 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 7 | - | - | 3 | mA |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------------|
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 7 | - | - | 5 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 9 | - | - | 7 | mA |
| V_T | on-state voltage | $I_T = 1.4\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10 | - | 1.3 | 1.6 | V |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 402\text{ V}$; $T_j = 110\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; Fig. 12 | 10 | - | - | V/ μ s |
| dV_{com}/dt | rate of change of commutating voltage | $V_D = 400\text{ V}$; $T_j = 110\text{ °C}$; $dI_{com}/dt = 0.44\text{ A/ms}$; $I_T = 1\text{ A}$; gate open circuit | 0.5 | - | - | V/ μ s |

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------|---------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|
| 1 | T2 | main terminal 2 |  <p>TO-92 (SOT54)</p> |  <p>sym051</p> |
| 2 | G | gate | | |
| 3 | T1 | main terminal 1 | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------|---------|-------------------------------------------------------------|---------|
| | Name | Description | Version |
| Z0103MA | TO-92 | plastic single-ended leaded (through hole) package; 3 leads | SOT54 |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------|--------------------------------------|-------------------------------------------------------------------------------------------------------------------------|-----|------|------------------|
| V_{DRM} | repetitive peak off-state voltage | | - | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{lead} \leq 45\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | 1 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | 8 | A |
| | | full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$ | - | 8.5 | A |
| I^2t | I^2t for fusing | $t_p = 10\text{ ms}$; SIN | - | 0.32 | A ² s |
| di_T/dt | rate of rise of on-state current | $I_G = 6\text{ mA}$ | - | 50 | A/ μ s |
| | | $I_G = 10\text{ mA}$ | - | 20 | A/ μ s |
| | | $I_G = 6\text{ mA}$ | - | 50 | A/ μ s |
| I_{GM} | peak gate current | | - | 1 | A |
| P_{GM} | peak gate power | | - | 2 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | - | 0.1 | W |
| T_{stg} | storage temperature | | -40 | 150 | °C |
| T_j | junction temperature | | - | 125 | °C |

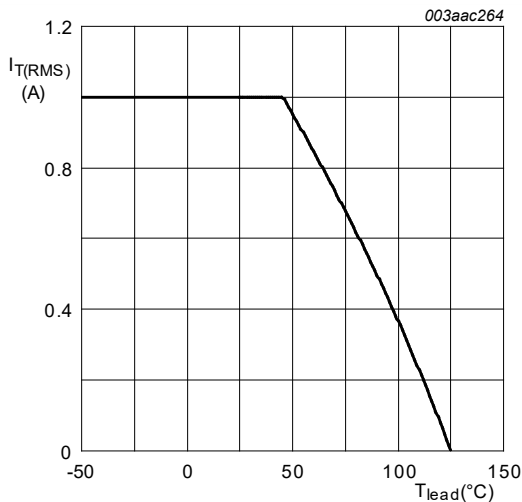


Fig. 1. RMS on-state current as a function of lead temperature; maximum values

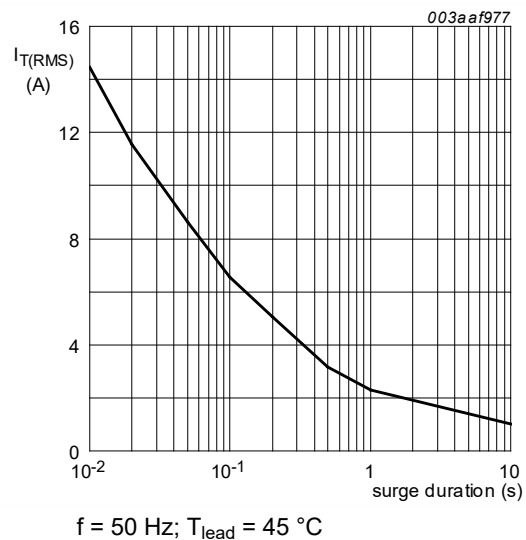


Fig. 2. RMS on-state current as a function of surge duration; maximum values

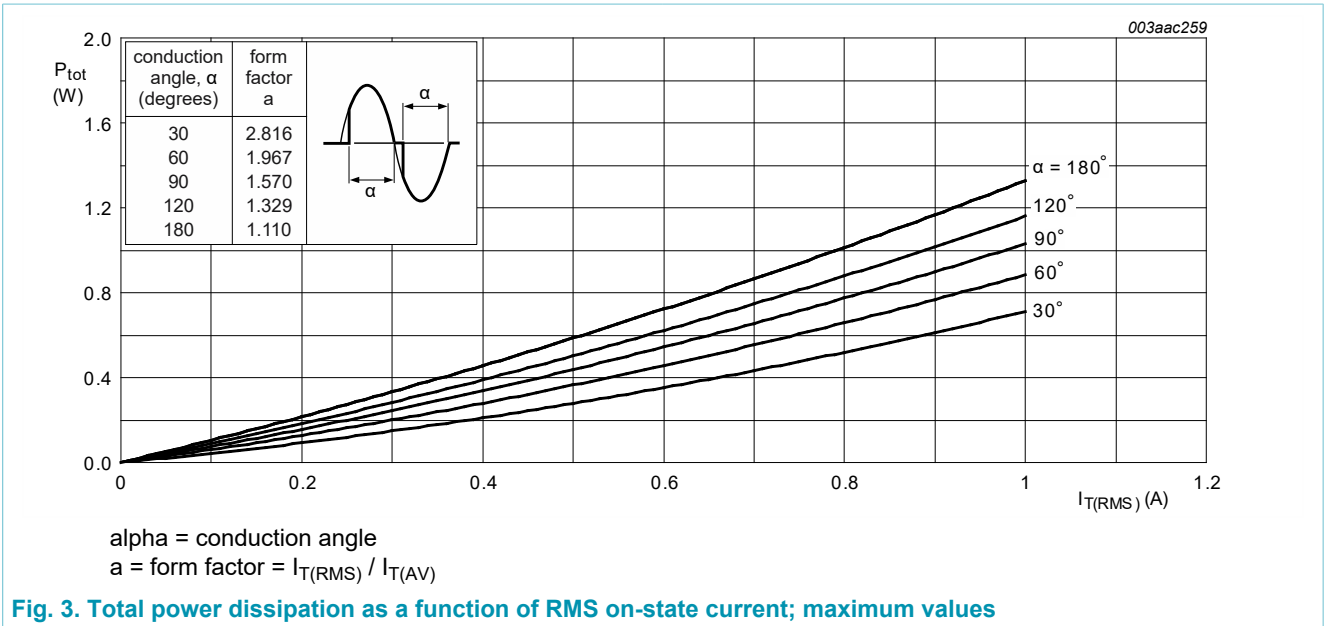


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

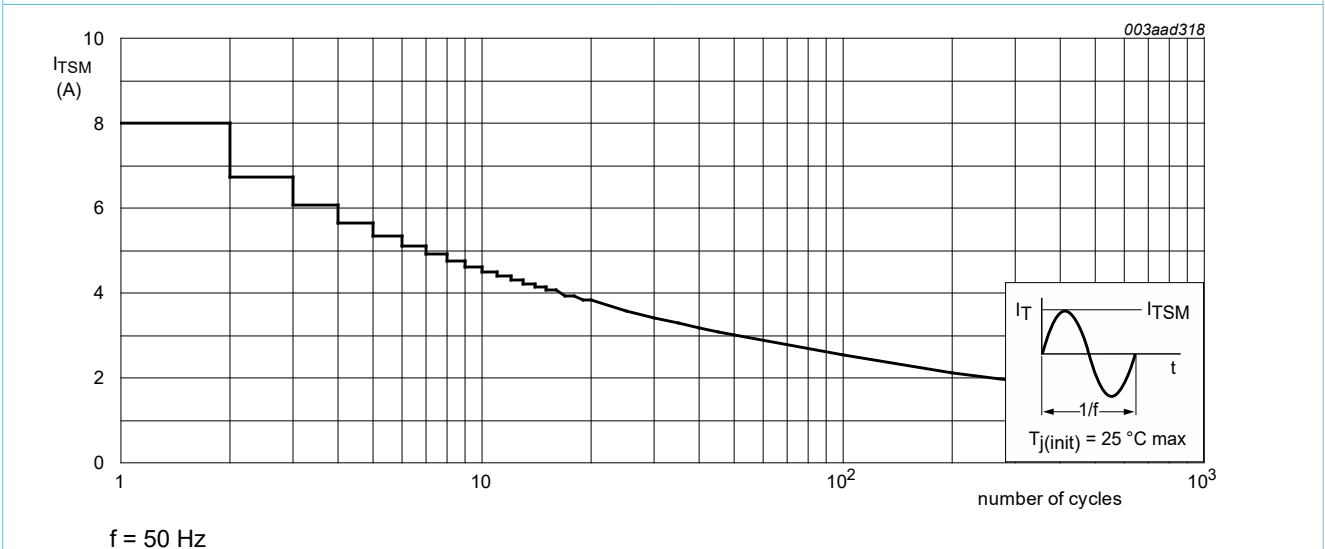
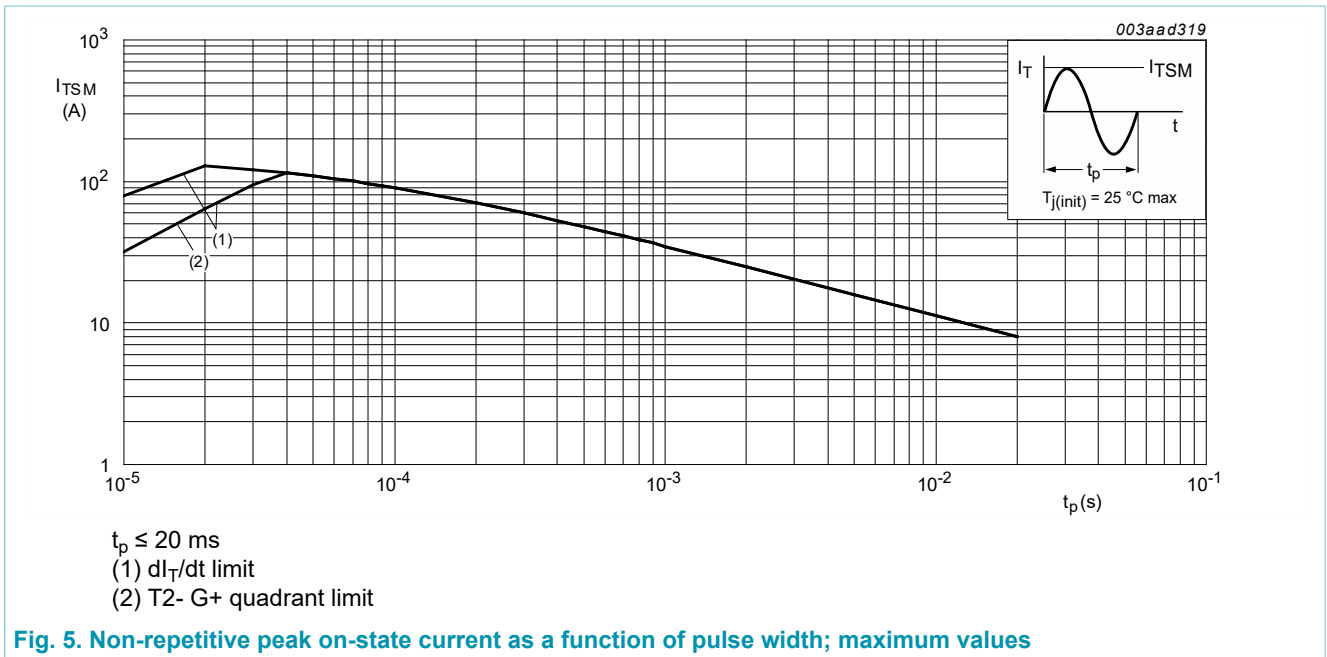


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|------------------------------------------------------|---------------------------------------------------------------|-----|-----|-----|------|
| $R_{th(j-lead)}$ | thermal resistance from junction to lead | full cycle; Fig. 6 | - | - | 60 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient free air | full cycle; printed circuit board mounted; lead length = 4 mm | - | 150 | - | K/W |

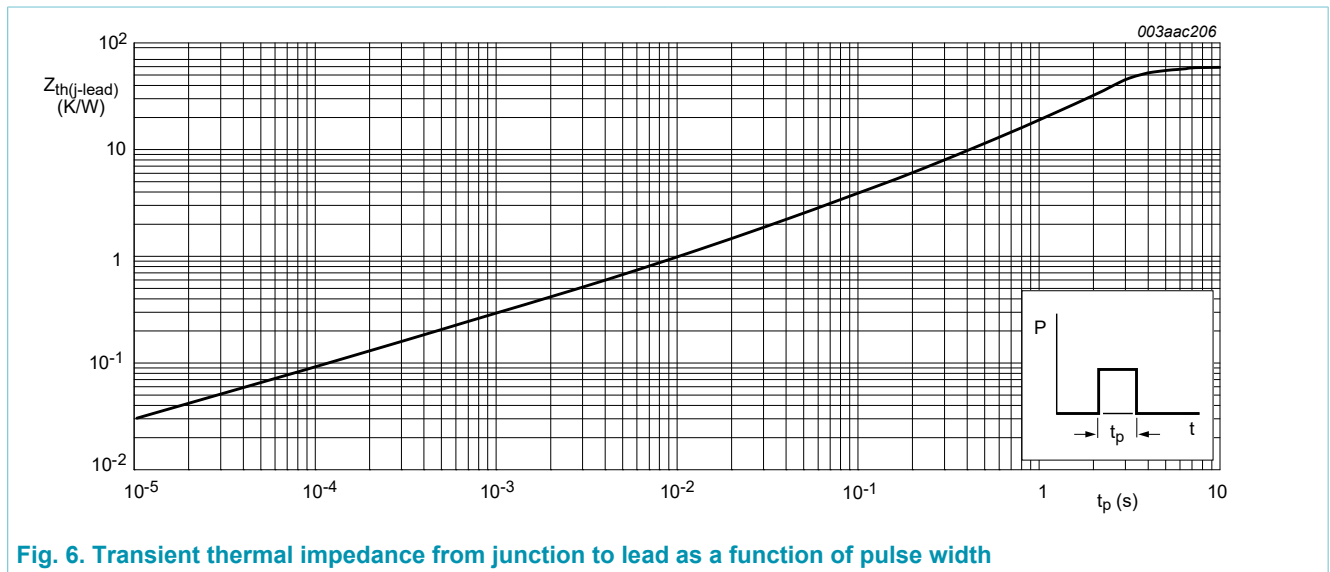


Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width

9. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------------|
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 7 | - | - | 3 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 7 | - | - | 3 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 7 | - | - | 3 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 7 | - | - | 5 | mA |
| I_L | latching current | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 8 | - | - | 7 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 8 | - | - | 15 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 8 | - | - | 7 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 8 | - | - | 7 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 9 | - | - | 7 | mA |
| V_T | on-state voltage | $I_T = 1.4\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10 | - | 1.3 | 1.6 | V |
| V_{GT} | gate trigger voltage | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11 | - | - | 1 | V |
| | | $V_D = 600\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ °C}$; Fig. 11 | 0.2 | - | - | V |
| I_D | off-state current | $V_D = 600\text{ V}$; $T_j = 125\text{ °C}$ | - | - | 0.5 | mA |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 402\text{ V}$; $T_j = 110\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; Fig. 12 | 10 | - | - | V/ μ s |
| dV_{com}/dt | rate of change of commutating voltage | $V_D = 400\text{ V}$; $T_j = 110\text{ °C}$; $dI_{com}/dt = 0.44\text{ A/ms}$; $I_T = 1\text{ A}$; gate open circuit | 0.5 | - | - | V/ μ s |

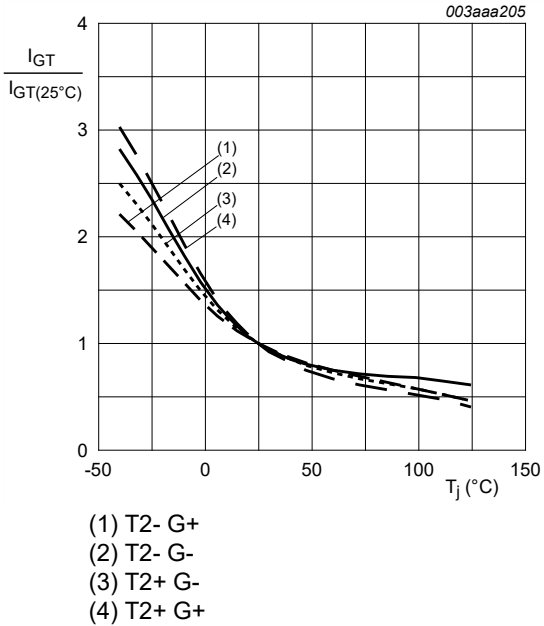


Fig. 7. Normalized gate trigger current as a function of junction temperature

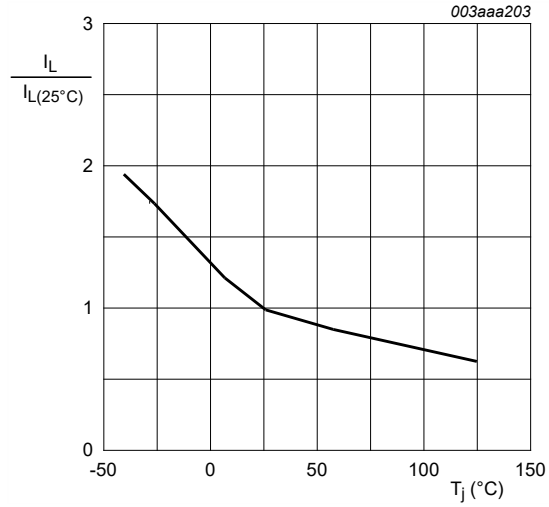


Fig. 8. Normalized latching current as a function of junction temperature

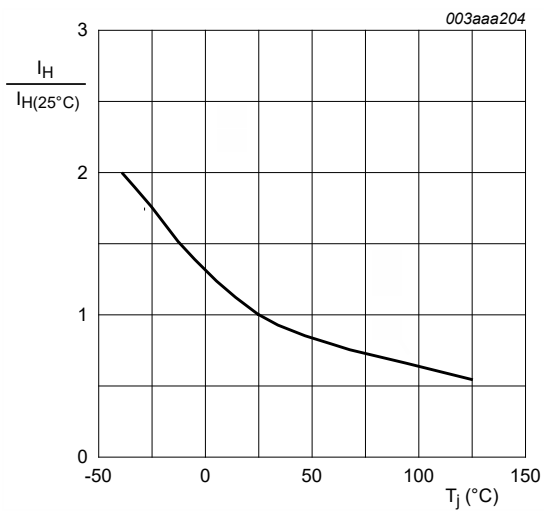
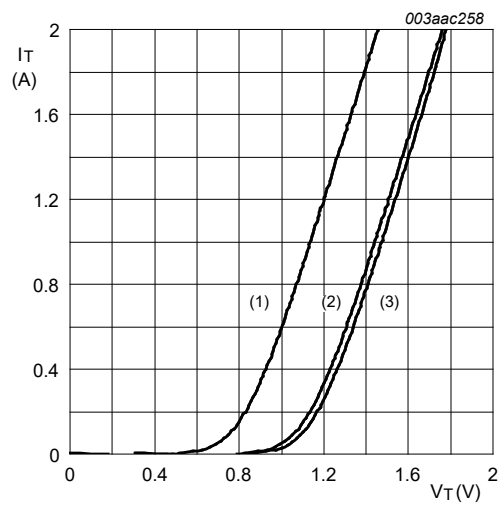


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 1.13 \text{ V}$
 $R_s = 0.31 \text{ } \Omega$
 (1) $T_j = 125 \text{ } ^\circ\text{C}$; typical values
 (2) $T_j = 125 \text{ } ^\circ\text{C}$; maximum values
 (3) $T_j = 25 \text{ } ^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

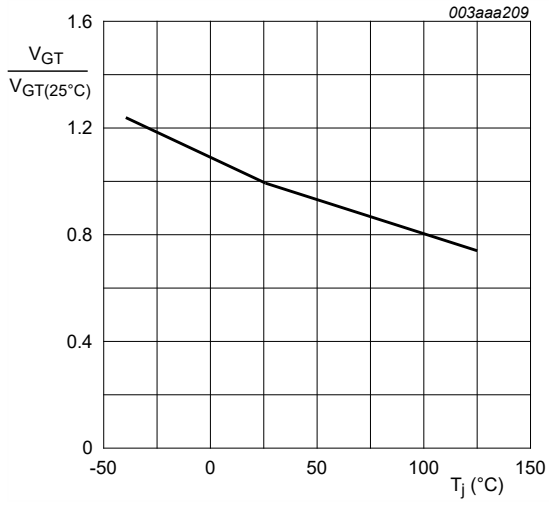
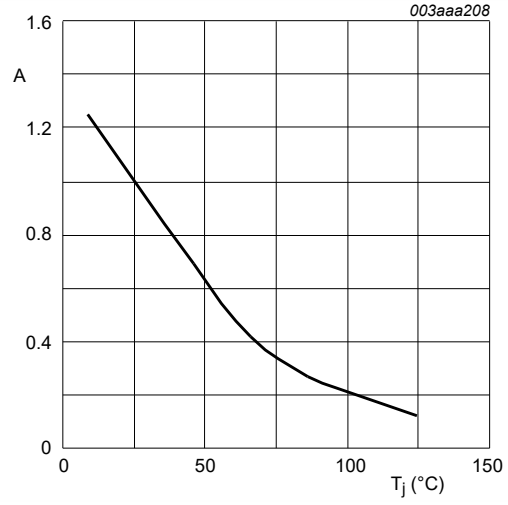


Fig. 11. Normalized gate trigger voltage as a function of junction temperature



$$A = \frac{dV_D(T_j \text{ } ^\circ\text{C}) / dt}{dV_D(25 \text{ } ^\circ\text{C}) / dt}$$

Fig. 12. Normalized critical rate of rise of off-state voltage as a function of junction temperature; typical values

10. Package outline

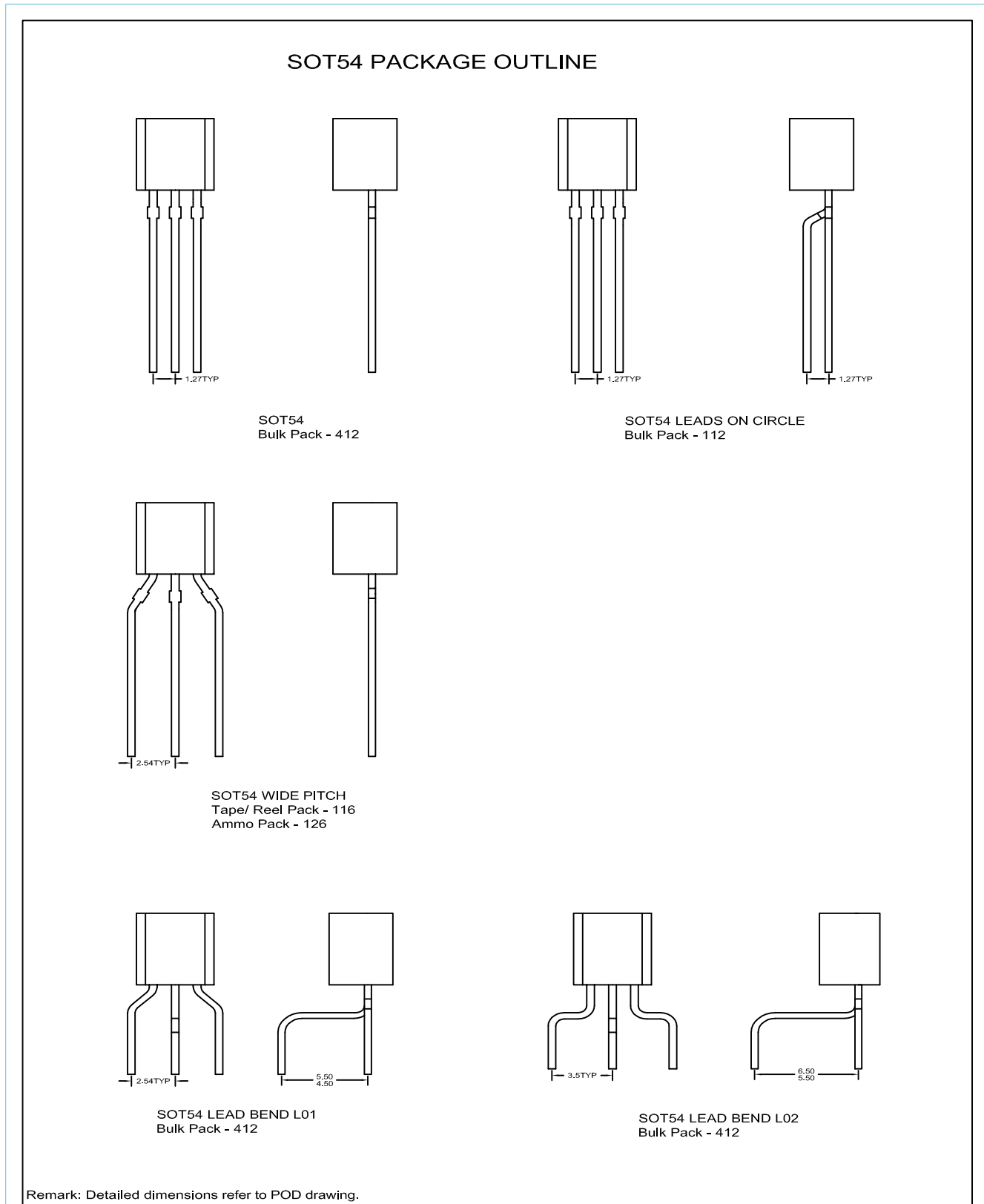


Fig. 13. Package outline TO-92 (SOT54)

11. Legal information

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|--------------------------------|--------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
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- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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For more information, please visit: <http://www.ween-semi.com>
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Date of release: 29 September 2016
