# PM4351

# COMET

# COMBINED E1/T1 TRANSCEIVER/FRAMER

# DATA SHEET

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# 1 FEATURES

- Monolithic device which integrates software selectable full-featured T1 and E1 framers and T1 and E1 short haul and long haul line interfaces.
- Meets or exceeds T1 and E1 shorthaul and longhaul network access specifications including ANSI T1.102, T1.403, T1.408, AT&T TR 62411, ITU-T G.703, G.704 as well as ETSI 300-011, CTR-4, CTR-12 and CTR-13.
- Provides encoding and decoding of B8ZS, HDB3 and AMI line codes.
- Provides receive equalization, clock recovery and line performance monitoring.
- Provides transmit jitter attenuation and digitally programmable long haul and short haul line build out.
- Provides on-board programmable binary sequence generators and detectors for error testing including support for patterns recommended in ITU-T O.151.
- Provides three full-featured HDLC controllers, each with 128-byte transmit and receive FIFO buffers.
- Automatically generates and transmits DS-1 performance report messages to ANSI T1.231 and ANSI T1.408 specifications.
- Compatible with Mitel ST®-bus, AT&T CHI® and MVIP PCM backplanes, supporting rates of 1.544 Mbit/s, 2.048 Mbit/s, 4.096 Mbit/s, and 8.192 Mbit/s. Up to four COMET devices may be byte-interleaved on a single backplane with no external circuitry.
- Supports NxDS0 fractional bandwidth backplane.
- Provides an 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Uses line rate system clock.
- Provides a IEEE P1149.1 (JTAG) compliant test access port (TAP) and controller for boundary scan test.
- Implemented in a low power 5 V tolerant +3.3 V CMOS technology.

- Available in a high density 80-pin MQFP (14 mm by 14 mm) package or an 81-ball CABGA (9 mm by 9 mm) package.

- Provides a -40°C to +85°C Industrial temperature operating range.

## 1.1 Receiver section:

- Guaranteed T1 signal reception for distances with up to 36 dB of cable attenuation under production test conditions (772 kHz, VDD = 3.069V and 25°C) using PIC 22 gauge cable emulation.

- Guaranteed E1 signal reception for distances with up to 36 dB of cable attenuation under production test conditions (1.024 MHz, VDD = 3.069V and 25°C) using PIC 22 gauge cable emulation.

- Recovers clock and data using a digital phase locked loop for high jitter tolerance.

- Provides an alternative digital interface for applications without line interface units.

- Frames to ITU-T G.704 basic and CRC-4 multiframe formatted E1 signals. The framing procedures are consistent ITU-T G.706 specifications.

- Frames to DSX/DS-1 signals in D4, SF, ESF and SLC®96 formats.

- Frames to TTC JT-G704 multiframe formatted J1 signals. Supports the alternate CRC-6 calculation for Japanese applications.

- Frames in the presence of and detects the “Japanese Yellow” alarm.

- Tolerates more than 0.3 UI peak-to-peak, high frequency jitter as required by AT&T TR 62411 and Bellcore TR-TSY-000170.

- Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192-bit window.

- Provides loss of signal detection as per ITU-T G.775 and ANSI T1.231. Red, Yellow, and AIS alarm detection and integration are according to ANSI T1.231 specifications.

- Provides programmable in-band loopback activate and deactivate code detection.

- Supports line and path performance monitoring according to AT&T and ANSI specifications. Accumulators are provided for counting ESF CRC-6 errors, framing bit errors, line code violations and loss of frame or change of frame alignment events.

- Provides ESF bit-oriented code detection and an HDLC/LAPD interface for terminating the ESF facility data link.

- Supports polled or interrupt-driven servicing of the HDLC interface.

- Extracts the data link in ESF and T1DM (DDS) modes. Optionally extracts a datalink in the E1 national use bits.

- Extracts 4-bit codewords from the E1 national use bits as specified in ETS 300 233

- Extracts up to three HDLC links from arbitrary time slots to support the D-channel for ISDN Primary Rate Interfaces and the C-channels for V5.1/V5.2 interfaces.

- Detects the V5.2 link identification signal.

- Provides a two-frame elastic store buffer for backplane rate adaptation that performs controlled slips and indicates slip occurrence and direction.

- Provides DS-1 robbed bit signaling extraction, with optional data inversion, programmable idle code substitution, digital milliwatt code substitution, bit fixing, and two superframes of signaling debounce on a per-channel basis.

- Frames to the E1 signaling multiframe alignment when enabled and extracts channel associated signaling. Alternatively, a common channel signaling data link may be extracted from timeslot 16.

- Can be programmed to generate an interrupt on change of signaling state.

- Provides trunk conditioning which forces programmable trouble code substitution and signaling conditioning on all channels or on selected channels.

- Provides diagnostic, line loopbacks and per-DS0 line loopback.

- Provides an integral pattern detector that may be programmed to detect common pseudo-random sequences. The programmed sequence may be detected in the entire frame, or on an NxDS0 basis.

- Provides an integral pattern generator that may be programmed to generate common pseudo-random or repetitive sequences towards the backplane.

- Provides tristateable single-rail PCM and signaling data outputs for 1.544 Mbit/s, 2.048 Mbit/s, 4.096 Mbit/s or 8.192 Mbit/s backplane buses.

## 1.2 Transmitter section:

- Supports transfer of transmitted single rail PCM and signaling data from 1.544 Mbit/s, 2.048 Mbit/s, 4.096 Mbit/s or 8.192 Mbit/s backplane buses.

- Generates DSX-1 shorthaul and DS-1 longhaul pulses with programmable pulse shape compatible with AT&T, ANSI and ITU requirements.

- Generates E1 pulses compliant to G.703 recommendations.

- Provides a digitally programmable pulse shape extending up to 5 transmitted bit periods for custom long haul pulse shaping applications.

- Provides line outputs which are current limited and may be tristated for protection or in redundant applications.

- Provides an alternative digital interface for external line interface units.

- Provides a digital phase locked loop for generation of a low jitter transmit clock complying with all jitter attenuation, jitter transfer and residual jitter specifications of AT&T TR 62411 and ETSI TBR 12 and TBR 13.

- Provides a FIFO buffer for jitter attenuation and rate conversion in the transmit path.

- Provides a two-frame payload slip buffer to allow independent backplane and line timing.

- Provides an integral pattern generator that may be programmed to generate common pseudo-random or repetitive sequences. The programmed sequence may be inserted in the entire frame, or on an NxDS0 basis.

- Provides an integral pattern detector that may be programmed to detect common pseudo-random or repetitive sequences from the backplane.

- Transmits G.704 basic and CRC-4 multiframe formatted E1 signals or D4, SF or ESF formatted DSX/DS-1 signals.

- Transmits TTC JT-G704 multiframe formatted J1 signals. Supports the alternate ESF CRC-6 calculation for Japanese applications.
- Transmits the “Japanese Yellow” alarm.
- Supports unframed mode and framing bit, CRC, or data link by-pass.
- Provides signaling insertion, programmable idle code substitution, digital milliwatt code substitution, and data inversion on a per channel basis.
- Provides trunk conditioning which forces programmable trouble code substitution and signaling conditioning on all channels or on selected channels.
- Provides minimum ones density through Bell (bit 7), GTE or DDS zero code suppression on a per channel basis.
- Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192-bit window and optionally stuffs ones to maintain minimum ones density.
- Allows insertion of framed or unframed in-band loopback code sequences.
- Allows insertion of a data link in ESF or T1DM (DDS) DS-1 modes. Optionally inserts a datalink in the E1 national use bits.
- Supports 4-bit codeword insertion in the E1 national use bits as specified in ETS 300 233
- Inserts up to three HDLC links into arbitrary time slots to support the D-channel for ISDN Primary Rate Interfaces and the C-channels for V5.1/V5.2 interfaces.
- Supports transmission of the alarm indication signal (AIS) and the Yellow alarm signal. Supports “Japanese Yellow” alarm generation.
- Provides ESF bit-oriented code generation.

# 2 APPLICATIONS

- T1/E1 Wireless Digital Loop Carriers (DLC's) and Cellular Base Stations
- T1/E1 Internet Access Equipment
- T1/E1 Channel Service Units (CSU)
- T1/E1 Frame Relay Interfaces
- T1/E1 ATM Interfaces
- T1/E1 Multiplexers (CPE MUX)
- Digital Private Branch Exchanges (PBX)
- Digital Access Cross-Connect Systems (DACS) and Electronic DSX Cross-Connect Systems (EDSX)
- ISDN Primary Rate Interfaces (PRI)
- Test Equipment

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2. ANSI - T1.102-1993 - American National Standard for Telecommunications - Digital Hierarchy - Electrical Interfaces.

3. ANSI - T1.107-1995 - American National Standard for Telecommunications - Digital Hierarchy - Formats Specification.

4. ANSI - T1.231-1993 - American National Standard for Telecommunications - Layer 1 In-Service Digital Transmission Performance Monitoring

5. ANSI - T1.403-1995 - American National Standard for Telecommunications - Carrier to Customer Installation - DS-1 Metallic Interface Specification.

6. ANSI - T1.408-1990 - American National Standard for Telecommunications - Integrated Services Digital Network (ISDN) Primary Rate - Customer Installation Metallic Interfaces Layer 1 Specification.

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8. AT&T - PUB 54016 - Requirements For Interfacing Digital Terminal Equipment To Services Employing The Extended Superframe Format, October 1984.

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10. AT&T - TR 62411 - Accunet T1.5 - Service Description and Interface Specification, Addendum 1, March 1991.

11. AT&T - TR 62411 - Accunet T1.5 - Service Description and Interface Specification, Addendum 2, October 1992.

12. AT&T - Interface Specification - Concentration Highway Interface - November 1990.

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17. ETSI - ETS 300 011 A2 – Integrated Services Digital Network (ISDN); Primary Rate User-Network Interface Layer 1 Specification and Test Principles, March 1996.

18. ETSI - ETS 300 166 – Transmission and Multiplexing (TM); Physical and Electrical Characteristics of Hierarchical Digital Interfaces for Equipment Using the 2 048 kbit/s - based Plesiochronous or Synchronous Digital Hierarchies, August 1993.

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20. ETSI - ETS 300 324-1 - Signaling Protocols and Switching (SPS); V interfaces at the Digital Local Exchange (LE) V5.1 Interface for the Support of Access Network (AN) Part 1: V5.1 Interface Specification, February 1994.

21. ETSI - ETS 300 347-1 - Signaling Protocols and Switching (SPS); V Interfaces at the Digital Local Exchange (LE) V5.2 Interface for the Support of Access Network (AN) Part 1: V5.2 Interface Specification, September 1994.

22. ETSI - CTR 4 - Integrated Services Digital Network (ISDN); Attachment requirements for terminal equipment to connect to an ISDN using ISDN primary rate access, November 1995.

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25. FCC Rules - Part 68.308 - Signal Power Limitations

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27. ITU-T - Recommendation G.704 - Synchronous Frame Structures Used at Primary Hierarchical Levels, July 1995.

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29. ITU-T - Recommendation G.732 – Characteristics of Primary PCM Multiplex Equipment Operating at 2048 kbit/s, 1993.

30. ITU-T - Recommendation G.711 – Pulse Code Modulation (PCM) of Voice Frequencies, 1993.

31. ITU-T - Recommendation G.775 - Loss of Signal (LOS), November 1994.

32. ITU-T Recommendation G.802, - Interworking Between Networks Based on Different Digital Hierarchies and Speech Encoding Laws, 1993.

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43. TTC Standard JT-I431 - ISDN Primary Rate User-Network Interface Layer 1 - Specification, 1995.

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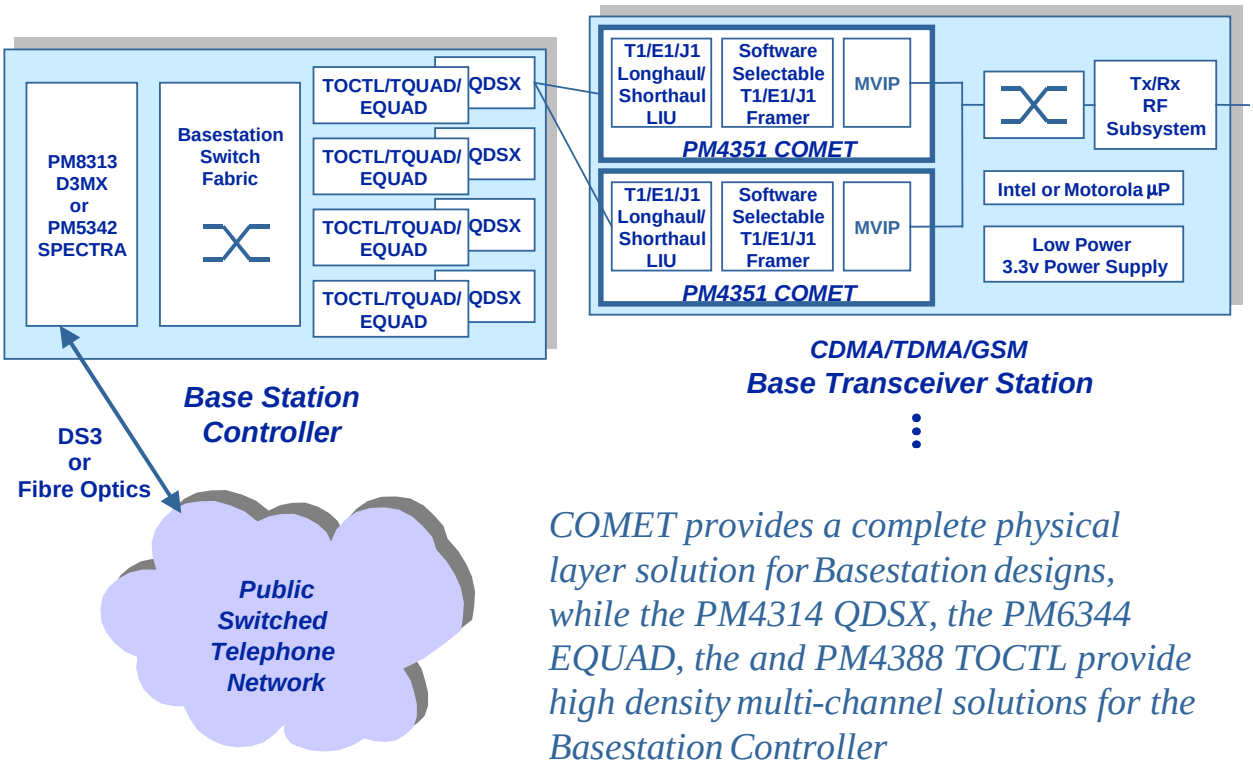
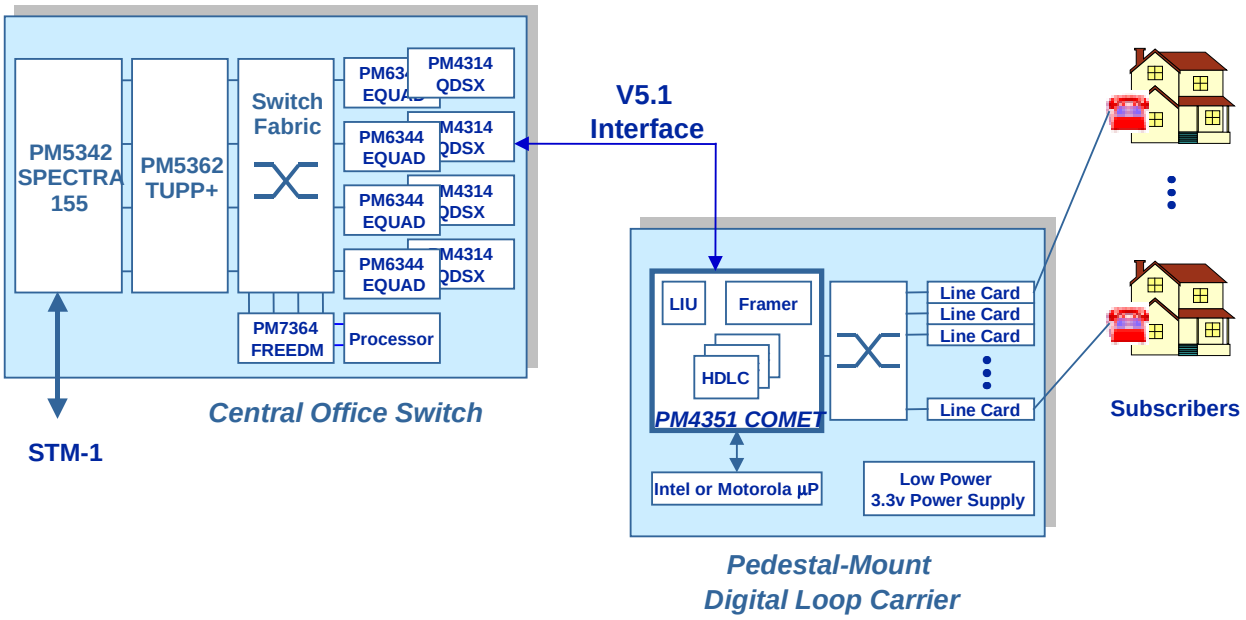
# 4 APPLICATION EXAMPLE

**Figure 1 - Wireless Base Station Application**



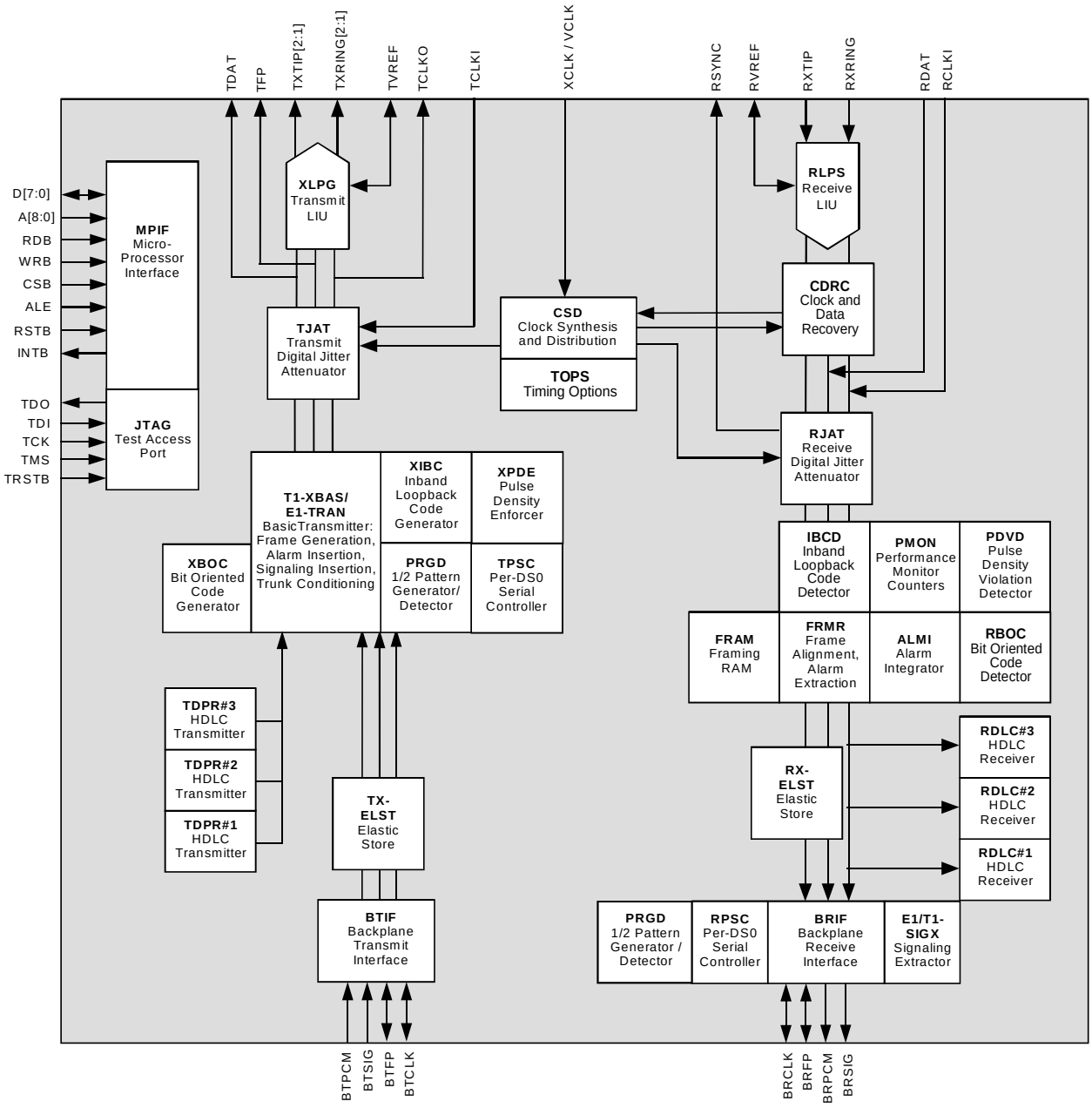

*COMET provides a complete physical layer solution for Basestation designs, while the PM4314 QDSX, the PM6344 EQUAD, the and PM4388 TOCTL provide high density multi-channel solutions for the Basestation Controller*

**Figure 2 - V5.1 Interface Application**




COMET used in conjunction with PM6344 EQUAD and PM7366 FREEDM-8 to provide a complete V5.1 solution for both the Access Network and the Central Office

# 5 BLOCK DIAGRAM



# 6 DESCRIPTION

The PM4351 Combined E1/T1 Transceiver (COMET) is a feature-rich monolithic integrated circuit suitable for use in long haul and short haul T1 and E1 systems with a minimum of external circuitry. The COMET is software configurable, allowing feature selection without changes to external wiring.

Analog circuitry is provided to allow direct reception of long haul E1 and T1 compatible signals with up to 36 dB cable loss (at 1.024 MHz in E1 mode) or up to 36 dB cable loss (at 772 kHz in T1 mode) using a minimum of external components. Typically, only line protection, a transformer and a line termination resistor are required. Digital line inputs are provided for applications not requiring a physical T1 or E1 interface.

The COMET recovers clock and data from the line and frames to incoming data. In T1 mode, it can frame to several DS-1 signal formats: SF, ESF, T1DM (DDS) and SLC®96. In E1 mode, the COMET frames to basic G.704 E1 signals and CRC-4 multiframe alignment signals, and automatically performs the G.706 interworking procedure. AMI, HDB3 and B8ZS line codes are supported.

The COMET supports detection of various alarm conditions such as loss of signal, pulse density violation, Red alarm, Yellow alarm, and AIS alarm in T1 mode and loss of signal, loss of frame, loss of signaling multiframe and loss of CRC multiframe in E1 mode. The COMET also supports reception of remote alarm signal, remote multiframe alarm signal, alarm indication signal, and time slot 16 alarm indication signal in E1 mode. The presence of Yellow and AIS patterns in T1 mode and remote alarm and AIS patterns in E1 mode is detected and indicated. In T1 mode, the COMET integrates Yellow, Red, and AIS alarms as per industry specifications. In E1 mode, the COMET integrates Red and AIS alarms.

Performance monitoring with accumulation of CRC-6 errors, framing bit errors, line code violations, and loss of frame events is provided in T1 mode. In E1 mode, CRC-4 errors, far end block errors, framing bit errors, and line code violation are monitored and accumulated.

The COMET provides three receive HDLC controllers for the detection and termination of messages on the ESF facility data link (T1) or national use bits (E1) and in any arbitrary time slot (T1 or E1). In T1 mode, the COMET also detects the presence of in-band loop back codes and ESF bit oriented codes. Detection and optional debouncing of the 4-bit Sa-bit codewords defined in ITU-T G.704 and ETSI 300-233 is supported. An interrupt may be generated on any change of state of the Sa codewords.

Dual (transmit and receive) elastic stores for slip buffering and rate adaptation to backplane timing are provided, as is a signaling extractor that supports signaling debounce, signaling freezing, idle code substitution, digital milliwatt tone substitution, data inversion, and signaling bit fixing on a per-channel basis. Receive side data and signaling trunk conditioning is also provided.

In T1 mode, the COMET generates framing for SF, ESF and T1DM (DDS) formats. In E1 mode, the COMET generates framing for a basic G.704 E1 signal. The signaling multiframe alignment structure and the CRC multiframe structure may be optionally inserted. Framing can be optionally disabled.

Internal analog circuitry allows direct transmission of long haul and short haul T1 and E1 compatible signals using a minimum of external components. Typically, only line protection, a transformer and an optional line termination resistor are required. Digitally programmable pulse shaping allows transmission of DSX-1 compatible signals up to 655 feet from the cross-connect, E1 short haul pulses into 120 ohm twisted pair or 75 ohm coaxial cable, E1 long haul pulses into 120 ohm twisted pair as well as long haul DS-1 pulses into 100 ohm twisted pair with integrated support for LBO filtering as required by the FCC rules. In addition, the programmable pulse shape extending over 5-bit periods allows customization of short haul and long haul line interface circuits to application requirements. Digital line inputs and outputs are provided for applications not requiring a physical T1 or E1 interface.

In the transmit path, the COMET supports signaling insertion, idle code substitution, digital milliwatt tone substitution, data inversion, and zero code suppression on a per-channel basis. Zero code suppression may be configured to Bell (bit 7), GTE, or DDS standards, and can also be disabled. Transmit side data and signaling trunk conditioning is also provided. Signaling bit transparency from the backplane may be enabled.

The COMET provides three transmit HDLC controllers. These controllers may be used for the transmission of messages on the ESF data link (T1) or national use bits (E1) and in any time slot. In T1 mode, the COMET can be configured to generate in-band loop back codes and ESF bit oriented codes. In E1 mode, transmission of the 4-bit Sa codewords defined in ITU-T G.704 and ETSI 300-233 is supported.

The COMET provides optional jitter attenuation in both the transmit and receive directions.

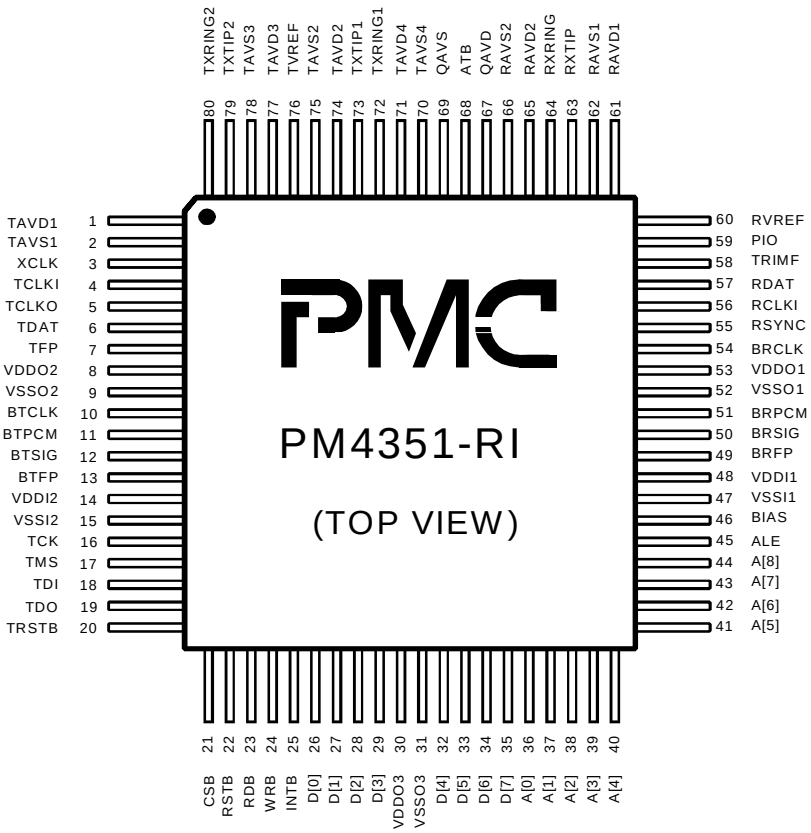
The COMET provides both a parallel microprocessor interface for controlling the operation of the device and serial PCM interfaces that allow backplane rates from 1.544 Mbit/s to 8.192 Mbit/s to be directly supported. Up to four COMET devices can be multiplexed on a byte-interleaved basis on a common bus with

no additional arbitration logic. The COMET supports the Mitel ST® bus, AT&T CHI® and MVIP standards.

# 7 PIN DIAGRAMS

The COMET is packaged in an 80-pin metric plastic quad flat pack (MQFP) package having a body size of 14 mm by 14 mm and a pin pitch of 0.65 mm.

**Figure 3 PM4351-RI COMET Pin Diagram**



The COMET is also available in an 81 pin Chip Array Ball Grid Array (CABGA) package having a body size of 9 mm by 9 mm and a pin pitch of 0.8 mm.

## Figure 4 PM4351-NI COMET Pin Diagram

(Bottom View)

| | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
|---|---|---|---|---|---|---|---|---|---|---|
| A | RAVD1 | RXRING | RAVD2 | QAVD | TAVD4 | TVREF | TAVS2 | TXTIP2 | TAVD1 | A |
| B | PIO | RAVS1 | RAVS2 | ATB | TAVD3 | TAVD2 | TAVS3 | TAVS1 | TCLKI | B |
| C | RSYNC | TRIMF | RXTIP | TAVS4 | TXRING 1 | TXRING 2 | XCLK/ VCLK | TDAT | TCLKO | C |
| D | RCLKI | BRCLK | RVREF | QAVS | TXTIP1 | VSSO1 | BTCLK | VDDO1 | TFP | D |
| E | BRPCM | RDAT | VSSO2 | VDDO2 | NC | BTFP | BTSIG | TMS | BTPCM | E |
| F | VSSI2 | VDDI2 | BRSIG | BRFP | D[5] | D[3] | TRSTB | VDDI1 | TCK | F |
| G | ALE | BIAS | A[7] | A[4] | D[4] | VDDO3 | RDB | TDI | VSSI1 | G |
| H | A[8] | A[6] | A[2] | D[6] | A[1] | D[2] | D[0] | RSTB | TDO | H |
| J | A[5] | A[3] | D[7] | A[0] | VSSO3 | D[1] | INTB | WRB | CSB | J |
| | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |

# 8 PIN DESCRIPTION

## Table 1 - Backplane Transmit Interface (4 pins)

| Pin Name | Type | Pin No. | | Function |
|---|---|---|---|---|
| | | -RI | -NI | |
| BTCLK | I/O | 10 | D3 | Backplane Transmit Clock (BTCLK). In synchronous backplane applications, the BTCLK input may be a 1.544 MHz, 2.048 MHz, 3.088 MHz, 4.096 MHz, 8.192 MHz or 16.384 MHz clock with optional gapping for adaptation from non-uniform system clocks.<br><br>BTCLK can be configured as a line-rate output, in which case it is referenced to TCLKI or the receive recovered clock (loop timed). In T1 NxDS0 mode, BTCLK is gapped during the framing bit position and optionally for between 1 and 23 DS0 channels in the backplane data stream. In E1 NxDS0 mode, BTCLK is gapped optionally for between 1 and 31 time slots in the backplane data stream.<br><br>When BTCLK is configured as an input, byte-interleaved backplanes are supported.<br><br>BTCLK may be configured to be active on either its rising or falling edge. BTPCM and BTSIG are sampled on the active edge of BTCLK. Depending on its configuration, BTFP is either sampled or updated on the selected active edge of BTCLK.<br><br>After a reset, BTCLK is configured as an input. |

| Pin Name | Type | Pin No. | | Function |
|---|---|---|---|---|
| | | -RI | -NI | |
| BTFP | I/O | 13 | E4 | Backplane Transmit Frame Pulse (BTFP). When BTFP is configured as an input, it is used to frame align the transmitter to the system backplane.<br>T1 mode:<br>If only frame alignment is required, a pulse at least one BTCLK cycle wide must be provided on BTFP at multiples of 193 bit periods. If superframe alignment is required, transmit superframe alignment must be enabled, and BTFP must be brought high for at least one BTCLK cycle to mark bit 1 of frame 1 of every 12-frame or 24-frame superframe.<br>E1 mode:<br>If basic frame alignment only is required, a pulse at least one BTCLK cycle wide must be provided on BTFP at multiples of 256 bit periods. If multiframe alignment is required, transmit multiframe alignment must be enabled, and BTFP must be brought high to mark bit 1 of frame 1 of every 16-frame signaling multiframe and brought low following bit 1 of frame 1 of every 16-frame CRC multiframe. This mode allows both multiframe alignments to be independently controlled using the single BTFP signal. Note that if the signaling and CRC multiframe alignments are coincident, BTFP must pulse high for one BTCLK cycle every 16 frames.<br>When BTFP is configured as an output (only valid when the transmit backplane clock rate is no greater than 2.048 MHz), transmit frame alignment is derived internally and BTFP is updated on the configured active edge of BTCLK. BTFP pulses high for one cycle to indicate the first bit of each frame or multiframe, as optioned.<br>After a reset, BTFP is configured as an input. |
| BTPCM | Input | 11 | E1 | Backplane Transmit PCM Data (BTPCM). The non-return to zero, digital data stream to be transmitted is input on this pin. BTPCM may present a 1.544 Mbit/s, 2.048 Mbit/s or sub-rate NxDS0 data stream or may present a byte-interleaved 4.096 Mbit/s or 8.192 Mbit/s multiplexed data stream.<br>The bit alignment of BTPCM relative to BTFP is configurable. Two mappings of a DS-1 into a 2.048 Mbit/s format are defined: every fourth timeslot unused and 24 contiguous timeslots.<br>The BTPCM signal is sampled on the configured active edge of BTCLK. |
| BTSIG | Input | 12 | E3 | Backplane Transmit Signaling (BTSIG). The BTSIG input signal contains the signaling bits for each channel in the transmit data frame, repeated for the entire superframe. Each channel's signaling bits are in bit locations 5, 6, 7 and 8 of the channel and are channel-aligned with the BTPCM data stream.<br>The BTSIG signal is sampled on the configured active edge of BTCLK. |

## Table 2 - Backplane Receive Interface (4 pins)

| Pin Name | Type | Pin No. | | Function |
|---|---|---|---|---|
| | | -RI | -NI | |
| BRCLK | I/O | 54 | D8 | Backplane Receive Clock (BRCLK). When BRCLK is configured as an input and the elastic store is enabled, BRCLK may be either a 1.544 MHz, 2.048 MHz, 3.088 MHz, 4.096 MHz, 8.192 MHz or 16.384 MHz clock with optional gapping for adaptation to non-uniform backplane data streams.<br><br>When BRCLK is configured as a output, it can be either a 1.544 MHz or 2.048 MHz clock derived from the recovered line rate timing (available on RSYNC), with optional jitter attenuation. In T1 NxDS0 mode, BRCLK is gapped during the framing bit position and optionally for between 1 and 23 DS0 channels in the backplane data stream. In E1 NxDS0 mode, BRCLK is gapped optionally for between 1 and 31 time slots in the backplane data stream.<br><br>Either the rising or falling edge of BRCLK may be configured as the active edge. BRPCM and BRSIG are updated on the active edge of BRCLK. When BRFP is configured as an input, it is sampled on the active edge of BRCLK. When BRFP is configured as an output, it is updated on the active edge of BRCLK.<br><br>After a reset, BRCLK is configured as an input. |

| Pin Name | Type | Pin No. | | Function |
|---|---|---|---|---|
| | | -RI | -NI | |
| BRFP | I/O | 49 | F6 | Backplane Receive Frame Pulse (BRFP). When BRFP is configured as an output, it indicates the frame alignment of BRPCM and BRSIG. BRFP is generated on the active edge of BRCLK.<br>T1 mode:<br>If basic frame alignment is desired, BRFP pulses high for one BRCLK cycle during bit 1 of each 193-bit frame. Optionally, BRFP may pulse high every second frame to ease the identification of data link bits. If superframe alignment is desired, BRFP pulses high for one BRCLK cycle during bit 1 of frame 1 of every 12-frame or 24-frame superframe. Optionally, BRFP may pulse high every second superframe to ease the conversion between SF and ESF.<br>E1 mode:<br>If basic frame alignment is desired, BRFP pulses high for one BRCLK cycle during bit 1 of each 256-bit frame. Optionally, BRFP may pulse high every second frame to ease the identification of NFAS frames. If multiframe alignment is desired, BRFP transitions high to mark bit 1 of frame 1 of every 16-frame signaling multiframe and transitions low following bit 1 of frame 1 of every 16-frame CRC multiframe. Note that if the signaling and CRC multiframe alignments are coincident, BRFP pulses high for one BRCLK cycle every 16 frames.<br>When BRFP is configured as an input, it is used to frame align the receive data to the backplane frame alignment. When frame alignment is required, a pulse at least one BRCLK cycle wide must be provided on BRFP a maximum of once every frame (193 bit periods in T1 mode or 256 bit periods in E1 mode). BRFP is sampled on the active edge of BRCLK.<br>After a reset, BRFP is configured as an input. |
| BRPCM | Output with Tristate | 51 | E9 | Backplane Receive PCM Data (BRPCM). BRPCM contains the recovered data stream passed through the elastic store, signaling extractor and per-DS0 serial controller. When the receive elastic store is not bypassed, the BRPCM stream is aligned to the backplane input timing. When BRCLK is either 4.096 MHz, 8.192 MHz or 16.384 MHz, BRPCM can be tristated and is only active during programmable timeslots. This allows byte interleaving of PCM data streams from up to 4 COMET devices with no external logic.<br>After a reset, BRPCM is high impedance.<br>BRPCM is updated on the active edge of BRCLK. |

| Pin Name | Type | Pin No. | | Function |
|---|---|---|---|---|
| | | -RI | -NI | |
| BRSIG | Output with Tristate | 50 | F7 | Backplane Receive Signaling (BRSIG). BRSIG contains the extracted signaling bits for each channel in the frame, repeated for the entire superframe. Each channel's signaling bits are valid in bit locations 5, 6, 7 and 8 of the channel and are channel-aligned with the BRPCM data stream. When the RX-ELST is not by-passed, the BRSIG stream is aligned to the backplane input timing. When BRCLK is either 4.096 MHz, 8.192 MHz or 16.384 MHz, BRSIG can be tristated and is only active during programmable timeslots to allow byte interleaving of signaling data streams from up to 4 COMET devices with no external logic.<br>After a reset, BRSIG is high impedance.<br>BRSIG is updated on the active edge of BRCLK. |

## Table 3 - Transmit Line Interface (6 pins)

| Pin Name | Type | Pin No. | | Function |
|---|---|---|---|---|
| | | -RI | -NI | |
| TXTIP1<br>TXTIP2 | Analog Output | 73<br>79 | D5<br>A2 | Transmit Analog Positive Pulse (TXTIP1 and TXTIP2). When the transmit analog line interface is enabled, the TXTIP1 and TXTIP2 analog outputs drive the transmit line pulse signal through an external matching transformer. Both TXTIP1 and TXTIP2 are normally connected to the positive lead of the transformer primary. Two outputs are provided for better signal integrity and should be shorted together on the board.<br>After a reset, TXTIP1 and TXTIP2 are high impedance. The HIGHZ bit of the XLPG Line Driver Configuration register (address 0F0H) must be programmed to logic 0 to remove the high impedance state. |
| TXRING1<br>TXRING2 | Analog Output | 72<br>80 | C5<br>C4 | Transmit Analog Negative Pulse (TXRING1 and TXRING2). When the transmit analog line interface is enabled, the TXRING1 and TXRING2 analog outputs drive the transmit line pulse signal through an external matching transformer. Both TXRING1 and TXRING2 are normally connected to the negative lead of the transformer primary. Two outputs are provided for better signal integrity and should be shorted together on the board.<br>After a reset, TXRING1 and TXRING2 are high impedance. The HIGHZ bit of the XLPG Line Driver Configuration register (address 0F0H) must be programmed to logic 0 to remove the high impedance state. |
| TDAT | Digital Output | 6 | C2 | Transmit Digital PCM Data (TDAT). When the transmit digital line interface is enabled, the TDAT output provides the line side NRZ PCM transmit data. This mode may be used in applications not requiring a physical T1/E1 interface (e.g. interfacing to HDSL transceivers). TDAT is updated on the either the rising or falling (default) edge of TCLKO. |

| Pin Name | Type | Pin No. | | Function |
|---|---|---|---|---|
| | | -RI | -NI | |
| TFP | Digital Output | 7 | D1 | Transmit Digital Frame Pulse (TFP). When the transmit digital line interface is enabled, the TFP output indicates frame alignment of the line side transmitted PCM stream (TDAT). This mode may be used in applications not requiring a physical T1/E1 interface (e.g. interfacing to HDSL transceivers). TFP is updated on the either the rising or falling (default) edge of TCLKO. |

## Table 4 - Receive Line Interface (4 pins)

| Pin Name | Type | Pin No. | | Function |
|---|---|---|---|---|
| | | -RI | -NI | |
| RXTIP | Analog Input | 63 | C7 | Receive Analog Positive Pulse (RXTIP). When the analog receive line interface is enabled, RXTIP samples the received line pulse signal from an external isolation transformer. RXTIP is normally connected directly to the positive lead of the receive transformer secondary. |
| RXRING | Analog Input | 64 | A8 | Receive Analog Negative Pulse (RXRING). When the analog receive line interface is enabled, RXRING samples the received line pulse signal from an external isolation transformer. RXRING is normally connected directly to the negative lead of the receive transformer secondary. |
| RDAT | Input | 57 | E8 | Receive Digital Line Data (RDAT). When the digital receive interface is enabled, the RDAT input samples the line side recovered NRZ PCM data stream. This mode may be used in applications not requiring a physical T1/E1 interface (e.g. interfacing to HDSL transceivers). In digital mode, clock and data recovery is disabled. RDAT is sampled on the rising (default) or falling edge of RCLKI. |
| RCLKI | Input | 56 | D9 | Receive Digital Line Clock (RCLKI). When the digital receive line interface is enabled, the externally recovered line rate clock must be provided on RCLKI. This mode may be used in applications not requiring a physical T1/E1 interface (e.g. interfacing to HDSL transceivers). RCLKI samples the receive PCM stream (RDAT) on its rising (default) or falling edge. |

## Table 5 - Timing Options Control (5 pins)

| Pin Name | Type | Pin No. | | Function |
|---|---|---|---|---|
| | | -RI | -NI | |
| PIO | I/O | 59 | B9 | Programmable I/O. PIO is an input/output pin controlled by a COMET register bit. As an output, the PIO bit can, under software control, be used to configure external circuitry dependent upon the mode of the COMET device. As an input, the state of the PIO pin can be read via a register bit. |

| Pin Name | Type | Pin No. | | Function |
|---|---|---|---|---|
| | | -RI | -NI | |
| TCLKO | Output | 5 | C1 | Transmit Clock Output (TCLKO). TCLKO is a clock at the transmit line rate and may be used by external circuits as a transmit clock reference. When the digital transmit line interface is enabled, TDAT and TFP are updated on the either the rising or falling (default) edge of TCLKO. |
| RSYNC | Output | 55 | C9 | Recovered Clock Synchronization Signal (RSYNC). This output signal is the dejittered recovered receiver line rate clock (1.544 or 2.048 MHz) or, optionally, the recovered clock synchronously divided by 193 (T1 mode) or 256 (E1 mode) to create a 8 kHz timing reference signal. When 8 kHz, the RSYNC phase is independent of frame alignment and is not affected by framing events.<br>When the COMET is in a loss of signal state, RSYNC is derived from the XCLK input or, optionally, is held high. |
| TCLKI | Input | 4 | B1 | Transmit Clock Reference (TCLKI). TCLKI may be used as a reference for the transmit line rate generation. TCLKI may be any multiple of 8 kHz (N x 8 kHz, where 1≤N≤256) so long as TCLKI has minimal jitter when divided down to 8 kHz. When the TCLKI frequency differs from the transmit line rate, the transmit jitter attenuation block (TJAT) must be enabled to attenuate jitter on the transmit clock in accordance with AT&T TR-62411 and ETS 300 011. When the TCLKI frequency is the same as the transmit line rate, TCLKI is optionally jitter attenuated by the TJAT in accordance with AT&T TR-62411 and ETS 300 011. When TCLKI jitter attenuation is enabled, the TCLKI frequency should be programmed into the TJAT Jitter Attenuation Divider N1 Control register.<br>The COMET may be configured to ignore the TCLKI input and utilize BTCLK or the receive recovered clock instead. |
| XCLK /<br><br><br><br><br><br>VCLK | Input | 3 | C3 | Crystal Clock Input (XCLK). This signal provides a stable, global timing reference for the COMET internal circuitry via an internal clock synthesizer. XCLK is a nominally jitter-free 50% duty cycle clock at 1.544 MHz in T1 mode and 2.048 MHz in E1 mode.<br>In T1 mode, a 2.048 MHz clock may be used as a reference. When used in this way, however, the intrinsic jitter specifications to AT&T TR62411 may not be met.<br>Vector Clock (VCLK). The VCLK signal is used during COMET production test to verify internal functionality. |

## Table 6 - Analog Support Circuitry (4 pins)

| Pin Name | Type | Pin No. | | Function |
|---|---|---|---|---|
| | | -RI | -NI | |
| ATB | Analog I/O | 68 | B6 | Analog Test Bus (ATB). Reserved for COMET production test. This pin must be connected to an analog ground for normal operation. |

| Pin Name | Type | Pin No. | | Function |
|---|---|---|---|---|
| | | -RI | -NI | |
| TVREF | Analog I/O | 76 | A4 | Transmit Voltage Reference (TVREF). This pin is reserved for a precision analog voltage or current reference. |
| RVREF | Analog I/O | 60 | D7 | Receive Voltage Reference (RVREF). This pin is reserved for a precision analog voltage or current reference. This pin must be connected to an external RC network consisting of a 100 kohm resistor connected in parallel with a 10 nF capacitor to analog ground. |
| TRIMF | Input | 58 | C8 | Trim Fuse. This pin is reserved for production purposes. The TRIMF signal is used during COMET production test to control the trimming of fuses. This pin must be tied low for normal operation. |

## Table 7 - JTAG (IEEE 1149.1) Boundary Scan Test Interface (5 pins)

| Pin Name | Type | Pin No. | | Function |
|---|---|---|---|---|
| | | -RI | -NI | |
| TCK | Input | 16 | F1 | Test Clock (TCK). The test clock (TCK) signal provides timing for test operations that are carried out using the IEEE P1149.1 test access port. |
| TMS | Input | 17 | E2 | Test Mode Select (TMS). The test mode select (TMS) signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull-up resistor. |
| TDI | Input | 18 | G2 | Test Data Input (TDI). The test data input (TDI) signal carries test data into the COMET via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull-up resistor. |
| TDO | Output with Tristate | 19 | H1 | Test Data Output (TDO). The test data output (TDO) signal carries test data out of the COMET via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tristate output which is tristated except when scanning of data is in progress. |
| TRSTB | Input | 20 | F3 | Active Low Test Reset (TRSTB). The test reset (TRSTB) signal provides an asynchronous COMET test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull-up resistor.<br>The JTAG TAP controller must be initialized when the COMET is powered up. If the JTAG port is not used, TRSTB should be connected to the RSTB input. |

## Table 8 - Microprocessor Interface (23 pins)

| Pin Name | Type | Pin No. | | Function |
|---|---|---|---|---|
| | | -RI | -NI | |
| CSB | Input | 21 | J1 | Active Low Chip Select (CSB). CSB must be low to enable COMET register accesses. CSB must go high at least once after power up to clear internal test modes. If CSB is not used, it should be tied to an inverted version of RSTB, in which case, RDB and WRB determine register accesses. |

| Pin Name | Type | Pin No. | | Function |
|---|---|---|---|---|
| | | -RI | -NI | |
| RDB | Input | 23 | G3 | Active Low Read Enable (RDB). RDB is pulsed low to enable a COMET register read access. The COMET drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are both low. |
| WRB | Input | 24 | J2 | Active Low Write Strobe (WRB). WRB is pulsed low to enable a COMET register write access. The D[7:0] bus contents are clocked into the addressed normal mode register on the rising edge of WRB while CSB is low. |
| ALE | Input | 45 | G9 | Address Latch Enable (ALE). This signal latches the address bus contents, A[8:0], when low, allowing the COMET to be interfaced to a multiplexed address/data bus. When ALE is high, the address latches are transparent. |
| D[0] | I/O | 26 | H3 | Bi-directional Data Bus (D[7:0]). This bus is used during read and write accesses to internal COMET registers. |
| D[1] | | 27 | J4 | |
| D[2] | | 28 | H4 | |
| D[3] | | 29 | F4 | |
| D[4] | | 32 | G5 | |
| D[5] | | 33 | F5 | |
| D[6] | | 34 | H6 | |
| D[7] | | 35 | J7 | |
| A[0] | Input | 36 | J6 | Address bus (A[8:0]). This bus selects specific registers during COMET register accesses. |
| A[1] | | 37 | H5 | |
| A[2] | | 38 | H7 | |
| A[3] | | 39 | J8 | |
| A[4] | | 40 | G6 | |
| A[5] | | 41 | J9 | |
| A[6] | | 42 | H8 | |
| A[7] | | 43 | G7 | |
| A[8] | | 44 | H9 | |
| RSTB | Input | 22 | H2 | Active Low Reset (RSTB). When forced low, RSTB will asynchronously reset the COMET. RSTB is a Schmitt-trigger input with integral pull-up. When resetting the device, RSTB must be asserted for a minimum of 100 ns to ensure that the COMET is completely reset. |
| INTB | OD Output | 25 | J3 | Active Low Open-drain Interrupt (INTB). INTB drives low when an unmasked interrupt event is detected on any of the internal interrupt sources. Note that INTB will remain low until all active, unmasked interrupt sources are acknowledged at their source at which time, INTB will tristate. |

## Table 9 - Power and Ground (25 pins)

| Pin Name | Type | Pin No. | | Function |
|---|---|---|---|---|
| | | -RI | -NI | |
| VDDO1<br>VDDO2<br>VDDO3 | Power | 53<br>8<br>30 | D2<br>E6<br>G4 | Output Power Pins (VDDO[3:1]). The output power pins should be connected to a well-decoupled +3.3 V DC supply in common with VDDI. |
| VSSO1<br>VSSO2<br>VSSO3 | Ground | 52<br>9<br>31 | D4<br>E7<br>J5 | Output Ground Pins (VSSO[3:1]). The output ground pins should be connected to GND in common with VSSI. |
| VDDI1<br>VDDI2 | Power | 48<br>14 | F2<br>F8 | Internal Power Pins (VDDI[2:1]). The internal power pins should be connected to a well-decoupled +3.3 V DC supply in common with VDDO. |
| VSSI1<br>VSSI2 | Ground | 47<br>15 | G1<br>F9 | Internal Ground Pins (VSSI[2:1]). The internal ground pins should be connected to GND in common with VSSO. |
| BIAS | Input | 46 | G8 | +5 V Bias (BIAS). The BIAS input facilitates 5 V tolerance on the inputs. BIAS must be connected to a well-decoupled +5 V rail if 5 V tolerant inputs are required. If 5 V tolerant inputs are not required, BIAS must be connected to a well-decoupled 3.3 V DC supply together with the power pins VDDO[3:1] and VDDI[3:1]. |
| TAVD1 | Analog Power | 1 | A1 | Transmit Analog Power (TAVD1). TAVD1 provides power for the transmit LIU reference circuitry. TAVD1 should be connected to analog +3.3 V. |
| TAVD2<br>TAVD3 | Analog Power | 74<br>77 | B4<br>B5 | Transmit Analog Power (TAVD2, TAVD3). TAVD2 and TAVD3 supply power for the transmit LIU output drivers. TAVD2 and TAVD3 should be connected to analog +3.3 V. |
| TAVD4 | Analog Power | 71 | A5 | Transmit Analog Power (TAVD4). TAVD4 supplies power for the transmit clock synthesis unit. TAVD4 should be connected to analog +3.3 V. |
| TAVS1 | Analog Ground | 2 | B2 | Transmit Analog Ground (TAVS1). TAVS1 provides ground for the transmit LIU reference circuitry. TAVS1 should be connected to analog GND. |
| TAVS2<br>TAVS3 | Analog Ground | 75<br>78 | A3<br>B3 | Transmit Analog Ground (TAVS2A, TAVD2B). TAVS2A and TAVS2B supply ground for the transmit LIU output drivers. TAVS2A and TAVS2B should be connected to analog GND. |
| TAVS4 | Analog Ground | 70 | C6 | Transmit Analog Ground (TAVS4). TAVS supplies ground for the transmit clock synthesis unit. TAVS4 should be connected to analog GND. |
| RAVD1 | Analog Power | 61 | A9 | Receive Analog Power (RAVD1). RAVD1 supplies power for the receive LIU input equalizer. RAVD1 should be connected to analog +3.3 V. |
| RAVD2 | Analog Power | 65 | A7 | Receive Analog Power (RAVD2). RAVD2 supplies power for the receive LIU peak detect and slicer. RAVD2 should be connected to analog +3.3 V. |
| RAVS1 | Analog Ground | 62 | B8 | Receive Analog Ground (RAVS1). RAVS1 supplies power for the receive LIU input equalizer. RAVS1 should be connected to analog GND. |

| Pin Name | Type | Pin No. | | Function |
|---|---|---|---|---|
| | | -RI | -NI | |
| RAVS2 | Analog Ground | 66 | B7 | Receive Analog Ground (RAVS2). RAVS2 supplies power for the receive LIU peak detect and slicer. RAVS2 should be connected to analog GND. |
| QAVD | Analog Power | 67 | A6 | Quiet Analog Power (QAVD). QAVD supplies power for the core analog circuitry. QAVD should be connected to analog +3.3 V. |
| QAVS | Analog Ground | 69 | D6 | Quiet Analog Ground (QAVS). QAVS supplies ground for the core analog circuitry. QAVS should be connected to analog GND. |

**Table 10 - PM4351-RI Pin Summary**

| Function | Pins |
|---|---|
| Backplane Transmit Interface | 4 pins |
| Backplane Receive Interface | 4 pins |
| Transmit Line Interface | 6 pins |
| Receive Line Interface | 4 pins |
| Timing Options Control | 5 pins |
| Analog Support Circuitry | 4 pins |
| JTAG (IEEE 1149.1) Boundary Scan Test Interface | 5 pins |
| Microprocessor Interface | 23 pins |
| Power and Ground | 25 pins |
| Total Functions Pins | 80 pins |
| Total | 80 pins |

**Table 11 PM4351-NI Pin Summary**

| Function | Pins |
|---|---|
| Backplane Transmit Interface | 4 pins |
| Backplane Receive Interface | 4 pins |
| Transmit Line Interface | 6 pins |
| Receive Line Interface | 4 pins |
| Timing Options Control | 5 pins |
| Analog Support Circuitry | 4 pins |
| JTAG (IEEE 1149.1) Boundary Scan Test Interface | 5 pins |
| Microprocessor Interface | 23 pins |
| Power and Ground | 25 pins |
| Total Functions Pins | 80 pins |
| Unused Pins | 1 pin |
| Total | 81 pins |

**Notes on Pin Description:**

1. All COMET digital inputs and bi-directional pins present minimum capacitive loading and operate at TTL logic levels.

2. All COMET digital outputs and bi-directional pins have at least 2 mA drive capability. The BTCLK and BRCLK outputs, have 6 mA drive capability. The transmit analog outputs (TXTIP and TXRING) have built-in short circuit current limiting.

3. Inputs RSTB, TMS, TDI and TRSTB have internal pull-up resistors.

4. The VSSI and VSSO ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the COMET.

5. The VDDI and VDDO power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the COMET.

6. The recommended power supply sequencing is as follows:

   a) During power-up, the voltage on the BIAS pin must be kept equal to or greater than the voltage on the VDDO3, VDDO2, VDDO1, VDDI2 and VDDI1 pins, to avoid damage to the device.

   b) VDDI power must be supplied either before VDDO or simultaneously with VDDO. Connection of VDDI and VDDO to a common VDD power plane is recommended.

   c) The VDDI power must be applied before input pins are driven or the input current per pin be limited to less than the maximum DC input current specification (20 mA).

   d) Analog power supplies (TAVD1, TAVD2, TAVD3, TAVD4, RAVD1, RAVD2, QAVD) must be applied after both VDDI and VDDO have been applied or they must be current limited to the maximum latch-up current specification (100 mA). In operation, the differential voltage measured between AVD supplies and VDDI must be less than 0.5 V. The relative power sequencing of the multiple AVD power supplies is not important.

   e) Power down the device in the reverse sequence.

# 9 FUNCTIONAL DESCRIPTION

## 9.1 Receive Interface

Two basic receive options are available: the receive stream is presented as a TTL-compatible unipolar signal with an associated clock, or the receive data is reconstructed from unequalized pulses from a center tapped signal transformer. See Figure 5 for the recommended external analog circuitry.

When the digital receive interface is enabled, the RDAT signal is expected to carry a decoded serial bit stream. RDAT can be sampled on either the rising or falling RCLKI edge. The polarity of RDAT can also be inverted.

The analog receive interface is configurable to operate in both E1 and T1 short-haul and long-haul applications. Short-haul T1 is defined as transmission over less than 655 ft of cable. Short-haul E1 is defined as transmission on any cable that attenuates the signal by less than 6 dB.

For long-haul signals, unequalized long- or short-haul bipolar alternate mark inversion (AMI) signals are received as the differential voltage between the RXTIP and RXRING inputs.

For short-haul, the slicing threshold is set to a fraction of the input signal's peak amplitude, and adapts to changes in this amplitude. The slicing threshold is 67% and 50% for DSX-1 and E1 applications, respectively. Abnormally low input signals are detected when the input level is below 140 mV for E1 and 105 mV for T1.

## Figure 5 - External Analog Interface Circuits

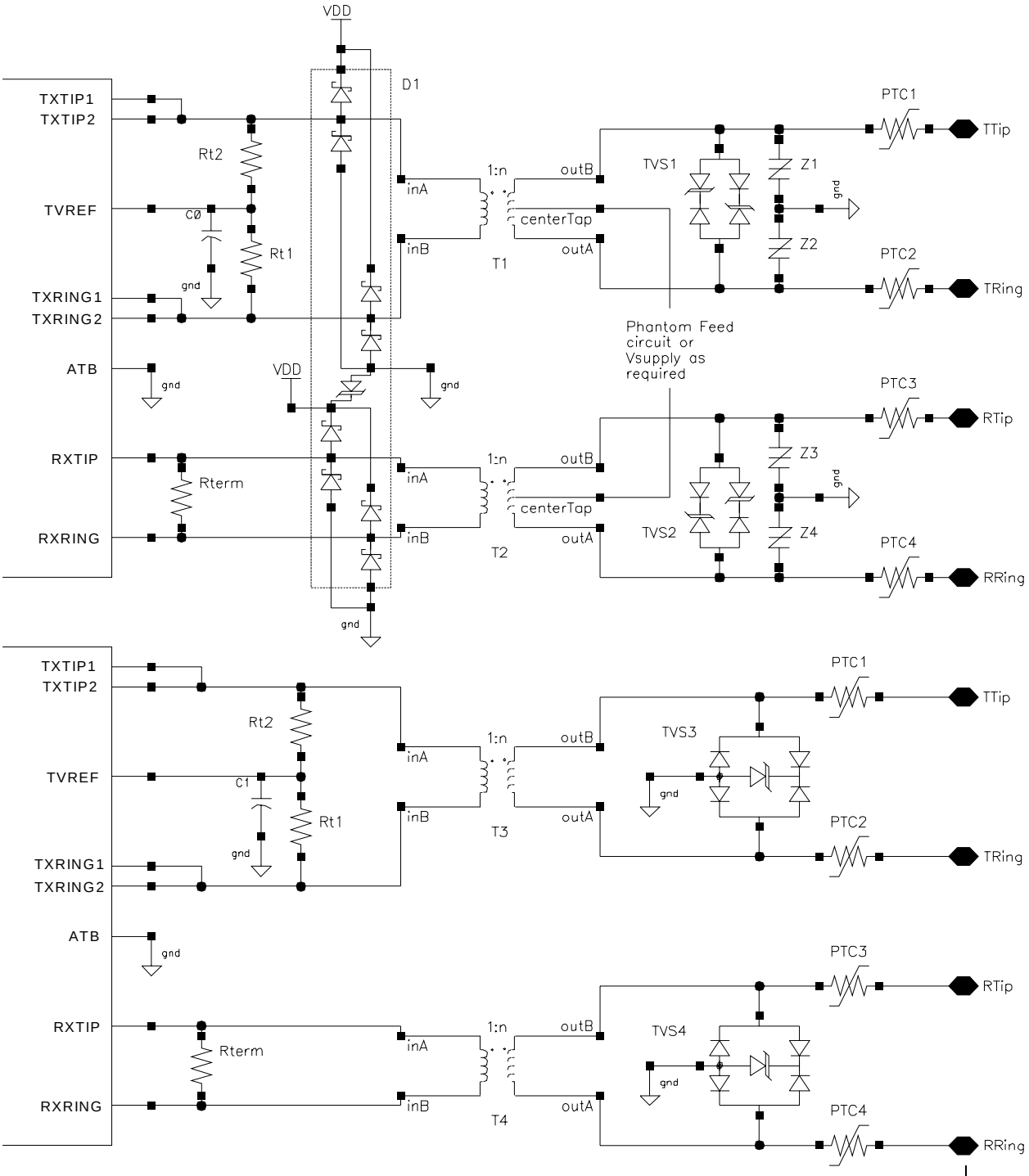



Figure 5 gives the recommended external protection circuitry for two cases:

1) for systems requiring phantom feed or inter-building line protection
2) for systems with no DC current requirements or intra-building line protection.

See Table 12 for the descriptions of components for Figure 5. See Table 14 for the descriptions of values for the transformer turns ratio, n, Rt1 and Rt2 for Figure 5.

Figure 5 assumes primary protectors (like carbon blocks) are also present. The protection resistors (PTCs) of 1Ω (but can be up to about 2Ω) are optional, but if not included then 1 to 2Ω resistor with a series fuse should be used instead. Note that the crowbar devices (Z1 – Z4) are not required if the transformer's isolation rating is not exceeded.

**Table 12 - External Component Descriptions**

| Component | Description | Part # | Source |
|---|---|---|---|
| Rt1 & Rt2 | Typically 12.7Ω ±1% Resistors (see Table 14) | | |
| Rterm | 18.2Ω ±1% Resistor for T1 & 120Ω E1<br>13Ω ±1% Resistor for 75Ω E1 (assuming a 1:2.42 transformer) | | |
| C0 & C1 | 4.7µF±10% Capacitors | | |
| PTC1 – PTC4 | 1Ω Positive Temperature Coefficient R | TC250-180 | Raychem |
| TVS1 & TVS2 | 6V Bi-directional Transient Voltage Suppressor Diode | LC01-6 | Semtech |
| TVS2 & TVS3 | 6V Bi-directional Transient Voltage Suppressor Diode | LC03-6 | Semtech |
| D1 | Surge Protector Diode Array | SRDA3.3-4 | Semtech |
| Z1 – Z4 | Bi-directional Transient Surge Suppressors | SGT27B13 | Harris |
| T1 & T2 | Generally 1:2.42CT Transformers (see Table 14) | 50436 (single)<br>T1137 (dual)<br>TG23-1505NS (single)<br>TG23-1505N1 (dual) | Midcom<br>Pulse<br>Halo<br>Halo |

| | | | |
|---|---|---|---|
| T3 & T4 | Generally 1:2.42CT Transformers with centre taps floating (see Table 14) | 50436 (single)<br>T1137 (dual)<br>TG23-1505NS (single)<br>TG23-1505N1 (dual) | Midcom<br>Pulse<br>Halo<br><br>Halo |

**Table 13 - Typical Input Return Loss at Receiver**

| Case | n | Rterm | Typical IRL |
|---|---|---|---|
| T1: Zo=100Ω | 1:2.42 | 18.2Ω ±1% | 30.2dB |
| E1: Zo=120Ω | 1:2.42 | 18.2Ω ±1% | 24.4dB |
| E1: Zo=75Ω | 1:2.42 | 13.0Ω ±1% | 43.3dB |

**Table 14 - Termination Resistors, Transformer Ratios and TRL**

| Case | n | Rt1 | Rt2 | Typical TRL |
|---|---|---|---|---|
| SH T1: Zo=100Ω | 1:2.42 | 12.7Ω ±1% | 12.7Ω ±1% | 14.1dB |
| SH T1: Zo=100Ω | 1:2.42 | | | 0dB |
| SH E1: Zo=120Ω | 1:2.42 | 12.7Ω ±1% | 12.7Ω ±1% | 19.4dB |
| SH E1: Zo=75Ω<br>SH E1: Zo=75Ω[1] | 1:2.42<br>1:2.42[1] | 12.7Ω ±1%<br>8.06Ω ±1% | 12.7Ω ±1%<br>8.06Ω ±1% | 9.6dB<br>18.8dB |
| LH T1 LBO=0dB: Zo=100Ω | 1:2.42 | 12.7Ω ±1% | 12.7Ω ±1% | 14.1dB |
| LH T1 LBO=-7.5dB: Zo=100Ω | 1:2.42 | 12.7Ω ±1% | 12.7Ω ±1% | 14.1dB |
| LH T1 LBO=-15dB: Zo=100Ω | 1:2.42 | 12.7Ω ±1% | 12.7Ω ±1% | 14.1dB |
| LH T1 LBO=-22.5dB: Zo=100Ω | 1:2.42 | 12.7Ω ±1% | 12.7Ω ±1% | 14.1dB |

Notes:
1) Headroom power is about 30% higher in this case.

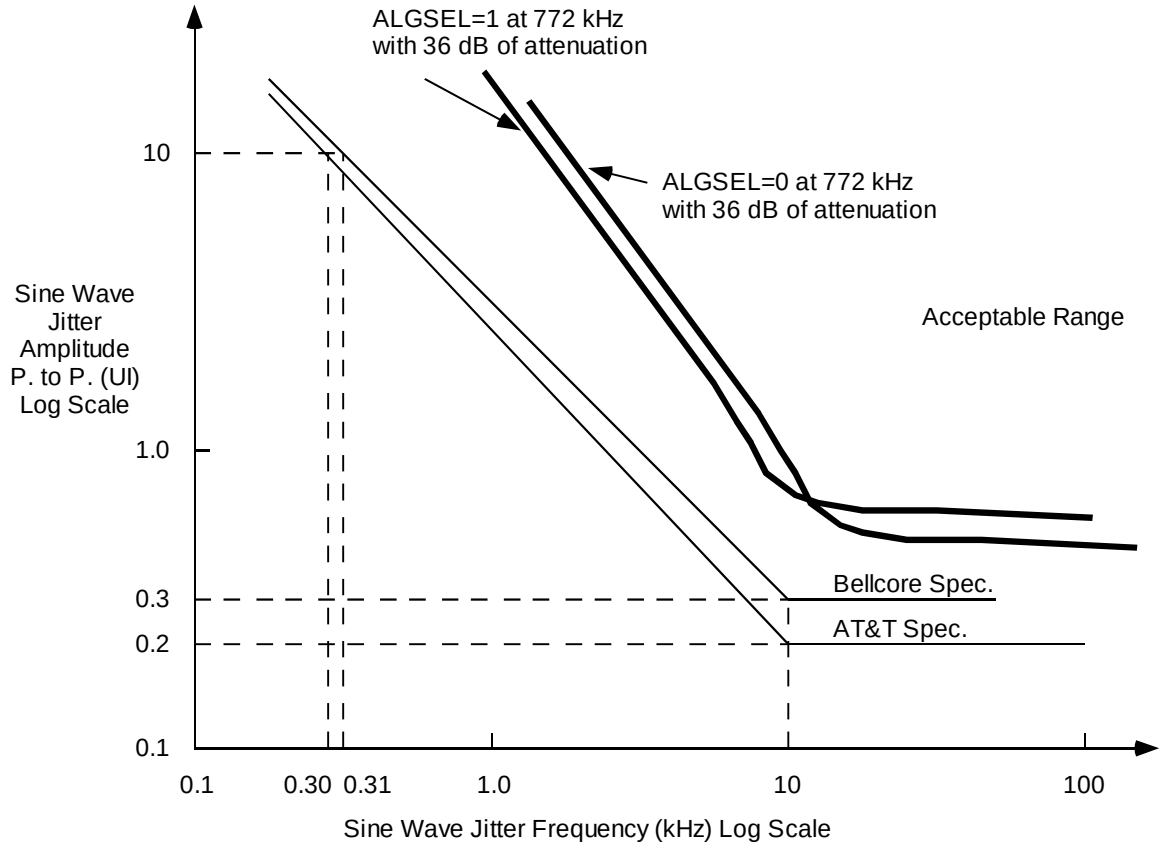
## 9.2 Clock and Data Recovery (CDRC)

The Clock and Data Recovery function is provided by the Clock and Data Recovery (CDRC) block. The CDRC provides clock and PCM data recovery,

B8ZS and HDB3 decoding, line code violation detection, and loss of signal detection. It recovers the clock from the incoming RZ data pulses using a digital phase-locked-loop and reconstructs the NRZ data. Loss of signal is indicated after a programmable threshold of consecutive bit periods of the absence of pulses on both the positive and negative line pulse inputs and is cleared after the occurrence of a single line pulse. An alternate loss of signal indication is provided which is cleared upon meeting an 1-in-8 pulse density criteria for T1 and a 1-in-4 pulse density criteria for E1. If enabled, a microprocessor interrupt is generated when a loss of signal is detected and when the signal returns. A line code violation is defined as a bipolar violation (BPV) for AMI-coded signals, is defined as a BPV that is not part of a zero substitution code for B8ZS-coded signals, and is defined as a bipolar violation of the same polarity as the last bipolar violation for HDB3-coded signals.

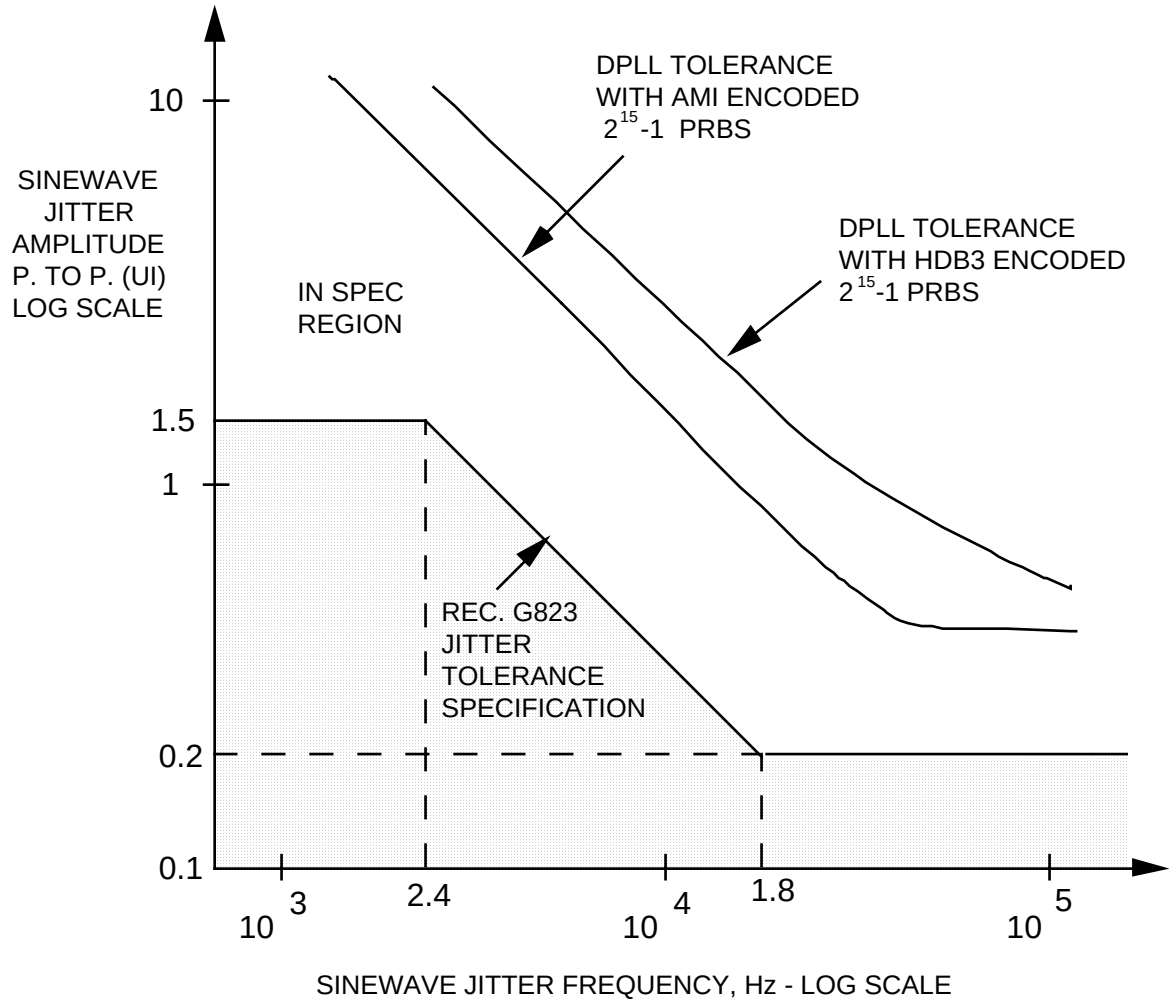
In T1 mode, the input jitter tolerance of the COMET complies with the Bellcore Document TA-TSY-000170 and with the AT&T specification TR62411, as shown in Figure 6. The tolerance is measured with a QRSS sequence ($2^{20}$-1 with 14 zero restriction). The CDRC block provides two algorithms for clock recovery that result in differing jitter tolerance characteristics. The first algorithm (when the ALGSEL register bit is logic 0) provides good low frequency jitter tolerance, but the high frequency tolerance is close to the TR62411 limit. The second algorithm (when ALGSEL is logic 1) provides much better high frequency jitter tolerance at the expense of the low frequency tolerance; the low frequency tolerance of the second algorithm is approximately 80% that of the first algorithm.

**Figure 6 - T1 Jitter Tolerance**




For E1 applications, the input jitter tolerance complies with the ITU-T Recommendation G.823 "The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy." Figure 7 illustrates this specification and the performance of the phase-locked loop when the ALGSEL register bit is logic 0.

**Figure 7 - Compliance with ITU-T Specification G.823 for E1 Input Jitter**




## 9.3 T1 Framer

The T1 framing function is provided by the T1-FRMR block. This block searches for the framing bit position of SF, ESF, J1, T1DM or SLC®96 framing formats in the incoming recovered PCM stream. When searching for frame, the T1-FRMR examines each of the 193 (SF, T1DM or SLC®96) or each of 4*193 (ESF or J1) framing bit candidates concurrently.

The time required to find frame alignment to an error-free PCM stream containing randomly distributed channel data (i.e. each bit in the channel data has a 50% probability of being 1 or 0) is dependent upon the framing format. For standard superframe format (SF, also known as D4 format), the T1-FRMR block

will determine frame alignment within 4.4 ms 99 times out of 100. For SLC®96 format, the T1-FRMR will determine frame alignment within 9.9 ms 99 times out of 100. For extended superframe format (ESF) and J1, the T1-FRMR will determine frame alignment within 15 ms 99 times out of 100. For T1DM format, the T1-FRMR will determine frame alignment within 1.125 ms 99 times out of 100.

Once the T1-FRMR has found frame, the incoming PCM data is continuously monitored for framing bit errors, bit error events (a framing bit error in SF or SLC®96, a framing bit error or sync bit error in T1DM, or a CRC-6 error in ESF and J1), and severe errored framing events. The T1-FRMR also detects loss of frame, based on a selectable ratio of framing bit errors.

The T1-FRMR extracts the Yellow alarm signal bits from the incoming PCM data stream in SF and SLC®96 framing formats, and extracts the Y-bit from the T1DM sync word in T1DM framing format. The T1-FRMR also extracts the SLC®96 data link in SLC®96 framing format (with external logic), extracts the facility data link bits in the ESF and J1 framing formats, and extracts the R-bit from the T1DM sync word in T1DM framing format.

The T1-FRMR can also be disabled to allow reception of unframed data.

## 9.4 E1 Framer

The E1 framing function is provided by the E1-FRMR block. The E1-FRMR block searches for basic frame alignment, CRC multiframe alignment, and channel associated signaling (CAS) multiframe alignment in the incoming recovered PCM stream.

Once the E1-FRMR has found basic (or FAS) frame alignment, the incoming PCM data stream is continuously monitored for FAS/NFAS framing bit errors. Framing bit errors are accumulated in the framing bit error counter contained in the PMON block. Once the E1-FRMR has found CRC multiframe alignment, the PCM data stream is continuously monitored for CRC multiframe alignment pattern errors, and CRC-4 errors. CRC-4 errors are accumulated in the CRC error counter of the PMON block. Once the E1-FRMR has found CAS multiframe alignment, the PCM data is continuously monitored for CAS multiframe alignment pattern errors. The E1-FRMR also detects and indicates loss of basic frame, loss of CRC multiframe, and loss of CAS multiframe, based on user-selectable criteria. The reframe operation can be initiated by software (via the E1-FRMR Frame Alignment Options Register), by excessive CRC errors, or when CRC multiframe alignment is not found within 400 ms. The E1-FRMR also identifies the position of the frame, the CAS multiframe, and the CRC multiframe.

The E1-FRMR extracts the contents of the International bits (from both the FAS frames and the NFAS frames), the National bits, and the Extra bits (from timeslot 16 of frame 0 of the CAS multiframe), and stores them in the E1-FRMR International/National Bits register and the E1-FRMR Extra Bits register. Moreover, the FRMR also extracts submultiframe-aligned 4-bit codewords from each of the National bit positions Sa4 to Sa8, and stores them in microprocessor-accessible registers that are updated every CRC submultiframe.

The E1-FRMR identifies the raw bit values for the Remote (or distant frame) Alarm (bit 3 in timeslot 0 of NFAS frames) and the Remote Signaling Multiframe (or distant multiframe) Alarm (bit 6 of timeslot 16 of frame 0 of the CAS multiframe) via the E1-FRMR International/National Bits Register, and the E1-FRMR Extra Bits Register respectively. Access is also provided to the "debounced" remote alarm and remote signaling multiframe alarm bits which are set when the corresponding signals have been a logic 1 for 2 or 3 consecutive occurrences, as per Recommendation O.162. Detection of AIS and timeslot 16 AIS are provided. AIS is also integrated, and an AIS Alarm is indicated if the AIS condition has persisted for at least 100 ms. The out of frame (OOF=1) condition is also integrated, indicating a Red Alarm if the OOF condition has persisted for at least 100 ms.

An interrupt may be generated to signal a change in the state of any status bits (OOF, OOSMF, OOCMF, AIS or RED), and to signal when any event (RAI, RMAI, AISD, COFA, FER, SMFER, CMFER, CRCE or FEBE) has occurred. Additionally, interrupts may be generated every frame, CRC submultiframe, CRC multiframe or signaling multiframe.

**Basic Frame Alignment Procedure**

The E1-FRMR searches for basic frame alignment using the algorithm defined in ITU-T Recommendation G.706 sections 4.1.2 and 4.2.

The algorithm finds frame alignment by using the following sequence:

1. Search for the presence of the correct 7-bit FAS (‘0011011’);

2. Check that the FAS is absent in the following frame by verifying that bit 2 of the assumed non-frame alignment sequence (NFAS) TS 0 byte is a logic 1;

3. Check that the correct 7-bit FAS is present in the assumed TS 0 byte of the next frame.

If either of the conditions in steps 2 or 3 are not met, a new search for frame alignment is initiated in the bit immediately following the second 7-bit FAS sequence check. This "hold-off" is done to ensure that new frame alignment

searches are done in the next bit position, modulo 512. This facilitates the discovery of the correct frame alignment, even in the presence of fixed timeslot data imitating the FAS.

These algorithms provide robust framing operation even in the presence of random bit errors: framing with algorithm #1 or #2 provides a 99.98% probability of finding frame alignment within 1 ms in the presence of $10^{-3}$ bit error rate and no mimic patterns.

Once frame alignment is found, the block sets the OOF indication low, indicates a change of frame alignment (if it occurred), and monitors the frame alignment signal, indicating errors occurring in the 7-bit FAS pattern and in bit 2 of NFAS frames, and indicating the debounced value of the Remote Alarm bit (bit 3 of NFAS frames). Using debounce, the Remote Alarm bit has <0.00001% probability of being falsely indicated in the presence of a $10^{-3}$ bit error rate. The block declares loss of frame alignment if 3 consecutive FASs have been received in error or, additionally, if bit 2 of NFAS frames has been in error for 3 consecutive occasions. In the presence of a random $10^{-3}$ bit error rate the frame loss criteria provides a mean time to falsely lose frame alignment of >12 minutes.

The E1-FRMR can be forced to initiate a basic frame search at any time when any of the following conditions are met:

- the software re-frame bit in the E1-FRMR Frame Alignment Options register goes to logic 1;
- the CRC Frame Find Block is unable to find CRC multiframe alignment; or
- the CRC Frame Find Block accumulates excessive CRC evaluation errors ($\geq$ 915 CRC errors in 1 second) and is enabled to force a re-frame under that condition.

**CRC Multiframe Alignment Procedure**

The E1-FRMR searches for CRC multiframe alignment by observing whether the International bits (bit 1 of TS 0) of NFAS frames follow the CRC multiframe alignment pattern. Multiframe alignment is declared if at least two valid CRC multiframe alignment signals are observed within 8 ms, with the time separating two alignment signals being a multiple of 2 ms

Once CRC multiframe alignment is found, the OOCMFV register bit is set to logic 0, and the E1-FRMR monitors the multiframe alignment signal, indicating errors occurring in the 6-bit MFAS pattern, errors occurring in the received CRC and the value of the FEBE bits (bit 1 of frames 13 and 15 of the multiframe). The E1-FRMR declares loss of CRC multiframe alignment if basic frame

alignment is lost. However, once CRC multiframe alignment is found, it cannot be lost due to errors in the 6-bit MFAS pattern.

Under the CRC-to-non-CRC interworking algorithm, if the E1-FRMR can achieve basic frame alignment with respect to the incoming PCM data stream, but is unable to achieve CRC-4 multiframe alignment within the subsequent 400 ms, the distant end is assumed is assumed to be a non CRC-4 interface. The details of this algorithm are illustrated in the state diagram in Figure 8.

**Figure 8 - CRC Multiframe Alignment Algorithm**

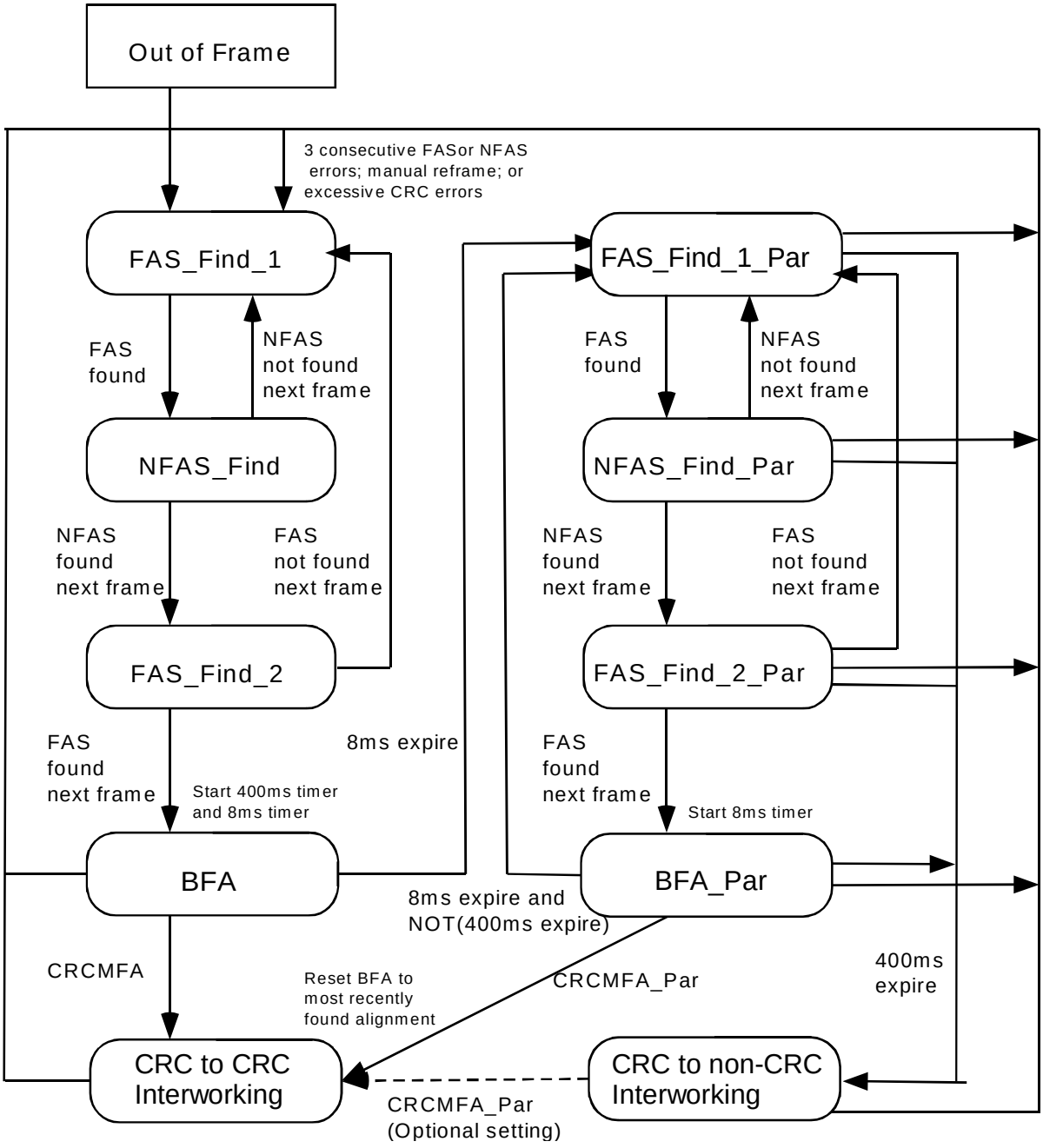


**Table 15 - E1-FRMR Framing States**

| State | Out of Frame | Out of Offline Frame |
|---|---|---|
| FAS_Find_1 | Yes | No |
| NFAS_Find | Yes | No |
| FAS_Find_2 | Yes | No |
| BFA | No | No |
| CRC to CRC Interworking | No | No |
| FAS_Find_1_Par | No | Yes |
| NFAS_Find_Par | No | Yes |
| FAS_Find_2_Par | No | Yes |
| BFA_Par | No | No |
| CRC to non-CRC Interworking | No | No |

The states of the primary basic framer and the parallel/offline framer in the E1-FRMR block at each stage of the CRC multiframe alignment algorithm are shown in Table 15.

From an out of frame state, the E1-FRMR attempts to find basic frame alignment in accordance with the FAS/NFAS/FAS G.706 Basic Frame Alignment procedure outlined above. Upon achieving basic frame alignment, a 400 ms timer is started, as well as an 8 ms timer. If two CRC multiframe alignment signals separated by a multiple of 2 ms are observed before the 8 ms timer has expired, CRC multiframe alignment is declared.

If the 8 ms timer expires without achieving multiframe alignment, a new offline search for basic frame alignment is initiated. This search is performed in accordance with the Basic Frame Alignment procedure outlined above. However, this search does not immediately change the actual basic frame alignment of the system (i.e., PCM data continues to be processed in accordance with the first basic frame alignment found after an out of frame state while this frame alignment search occurs as a parallel operation).

When a new basic frame alignment is found by this offline search, the 8 ms timer is restarted. If two CRC multiframe alignment signals separated by a multiple of 2 ms are observed before the 8 ms timer has expired, CRC multiframe alignment

is declared and the basic frame alignment is set accordingly (i.e., the basic frame alignment is set to correspond to the frame alignment found by the parallel offline search, which is also the basic frame alignment corresponding to the newly found CRC multiframe alignment).

Subsequent expirations of the 8 ms timer will likewise reinitiate a new search for basic frame alignment. If, however, the 400 ms timer expires at any time during this procedure, the E1-FRMR stops searching for CRC multiframe alignment and declares CRC-to-non-CRC interworking. In this mode, the E1-FRMR may be optionally set to either halt searching for CRC multiframe altogether, or may continue searching for CRC multiframe alignment using the established basic frame alignment. In either case, no further adjustments are made to the basic frame alignment, and no offline searches for basic frame alignment occur once CRC-to-non-CRC interworking is declared: it is assumed that the established basic frame alignment at this point is correct.

### AIS Detection

When an unframed all-ones receive data stream is received, an AIS defect is indicated by setting the AISD bit to logic 1 when fewer than three zero bits are received in 512 consecutive bits or, optionally, in each of two consecutive periods of 512 bits. The AISD bit is reset to logic 0 when three or more zeros in 512 consecutive bits or in each of two consecutive periods of 512 bits. Finding frame alignment will also cause the AISD bit to be set to logic 0.

### Signaling Frame Alignment

Once the basic frame alignment has been found, the E1-FRMR searches for Channel Associated Signaling (CAS) multiframe alignment using the following G.732 compliant algorithm: signaling multiframe alignment is declared when at least one non-zero time slot 16 bit is observed to precede a time slot 16 containing the correct CAS alignment pattern, namely four zeros (“0000”) in the first four bit positions of timeslot 16.

Once signaling multiframe alignment has been found, the E1-FRMR sets the OOSMFV bit of the E1-FRMR Framing Status register to logic 0, and monitors the signaling multiframe alignment signal, indicating errors occurring in the 4-bit pattern, and indicating the debounced value of the Remote Signaling Multiframe Alarm bit (bit 6 of timeslot 16 of frame 0 of the multiframe). Using debounce, the Remote Signaling Multiframe Alarm bit has < 0.00001% probability of being falsely indicated in the presence of a $10^{-3}$ bit error rate.

The block declares loss of CAS multiframe alignment if two consecutive CAS multiframe alignment signals have been received in error, or additionally, if all the bits in time slot 16 are logic 0 for 1 or 2 (selectable) CAS multiframes. Loss of

CAS multiframe alignment is also declared if basic frame alignment has been lost.

### National Bit Extraction

The E1-FRMR extracts and assembles the submultiframe-aligned National bit codewords Sa4[1:4] , Sa5[1:4] , Sa6[1:4] , Sa7[1:4] and Sa8[1:4]. The corresponding register values are updated upon generation of the CRC submultiframe interrupt.

This E1-FRMR also detects the V5.2 link ID signal, which is defined as the condition where 2 out of 3 Sa7 bits are zeroes. Upon reception of this Link ID signal, the V52LINKV bit of the E1-FRMR Framing Status register is set to logic 1. This bit is cleared to logic 0 when 2 out of 3 Sa7 bits are ones.

### Alarm Integration

The OOF and the AIS defects are integrated, verifying that each condition has persisted for 104 ms (± 6 ms) before indicating the alarm condition. The alarm is removed when the condition has been absent for 104 ms (± 6 ms).

The AIS alarm algorithm accumulates the occurrences of AISD (AIS detection). The E1-FRMR counts the occurrences of AISD over a 4 ms interval and indicates a valid AIS is present when 13 or more AISD indications (of a possible 16) have been received. Each interval with a valid AIS presence indication increments an interval counter which declares AIS Alarm when 25 valid intervals have been accumulated. An interval with no valid AIS presence indication decrements the interval counter. The AIS Alarm declaration is removed when the counter reaches 0. This algorithm provides a 99.8% probability of declaring an AIS Alarm within 104 ms in the presence of a $10^{-3}$ mean bit error rate.

The Red alarm algorithm monitors occurrences of OOF over a 4 ms interval, indicating a valid OOF interval when one or more OOF indications occurred during the interval, and indicating a valid in frame (INF) interval when no OOF indication occurred for the entire interval. Each interval with a valid OOF indication increments an interval counter which declares Red Alarm when 25 valid intervals have been accumulated. An interval with valid INF indication decrements the interval counter; the Red Alarm declaration is removed when the counter reaches 0. This algorithm biases OOF occurrences, leading to declaration of Red alarm when intermittent loss of frame alignment occurs.

## 9.5 T1 Inband Loopback Code Detector (IBCD)

The T1 Inband Loopback Code Detection function is provided by the IBCD block. This block detects the presence of either of two programmable INBAND LOOPBACK ACTIVATE and DEACTIVATE code sequences in either framed or unframed data streams. Each INBAND LOOPBACK code sequence is defined as the repetition of the programmed code in the PCM stream for at least 5.1 seconds. The code sequence detection and timing is compatible with the specifications defined in T1.403-1993, TA-TSY-000312, and TR-TSY-000303. LOOPBACK ACTIVATE and DEACTIVATE code indication is provided through internal register bits. An interrupt is generated to indicate when either code status has changed.

## 9.6 T1 Pulse Density Violation Detector (PDVD)

The Pulse Density Violation Detection function is provided by the PDVD block. The block detects pulse density violations of the requirement that there be N ones in each and every time window of 8(N+1) data bits (where N can equal 1 through 23). The PDVD also detects periods of 16 consecutive zeros in the incoming data. Pulse density violation detection is provided through an internal register bit. An interrupt is generated to signal a 16 consecutive zero event, and/or a change of state on the pulse density violation indication.

The PDVD block is available when the analog RXTIP and RXRING inputs are enabled (i.e., when the RUNI bit in the Receive Line Interface Configuration register is logic 0).

## 9.7 Performance Monitor Counters (PMON)

The Performance Monitor Counters function is provided by the PMON block. The block accumulates CRC error events, Frame Synchronization bit error events, Line Code Violation events, and Out Of Frame events, or optionally, Change of Frame Alignment (COFA) events with saturating counters over consecutive intervals as defined by the period of the supplied transfer clock signal (typically 1 second). When the transfer clock signal is applied, the PMON transfers the counter values into holding registers and resets the counters to begin accumulating events for the interval. The counters are reset in such a manner that error events occurring during the reset are not missed. If the holding registers are not read between successive transfer clocks, an OVERRUN register bit is asserted.

For T1, a line code violation is either a bipolar violation (only those not part of a zero substitution code for B8ZS-coded and HDB3 signals) or excessive zeros. Excessive zeros is a sequence of zeros greater than 15 bits long for an AMI-code

signal and greater than 7 bits long for a B8ZS-coded signals. The inclusion of excessive zeros in the line code violation count can be disabled.

For E1, a line code violation is defined as a bipolar violation (BPV) for AMI-coded signals and is defined as a bipolar violation of the same polarity as the last bipolar violation for HDB3-coded signals.

Generation of the transfer clock within the COMET chip is performed by writing to any counter register location or by writing to the Global PMON Update register. The holding register addresses are contiguous to facilitate faster polling operations.

## 9.8 T1 Bit Oriented Code Detector (RBOC)

The Bit Oriented Code detection function is provided by the RBOC block. This block detects the presence of 63 of the possible 64 bit oriented codes transmitted in the Facility Data Link channel in ESF framing format, as defined in ANSI T1.403-1993 and in TR-TSY-000194. The 64$^{th}$ code (111111) is similar to the DL FLAG sequence and is used by the RBOC to indicate no valid code received.

Bit oriented codes are received on the Facility Data Link channel as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated at least 10 times. The RBOC can be enabled to declare a received code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit in the control register.

Valid BOC are indicated through an internal status register. The BOC bits are set to all ones (111111) if no valid code has been detected. An interrupt is generated to signal when a detected code has been validated, or optionally, when a valid code goes away (i.e. the BOC bits go to all ones).

## 9.9 HDLC Receiver (RDLC)

The HDLC Receiver function is provided by the RDLC block. The RDLC is a microprocessor peripheral used to receive HDLC frames. Three RDLC blocks are provided for flexible extraction of standardized data links:

- T1 ESF facility data link
- T1DM data link
- ISDN D-channel
- E1 Common Channel Signaling data link

- V5.1/V5.2 D-channel and C-channels.
- E1 Sa-bit data link

The RDLC detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives packet data, and calculates the CRC-CCITT frame check sequence (FCS).

In the address matching mode, only those packets whose first data byte matches one of two programmable bytes or the universal address (all ones) are stored in the FIFO. The two least significant bits of the address comparison can be masked for LAPD SAPI matching.

Received data is placed into a 128-byte FIFO buffer. An interrupt is generated when a programmable number of bytes are stored in the FIFO buffer. Other sources of interrupt are detection of the terminating flag sequence, abort sequence, or FIFO buffer overrun.

The Status Register contains bits which indicate the overrun or empty FIFO status, the interrupt status, and the occurrence of first flag or end of message bytes written into the FIFO. The Status Register also indicates the abort, flag, and end of message status of the data just read from the FIFO. On end of message, the Status Register indicates the FCS status and if the packet contained a non-integer number of bytes.

## 9.10 T1 Alarm Integrator (ALMI)

The T1 Alarm Integration function is provided by the ALMI block. This block detects the presence of Yellow, Red, and AIS Carrier Fail Alarms (CFA) in SF, T1DM, SLC®96, or ESF formats. The alarm detection and integration is compatible with the specifications defined in Bell Pub 43801, TA-TSY-000278, TR-TSY-000008, ANSI T1.403-1993, and TR-TSY-000191. Alarm detection and validation for SLC®96 is handled the same as SF framing format.

The ALMI block declares the presence of Yellow alarm when the Yellow pattern has been received for 425 ms (± 50 ms); the Yellow alarm is removed when the Yellow pattern has been absent for 425 ms (± 50 ms). The presence of Red alarm is declared when an out-of-frame condition has been present for 2.55 sec (± 40 ms); the Red alarm is removed when the out-of-frame condition has been absent for 16.6 sec (± 500 ms). In T1DM framing format the Red alarm declaration criteria can be selected to be either 400 ms (± 100 ms) or 2.55 sec (± 40 ms); removal of the Red alarm in T1DM can be selected to be either 100 ms (± 50 ms) or 16.6 sec (± 500 ms). The presence of AIS alarm is declared when an out-of-frame condition and all-ones in the PCM data stream

have been present for 1.5 sec (± 100 ms); the AIS alarm is removed when the AIS condition has been absent for 16.8 sec (± 500 ms).

CFA alarm detection algorithms operate in the presence of a random $10^{-3}$ bit error rate.

The ALMI also indicates the presence or absence of the Yellow, Red, and AIS alarm signal conditions over 40 ms , 40 ms and 60 ms intervals, respectively, allowing an external microprocessor to integrate the alarm conditions via software with any user-specific algorithms. Alarm indication is provided through internal register bits.

## 9.11 Receive Elastic Store (RX-ELST)

The Receive Elastic Store (RX-ELST) synchronizes incoming PCM frames to the local backplane clock, BRCLK. The frame data is buffered in a two-frame circular data buffer. Input data is written to the buffer using a write pointer and output data is read from the buffer using a read pointer.

When the elastic store is being used, if the average frequency of the incoming data is greater than the average frequency of the backplane clock, the write pointer will catch up to the read pointer and the buffer will be filled. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The following frame of PCM data will be deleted.

If the average frequency of the incoming data is less than the average frequency of the backplane clock, the read pointer will catch up to the write pointer and the buffer will be empty. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The last frame which was read will be repeated.

A slip operation is always performed on a frame boundary.

When the backplane timing is derived from the receive line data (i.e. BRCLK is an output), the elastic store can be bypassed to eliminate the two frame delay. In this configuration the elastic store can be used to measure frequency differences between the recovered line clock and another 1.544 MHz or 2.048 MHz clock applied to the BRCLK input. A typical example might be to measure the difference in frequency between two received streams (i.e. East-West frequency difference) by monitoring the number of SLIP occurrences of one direction with respect to the other.

To allow for the extraction of signaling information in the PCM data channels, superframe identification is also passed through the RX-ELST.

For payload conditioning, the RX-ELST may optionally insert a programmable idle code into all channels when the framer is out of frame synchronization. This code is set to all 1's when the RX-ELST is reset.

## 9.12 Receive Jitter Attenuator (RJAT)

The Receive Jitter Attenuator (RJAT) digital PLL attenuates the jitter present on the RXTIP/RXRING or RDAT inputs. The attenuation is only performed when the RJATBYP register bit is a logic 0.

The jitter characteristics of the Receive Jitter Attenuator (RJAT) are the same as the Transmit Jitter Attenuator (TJAT).

## 9.13 Signaling Extractor (SIGX)

The Signaling Extraction (SIGX) block provides channel associated signaling (CAS) extraction from an E1 signaling multiframe or from SF and ESF T1 formats. With external logic the Signaling Extraction (SIGX) block extracts the nine bit signaling format from SLC®96 T1 formats.

The SIGX block provides signaling bit extraction from the received data stream for T1 ESF, SF, SLC®96 and E1 framing formats. It selectively debounces the bits, and serializes the results onto the BRSIG output. Debouncing is performed on individual signaling bits. This BRSIG output is channel aligned with BRPCM output, and the signaling bits are repeated for the entire superframe, allowing downstream logic to reinsert signaling into any frame, as determined by system timing. The signaling data stream contains the A,B,C,D bits in the lower 4 channel bit locations (bits 5, 6, 7 and 8) in T1 ESF and E1 framing formats; in SF and SLC®96 formats the A and B bits are repeated in locations C and D (i.e. the signaling stream contains the bits ABAB for each channel).

The SIGX block contains three superframes worth of signal buffering to ensure that there is a greater than 95% probability that the signaling bits are frozen in the correct state for a 50% ones density out-of-frame condition, as specified in TR-TSY-000170 and BELL PUB 43801. With signaling debounce enabled, the per-channel signaling state must be in the same state for 2 superframes before appearing on the serial output stream.

The SIGX block provides one superframe or signaling-multiframe of signal freezing on the occurrence of slips. When a slip event occurs, the SIGX freezes the output signaling for the entire superframe in which the slip occurred; the signaling is unfrozen when the next slip-free superframe occurs.

The SIGX also provides control over timeslot signaling bit fixing, data inversion and signaling debounce on a per-timeslot basis.

The SIGX block also provides an interrupt to indicate a change of signaling state on a per channel basis.

## 9.14 Receive Per-channel Serial Controller (RPSC)

The Receive Per-channel Serial Controller (RPSC) function is provided by a PCSC block.

The RPSC allows data and signaling trunk conditioning to be applied independently on the receive stream on a per-channel basis.

## 9.15 T1 Signaling Aligner (SIGA)

The T1 Signaling Aligner can be positioned before the T1 basic transmitter to provide superframe alignment of the signaling bits between the backplane and the transmit DS-1 stream. The signaling alignment block maintains signaling bit integrity across superframe boundaries.

## 9.16 T1 Basic Transmitter (XBAS)

The T1 Basic Transmitter (XBAS) block generates the 1.544 Mbit/s T1 data stream according to SF, ESF, T1DM or SLC®96 formats.

In concert with the Transmit Per-Channel Serial Controller (TPSC), the XBAS block provides per channel control of idle code substitution, data inversion (either all 8 bits, sign bit only or magnitude only), digital milliwatt substitution, and zero code suppression. Three types of zero code suppression (GTE, Bell and DDS) are supported and selected on a per channel basis to provide minimum ones density control. Robbed bit signaling control and selection of the signaling source are also performed on a per-channel basis. All channels can be forced into a trunk conditioning state (idle code substitution and signaling conditioning) by use of the Master Trunk Conditioning bit in the T1 XBAS Configuration Register.

A data link is provided for ESF, T1DM and SLC®96 modes. The data link sources include bit oriented codes and HDLC messages. Support is provided for the transmission of framed or unframed Inband Code sequences and transmission of AIS or Yellow alarm signals for all formats.

PCM output signals may be selected to conform to B8ZS or AMI line coding.

The transmitter can be disabled for framing via the FDIS bit in the Transmit Framing and Bypass Options register. When transmitting ESF formatted data, the framing bit, datalink bit, or the CRC-6 bit from the input PCM stream can be by-passed to the output PCM stream.

## 9.17 E1 Transmitter (E1-TRAN)

The E1 Transmitter (E1-TRAN) generates a 2048 kbit/s data stream according to ITU-T recommendations, providing individual enables for frame generation, CRC multiframe generation, and channel associated signaling (CAS) multiframe generation.

In concert with Transmit Per-Channel Serial Controller (TPSC), the E1-TRAN block provides per-timeslot control of idle code substitution, data inversion, digital milliwatt substitution, selection of the signaling source and CAS data. All timeslots can be forced into a trunk conditioning state (idle code substitution and signaling substitution) by use of the master trunk conditioning bit in the Configuration Register.

Common Channel Signaling (CCS) is supported in time slot 16 either through the internal HDLC Transmitter (TDPR) and the Transmit Channel Insertion (TXCI) block. Support is provided for the transmission of AIS and the transmission of remote alarm (RAI) and remote multiframe alarm signals.

The National Use bits (Sa-bits) can be sourced from the E1-TRAN National Bits Codeword registers as 4-bit codewords aligned to the submultiframe. Alternatively, the Sa-bits may individually carry data links sourced from the internal HDLC controllers, or may be passed transparently from the BTPCM input.

PCM output signals may be selected to conform to HDB3 or AMI line coding.

## 9.18 Transmit Elastic Store (TX-ELST)

The Transmit Elastic Store (TX-ELST) provides the ability to decouple the line timing from the backplane timing. The TX-ELST is required whenever the BTCLK and TCLKO clocks are not traceable to a common source. The elastic store function is in effect (with a nominal one frame delay) when:

1. BTCLK is an input (CMODE = 1) and the transmitter is loop timed to the receive recovered clock (PLLREF[1:0] = ‘b10, OCLKSEL1 = 0, OCLKSEL0 = 0).

2. BTCLK is an input (CMODE = 1) and the transmitter is clocked by TCLKI (OCLKSEL1 = 0, OCLKSEL0 = 1) or a jitter attenuated version of TCLKI (PLLREF[1:0] = ‘b11, OCLKSEL1 = 0, OCLKSEL0 = 0).

3. BTCLK is an output (CMODE = 0) referenced to the receive recovered clock (PLLREF[1:0] = ‘b10) and the transmitter is clocked by TCLKI (OCLKSEL1 = 0, OCLKSEL0 = 1).

When the elastic store is being used, if the average frequency of the backplane data is greater than the average frequency of the line clock, the buffer will fill. Under this condition a controlled slip will occur upon the next frame boundary. The following frame of PCM data will be deleted.

If the average frequency of the backplane data is less than the average frequency of the line clock, the buffer empty. Under this condition a controlled slip will occur upon the next frame boundary. The latest frame will be repeated.

A slip operation is always performed on a frame boundary. The TX-ELST is upstream of the frame overhead insertion; therefore, frame slips do not corrupt the frame alignment signal.

When the line timing is derived from BTCLK or BTCLK is an output, the elastic store is bypassed to eliminate the two frame delay.

## 9.19 Transmit Per-Channel Serial Controller (TPSC)

The Transmit Per-channel Serial Controller allows data and signaling trunk conditioning or idle code to be applied on the transmit DS-1 stream on a per-channel basis. It also allows per-channel control of zero code suppression, data inversion, and application of digital milliwatt.

The Transmit Per-channel Serial Controller function is provided by a Per-Channel Serial Controller (PCSC) block. The PCSC is a general purpose triple serializer. Data is sourced from three banks of thirty-two 8-bit registers, with each bank supporting a single serial output.

The TPSC interfaces directly to the E1-TRAN and T1-XBAS blocks to provide serial streams for signaling control, idle code data and PCM data control.

The registers are accessible from the µP interface in an indirect address mode. The BUSY indication signal can be polled from an internal status register to check for completion of the current operation.

## 9.20 T1 Inband Loopback Code Generator (XIBC)

The T1 Inband Loopback Code Generator (XIBC) block generates a stream of inband loopback codes (IBC) to be inserted into a T1 data stream. The IBC stream consists of continuous repetitions of a specific code and can be either framed or unframed. When the XIBC is enabled to generate framed IBC, the framing bit overwrites the inband code pattern. The contents of the code and its length are programmable from 3 to 8 bits. The XIBC interfaces directly to the XBAS Basic Transmitter block.

## 9.21 T1 Bit Oriented Code Generator (XBOC)

The T1 Bit Oriented Code Generator function is provided by the XBOC block. This block transmits 63 of the possible 64 bit oriented codes in the Facility Data Link channel in ESF framing format, as defined in ANSI T1.403-1989. The 64th code (111111) is similar to the HDLC Flag sequence and is used in the XBOC to disable transmission of any bit oriented codes.

Bit oriented codes are transmitted on the Facility Data Link channel as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated as long as the code is not 111111. The transmitted bit oriented codes have priority over any data transmitted on the FDL except for ESF Yellow Alarm. The code to be transmitted is programmed by writing the code register.

## 9.22 HDLC Transmitters

The HDLC Transmit function is provided by the TDPR block. Three TDPR blocks are provided for flexible insertion of standardized data links:

- T1 ESF facility data link
- T1DM data link
- ISDN D-channel
- E1 Common Channel Signaling data link
- V5.1/V5.2 D-channel and C-channels.
- E1 Sa-bit data link

The TDPR is a general purpose HDLC transmitter. The TDPR is used under microprocessor control to transmit HDLC data frames. The TDPR performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, idle, and abort sequence insertion. Data to be transmitted is provided by writing to a transmit data register. Upon completion of the frames, a CRC-CCITT frame check sequence is transmitted, followed by flag sequences. If the transmit data register underflows, an abort sequence is automatically transmitted.

When enabled, the TDPR continuously transmits the flag sequence (01111110) until data is ready to be transmitted. Data bytes to be transmitted are written into the Transmit Data Register. The TDPR performs a parallel-to-serial conversion of each data byte and transmits it using one of two procedures.

The default procedure provides automatic transmission of data once a complete packet is written. All complete packets of data will be transmitted. After the last data byte of a packet, the CRC word (if CRC insertion has been enabled) and a flag, or just a flag (if CRC insertion has not been enabled) is transmitted. The TDPR then returns to the transmission of flag characters until the next packet is available for transmission. While working in this mode, the user must only be careful to avoid overfilling the FIFO; underruns cannot occur unless the packet is greater than 128 bytes long. The TDPR will force transmission if the FIFO is filled up regardless of whether or not the packet has been completely written into the FIFO.

The second procedure transmits data only when the FIFO depth has reached a user configured upper threshold. The TDPR will continue to transmit data until the FIFO depth has fallen below the upper threshold and the transmission of the last packet with data above the upper threshold has completed. In this mode, the user must be careful to avoid overruns and underruns. An interrupt can be generated once the FIFO depth has fallen below a user configured lower threshold as an indicator for the user to write more data.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort characters.

Abort characters can be continuously transmitted at any time by setting a control bit. During transmission, an underrun situation can occur if data is not written to the Transmit Data Register before the previous byte of a packet currently being transmitted has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the UDR signal.

## 9.23 T1 Automatic Performance Report Generation

In compliance with the ANSI T1.231, T1.403 and T1.408 standards, a performance report is generated each second for T1 ESF applications. The report conforms to the HDLC protocol and is inserted into the ESF facility data link.

The performance report can only be transmitted if TDPR #1 is configured to insert the ESF Facility Data Link and the PREN bit of the TDPR #1 Configuration register is logic 1. The performance report takes precedence over incompletely written packets, but it does not pre-empt packets already being transmitted.

See the Operation section for details on the performance report encoding.

## 9.24 Pulse Density Enforcer (XPDE)

The Pulse Density Enforcer function is provided by the XPDE block. Pulse density enforcement is enabled by a register bit within the XPDE.

This block monitors the digital output of the transmitter and detects when the stream is about to violate the ANSI T1.403 12.5% pulse density rule over a moving 192-bit window. If a density violation is detected, the block can be enabled to insert a logic 1 into the digital stream to ensure the resultant output no longer violates the pulse density requirement. When the XPDE is disabled from inserting logic 1s, the digital stream from the transmitter is passed through unaltered.

## 9.25 Pseudo Random Pattern Generation and Detection

The Pseudo Random Sequence Generator/Processor (PRGD) is a software programmable test pattern generator, receiver and analyzer. Two types of test patterns (pseudo random and repetitive) conform to ITU-T O.151, O.152 and O.153 standards.

The PRGD can be programmed to generate pseudo random patterns with lengths up to 32 bits or any user programmable bit pattern from 1 to 32 bits in length. In addition, the PRGD can insert single bit errors or a bit error rate between $10^{-1}$ to $10^{-7}$.

The PRGD can be programmed to check for the generated pseudo random pattern. The PRGD can perform an auto synchronization to the expected pattern and accumulates the total number of bits received and the total number of bit errors in two 32-bit counters. The counters accumulate either over intervals defined by writes to the Pattern Detector registers or upon writes to the Global PMON Update Register. When an accumulation is forced, the holding registers are updated, and the counters reset to begin accumulating for the next interval. The counters are reset in such a way that no events are missed. The data is then available in the holding registers until the next accumulation.

## 9.26 Transmit Jitter Attenuator (TJAT)

The Transmit Jitter Attenuation function is provided by a digital phase lock loop and 80-bit deep FIFO. The TJAT receives jittery, dual-rail data in NRZ format on two separate inputs, which allows bipolar violations to pass through the block uncorrected. The incoming data streams are stored in a FIFO timed to the transmit clock (either BTCLK or the recovered clock). The respective input data emerges from the FIFO timed to the jitter attenuated clock (TCLKO) referenced to either TCLKI, BTCLK, or the recovered clock.

The jitter attenuator generates the jitter-free 1.544 MHz or 2.048 MHz TCLKO output transmit clock by adjusting TCLKO's phase in 1/96 UI increments to minimize the phase difference between the generated TCLKO and input data clock to TJAT (either BTCLK or the recovered clock). Jitter fluctuations in the phase of the input data clock are attenuated by the phase-locked loop within TJAT so that the frequency of TCLKO is equal to the average frequency of the input data clock. For T1 applications, to best fit the jitter attenuation transfer function recommended by TR 62411, phase fluctuations with a jitter frequency above 5.7 Hz are attenuated by 6 dB per octave of jitter frequency. Wandering phase fluctuations with frequencies below 5.7 Hz are tracked by the generated TCLKO. In E1 applications, the corner frequency is 7.6 Hz. To provide a smooth flow of data out of TJAT, TCLKO is used to read data out of the FIFO.

If the FIFO read pointer (timed to TCLKO) comes within one bit of the write pointer (timed to the input data clock, BTCLK or RSYNC), TJAT will track the jitter of the input clock. This permits the phase jitter to pass through unattenuated, inhibiting the loss of data.

### Jitter Characteristics

The TJAT Block provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. It can accommodate up to 61 UIpp of input jitter at jitter frequencies above 5.7 Hz (7.6 Hz for E1). For jitter frequencies below 5.7 Hz (7.6 Hz for E1), more correctly called wander, the tolerance increases 20 dB per decade. In most applications the TJAT Block will limit jitter tolerance at lower jitter frequencies only. For high frequency jitter, above 10 kHz for example, other factors such as clock and data recovery circuitry may limit jitter tolerance and must be considered. For low frequency wander, below 10 Hz for example, other factors such as slip buffer hysteresis may limit wander tolerance and must be considered. The TJAT block meets the stringent low frequency jitter tolerance requirements of AT&T TR 62411 and thus allows compliance with this standard and the other less stringent jitter tolerance standards cited in the references.

The corner frequency in the jitter transfer response can be altered through programming.

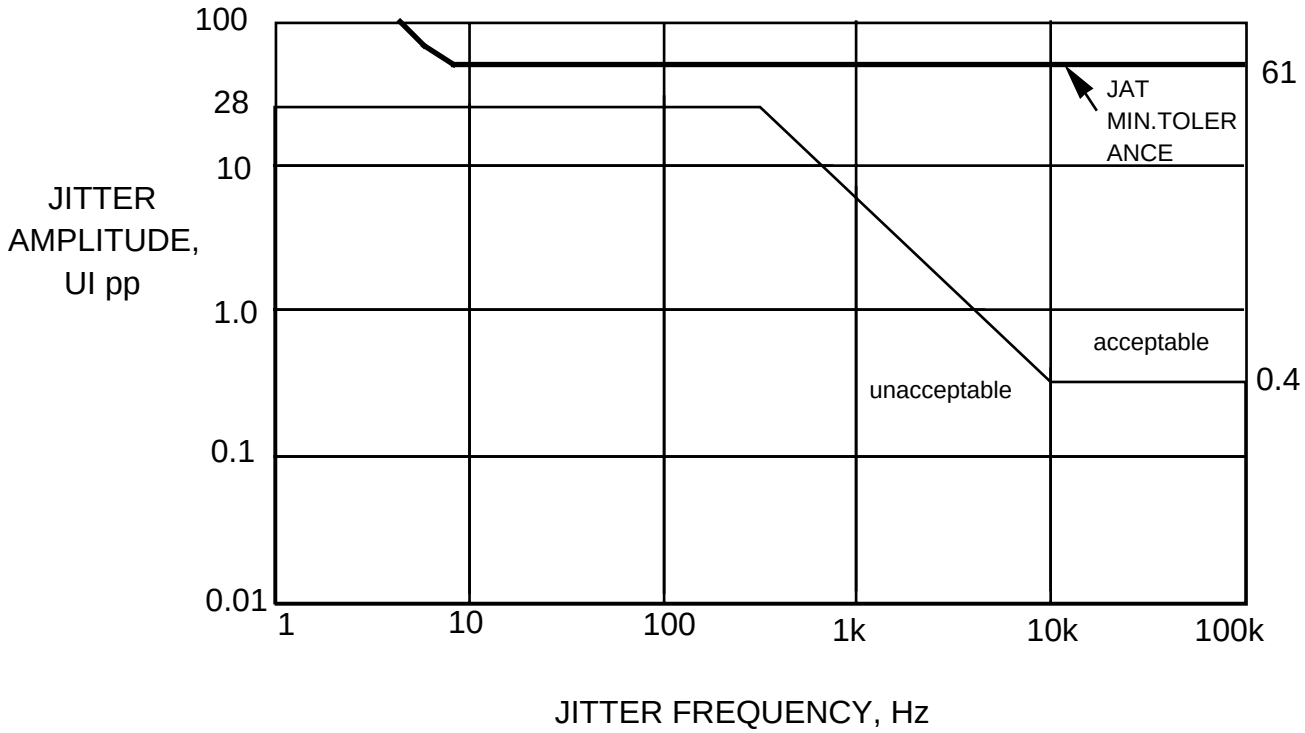
TJAT exhibits negligible jitter gain for jitter frequencies below 5.7 Hz (7.6 Hz for E1), and attenuates jitter at frequencies above 5.7 Hz (7.6 Hz for E1) by 20 dB per decade. In most applications, the TJAT block will determine jitter attenuation for higher jitter frequencies only. Wander, below 10 Hz for example, will essentially be passed unattenuated through TJAT. Jitter, above 10 Hz for example, will be attenuated as specified, however, outgoing jitter may be dominated by the generated residual jitter in cases where incoming jitter is insignificant. This generated residual jitter is directly related to the use of a

1/96 UI phase adjustment quantum. TJAT meets the jitter attenuation requirements of AT&T TR 62411. The block allows the implied jitter attenuation requirements for a TE or NT1 given in ANSI Standard T1.408, and the implied jitter attenuation requirements for a type II customer interface given in ANSI T1.403 to be met.

**Jitter Tolerance**

Jitter tolerance is the maximum input phase jitter at a given jitter frequency that a device can accept without exceeding its linear operating range, or corrupting data. For TJAT, the input jitter tolerance is 61 Unit Intervals peak-to-peak (UIpp) with a worst case frequency offset of 354 Hz. It is 80 UIpp with no frequency offset. The frequency offset is the difference between the frequency of XCLK and that of the input data clock. Values above 2 kHz in the below graph are based on simulation results.

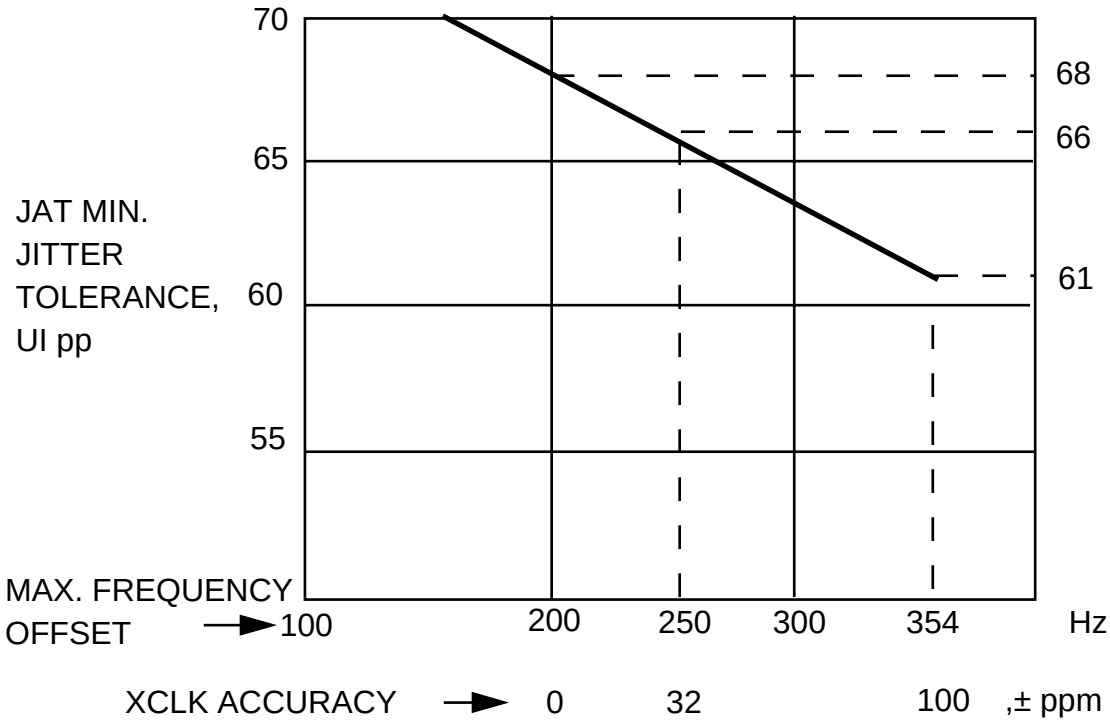
**Figure 9 - TJAT Jitter Tolerance**




The accuracy of the XCLK frequency and that of the TJAT PLL reference input clock used to generate the jitter-free TCLKO output have an effect on the minimum jitter tolerance. Given that the TJAT PLL reference clock accuracy can

be ±200 Hz and that the XCLK input accuracy can be ±100 ppm, the minimum jitter tolerance for various differences between the frequency of PLL reference clock and XCLK are shown in Figure 10.

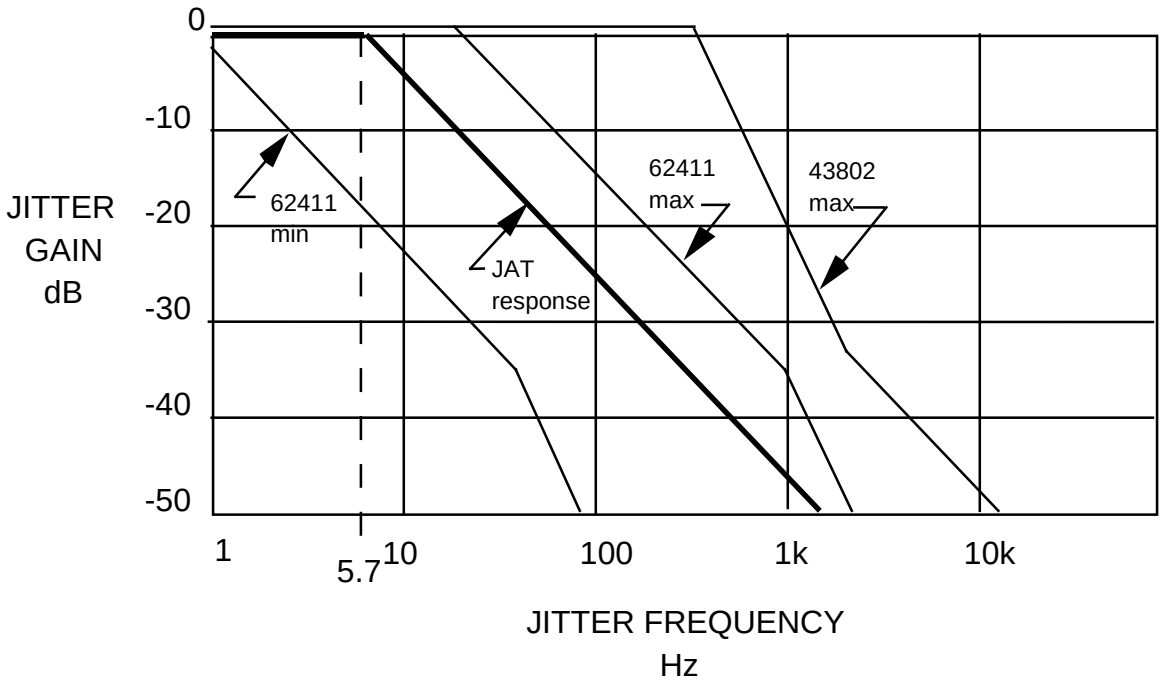
**Figure 10 - TJAT Minimum Jitter Tolerance vs. XCLK Accuracy**




### Jitter Transfer

For T1 applications, the output jitter for jitter frequencies from 0 to 5.7 Hz (7.6 Hz for E1) is no more than 0.1 dB greater than the input jitter, excluding residual jitter. Jitter frequencies above 5.7 Hz (7.6 Hz for E1) are attenuated at a level of 6 dB per octave, as shown in Figure 11.

**Figure 11 - TJAT Jitter Transfer**




**T1**

In the non-attenuating mode, when the FIFO is within one UI of overrunning or under running, the tracking range is 1.48 MHz to 1.608 MHz.

The guaranteed linear operating range for the jittered input clock is 1.544 MHz ± 200 Hz with worst case jitter (61 UIpp), and maximum system clock frequency offset (± 100 ppm). The nominal range is 1.544 MHz ± 963 Hz with no jitter or system clock frequency offset.

**E1**

In the non-attenuating mode, when the FIFO is within one UI of overrunning or under running, the tracking range is 2.13 MHz to 1.97 MHz.

The guaranteed linear operating range for the jittered input clock is 2.048 MHz ± 300 Hz with worst case jitter (61 UIpp), and maximum system clock frequency offset (± 100 ppm). The nominal range is 2.048 MHz ± 1277 Hz with no jitter or system clock frequency offset.

### Jitter Generation

In the absence of input jitter, the output jitter shall be less than 0.025 UIpp. This complies with the AT&T TR 62411 requirement of less than 0.025 UIpp of jitter generation.

## 9.27 Timing Options (TOPS)

The Timing Options block provides a means of selecting the source of the reference signal for the transmit digital PLL and the clock source used to derive the output TCLKO signal.

## 9.28 Line Transmitter

The line transmitter generates Alternate Mark Inversion (AMI) transmit pulses suitable for use in the DSX-1 (short haul T1), short haul E1, long haul T1 and long haul E1 environments. The voltage pulses are produced by applying a current to a known termination (termination resistor plus line impedance). The use of current (instead of a voltage driver) simplifies transmit Input Return Loss (IRL), transmit short circuit protection (none needed) and transmit tri-stating.

The output pulse shape is synthesized digitally with current digital-to-analog (DAC) converters which produce 24 samples per symbol. The current DAC's produce differential bipolar outputs that directly drive the TXTIP[1:0] and TXRING[1:0] pins. The current output is applied to a terminating resistor (optional) and line-coupling transformer in a differential manner, which when viewed from the line side of the transformer produce the output pulses at the required levels and insures a small positive to negative pulse imbalance.

The pulse shape is user programmable. For T1 short haul, the cable length between the TLONG and the cross-connect (where the pulse template specifications are given) greatly affects the resulting pulse shapes. Hence, the data applied to the converter must account for different cable lengths. For CEPT E1 applications the pulse template is specified at the transmitter, thus only one setting is required. For T1 long haul with a LBO of 7.5 dB the previous bits effect what the transmitter must drive to compensate for inter-symbol interference; for LBO's of 15 dB or 22.5 dB the previous 3 or 4 bits effect what the transmitter must send out.

Refer to the Operation section for details on creating the synthesized pulse shape.

## 9.29 Backplane Receive Interface (BRIF)

The Backplane Receive Interface allows data to be presented to a backplane in either a 1.544 Mbit/s, 2.048 Mbit/s, 4.096 Mbit/s, 8.192 Mbit/s or sub-rate NxDS0 serial stream.

All receive backplane signals are synchronous to BRCLK. BRCLK may be an output, in which case it is a jitter attenuated version of the recovered clock. If BRCLK is an input, it clocks the output of the frame slip buffer; therefore, it must be plesiochronous to the recovered clock.

When configured to provide a 1.544 Mbit/s data rate, the block generates the output data stream on the BRPCM pin containing 24 channel bytes of data followed by a single bit containing the framing bit or parity over the 24 channels. The BRSIG output pin contains 24 bytes of signaling nibble data located in the least significant nibble of each byte followed by a single bit position representing the "place holder" for the framing bit or parity over the 24 channels. The framing alignment indication on the BRFP pin indicates the first bit of the 193-bit frame (or, optionally, the first bit of every second frame, the first bit of the first frame of the superframe, or every second superframe). When BRFP is an input, the data read from the frame slip buffer is aligned to it.

In T1 mode, when configured to provide a 2.048 Mbit/s data rate, the block internally gaps the 2.048 MHz rate backplane clock to provide a serial PCM data on the BRPCM pin containing three channel bytes of data followed by one unused byte (can be logic 0 or logic 1). The signaling on the BRSIG pin is aligned to the least significant nibble of the associated channel on BRPCM. The frame alignment indication is provided on the BRFP pin, going high for one BRCLK cycle during the first bit of the unused byte, indicating the next data byte is the first channel of the frame, or the first channel of the first frame of the superframe. Alternatively, the PCM and signaling can be arranged in 24 contiguous timeslots, starting at the timeslot indicated by the BRFP pulse.

In E1 mode, the 2.048 Mbit/s data stream consumes all timeslots of BRPCM. The BRSIG output pin present 30 bytes of signaling nibble data located in the least significant nibble of each byte. The framing alignment indication on the BRFP output can be configured to indicate the first bit of each 256-bit frame, the first bit of every other 256-bit frame, the first bit of the first frame of the CRC multiframe, the first bit of the first frame of the signaling multiframe or all overhead bits. If BRFP is configured as an input, the BRPCM and BRSIG can be forced to an specific alignment provided the elastic store is used (the RXELSTBYP register bit is logic 0).

When configured for NxDS0 operation, no output clock edges are generated during the framing bit positions and idle channels.

As a programming option, the data stream bit and timeslot alignment relative to BRFP can be modified for Concentration Highway Interface (CHI) applications.

When configured for a multiplexed backplane, the two or four sets of PCM and signaling streams are byte-interleaved into a 4.096 Mbit/s or 8.192 Mbit/s serial stream.

## 9.30 Backplane Transmit Interface (BTIF)

The Backplane Transmit Interface allows data to be taken from a backplane in either a 1.544 Mbit/s, 2.048 Mbit/s, 4.096 Mbit/s, 8.192 Mbit/s or sub-rate NxDS0 serial stream.

When configured to receive a 1.544 Mbit/s data rate stream, the input data stream on the BTPCM pin to is expected to contain 24 channel bytes of data followed by a single bit location for the framing bit or optional parity over the previous 24 channels. The BTSIG input pin must contain 24 bytes of signaling nibble data located in the least significant nibble of each byte followed by a single bit position for the framing bit or optional parity over the previous frame. The framing alignment indication on the BTFP input must indicate the framing bit position of the 193-bit frame (or, optionally, the framing bit position of the first frame of the superframe).

In T1 mode, when configured to provide a 2.048 Mbit/s data rate, the block expects serial PCM data on the BTPCM pin to contain three channel bytes of data followed by one unused byte. The signaling on the BTSIG pin must be aligned to the least significant nibble of the associated channel on BTPCM. The frame alignment indication is expected on the BTFP pin, going to high during the first bit of the unused byte, indicating the next data byte is the first channel of the frame. Alternatively, the PCM and signaling can be arranged in 24 contiguous timeslots, starting at the timeslot indicated by the BTFP pulse.

In E1 mode, the 2.048 Mbit/s data stream consumes all timeslots of BRPCM. The BTSIG input presents 30 bytes of signaling nibble data located in the least significant nibble of each timeslot. The framing alignment indication on the BTFP pin can be configured to indicate the first bit of each 256-bit frame or the first bit of the first frame of the CRC multiframe and signaling multiframes.

BTCLK can be configured as an output, in which case, BTCLK is generated from TCLKO. When configured for NxDS0 operation, no output clock edges are generated during the framing bit positions and idle channels.

BTFP can be configured as an output, in which case, the COMET dictates the frame alignment.

As a programming option, the data stream bit and timeslot alignment relative to BTFP can be modified for Concentration Highway Interface (CHI) applications.

When configured for a multiplexed backplane, one of two or four sets of PCM and signaling streams are extracted from the byte-interleaved 4.096 Mbit/s or 8.192 Mbit/s serial stream.

## 9.31 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The COMET revision E identification code is 443510CD hexadecimal. The revision F code is 543510CD.

## 9.32 Microprocessor Interface (MPIF)

The Microprocessor Interface allows the COMET to be configured, controlled and monitored via internal registers.

# 10 REGISTER DESCRIPTION

## 10.1 Normal Mode Register Memory Map

**Table 16 - Normal Mode Register Memory Map**

| Addr | Register |
|---|---|
| 000H | Global Configuration |
| 001H | Clock Monitor |
| 002H | Receive Options |
| 003H | Receive Line Interface Configuration |
| 004H | Transmit Line Interface Configuration |
| 005H | Transmit Framing and Bypass Options |
| 006H | Transmit Timing Options |
| 007H | Interrupt Source #1 |
| 008H | Interrupt Source #2 |
| 009H | Interrupt Source #3 |
| 00AH | Master Diagnostics |
| 00BH | Master Test |
| 00CH | Analog Diagnostics |
| 00DH | Revision/Chip ID/Global PMON Update |
| 00EH | Reset |
| 00FH | PRGD Positioning/Control and HDLC Control |
| 010H | CDRC Configuration |
| 011H | CDRC Interrupt Enable |
| 012H | CDRC Interrupt Status |
| 013H | CDRC Alternate Loss of Signal |
| 014H | RJAT Interrupt Status |
| 015H | RJAT Reference Clock Divisor (N1) Control |
| 016H | RJAT Output Clock Divisor (N2) Control |
| 017H | RJAT Configuration |

| Addr | Register |
|---|---|
| 018H | TJAT Interrupt Status |
| 019H | TJAT Reference Clock Divisor (N1) Control |
| 01AH | TJAT Output Clock Divisor (N2) Control |
| 01BH | TJAT Configuration |
| 01CH | RX-ELST Configuration |
| 01DH | RX-ELST Interrupt Enable/Status |
| 01EH | RX-ELST Idle Code |
| 01FH | RX-ELST Reserved |
| 020H | TX-ELST Configuration |
| 021H | TX-ELST Interrupt Enable/Status |
| 022H-023H | TX-ELST Reserved |
| 024H-027H | Reserved |
| 028H | RXCE Receive Data Link 1 Control |
| 029H | RXCE Receive Data Link 1 Bit Select |
| 02AH | RXCE Receive Data Link 2 Control |
| 02BH | RXCE Receive Data Link 2 Bit Select |
| 02CH | RXCE Receive Data Link 3 Control |
| 02DH | RXCE Receive Data Link 3 Bit Select |
| 02EH-02FH | RXCE Reserved |
| 030H | BRIF Receive Backplane Configuration |
| 031H | BRIF Receive Backplane Frame Pulse Configuration |
| 032H | BRIF Receive Backplane Parity/F-Bit Configuration |
| 033H | BRIF Receive Backplane Time Slot Offset |
| 034H | BRIF Receive Backplane Bit Offset |
| 035H-037H | BRIF Receive Backplane Reserved |
| 038H | TXCI Transmit Data Link 1 Control |
| 039H | TXCI Transmit Data Link 1 Bit Select |
| 03AH | TXCI Transmit Data Link 2 Control |
| 03BH | TXCI Transmit Data Link 2 Bit Select |

| Addr | Register |
|---|---|
| 03CH | TXCI Transmit Data Link 3 Control |
| 03DH | TXCI Transmit Data Link 3 Bit Select |
| 03EH-03FH | TXCI Reserved |
| 040H | BTIF Transmit Backplane Configuration |
| 041H | BTIF Transmit Backplane Frame Pulse Configuration |
| 042H | BTIF Transmit Backplane Parity Configuration and Status |
| 043H | BTIF Transmit Backplane Time Slot Offset |
| 044H | BTIF Transmit Backplane Bit Offset Register |
| 045H | BTIF Transmit Backplane Reserved |
| 046H | BTIF Transmit Backplane Reserved |
| 047H | BTIF Transmit Backplane Reserved |
| 048H | T1 FRMR Configuration |
| 049H | T1 FRMR Interrupt Enable |
| 04AH | T1 FRMR Interrupt Status |
| 04BH | Reserved |
| 04CH | IBCD Configuration |
| 04DH | IBCD Interrupt Enable/Status |
| 04EH | IBCD Activate Code |
| 04FH | IBCD Deactivate Code |
| 050H | SIGX Configuration/Change of Signaling State |
| 051H | SIGX µP Access Status/Change of Signaling State |
| 052H | SIGX Channel Indirect Address/Control/ Change of Signaling State |
| 053H | SIGX Channel Indirect Data Buffer/Change of Signaling State |
| 054H | T1 XBAS Configuration |
| 055H | T1 XBAS Alarm Transmit |
| 056H | T1 XIBC Control |
| 057H | T1 XIBC Loopback Code |
| 058H | PMON Interrupt Enable/Status |

| Addr | Register |
|---|---|
| 059H | PMON Framing Bit Error Count |
| 05AH | PMON OOF/COFA/Far End Block Error Count (LSB) |
| 05BH | PMON OOF/COFA/Far End Block Error Count (MSB) |
| 05CH | PMON Bit Error/CRCE Count (LSB) |
| 05DH | PMON Bit Error/CRCE Count (MSB) |
| 05EH | PMON LCV Count (LSB) |
| 05FH | PMON LCV Count (MSB) |
| 060H | T1 ALMI Configuration |
| 061H | T1 ALMI Interrupt Enable |
| 062H | T1 ALMI Interrupt Status |
| 063H | T1 ALMI Alarm Detection Status |
| 064H | T1 PDVD Reserved |
| 065H | T1 PDVD Interrupt Enable/Status |
| 066H | T1 XBOC Reserved |
| 067H | T1 XBOC Code |
| 068H | T1 XPDE Reserved |
| 069H | T1 XPDE Interrupt Enable/Status |
| 06AH | T1 RBOC Enable |
| 06BH | T1 RBOC Code Status |
| 06CH | TPSC Configuration |
| 06DH | TPSC µP Access Status |
| 06EH | TPSC Channel Indirect Address/Control |
| 06FH | TPSC Channel Indirect Data Buffer |
| 070H | RPSC Configuration |
| 071H | RPSC µP Access Status |
| 072H | RPSC Channel Indirect Address/Control |
| 073H | RPSC Channel Indirect Data Buffer |
| 074H-077H | Reserved |
| 078H | T1 APRM Configuration/Control |

| Addr | Register |
|---|---|
| 079H | T1 APRM Manual Load |
| 07AH | T1 APRM Interrupt Status |
| 07BH | T1 APRM One Second Content Octet 2 |
| 07CH | T1 APRM One Second Content Octet 3 |
| 07DH | T1 APRM One Second Content Octet 4 |
| 07EH | T1 APRM One Second Content MSB (Octet 5) |
| 07FH | T1 APRM One Second Content LSB (Octet 6) |
| 080H | E1 TRAN Configuration |
| 081H | E1 TRAN Transmit Alarm/Diagnostic Control |
| 082H | E1 TRAN International Control |
| 083H | E1 TRAN Extra Bits Control |
| 084H | E1 TRAN Interrupt Enable |
| 085H | E1 TRAN Interrupt Status |
| 086H | E1 TRAN National Bit Codeword Select |
| 087H | E1 TRAN National Bit Codeword |
| 088H-08BH | Reserved |
| 08CH | T1 FRMR Reserved |
| 08DH | T1 FRMR Reserved |
| 08EH | Reserved |
| 08FH | Reserved |
| 090H | E1 FRMR Frame Alignment Options |
| 091H | E1 FRMR Maintenance Mode Options |
| 092H | E1 FRMR Framing Status Interrupt Enable |
| 093H | E1 FRMR Maintenance/Alarm Status Interrupt Enable |
| 094H | E1 FRMR Framing Status Interrupt Indication |
| 095H | E1 FRMR Maintenance/Alarm Status Interrupt Indication |
| 096H | E1 FRMR Framing Status |
| 097H | E1 FRMR Maintenance/Alarm Status |
| 098H | E1 FRMR International/National Bits |

| Addr | Register |
|---|---|
| 099H | E1 FRMR CRC Error Count - LSB |
| 09AH | E1 FRMR CRC Error Count - MSB |
| 09BH | E1 FRMR National Bit Codeword Interrupt Enables |
| 09CH | E1 FRMR National Bit Codeword Interrupts |
| 09DH | E1 FRMR National Bit Codewords |
| 09EH | E1 FRMR Frame Pulse/Alarm Interrupt Enables |
| 09FH | E1 FRMR Frame Pulse/Alarm Interrupt |
| 0A0H-0A7H | Reserved |
| 0A8H | TDPR #1 Configuration |
| 0A9H | TDPR #1 Upper Transmit Threshold |
| 0AAH | TDPR #1 Lower Transmit Threshold |
| 0ABH | TDPR #1 Interrupt Enable |
| 0ACH | TDPR #1 Interrupt Status/UDR Clear |
| 0ADH | TDPR #1 Transmit Data |
| 0AEH | Reserved |
| 0AFH | Reserved |
| 0B0H | TDPR #2 Configuration |
| 0B1H | TDPR #2 Upper Transmit Threshold |
| 0B2H | TDPR #2 Lower Transmit Threshold |
| 0B3H | TDPR #2 Interrupt Enable |
| 0B4H | TDPR #2 Interrupt Status/UDR Clear |
| 0B5H | TDPR #2 Transmit Data |
| 0B6H | Reserved |
| 0B7H | Reserved |
| 0B8H | TDPR #3 Configuration |
| 0B9H | TDPR #3 Upper Transmit Threshold |
| 0BAH | TDPR #3 Lower Transmit Threshold |
| 0BBH | TDPR #3 Interrupt Enable |
| 0BCH | TDPR #3 Interrupt Status/UDR Clear |

| Addr | Register |
|---|---|
| 0BDH | TDPR #3 Transmit Data |
| 0BEH | Reserved |
| 0BFH | Reserved |
| 0C0H | RDLC #1 Configuration |
| 0C1H | RDLC #1 Interrupt Control |
| 0C2H | RDLC #1 Status |
| 0C3H | RDLC #1 Data |
| 0C4H | RDLC #1 Primary Address Match |
| 0C5H | RDLC #1 Secondary Address Match |
| 0C6H | Reserved |
| 0C7H | Reserved |
| 0C8H | RDLC #2 Configuration |
| 0C9H | RDLC #2 Interrupt Control |
| 0CAH | RDLC #2 Status |
| 0CBH | RDLC #2 Data |
| 0CCH | RDLC #2 Primary Address Match |
| 0CDH | RDLC #2 Secondary Address Match |
| 0CEH | Reserved |
| 0CFH | Reserved |
| 0D0H | RDLC #3 Configuration |
| 0D1H | RDLC #3 Interrupt Control |
| 0D2H | RDLC #3 Status |
| 0D3H | RDLC #3 Data |
| 0D4H | RDLC #3 Primary Address Match |
| 0D5H | RDLC #3 Secondary Address Match |
| 0D6H | CSU Configuration |
| 0D7H | CSU Reserved |
| 0D8H | RLPS Indirect Data Register |
| 0D9H | RLPS Indirect Data Register |

| Addr | Register |
|---|---|
| 0DAH | RLPS Indirect Data Register |
| 0DBH | RLPS Indirect Data Register |
| 0DCH | RLPS Equalizer Voltage Reference |
| 0DDH-0DFH | RLPS Reserved |
| 0E0H | PRGD Control |
| 0E1H | PRGD Interrupt Enable/Status |
| 0E2H | PRGD Shift Register Length |
| 0E3H | PRGD Tap |
| 0E4H | PRGD Error Insertion |
| 0E5H | PRGD Reserved |
| 0E6H | PRGD Reserved |
| 0E7H | PRGD Reserved |
| 0E8H | PRGD Pattern Insertion #1 |
| 0E9H | PRGD Pattern Insertion #2 |
| 0EAH | PRGD Pattern Insertion #3 |
| 0EBH | PRGD Pattern Insertion #4 |
| 0ECH | PRGD Pattern Detector #1 |
| 0EDH | PRGD Pattern Detector #2 |
| 0EEH | PRGD Pattern Detector #3 |
| 0EFH | PRGD Pattern Detector #4 |
| 0F0H | XLPG Line Driver Configuration |
| 0F1H | XLPG Control/Status |
| 0F2H | XLPG Pulse Waveform Storage Write Address |
| 0F3H | XLPG Pulse Waveform Storage Data |
| 0F4H | XLPG Analog Test Positive Control |
| 0F5H | XLPG Analog Test Negative Control |
| 0F6H | XLPG Fuse Data Select |
| 0F7H | XLPG Reserved |
| 0F8H | RLPS Configuration and Status |

| Addr | Register |
|---|---|
| 0F9H | RLPS ALOS Detection/Clearance Threshold |
| 0FAH | RLPS ALOS Detection Period |
| 0FBH | RLPS ALOS Clearance Period |
| 0FCH | RLPS Equalization Indirect Address |
| 0FDH | RLPS Equalization Read/WriteB Select |
| 0FEH | RLPS Equalizer Loop Status and Control |
| 0FFH | RLPS Equalizer Configuration |
| 100H-1FFH | Reserved for Test |

# 11 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the COMET. Normal mode registers (as opposed to test mode registers) are selected when A[8] is low.

**Notes on Normal Mode Register Bits:**

1. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the COMET to determine the programming state of the chip.

3. Writeable normal mode register bits are cleared to zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect COMET operation unless otherwise noted.

### Register 000H: Global Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | PIO_OE | 1 |
| Bit 6 | R/W | PIO | 0 |
| Bit 5 | R/W | IBCD_IDLE | 0 |
| Bit 4 | R/W | RSYNC_ALOSB | 0 |
| Bit 3 | R/W | OOSMFAIS | 0 |
| Bit 2 | R/W | TRKEN | 0 |
| Bit 1 | R/W | RXMTKC | 0 |
| Bit 0 | R/W | E1/T1B | 0 |

PIO_OE:

The programmable I/O output enable, PIO_OE, bit controls the PIO pin. When PIO_OE is logic 1, the PIO pin is configured as an output and driven by the COMET. When PIO_OE is logic 0, the PIO pin is configured as an input. Upon reset, the PIO pin is configured as an output.

PIO:

The programmable I/O, PIO, bit controls/reflects the state of the PIO pin. When the PIO pin is configured as an output, the PIO bit controls the state of the PIO pin. When the PIO pin is configured as an input, the PIO bit reflects the state of the PIO pin. Upon reset, the PIO pin has an output value of logic 0.

OOSMFAIS:

In E1 mode, this bit controls the receive backplane signaling trunk conditioning in an out of signaling multiframe condition. If OOSMFAIS is set to a logic 0, an OOSMF indication from the E1-FRMR does not affect the BRSIG output. When OOSMFAIS is a logic 1, an OOSMF indication from the E1-FRMR will cause the BRSIG output to be set to all 1's.

RSYNC_ALOSB:

The RSYNC_ALOSB bit controls the source of the loss of signal condition used to control the behaviour of the receive reference presented on the RSYNC. If RSYNC_ALOSB is a logic 0, analog loss of signal is used. If RSYNC_ALOSB is a logic 1, digital loss of signal is used. When COMET is in a loss of signal state, the RSYNC output is derived from XCLK. When

COMET is not in a loss of signal state, the RSYNC output is derived from the recovered receiver clock.

IBCD_IDLE:

When the IBCD_IDLE bit is set to logic 1 gaps the data to the inband code detector (IBCD) block during the framing bit. This allows the IBCD to be used to detect an idle code that is inserted only in the payload of the receive DS1 PCM stream. The IBCD must still be programmed to detect the desired pattern, and otherwise operates unchanged. The IBCD_IDLE bit is only valid in T1 mode.

TRKEN:

The TRKEN bit enables receive trunk conditioning upon an out-of-frame condition. If TRKEN is logic 1, the contents of the RX-ELST Idle Code register are inserted into all time slots (including TS0 and TS16) of BRPCM if the framer is out-of-basic frame (i.e. the OOF status bit is logic 1). The TRKEN bit only has effect if RXELSTBYP bit is logic 0. If TRKEN is a logic 0, receive trunk conditioning can still be performed on a per-timeslot basis via the RPSC Data Trunk Conditioning and Signaling Trunk Conditioning registers.

RXMTKC:

The RXMTKC bit allows global trunk conditioning to be applied to the received data and signaling streams, BRPCM and BRSIG. When RXMTKC is set to logic 1, the data on BRPCM for each channel is replaced with the data contained in the data trunk conditioning registers within RPSC; similarly, the signaling data on BRSIG for each channel is replaced with the data contained in the signaling trunk conditioning registers. When RXMTKC is set to logic 0, the data and signaling signals are modified on a per-channel basis in accordance with the control bits contained in the per-channel control registers within the RPSC.

E1/T1B:

The E1/T1B bit selects the operating mode of COMET. If E1/T1B is logic 1, the 2.048 Mbit/s E1 mode is selected. If E1/T1B is logic 0, the 1.544 Mbit/s T1 mode is selected.

### Register 001H: Clock Monitor

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R | XCLKA | X |
| Bit 3 | R | BTCLKA | X |
| Bit 2 | R | TCLKIA | X |
| Bit 1 | R | BRCLKA | X |
| Bit 0 | R | RCLKIA | X |

When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

BTCLKA:

The BTCLK active (BTCLKA) bit detects low to high transitions on the BTCLK input. BTCLKA is set high on a rising edge of BTCLK, and is set low when this register is read.

TCLKIA:

The TCLKI active (TCLKIA) bit detects low to high transitions on the TCLKI input. TCLKIA is set high on a rising edge of TCLKI, and is set low when this register is read.

BRCLKA:

The BRCLK active (BRCLKA) bit detects low to high transitions on the BRCLK input. BRCLKA is set high on a rising edge of BRCLK, and is set low when this register is read.

RCLKIA:

The RCLKI active (RCLKA) bit detects low to high transitions on the RCLKI input. RCLKIA is set high on a rising edge of RCLKI, and is set low when this register is read.

XCLKA:

The XCLK active (XCLKA) bit detects for low to high transitions on the XCLK input. XCLKA is set high on a rising edge of XCLK, and is set low when this register is read.

### Register 002H: Receive Options

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | RJATBYP | 1 |
| Bit 6 | R/W | UNF | 0 |
| Bit 5 | R/W | RXELSTBYP | 0 |
| Bit 4 | R/W | RSYNC_MEM | 0 |
| Bit 3 | R/W | RSYNCSEL | 0 |
| Bit 2 | R/W | WORDERR | 0 |
| Bit 1 | R/W | CNTNFAS | 0 |
| Bit 0 | R/W | CCOFA | 0 |

This register allows software to configure the receive functions of each framer.

RJATBYP:

The RJATBYP bit disables jitter attenuation in the receive direction. When receive jitter attenuation is not being used, setting RJATBYP to logic 1 will reduce the latency through the receiver section by typically 40 bits. When RJATBYP is set to logic 0, the RSYNC output and the BRCLK output (if BRCLK is configured to be an output by setting the CMODE bit of the Receive Backplane Configuration register to logic 0), are jitter attenuated. When the RJAT is bypassed, RSYNC and BRCLK are not jitter attenuated.

UNF:

The UNF bit allows the framer to operate with unframed DS-1 or E1 data. When UNF is set to logic 1, the framer is disabled (both the T1-FRMR and E1-FRMR are held reset) and the recovered data passes through the receiver section of the framer without frame or channel alignment. While UNF is set to logic 1, the Alarm Integrator continues to operate and detects and integrates AIS alarm. When UNF is set to logic 0, the framer operates normally, searching for frame alignment on the incoming data.

When UNF is a logic 1, the BRFP pin (if configured as an output) is held low.

RXELSTBYP:

The RXELSTBYP bit allows the Receive Elastic Store (RX-ELST) to be bypassed, eliminating the one frame delay incurred through the RX-ELST. When set to logic 1, the received data and clock inputs to RX-ELST are internally routed directly to the RX-ELST output.

If RXELSTBYP is logic 1, the CMODE bit of the Receive Backplane Configuration register must be logic 0 and the FPMODE bit of the Receive Backplane Frame Pulse Configuration register must be logic 0.

RSYNC_MEM:

The RSYNC_MEM bit controls the RSYNC output under a loss of signal condition (as determined by the RSYNC_ALOSB register bit). When RSYNC_MEM is a logic 1, the RSYNC output is held high during a loss of signal condition. When RSYNC_MEM is a logic 0, the RSYNC output is derived from XCLK during a loss of signal condition.

RSYNCSEL:

The RSYNCSEL bit selects the frequency of the receive reference presented on the RSYNC output. If RSYNCSEL is a logic 1, RSYNC will be an 8 kHz clock. If RSYNCSEL is a logic 0, RSYNC will be an 1.544 MHz (T1) or 2.048 MHz (E1) clock.

WORDERR:

In E1 mode, the WORDERR bit determines how frame alignment signal (FAS) errors are reported. When WORDERR is logic 1, one or more errors in the seven bit FAS word results in a single framing error count. When WORDERR is logic 0, each error in a FAS word results in a single framing error count.

CNTNFAS:

In E1 mode, when the CNTNFAS bit is a logic 1, a zero in bit 2 of time slot 0 of non-frame alignment signal (NFAS) frames results in an increment of the framing error count. If WORDERR is also a logic 1, the word is defined as the eight bits consisting of the seven-bit FAS pattern and bit 2 of time slot 0 of the next NFAS frame. When the CNTNFAS bit is a logic 0, only errors in the FAS affect the framing error count.

CCOFA

The CCOFA bit determines whether the PMON counts Change-Of-Frame Alignment (COFA) events or out-of-frame (OOF ) events. When CCOFA is set to logic 1, COFA events are counted by PMON. When CCOFA is set to logic 0, OOF events are counted by PMON. The CCOFA bit is only valid in T1 mode.

### Register 003H: Receive Line Interface Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | AUTOYELLOW | 0 |
| Bit 6 | R/W | AUTORED | 0 |
| Bit 5 | R/W | AUTOOOF | 0 |
| Bit 4 | R/W | AUTOAIS | 0 |
| Bit 3 | R/W | RUNI | 0 |
| Bit 2 | R/W | BPV | 0 |
| Bit 1 | R/W | RDATINV | 0 |
| Bit 0 | R/W | RFALL | 0 |

AUTOYELLOW:

In T1 mode, when the AUTOYELLOW bit is set to logic 1, whenever the alarm integrator declares a Red alarm in the receive direction, Yellow alarm will be transmitted to the far end. When AUTOYELLOW is set to logic 0, Yellow alarm will only be transmitted when the XYEL bit is set in the T1-XBAS Alarm Transmit Register. Note that the Red alarm is not deasserted on detection of AIS.

In E1 mode, when the AUTOYELLOW bit is set to logic 1, The RAI bit in the transmit stream is set to a logic 1 for the duration of a loss of frame alignment or AIS. The G706ANNBRAI bit of the Transmit Framing and Bypass Options register optionally also allows for the transmission of RAI when CRC-to-non-CRC interworking has been established. When AUTOYELLOW is set to logic 0, RAI will only be transmitted when the RAI bit is set in the E1-TRAN Transmit Alarm/Diagnostic Control register.

AUTORED:

The AUTORED bit allows global trunk conditioning to be applied to the receive data and signaling streams, BRPCM and BRSIG, immediately upon declaration of Red carrier failure alarm. When AUTORED is set to logic 1, the data on BRPCM for each channel is replaced with the data contained in the Data Trunk Conditioning registers within RPSC and the data on BRSIG for each channel is replaced with the data contained in the Signaling Trunk Conditioning registers within the RPSC while Red CFA is declared. When AUTORED is set to logic 0, the receive data is not automatically conditioned when Red CFA is declared.

AUTOOOF:

The AUTOOOF bit allows global trunk conditioning to be applied to the receive data stream, BRPCM, immediately upon declaration of out of frame (OOF). When AUTOOOF is set to logic 1, while OOF is declared, the data on BRPCM for each channel is replaced with the data contained in the data trunk conditioning registers within RPSC. When AUTOOOF is set to logic 0, the ingress data is not automatically conditioned by RPSC when OOF is declared. However, if the RX-ELST is not bypassed, the RX-ELST trouble code will still be inserted in channel data while OOF is declared if the TRKEN register bit is logic 1. RPSC data and signaling trunk conditioning overwrites the RX-ELST trouble code.

AUTOAIS:

If the AUTOAIS bit is logic 1, AIS is inserted in the receive path and the signaling is frozen for the duration of a loss of signal condition. If AUTOAIS is logic 0, AIS may be inserted manually via the RAIS register bit.

RUNI:

The RUNI bit selects the source of receive data. If RUNI is a logic 1, the receive data stream and clock are expected to be presented on the RDAT and RCLKI inputs, respectively.

If RUNI is a logic 0, the receive data and clock will be recovered from the analog RXTIP and RXRING inputs. These inputs will typically be connected to a signal transformer and may exhibit the attenuation and dispersion characteristics of short or long haul lines.

BPV:

In T1 mode, the BPV bit enables only bipolar violations to indicate line code violations and be accumulated in the PMON LCV Count Registers. When BPV is set to logic 1, BPVs (which are not part of a valid B8ZS signature if B8ZS line coding is used) generate an LCV indication and increment the PMON LCV counter. When BPV is set to logic 0, both BPVs (which are not part of a valid B8ZS signature if B8ZS line coding is used) and excessive zeros (EXZ) generate an LCV indication and increment the PMON LCV counter. Excessive zeros is a sequence of zeros greater than fifteen bits long for an AMI-coded signal and greater than seven bits long for a B8ZS-coded signal.

In E1 mode, the BPV bit enables only bipolar violations to indicate line code violations and be accumulated in the PMON LCV Count Registers. (The O162 bit in the CDRC Configuration register provides two E1 LCV definitions.) When BPV is set to logic 1, BPVs (which are not part of a valid HDB3 signature if HDB3 line coding is used) generate an LCV indication and

increment the PMON LCV counter. When BPV is set to logic 0, both BPVs (which are not part of a valid HDB3 signature if HDB3 line coding is used) and excessive zeros (EXZ) generate an LCV indication and increment the PMON LCV counter. Excessive zeros is a sequence of zeros greater than four bits long.

RDATINV:

When RDATINV is set to logic 1, the receive digital interface assumes the RDAT input is active low. When RDATINV is set to logic 0, the interface assumes the RDAT input is active high.

This bit only has effect if the RUNI bit is logic 1.

RFALL:

When RFALL is set to logic 1, the RDAT signal is sampled by the falling RCLKI edge. When RFALL is set to logic 0, the RDAT signal is sampled by the rising RCLKI edge.

This bit only has effect if the RUNI bit is logic 1.

### Register 004H: Transmit Line Interface Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | TJATBYP | 0 |
| Bit 6 | R/W | TAISEN | 0 |
| Bit 5 | R/W | TAUXP | 0 |
| Bit 4 | R/W | TDATINV | 0 |
| Bit 3 | R/W | TUNI | 0 |
| Bit 2 | | Unused | X |
| Bit 1 | R/W | TRISE | 0 |
| Bit 0 | | Unused | X |

This register enables the transmit interface to generate the required digital output waveform format.

TJATBYP:

The TJATBYP bit enables the transmit jitter attenuator's FIFO to be removed from the transmit data path. When transmit jitter attenuation is not being used, setting TJATBYP to logic 1 will reduce the latency through the transmitter section by typically 40 bits.

TAISEN:

The TAISEN bit enables the interface to generate an unframed all-ones AIS alarm on the TXTIP, TXRING and TDAT pins. When TAISEN is set to logic 1 and TUNI is set to logic 0, the bipolar TXTIP and TXRING outputs are forced to pulse alternately, creating an all-ones signal; when TAISEN and TUNI are both set to logic 1, the unipolar TDAT output is forced to all-ones. The transition to transmitting AIS on the TXTIP and TXRING outputs is done in such a way as to not introduce any bipolar violations.

The TAISEN bit only takes effect when the AISE bit of the XLPG Control/Status register is logic 1.

The diagnostic loopback point is upstream of this AIS insertion point.

TAUXP:

The TAUXP bit enables the interface to generate an unframed alternating zeros and ones (i.e. 010101...) auxiliary pattern (AUXP) on the TXTIP, TXRING and TDAT pins. When TAUXP is set to logic 1 and TUNI is set to

logic 0, the bipolar TXTIP and TXRING outputs are forced to pulse alternately every other cycle; when TAUXP and TUNI are both set to logic 1, the unipolar TDAT output is forced to toggle every cycle. The transition to transmitting AUXP on the TXTIP and TXRING outputs is done in such a way as to not introduce any bipolar violations.

The diagnostic loopback point is upstream of this AUXP insertion point.

TDATINV:

The TDATINV bit enables the digital transmit interface to logically invert the TDAT signal. When TDATINV is set to logic 1, the TDAT output is active low. When TDATINV is set to logic 0, the TDAT output is active high.

TDATINV only has effect when TUNI is a logic 1.

TUNI:

The TUNI bit determines which interface presents the transmit data.

If TUNI is a logic 1, the transmit data is presented as TTL compatible unipolar data on the TDAT output with an associated clock on the TCLKO output and frame alignment pulse on the TFP output. The transmit line interface is held reset; therefore, the TXTIP and TXRING outputs are high-impedance.
If TUNI is a logic 0, the transmit data is presented on the TXTIP and TXRING as pulses suitable for driving a transformer directly and the TDAT, TFP and TCLKO outputs are held low.

TRISE:

When TRISE is set to logic 1, the interface is enabled to update the TDAT and TFP output pins on the rising edge of TCLKO. When TRISE is set to logic 0, the interface is enabled to update the outputs on the falling edge of TCLKO.

### Register 005H: Transmit Framing and Bypass Options

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | PATHCRC | 0 |
| Bit 6 | R/W | G706ANNBRAI | 0 |
| Bit 5 | R/W | SIGAEN | 0 |
| Bit 4 | R/W | OOCMFE0 | 0 |
| Bit 3 | R/W | FDIS | 0 |
| Bit 2 | R/W | FBITBYP | 0 |
| Bit 1 | R/W | CRCBYP | 0 |
| Bit 0 | R/W | FDLBYP | 0 |

This register allows software to configure the bypass and framing options of the transmitter, the use of the Signaling Alignment block, and controls the global transmit framing disable.

PATHCRC:

This bit only has effect in E1 mode.

When in E1 mode, the PATHCRC bit allows upstream block errors to be preserved in the transmit CRC bits. If PATHCRC is a logic 1, the CRC-4 bits are modified to reflect any bit values in BTPCM which have changed prior to transmission. When PATHCRC is set to logic 0, a new CRC-4 value overwrites the incoming CRC-4 word. For the PATHCRC bit to be effective, the FPTYP bit of the Transmit Backplane Frame Pulse Configuration register must be a logic 1; otherwise, the identification of the incoming CRC-4 bits would be impossible. The PATHCRC bit only takes effect if the GENCRC bit of the E1-TRAN Configuration register is a logic 1 and either the INDIS or FDIS bit in the same register are set to logic 1.

G706ANNBRAI:

When in E1 mode, the G.706 Annex B RAI bit, G706ANNBRAI, selects between two modes of operation concerning the transmission of RAI when the COMET is out of CRC-4 multiframe. When G706ANNBRAI is logic 1, the behaviour of RAI follows Annex B of G.706, i.e., RAI is transmitted only when out of basic frame, not when CRC-4-to-non-CRC-4 interworking is declared, nor when the offline framer is out of frame. When G706ANNBRAI is logic 0, the behaviour of RAI follows ETSI standards, i.e., RAI is transmitted when out

of basic frame, when CRC-4-to-non-CRC-4 interworking is declared, and when the offline framer is out of frame.

This bit only has effect in E1 mode.

SIGAEN:

The SIGAEN bit enables the operation of the signaling aligner (SIGA) to ensure superframe alignment of signaling bits between the backplane and the transmit DS-1 stream. When set to logic 1, the SIGA is inserted into the signaling bit data path before the T1-XBAS. When the signaling aligner is used, the backplane frame alignment indication must also be changed to indicate superframe alignment for the transmit backplane. When SIGAEN is set to logic 0, the SIGA is removed from the circuit. It is recommended that SIGAEN be set to logic 1 in T1 mode.

This bit has no effect in E1 mode.

OOCMFE0:

When in E1 mode, the OOCMFE0 bit selects between two modes of operation concerning the transmission of E-bits when the COMET is out of CRC-4 multiframe. When OOCMFE0 is logic 0, the COMET transmits ones for the E-bits while out of CRC-4 multiframe. When OOCMFE0 is logic 1, the COMET transmits zeroes for the E-bits while out of CRC-4 multiframe. The option to transmit zeroes as E-bits while out of CRC-4 multiframe is provided to allow compliance with the CRC-4 to non-CRC-4 interworking procedure in Annex B of G.706.

This bit only has effect in E1 mode.

FDIS:

The FDIS bit allows the framing generation through the transmitter to be disabled and the transmit data to pass through the transmitter unchanged. When FDIS is set to logic 1, the transmitter is disabled from generating framing. When FDIS is set to logic 0, the transmitter is enabled to generate and insert the framing into the transmit data.

FBITBYP:

The FBITBYP bit allows the frame synchronization bit in the input data stream, BTPCM, to bypass the generation through the XBAS and be re-inserted into the appropriate position in the digital output stream. When FBITBYP is set to logic 1, the input frame synchronization bit is re-inserted into the output data stream. When FBITBYP is set to logic 0, the XBAS is allowed to generate the output frame synchronization bits.

This bit must be set to logic 0 when not in T1 ESF mode.

CRCBYP:

In T1 mode, when the CRCBYP bit is a logic 1, the framing bit corresponding to the CRC-6 bit position in the input data stream, BTPCM, passes transparently to the transmit output data stream. When CRCBYP is set to logic 0, the XBAS is allowed to generate the output CRC-6 bits.

This bit must be set to logic 0 when not in T1 ESF mode.

FDLBYP:

In T1 mode, when the FDLBYP bit is a logic 1, the framing bit corresponding to the facility data link bit position in the input data stream, BTPCM, passes transparently to the transmit output data stream. When FDLBYP is set to logic 0, the XBAS is allowed to generate the output facility data link.

This bit must be set to logic 0 when not in T1 ESF mode.

### Register 006H: Transmit Timing Options

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | R/W | OCLKSEL1 | 0 |
| Bit 4 | R/W | OCLKSEL0 | 0 |
| Bit 3 | R/W | PLLREF1 | 0 |
| Bit 2 | R/W | PLLREF0 | 0 |
| Bit 1 | | Unused | X |
| Bit 0 | R/W | TXELSTBYP | 1 |

This register allows software to configure the options of the transmit timing section.

TXELSTBYP:

The TXELSTBYP bit allows the Transmit Elastic Store (TX-ELST) to be bypassed, eliminating the one frame delay incurred through the TX-ELST. When set to logic 1, the received data and clock inputs to TX-ELST are internally routed directly to the TX-ELST outputs.

OCLKSEL1, OCLKSEL0:

The OCLKSEL[1:0] bits select the source of the Transmit Jitter Attenuator FIFO output clock signal.

**Table 17 - TJAT FIFO Output Clock Source**

| OCLKSEL1 | OCLKSEL0 | Source of FIFO Output Clock |
|---|---|---|
| 0 | 0 | The TJAT FIFO output clock is driven with the internal jitter-attenuated 1.544 MHz or 2.048 MHz clock. |
| 0 | 1 | The TJAT FIFO output clock is driven with the TCLKI input clock. In this mode, PLLREF[1:0] must be programmed to ‘b11. |

| OCLKSEL1 | OCLKSEL0 | Source of FIFO Output Clock |
|---|---|---|
| 1 | X | The TJAT FIFO output clock is driven with the FIFO input clock. In this mode the jitter attenuation is disabled and the input clock must be jitter-free. In this mode, PLLREF[1:0] must be programmed to 'b00. |

PLLREF1, PLLREF0:

The PLLREF[1:0] bits select the source of the Transmit Jitter Attenuator phase locked loop reference signal as follows:

**Table 18 - TJAT PLL Source**

| PLLREF1 | PLLREF0 | Source of PLL Reference |
|---|---|---|
| 0 | 0 | TJAT FIFO input clock (either the conditioned BTCLK or the receive recovered clock, as selected by LINELB, assuming the TX-ELST is bypassed) |
| 0 | 1 | conditioned BTCLK input (assuming the TX-ELST is bypassed) |
| 1 | 0 | Receive recovered clock |
| 1 | 1 | TCLKI input |

If the BTCLK is configured as an output (CMODE bit of the Transmit Backplane Configuration register is a logic 0), only the recovered clock or the TCLKI input should be selected, or else the timing becomes self-referential and unpredictable.

The following table illustrates the required bit settings for these various clock sources to affect the transmitted data:

**Table 19 - Transmit Timing Options Summary**

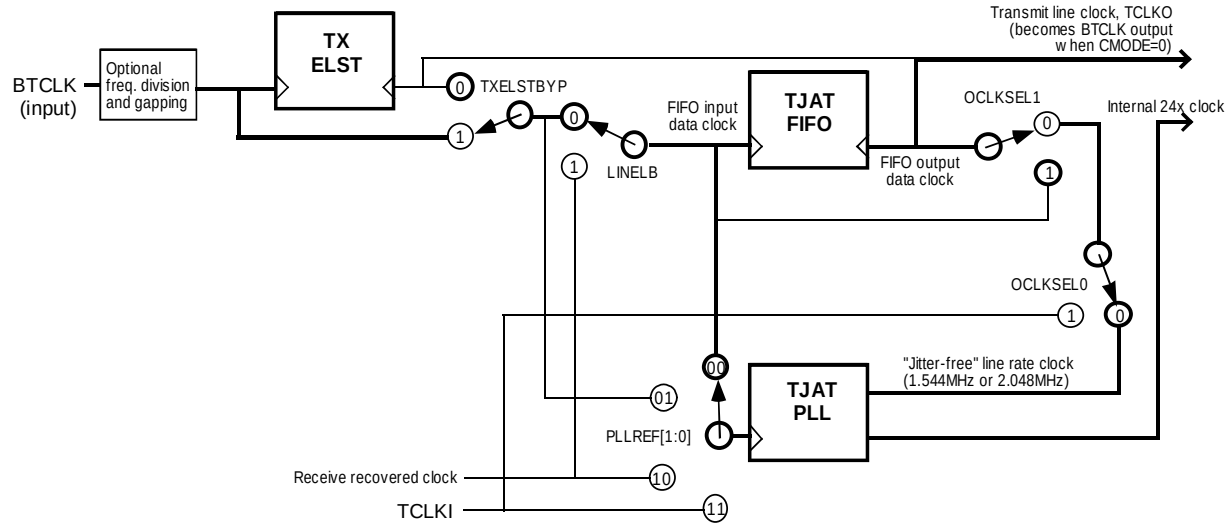
| Input Transmit Data | Bit Settings | Effect on Output Transmit Data |
|---|---|---|
| Synchronous to BTCLK input.<br>Transmit Backplane Configuration register CMODE =1. | OCLKSEL1=0<br>OCLKSEL0=0<br>PLLREF1=0<br>PLLREF0=X<br>LINELB=0<br>TXELSTBYP=1 | Jitter attenuated. TCLKO is a smooth 1.544 MHz or 2.048 MHz.<br>TCLKO referenced to BTCLK input. TX-ELST bypassed. |

| Input Transmit Data | Bit Settings | Effect on Output Transmit Data |
|---|---|---|
| Synchronous to BTCLK output.<br>Transmit Backplane Configuration register CMODE =0. | OCLKSEL1=0<br>OCLKSEL0=0<br>PLLREF1=1<br>PLLREF0=0<br>LINELB=0<br>TXELSTBYP=1 | Jitter attenuated looptiming. TCLKO is a smooth 1.544 MHz or 2.048 MHz.<br>Loop timed to the receive recovered clock. TX-ELST bypassed. |
| Synchronous to BTCLK input.<br>Transmit Backplane Configuration register CMODE =1. | OCLKSEL1=0<br>OCLKSEL0=0<br>PLLREF1=1<br>PLLREF0=0<br>LINELB=0<br>TXELSTBYP=0 | Jitter attenuated looptiming. TCLKO is a smooth 1.544 MHz or 2.048 MHz.<br>Loop timed to the receive recovered clock. TX-ELST allows BTCLK to be plesiochronous. |
| Synchronous to BTCLK output.<br>Transmit Backplane Configuration register CMODE =0. | OCLKSEL1=0<br>OCLKSEL0=0<br>PLLREF1=1<br>PLLREF0=1<br>LINELB=0<br>TXELSTBYP=1 | Jitter attenuated. TCLKO is a smooth 1.544 MHz or 2.048 MHz. TCLKO and BTCLK referenced to TCLKI input. TX-ELST bypassed. |
| Synchronous to BTCLK input.<br>Transmit Backplane Configuration register CMODE =1. | OCLKSEL1=0<br>OCLKSEL0=0<br>PLLREF1=1<br>PLLREF0=1<br>LINELB=0<br>TXELSTBYP=0 | Jitter attenuated. TCLKO is a smooth 1.544 MHz or 2.048 MHz. TCLKO referenced to TCLKI input. TX-ELST allows BTCLK to be plesiochronous. |
| Synchronous to BTCLK input.<br>Transmit Backplane Configuration register CMODE =1. | OCLKSEL1=1<br>OCLKSEL0=X<br>PLLREF1=1<br>PLLREF0=1<br>LINELB=0<br>TXELSTBYP=1 | No jitter attenuation. TCLKO is equivalent to BTCLK. TX-ELST bypassed. |

| Input Transmit Data | Bit Settings | Effect on Output Transmit Data |
|---|---|---|
| Synchronous to BTCLK output. Transmit Backplane Configuration register CMODE =0. | OCLKSEL1=0<br>OCLKSEL0=1<br>PLLREF1=1<br>PLLREF0=1<br>LINELB=0<br>TXELSTBYP=1 | No jitter attenuation. TCLKO is equal to TCLKI (useful for higher rate MUX applications). The BTCLK output referenced to TCLKI. TX-ELST bypassed. |
| Synchronous to BTCLK input. Transmit Backplane Configuration register CMODE =1. | OCLKSEL1=0<br>OCLKSEL0=1<br>PLLREF1=1<br>PLLREF0=1<br>LINELB=0<br>TXELSTBYP=0 | No jitter attenuation. TCLKO is equal to TCLKI (useful for higher rate MUX applications). TX-ELST allows BTCLK to be plesiochronous. |
| Transmit data ignored. Receive data is looped back. | OCLKSEL1=0<br>OCLKSEL0=0<br>PLLREF1=X<br>PLLREF0=0<br>LINELB=1<br>TXELSTBYP=X | Line loopback with jitter attenuation. |

Upon reset of the COMET, these bits are cleared to zero, selecting jitter attenuation with TCLKO referenced to the backplane transmit clock, BTCLK. Figure 12 illustrates the various bit setting options, with the reset condition highlighted. When TUNI is logic 0, PLLREF[1:0] must be configured such that the internal 24x clock references the Transmit line clock.

## Figure 12 - Transmit Timing Options



### Register 007H: Interrupt Source #1

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | PMON | 0 |
| Bit 6 | R | PRGD | 0 |
| Bit 5 | R | FRMR | 0 |
| Bit 4 | R | SIGX | 0 |
| Bit 3 | R | APRM | 0 |
| Bit 2 | R | TJAT | 0 |
| Bit 1 | R | RJAT | 0 |
| Bit 0 | R | CDRC | 0 |

This register allows software to determine the block which produced the interrupt on the INTB output pin.

Reading this register does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

### Register 008H: Interrupt Source #2

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | RX-ELST | 0 |
| Bit 6 | R | RDLC #3 | 0 |
| Bit 5 | R | RDLC #2 | 0 |
| Bit 4 | R | RDLC #1 | 0 |
| Bit 3 | R | TX-ELST | 0 |
| Bit 2 | R | TDPR #3 | 0 |
| Bit 1 | R | TDPR #2 | 0 |
| Bit 0 | R | TDPR #1 | 0 |

This register allows software to determine the block that produced the interrupt on the INTB output pin.

Reading this register does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

### Register 009H: Interrupt Source #3

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | IBCD | 0 |
| Bit 6 | R | PDVD | 0 |
| Bit 5 | R | RBOC | 0 |
| Bit 4 | R | XPDE | 0 |
| Bit 3 | R | ALMI | 0 |
| Bit 2 | R | TRAN | 0 |
| Bit 1 | R | RLPS | 0 |
| Bit 0 | R | BTIF | 0 |

This register allows software to determine the block that produced the interrupt on the INTB output pin.

Reading this register does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

### Register 00AH: Master Diagnostics

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | R | ID[5] | 1 |
| Bit 5 | R/W | PAYLB | 0 |
| Bit 4 | R/W | LINELB | 0 |
| Bit 3 | R/W | RAIS | 0 |
| Bit 2 | R/W | DDLB | 0 |
| Bit 1 | R/W | TXMFP | 0 |
| Bit 0 | R/W | TXLOS | 0 |

ID[5]:

The ID[5] bit was added for COMET Rev G. In prior revisions, this bit was unused and defaulted to X. Please see the Register 00DH: Revision/Chip ID/Global PMON Update description for how to distinguish between COMET Rev F and G in software.

PAYLB:

The PAYLB bit selects the payload loopback mode, where the received data output from the RX-ELST is internally connected to the transmit data input of the transmitter. The data read out of RX-ELST is timed to the transmitter clock, and the transmit frame alignment is used to synchronize the output frame alignment of RX-ELST. The transmit frame alignment is either arbitrary (when the TX-ELST is used) or is specified by the BTFP input (when the TX-ELST is bypassed). During payload loopback, the data on BRPCM is only valid when the COMET is configured as a BRCLK master, BRFP master and the RX-ELST is bypassed. When the RX-ELST is not bypassed, the BRPCM output is forced to all-ones. When PAYLB is set to logic 1, the payload loopback mode is enabled. When PAYLB is set to logic 0, the loopback mode is disabled. In T1 mode, if the TDPR #1 is configured to send performance reports from the T1-APRM, this bit requires two updating cycles before being included in the performance report. Only one of PAYLB, LINELB, and DDLB can be enabled at any one time.

LINELB:

The LINELB bit selects the line loopback mode, where the recovered data are internally directed to the digital inputs of the transmit jitter attenuator. In analog mode (RUNI is logic 0), the data sent to the TJAT is the recovered

data from the output of the CDRC block. In digital mode (RUNI is logic 1), the data sent to the TJAT is a sampled version of the RDAT digital input. When LINELB is set to logic 1, the line loopback mode is enabled. When LINELB is set to logic 0, the line loopback mode is disabled. Note that when line loopback is enabled, to correctly attenuate the jitter on the receive clock, the contents of the TJAT Reference Clock Divisor and Output Clock Divisor registers should be programmed to 2FH in T1 or FFH in E1 and the Transmit Timing Options register should be cleared to all zeros. Only one of PAYLB, LINELB, and DDLB can be enabled at any one time.

RAIS:

When a logic 1, the RAIS bit forces all ones into the BRPCM data stream. The BRSIG data stream will freeze at the current valid signaling. This capability is provided to indicate the unavailability of the line when line loopback is active.

DDLB:

The DDLB bit selects the diagnostic digital loopback mode, where the COMET is configured to internally direct the output of the TJAT to the inputs of the receiver section. In analog mode (RUNI is logic 0), the dual-rail RZ outputs of the TJAT are directed to the dual-rail inputs of the CDRC. In digital mode (RUNI is logic 1), the single-rail NRZ outputs of the TJAT are directed to the inputs of the RJAT. When DDLB is set to logic 1, the diagnostic digital loopback mode is enabled. When DDLB is set to logic 0, the diagnostic digital loopback mode is disabled. When configured for diagnostic digital loopback, the TUNI and RUNI bits must be set to the same value. Only one of PAYLB, LINELB, and DDLB can be enabled at any one time.

TXMFP:

In T1 mode, the TXMFP bit introduces a mimic framing pattern in the digital output of the basic transmitter by forcing a copy of the current framing bit into bit location 1 of the frame, thereby creating a mimic pattern in the bit position immediately following the correct framing bit. When TXMFP is set to logic 1, the mimic framing pattern is generated. When TXMFP is set to logic 0, no mimic pattern is generated.

TXLOS:

The TXLOS bit provides a method of suppressing the output of the transmitter in T1 digital mode. When TXLOS is set to logic 1, the E1/T1B bit in the Global Configuration register is a logic 0 and the TUNI bit in the Transmit Line Interface Configuration register is a logic 1, the transmit output, TDAT is forced to all-zeros. In both E1 and T1 analog mode (TUNI is logic 0), the TXTIP and TXRING outputs can be forced to all-zeros by programming the XLPG Line Driver Configuration register.

### Register 00BH: Master Test

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | W | IDDQEN | X |
| Bit 5 | W | PMCATST | X |
| Bit 4 | W | PMCTST | X |
| Bit 3 | W | DBCTRL | 0 |
| Bit 2 | R/W | IOTST | 0 |
| Bit 1 | W | HIZDATA | 0 |
| Bit 0 | R/W | HIZIO | 0 |

This register is used to select COMET test features. All bits, except for PMCTST, PMCATST and IDDQEN are reset to zero by a hardware reset of the COMET; a software reset of the COMET does not affect the state of the bits in this register. Refer to the Test Features Description section for more information.

IDDQEN:

The IDDQEN bit is used to configure the COMET for IDDQ tests. IDDQEN is cleared when CSB is high and RSTB is low or when IDDQEN is written as logic 0. When the IDDQEN bit is set to logic 1, the HIGHZ bit in the XLPG Line Driver Configuration register must also be set to logic 1.

PMCATST:

The PMCATST bit is used to configure the analog portion of the COMET for PMC's manufacturing tests. PMCATST is cleared when CSB is high and RSTB is low or when PMCATST is written as logic 0.

PMCTST:

The PMCTST bit is used to configure the COMET for PMC's manufacturing tests. When PMCTST is set to logic 1, the COMET microprocessor port becomes the test access port used to run the PMC manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and is cleared by setting CSB high.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output

enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the COMET to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit only has effect when the IOTST or PMCTST bit is set to logic 1. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each block in the COMET for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the COMET . While the HIZIO bit is a logic 1, all output pins of the COMET except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

### Register 00CH: Analog Diagnostics

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | R/W | Reserved | 0 |
| Bit 4 | R/W | Reserved | 0 |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | R/W | Reserved | 0 |
| Bit 0 | R/W | Reserved | 0 |

Reserved:

These bits must be a logic 0 for correct operation.

### Register 00DH: Revision/Chip ID/Global PMON Update

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | TYPE[2] | 0 |
| Bit 6 | R | TYPE[1] | 0 |
| Bit 5 | R | TYPE[0] | 1 |
| Bit 4 | R | ID[4] | 0 |
| Bit 3 | R | ID[3] | 0 |
| Bit 2 | R | ID[2] | 1 |
| Bit 1 | R | ID[1] | 0 |
| Bit 0 | R | ID[0] | 1 |

The version identification bits, ID[4:0], are set to a fixed value representing the version number of the COMET. For COMET Rev G, ID[5] was added to the Master Diagnostics register (address 00AH).

In order to uniquely identify Rev G in software, the following routine can be executed:

i. Read Register 00DH: Revision/Chip ID/Global PMON Update. Revision F or Revision G will contain “00100101”.

ii. Read Register 00AH: Master Diagnostics. In Revision F, bit 6 will read logic 0, as this is the value charged on the bus-holder due to the last read. In Revision G, bit 6 will read logic 1, as this is the value driven by the new ID[5] bit.

NOTE: For this two step sequence to work, step (ii) must follow immediately after step (i) without any intervening microprocessor accesses. Any intervening accesses could change the value charged onto the bit 6 bus-holder, invalidating step (ii).

Writing any value to this register causes all performance monitor counters to be updated simultaneously.

The chip identification bits, TYPE[2:0], are set to “001” representing the COMET.

### Register 00EH: Reset

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | R/W | RESET | 0 |

RESET:

The RESET bit implements a software reset. If the RESET bit is a logic 1, the COMET is held in reset. This bit is not self-clearing; therefore, a logic 0 must be written to bring the COMET out of reset. Holding the COMET in a reset state effectively puts it into a low-power, stand-by mode. A hardware reset clears the RESET bit, thus deasserting the software reset.

### Register 00FH: PRGD Positioning/Control and HDLC Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | HDLC3_DIS | 0 |
| Bit 6 | R/W | HDLC2_DIS | 0 |
| Bit 5 | R/W | HDLC1_DIS | 0 |
| Bit 4 | R/W | Nx56k_GEN | 0 |
| Bit 3 | R/W | Nx56k_DET | 0 |
| Bit 2 | R/W | RXPATGEN | 0 |
| Bit 1 | R/W | UNF_GEN | 0 |
| Bit 0 | R/W | UNF_DET | 0 |

This register modifies the way in which the PRGD is used by the TPSC and RPSC. More information on using PRGD is available in the Operation section.

HDLC3_DIS:

The HDLC3_DIS bit, when set to logic 1, is used to disable the clock to the TDPR #3 and RDLC #3, putting them into a low power, stand-by mode. When the HDLC3_DIS bit is set to logic 0, the clock to the TDPR #3 and RDLC #3 is enabled.

HDLC2_DIS:

The HDLC2_DIS bit, when set to logic 1, is used to disable the clock to the TDPR #2 and RDLC #2, putting them into a low power, stand-by mode. When the HDLC2_DIS bit is set to logic 0, the clock to the TDPR #2 and RDLC #2 is enabled.

HDLC1_DIS:

The HDLC1_DIS bit, when set to logic 1, is used to disable the clock to the TDPR #1 and RDLC #1, putting them into a low power, stand-by mode. When the HDLC1_DIS bit is set to logic 0, the clock to the TDPR #1 and RDLC #1 is enabled.

Nx56k_GEN:

The Nx56k_GEN bit is active when the RPSC or TPSC is used to insert PRBS into selected DS0 channels of the transmit or receive stream. When the Nx56kbps generation bit is set to logic 1, the pattern is only inserted in the first 7 bits of the selected DS0 channels, and gapped on the eighth bit. This

is particularly useful when using the jammed-bit-8 zero code suppression in the transmit direction, for instance when sending a Nx56kbps fractional T1/E1 loopback sequence. This bit has no effect when UNF_GEN is set to logic 1.

Nx56k_DET:

The Nx56k_DET bit is active when the RPSC or TPSC is used to detect PRBS in selected DS0 channels of the transmit or receive stream. When the Nx56kbps detection bit is set to logic 1, the pattern generator only looks at the first 7 bits of the selected DS0 channels, and gaps out the eighth bit. This is particularly useful when searching for fractional T1 loopback codes in an Nx56kbps fractional T1 signal. This bit has no effect when UNF_DET is set to logic 1.

RXPATGEN:

The Receive Pattern Generate (RXPATGEN) bit controls the location of the pattern generator/detector. When RXPATGEN is set to logic 1, the pattern generator is inserted in the receive path and the pattern detector is inserted in the transmit path. Timeslots from the receive line may be overwritten with generated patterns before appearing on the receive backplane interface, and timeslots from the transmit backplane interface may be checked for the generated pattern before appearing on the transmit line. When RXPATGEN is set to logic 0, the pattern detector is inserted in the receive path and the pattern generator is inserted in the transmit path. Timeslots from the transmit backplane interface may be overwritten with generated patterns before appearing on the transmit line, and timeslots from the receive line may be checked for the generated pattern before appearing on the receive backplane interface.

UNF_GEN

When the Unframed Pattern Generation bit (UNF_GEN) is set to logic 1, the PRGD will overwrite all 193 bits/256 bits in every frame in the direction specified by the RXPATGEN bit. If the generator is enabled in the transmit path, unless signaling and/or framing is disabled, the transmitter will still overwrite the signaling bit positions and/or the framing bit position. Similarly, if pattern generation is enabled in the receive direction, the pattern will overwrite the framing bit positions. The UNF_GEN bit overrides any per-timeslot pattern generation specified in the TPSC or RPSC. When RXPATGEN = 0, UNF_GEN also overrides idle code insertion and data inversion in the transmit direction, just like the TEST bit in the TPSC.

UNF_DET

When the Unframed Pattern Detection bit (UNF_DET) is set to logic 1, the PRGD will search for the pattern in all 193 bits/256 bits of the transmit or

receive stream, depending on the setting of RXPATGEN. The UNF_DET bit overrides any per-timeslot pattern detection specified in the TPSC or RPSC.

### Register 010H: CDRC Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | AMI | 0 |
| Bit 6 | R/W | LOS[1] | 0 |
| Bit 5 | R/W | LOS[0] | 0 |
| Bit 4 | R/W | Reserved | 0 |
| Bit 3 | R/W | Reserved | 0 |
| Bit 2 | R/W | ALGSEL | 0 |
| Bit 1 | R/W | O162 | 0 |
| Bit 0 | R/W | Reserved | 0 |

When the RUNI bit of the Receive Line Interface Configuration register is a logic 1, this register is held reset.

Reserved:

These bits must be a logic 0 for correct operation.

O162:

If the AMI bit is logic 0 in E1 mode, the Recommendation O.162 compatibility select bit (O162) allows selection between two line code violation definitions:

If O162 is a logic 0, a line code violation is indicated if the serial stream does not match the verbatim HDB3 definition given in Recommendation G.703. A bipolar violation that is not part of an HDB3 signature or a bipolar violation in an HDB3 signature that is the same polarity as the last bipolar violation results in a line code violation indication.

If O162 is a logic 1, a line code violation is indicated if a bipolar violation is of the same polarity as the last bipolar violation, as per Recommendation O.162.

The O162 bit has no effect in T1 mode.

ALGSEL:

The Algorithm Select (ALGSEL) bit specifies the algorithm used by the DPLL for clock and data recovery. The choice of algorithm determines the high frequency input jitter tolerance of the CDRC. When ALGSEL is set to logic 1, the CDRC jitter tolerance is increased to approach 0.5 UIpp for jitter

frequencies above 20 kHz. When ALGSEL is set to logic 0, the jitter tolerance is increased for frequencies below 20 kHz (i.e. the tolerance is improved by 20% over that of ALGSEL=1 at these frequencies), but the tolerance approaches 0.4 UIpp at the higher frequencies.

AMI:

The alternate mark inversion (AMI) bit specifies the line coding of the incoming signal. A logic 1 selects AMI line coding by disabling HDB3 decoding if E1 mode and B8ZS in T1 mode. In E1 mode, a logic 0 selects HDB3 line decoding which entails substituting an HDB3 signature with four zeros. In T1 mode, a logic 0 selects B8ZS line decoding which entails substituting an B8ZS signature with eight zeros.

LOS[1:0]:

The loss of signal threshold is set by the operating mode and the state of the AMI, LOS[1] and LOS[0] bits:

**Table 20 - Loss of Signal Thresholds**

| Mode | AMI | LOS[1] | LOS[0] | Threshold (PCM periods) |
|---|---|---|---|---|
| E1 | 0 | 0 | 0 | 10 |
| T1 | 0 | 0 | 0 | 15 |
| X | 1 | 0 | 0 | 15 |
| X | X | 0 | 1 | 31 |
| X | X | 1 | 0 | 63 |
| X | X | 1 | 1 | 175 |

When the number of consecutive zeros on the incoming PCM line exceeds the programmed threshold, the LOSV status bit is set. For example, if the threshold is set to 10, the 11th zero causes the LOSV bit to be set. The LOSV bit clears when a pulse occurs.

### Register 011H: CDRC Interrupt Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | LCVE | 0 |
| Bit 6 | R/W | LOSE | 0 |
| Bit 5 | R/W | LCSDE | 0 |
| Bit 4 | R/W | ZNDE | 0 |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | | Unused | X |

When the RUNI bit of the Receive Line Interface Configuration register is a logic 1, this register is held reset.

The bit positions LCVE, LOSE, LCSDE and ZNDE (bits 7 to 4) of this register are interrupt enables to select which of the status events (Line Code Violation , Loss Of Signal, HDB3 signature, B8ZS signature or N Zeros), either singly or in combination, are enabled to generate an interrupt on the microprocessor INTB pin when they are detected. A logic 1 bit in the corresponding bit position enables the detection of these signals to generate an interrupt; a logic 0 bit in the corresponding bit position disables that signal from generating an interrupt.

When the COMET is reset, LCVE, LOSE, LCSDE and ZNDE are set to logic 0, disabling these events from generating an interrupt.

### Register 012H: CDRC Interrupt Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | LCVI | X |
| Bit 6 | R | LOSI | X |
| Bit 5 | R | LCSDI | X |
| Bit 4 | R | ZNDI | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | R | LOSV | X |

When the RUNI bit of the Receive Line Interface Configuration register is a logic 1, this register is held reset.

The ZNDI, LCSDI, LOSI and LCVI (bits 4 to 7) of this register indicate which of the status events have occurred since the last time this register was read. A logic 1 in any of these bit positions indicates that the corresponding event was detected.

Bits ZNDI, LCSDI, LOSI and LCVI are cleared to logic 0 by reading this register.

LOSV:

The LOSV bit reflects the status of the LOS alarm.

ZNDI:

The consecutive zeros detection interrupt (ZNDI) indicates that N consecutive spaces have occurred, where N is four for E1 and eight for T1. This bit can be used to detect an AMI coded signal.

LCSDI:

The line code signature detection interrupt (LCSDI) indicates that a valid line code signature has occurred. In T1 mode, the B8ZS signature is defined as 000+-0-+ if the previous impulse is positive, or 000-+0+- if it is negative. In E1 mode, a valid HDB3 signature is defined as a bipolar violation preceded by two zeros. This bit can be used to detect an HDB3 coded signal in E1 mode and B8ZS coded signal in T1.

LOSI:

The LOSI bit is set to a logic 1 when the LOSV bit changes state.

LCVI:

The line code violation interrupt (LCVI) indicates a series of marks and spaces has occurred in contradiction to the defined line code (AMI, B8ZS or HDB3).

### Register 013H: Alternate Loss of Signal Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | ALTLOSE | 0 |
| Bit 6 | R | ALTLOSI | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | R | ALTLOS | X |

This register is only operational when the RUNI bit of the Receive Line Interface Configuration register is a logic 0.

The alternate loss of signal status provides a more stringent criteria for the deassertion of the alarm than the LOS indication in the CDRC Interrupt Status register.

ALTLOSE:

If the ALTLOSE bit is a logic 1, the INTB output is asserted low when the ALTLOS status bit changes state.

ALTLOSI:

The ALTLOSI bit is set high when the ALTLOS status bit changes state. It is cleared when this register is read.

ALTLOS:

The ALTLOS bit is asserted upon the absence of marks for the threshold of bit periods specified by the LOS[1:0] register bits. The ALTLOS bit is deasserted only after pulse density requirements have been met. In T1 mode, there must be N ones in each and every time window of 8(N+1) data bits (where N can equal 1 through 23). In E1 mode, ALTLOS is deasserted only after 255 bit periods during which no sequence of four zeros has been received.

### Register 014H: RJAT Interrupt Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | R | OVRI | X |
| Bit 0 | R | UNDI | X |

UNDI:

The UNDI bit is asserted when an attempt is made to read data from the receive FIFO when the FIFO is already empty. When UNDI is a logic 1, an underrun event has occurred. Reading this register will clear the UNDI bit to logic 0.

OVRI:

The OVRI bit is asserted when an attempt is made to write data into the receive FIFO when the FIFO is already full. When OVRI is a logic 1, an overrun event has occurred. Reading this register will clear the OVRI bit to logic 0.

### Register 015H: RJAT Divider N1 Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | N1[7] | 0 |
| Bit 6 | R/W | N1[6] | 0 |
| Bit 5 | R/W | N1[5] | 1 |
| Bit 4 | R/W | N1[4] | 0 |
| Bit 3 | R/W | N1[3] | 1 |
| Bit 2 | R/W | N1[2] | 1 |
| Bit 1 | R/W | N1[1] | 1 |
| Bit 0 | R/W | N1[0] | 1 |

This register contains an 8-bit binary number, N1, which is one less than the magnitude of the reference clock divisor. The reference divisor magnitude, (N1+1), is the ratio between the frequency of the recovered clock (or the transmit clock if a diagnostic loopback is enabled) and the frequency at the phase discriminator input.

Writing to this register will reset the PLL. If the FIFORST bit of the RJAT Configuration register is set high, a write to this register will reset both the PLL and FIFO.

The default value of N1 after a device reset is 47 = 2FH.

### Register 016H: RJAT Divider N2 Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | N2[7] | 0 |
| Bit 6 | R/W | N2[6] | 0 |
| Bit 5 | R/W | N2[5] | 1 |
| Bit 4 | R/W | N2[4] | 0 |
| Bit 3 | R/W | N2[3] | 1 |
| Bit 2 | R/W | N2[2] | 1 |
| Bit 1 | R/W | N2[1] | 1 |
| Bit 0 | R/W | N2[0] | 1 |

This register contains an 8-bit binary number, N2, which is one less than the magnitude of the output clock divisor. The output clock divisor magnitude, (N2+1), is the ratio between the frequency of the smooth output clock, BRCLK, and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL.

Writing to this register will reset the PLL. If the FIFORST bit of the RJAT Configuration register is set high, a write to this register will reset both the PLL and FIFO.

The default value of N2 after a device reset is 47 = 2FH.

**Recommendations**

In general, the relationship N1 = N2 must always be true in order for the PLL to operate correctly.

In order to meet jitter transfer specifications for some modes, such as basic E1 operation, N1 and N2 must be large in order to reduce the PLL transfer cutoff frequency. In general, for E1 operation, N2 is set to FFH to meet ETSI jitter transfer specifications.

For T1 mode, the recommended values are N1 = N2 = 2FH. For E1 mode, the recommended values are N1 = N2 = FFH.

### Register 017H: RJAT Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R/W | CENT | 0 |
| Bit 3 | R/W | UNDE | 0 |
| Bit 2 | R/W | OVRE | 0 |
| Bit 1 | R/W | FIFORST | 0 |
| Bit 0 | R/W | LIMIT | 1 |

CENT:

The CENT bit allows the FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full. When CENT is set to logic 1, the FIFO is enabled to self-center for the next 384 transmit data bit period, and for the first 384 bit periods following an overrun or underrun event. If an EMPTY or FULL alarm occurs during this 384 UI period, the period will be extended by the number of UI that the EMPTY or FULL alarm persists. During the EMPTY or FULL alarm conditions, data is lost. When CENT is set to logic 0, the self-centering function is disabled, allowing the data to pass through uncorrupted during EMPTY or FULL alarm conditions.

The recommended value of CENT is logic 1.

UNDE:

Setting the UNDE bit to logic 1 enables an underrun event to assert the INTB output low.

OVRE:

Setting the OVRE bit to logic 1 enables an overrun event to assert the INTB output low.

FIFORST:

Setting the FIFORST bit allows the FIFO to reset when the PLL is reset by software. When FIFORST is logic 1, writing to the PLL Divider Control Registers N1 and N2 will cause both the PLL and FIFO to reset. When

FIFORST is logic 0, writing to the Divider Control Registers N1 and N2 will cause only the PLL to reset.

LIMIT:

Setting the LIMIT bit to logic 1 will limit the PLL jitter attenuation by enabling the FIFO to increase or decrease the frequency of the smooth output clock whenever the FIFO is within one UI of overflowing or underflowing. This limiting of jitter ensures that no data is lost during high phase shift conditions. When LIMIT is set to logic 0, underflows and overflows may occur.

The recommended value of LIMIT is logic 0.

### Register 018H: TJAT Interrupt Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | R | OVRI | X |
| Bit 0 | R | UNDI | X |

UNDI:

The UNDI bit is asserted when an attempt is made to read data from the transmit FIFO when the FIFO is already empty. When UNDI is a logic 1, an underrun event has occurred. Reading this register will clear the UNDI bit to logic 0.

OVRI:

The OVRI bit is asserted when an attempt is made to write data into the transmit FIFO when the FIFO is already full. When OVRI is a logic 1, an overrun event has occurred. Reading this register will clear the OVRI bit to logic 0.

### Register 019H: TJAT Jitter Attenuator Divider N1 Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | N1[7] | 0 |
| Bit 6 | R/W | N1[6] | 0 |
| Bit 5 | R/W | N1[5] | 1 |
| Bit 4 | R/W | N1[4] | 0 |
| Bit 3 | R/W | N1[3] | 1 |
| Bit 2 | R/W | N1[2] | 1 |
| Bit 1 | R/W | N1[1] | 1 |
| Bit 0 | R/W | N1[0] | 1 |

This register contains an 8-bit binary number, N1, which is one less than the magnitude of the reference clock divisor. The reference divisor magnitude, (N1+1), is the ratio between the frequency of the reference clock (as selected by the PLLREF1 and PLLREF0 bits of the Transmit Timing Options register) and the frequency at the phase discriminator input.

Writing to this register will reset the PLL. If the FIFORST bit of the TJAT Configuration register is set high, a write to this register will reset both the PLL and FIFO.

The default value of N1 after a device reset is 47 = 2FH.

### Register 01AH: TJAT Divider N2 Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | N2[7] | 0 |
| Bit 6 | R/W | N2[6] | 0 |
| Bit 5 | R/W | N2[5] | 1 |
| Bit 4 | R/W | N2[4] | 0 |
| Bit 3 | R/W | N2[3] | 1 |
| Bit 2 | R/W | N2[2] | 1 |
| Bit 1 | R/W | N2[1] | 1 |
| Bit 0 | R/W | N2[0] | 1 |

This register contains an 8-bit binary number, N2, which is one less than the magnitude of the output clock divisor. The output clock divisor magnitude, (N2+1), is the ratio between the frequency of the smooth output clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL. If the FIFORST bit of the TJAT Configuration register is set high, a write to this register will reset both the PLL and FIFO.

The default value of N2 after a device reset is 47 = 2FH.

**Recommendations**

In general, the relationship $F_{ref}/(N1+1) = F_{out}/(N2+1)$ must always be true in order for the PLL to operate correctly.

Minimizing the values of N1 and N2 while keeping the above equation true minimizes intrinsic jitter. However, the minimum valid value for N2 is 1FH.

In order to meet jitter transfer specifications for some modes, such as basic E1 operation, N1 and N2 must be large in order to reduce the PLL transfer cutoff frequency. In general, for E1 operation, N2 is set to FFH to meet ETSI jitter transfer specifications.

When dealing with extremely low frequency references, such as an 8kHz reference clock, the N1 and N2 should configured so that $F_{ref}/(N1+1)$ and $F_{out}/(N2+1)$ are both 8kHz results. Thus, for an 8kHz reference, N1 is 00H.

The table below summarizes the recommended values for N1 and N2 for common modes of operation.

| PLL Reference, as set by register bits PLLREF[1:0] | PLL Output Frequency | N1[7:0] | N2[7:0] |
|---|---|---|---|
| 1.544 MHz | 1.544 MHz (T1) | 2FH | 2FH |
| 2.048 MHz | 2.048 MHz (E1) | FFH | FFH |
| 2.048 MHz | 1.544 MHz (T1) | FFH | C0H |
| 1.544 MHz | 2.048 MHz (E1) | C0H | FFH |
| nominal 1.544 MHz (derived from gapped 2.048 MHz)[1] | 1.544 MHz (T1) | C0H | C0H |
| 8 kHz | 1.544 MHz (T1) | 00H | C0H |
| 16 kHz | 1.544 MHz (T1) | 01H | C0H |
| 8 kHz | 2.048 MHz (E1) | 00H | FFH |
| 16 kHz | 2.048 MHz (E1) | 01H | FFH |

[1] Nominal 1.544 MHz is derived from a gapped 2.048 MHz when in T1 mode with the BTIF's RATE[1:0] bits set to "01", "10", or "11" and BTCLK configured as the reference.

### Register 01BH: TJAT Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R/W | CENT | 0 |
| Bit 3 | R/W | UNDE | 0 |
| Bit 2 | R/W | OVRE | 0 |
| Bit 1 | R/W | FIFORST | 0 |
| Bit 0 | R/W | LIMIT | 1 |

CENT:

The CENT bit allows the FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full. When CENT is set to logic 1, the FIFO is enabled to self-center for the next 384 transmit data bit period, and for the first 384 bit periods following an overrun or underrun event. If an EMPTY or FULL alarm occurs during this 384 UI period, the period will be extended by the number of UI that the EMPTY or FULL alarm persists. During the EMPTY or FULL alarm conditions, data is lost. When CENT is set to logic 0, the self-centering function is disabled, allowing the data to pass through uncorrupted during EMPTY or FULL alarm conditions.

The recommended value of CENT is logic 1.

UNDE:

Setting the UNDE bit to logic 1 enables an underrun event to assert the INTB output low.

OVRE:

Setting the OVRE bit to logic 1 enables an overrun event to assert the INTB output low.

FIFORST:

Setting the FIFORST bit allows the FIFO to reset when the PLL is reset by software. When FIFORST is logic 1, writing to the PLL Divider Control Registers N1 and N2 will cause both the PLL and FIFO to reset. When

FIFORST is logic 0, writing to the Divider Control Registers N1 and N2 will cause only the PLL to reset.

LIMIT:

Setting the LIMIT bit to logic 1 will limit the PLL jitter attenuation by enabling the FIFO to increase or decrease the frequency of the smooth output clock whenever the FIFO is within one UI of overflowing or underflowing. This limiting of jitter ensures that no data is lost during high phase shift conditions. When LIMIT is set to logic 0, underflows and overflows may occur.

The recommended value of LIMIT is logic 0.

### Register 01CH: RX-ELST Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | Reserved | 0 |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | R/W | IR | 1 |
| Bit 0 | R/W | OR | 1 |

Reserved:

This bit must be a logic 0 for correct operation.

IR:

The IR bit selects the input frame format. The IR bit must be set to logic 1 for E1 mode; it must be logic 0 for T1 mode.

OR:

The OR bit selects the output frame format. The OR bit must be set to logic 1 for E1 mode; it must be logic 0 for T1 mode.

### Register 01DH: RX-ELST Interrupt Enable/Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | R/W | SLIPE | 0 |
| Bit 1 | R | SLIPD | X |
| Bit 0 | R | SLIPI | X |

SLIPE:

The SLIPE bit position is an interrupt enable that when set, enables the INTB output to assert low when a slip occurs. When the block is reset the SLIPE bit position is cleared and interrupt generation is disabled.

SLIPD:

The SLIPD bit indicates the direction of the last slip. If the SLIPD bit is a logic 1 then the last slip was due to the frame buffer becoming full; a frame was deleted. If the SLIPD bit is a logic 0 then the last slip was due to the frame buffer becoming empty; a frame was duplicated.

SLIPI:

The SLIPI bit is set if a slip occurred since the last read of this register. The SLIPI bit is cleared upon reading this register.

### Register 01EH: RX-ELST Idle Code

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | D7 | 1 |
| Bit 6 | R/W | D6 | 1 |
| Bit 5 | R/W | D5 | 1 |
| Bit 4 | R/W | D4 | 1 |
| Bit 3 | R/W | D3 | 1 |
| Bit 2 | R/W | D2 | 1 |
| Bit 1 | R/W | D1 | 1 |
| Bit 0 | R/W | D0 | 1 |

The contents of this register replace the timeslot data in the BRPCM serial data stream when the framer is out of frame and the TRKEN bit in the Receive Options register is a logic 1. Since the transmission of all ones timeslot data is a common requirement, this register is set to all ones on a reset condition. D7 is the first to be transmitted.

The writing of the idle code pattern is asynchronous with respect to the output data clock. One timeslot of idle code data will be corrupted if the register is written to when the framer is out of frame.

### Register 020H: TX-ELST Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | Reserved | 0 |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | R/W | IR | 1 |
| Bit 0 | R/W | OR | 1 |

Reserved:

This bit must be programmed to logic 0 for correct operation.

IR:

The IR bit selects the input frame format. The IR bit must be set to logic 1 for E1 mode; it must be logic 0 for T1 mode.

OR:

The OR bit selects the output frame format. The OR bit must be set to logic 1 for E1 mode; it must be logic 0 for T1 mode.

### Register 021H: TX-ELST Interrupt Enable/Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | R/W | SLIPE | 0 |
| Bit 1 | R | SLIPD | X |
| Bit 0 | R | SLIPI | X |

SLIPE:

The SLIPE bit position is an interrupt enable that when set, enables the INTB output to assert low when a slip occurs. When the block is reset the SLIPE bit position is cleared and interrupt generation is disabled.

SLIPD:

The SLIPD bit indicates the direction of the last slip. If the SLIPD bit is a logic 1 then the last slip was due to the frame buffer becoming full; a frame was deleted. If the SLIPD bit is a logic 0 then the last slip was due to the frame buffer becoming empty; a frame was duplicated.

SLIPI:

The SLIPI bit is set if a slip occurred since the last read of this register. The SLIPI bit is cleared upon reading this register.

### Register 028H: RXCE Receive Data Link 1 Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | DL1_EVEN | 0 |
| Bit 6 | R/W | DL1_ODD | 0 |
| Bit 5 | R/W | T1_DL_EN | 1 |
| Bit 4 | R/W | DL1_TS[4] | 0 |
| Bit 3 | R/W | DL1_TS[3] | 0 |
| Bit 2 | R/W | DL1_TS[2] | 0 |
| Bit 1 | R/W | DL1_TS[1] | 0 |
| Bit 0 | R/W | DL1_TS[0] | 0 |

This register, along with the RXCE Data Link 1 Bit Select register, controls the extraction of the data link terminated by RDLC #1. Refer to the "Using the Internal HDLC Receivers" description in the Operation section for details on terminating HDLC frames.

DL1_EVEN:

The data link 1 even select (DL1_EVEN) bit controls whether or not the first data link is extracted from the even frames of the receive data stream. If DL1_EVEN is a logic 0, the data link is not extracted from the even frames. If DL1_EVEN is a logic 1, the data link is extracted from the even frames. In E1 mode, the frames in an E1 CRC-4 multiframe are considered to be numbered from 0 to 15; in T1 mode, the frames in a superframe are considered to be numbered from 1 to 12 (or 1 to 24 in an extended superframe).

DL1_ODD:

The data link 1 odd select (DL1_ODD) bit controls whether or not the first data link is extracted from the odd frames of the receive data stream. If DL1_ODD is a logic 0, the data link is not extracted from the odd frames. If DL1_ODD is a logic 1, the data link is extracted from the odd frames.

T1_DL_EN:

The T1 data link enable bit allows the termination of the ESF or T1DM data links when in T1 mode. If T1_DL_EN is a logic 1, the ESF, FMS1 and FMS0 bits of the T1 FRMR Configuration register determine the bit locations from which the data link is extracted. When the T1_DL_EN bit is a logic 1, the DL1_EVEN and DL1_ODD bits must both be set to logic 0. This bit must be set to logic 0 when in E1 mode.

DL1_TS[4:0]:

The data link 1 time slot (DL1_TS[4:0]) bits gives a binary representation of the time slot/channel from which the data link is to be extracted. Note that T1 channels 1 to 24 are mapped to values 0 to 23. The DL1_TS[4:0] bits have no effect when DL1_EVEN and DL1_ODD are both a logic 0.

### Register 029H: RXCE Receive Data Link 1 Bit Select

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | DL1_BIT[7] | 0 |
| Bit 6 | R/W | DL1_BIT[6] | 0 |
| Bit 5 | R/W | DL1_BIT[5] | 0 |
| Bit 4 | R/W | DL1_BIT[4] | 0 |
| Bit 3 | R/W | DL1_BIT[3] | 0 |
| Bit 2 | R/W | DL1_BIT[2] | 0 |
| Bit 1 | R/W | DL1_BIT[1] | 0 |
| Bit 0 | R/W | DL1_BIT[0] | 0 |

DL1_BIT[7:0]:

The data link 1 bit select (DL1_BIT[7:0]) bits controls which bits of the time slot/channel are to be extracted and passed to RDLC #1. If DL1_BIT[x] is a logic 1, that bit is extracted as part of the data link. To extract the data link from the entire time slot, all eight DL1_BIT[x] bits must be set to a logic 1. DL1_BIT[7] corresponds to the most significant bit (bit 1, the first bit received) of the time slot and DL1_BIT[0] corresponds to the least significant bit (bit 8, the last bit received) of the time slot. The DL1_BIT[7:0] bits have no effect when the DL1_EVEN and DL1_ODD bits of the RXCE Data Link 1 Control register are both logic 0.

### Register 02AH: RXCE Receive Data Link 2 Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | DL2_EVEN | 0 |
| Bit 6 | R/W | DL2_ODD | 0 |
| Bit 5 | R/W | Unused | X |
| Bit 4 | R/W | DL2_TS[4] | 0 |
| Bit 3 | R/W | DL2_TS[3] | 0 |
| Bit 2 | R/W | DL2_TS[2] | 0 |
| Bit 1 | R/W | DL2_TS[1] | 0 |
| Bit 0 | R/W | DL2_TS[0] | 0 |

This register, along with the RXCE Data Link 2 Bit Select register, controls the extraction of the data link terminated by RDLC #2. Refer to the "Using the Internal HDLC Receivers" description in the Operation section for details on terminating HDLC frames.

DL2_EVEN:

The data link 2 even select (DL2_EVEN) bit controls whether or not the second data link is extracted from the even frames of the receive data stream. If DL2_EVEN is a logic 0, the data link is not extracted from the even frames. If DL2_EVEN is a logic 1, the data link is extracted from the even frames. In E1 mode, the frames in an E1 CRC-4 multiframe are considered to be numbered from 0 to 15; in T1 mode, the frames in a superframe are considered to be numbered from 1 to 12 (or 1 to 24 in an extended superframe).

DL2_ODD:

The data link 2 odd select (DL2_ODD) bit controls whether or not the second data link is extracted from the odd frames of the receive data stream. If DL2_ODD is a logic 0, the data link is not extracted from the odd frames. If DL2_ODD is a logic 1, the data link is extracted from the odd frames.

DL2_TS[4:0]:

The data link 2 time slot (DL2_TS[4:0]) bits gives a binary representation of the time slot/channel from which the data link is to be extracted. Note that T1 channels 1 to 24 are mapped to values 0 to 23. The DL2_TS[4:0] bits have no effect when DL2_EVEN and DL2_ODD are both a logic 0.

### Register 02BH: RXCE Receive Data Link 2 Bit Select

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | DL2_BIT[7] | 0 |
| Bit 6 | R/W | DL2_BIT[6] | 0 |
| Bit 5 | R/W | DL2_BIT[5] | 0 |
| Bit 4 | R/W | DL2_BIT[4] | 0 |
| Bit 3 | R/W | DL2_BIT[3] | 0 |
| Bit 2 | R/W | DL2_BIT[2] | 0 |
| Bit 1 | R/W | DL2_BIT[1] | 0 |
| Bit 0 | R/W | DL2_BIT[0] | 0 |

DL2_BIT[7:0]:

The data link 2 bit select (DL2_BIT[7:0]) bits controls which bits of the time slot/channel are to be extracted and passed to RDLC #2. If DL2_BIT[x] is a logic 1, that bit is extracted as part of the data link. To extract the data link from the entire time slot, all eight DL2_BIT[x] bits must be set to a logic 1. DL2_BIT[7] corresponds to the most significant bit (bit 1, the first bit received) of the time slot and DL2_BIT[0] corresponds to the least significant bit (bit 8, the last bit received) of the time slot. The DL2_BIT[7:0] bits have no effect when the DL2_EVEN and DL2_ODD bits of the RXCE Data Link 2 Control register are both logic 0.

### Register 02CH: RXCE Receive Data Link 3 Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | DL3_EVEN | 0 |
| Bit 6 | R/W | DL3_ODD | 0 |
| Bit 5 | R/W | Unused | X |
| Bit 4 | R/W | DL3_TS[4] | 0 |
| Bit 3 | R/W | DL3_TS[3] | 0 |
| Bit 2 | R/W | DL3_TS[2] | 0 |
| Bit 1 | R/W | DL3_TS[1] | 0 |
| Bit 0 | R/W | DL3_TS[0] | 0 |

This register, along with the RXCE Data Link 3 Bit Select register, controls the extraction of the data link terminated by RDLC #3. Refer to the "Using the Internal HDLC Receivers" description in the Operation section for details on terminating HDLC frames.

DL3_EVEN:

The data link 3 even select (DL3_EVEN) bit controls whether or not the third data link is extracted from the even frames of the receive data stream. If DL3_EVEN is a logic 0, the data link is not extracted from the even frames. If DL3_EVEN is a logic 1, the data link is extracted from the even frames. In E1 mode, the frames in an E1 CRC-4 multiframe are considered to be numbered from 0 to 15; in T1 mode, the frames in a superframe are considered to be numbered from 1 to 12 (or 1 to 24 in an extended superframe).

DL3_ODD:

The data link 3 odd select (DL3_ODD) bit controls whether or not the third data link is extracted from the odd frames of the receive data stream. If DL3_ODD is a logic 0, the data link is not extracted from the odd frames. If DL3_ODD is a logic 1, the data link is extracted from the odd frames.

DL3_TS[4:0]:

The data link 3 time slot (DL3_TS[4:0]) bits gives a binary representation of the time slot/channel from which the data link is to be extracted. Note that T1 channels 1 to 24 are mapped to values 0 to 23. The DL3_TS[4:0] bits have no effect when DL3_EVEN and DL3_ODD are both a logic 0.

### Register 02DH: RXCE Receive Data Link 3 Bit Select

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | DL3_BIT[7] | 0 |
| Bit 6 | R/W | DL3_BIT[6] | 0 |
| Bit 5 | R/W | DL3_BIT[5] | 0 |
| Bit 4 | R/W | DL3_BIT[4] | 0 |
| Bit 3 | R/W | DL3_BIT[3] | 0 |
| Bit 2 | R/W | DL3_BIT[2] | 0 |
| Bit 1 | R/W | DL3_BIT[1] | 0 |
| Bit 0 | R/W | DL3_BIT[0] | 0 |

DL3_BIT[7:0]:

The data link 3 bit select (DL3_BIT[7:0]) bits controls which bits of the time slot/channel are to be extracted and passed to RDLC #3. If DL3_BIT[x] is a logic 1, that bit is extracted as part of the data link. To extract the data link from the entire time slot, all eight DL3_BIT[x] bits must be set to a logic 1. DL3_BIT[7] corresponds to the most significant bit (bit 1, the first bit received) of the time slot and DL3_BIT[0] corresponds to the least significant bit (bit 8, the last bit received) of the time slot. The DL3_BIT[7:0] bits have no effect when the DL3_EVEN and DL3_ODD bits of the RXCE Data Link 3 Control register are both logic 0.

### Register 030H: BRIF Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | NXDS0[1] | 0 |
| Bit 6 | R/W | NXDS0[0] | 0 |
| Bit 5 | R/W | CMODE | 1 |
| Bit 4 | R/W | DE | 1 |
| Bit 3 | R/W | FE | 1 |
| Bit 2 | R/W | CMS | 0 |
| Bit 1 | R/W | RATE[1] | 0 |
| Bit 0 | R/W | RATE[0] | 0 |

NXDS0[1:0]:

The NXDS0[1:0] bits determine the mode of operation when BRCLK clock master mode is selected, as shown in the following table. Note that these bits are ignored when clock slave mode is selected.

**Table 21 - Receive Backplane NXDS0 Mode Selection**

| NXDS0[1] | NXDS0[0] | Operation |
|---|---|---|
| 0 | 0 | Full Frame |
| 0 | 1 | 56 kbit/s NxDS0 |
| 1 | 0 | 64 kbit/s NxDS0 |
| 1 | 1 | 64 kbit/s NxDS0 with F-bit (only valid for E1 mode) |

When in Full Frame mode, the entire frame (193 bits for T1 or 256 bits for E1) is presented and the BRCLK pulse train contains no gaps.

When in any of the NxDS0 modes, only those time slots with their DTRKC bit cleared (logic 0) are clocked out the backplane. BRCLK does not pulse during those time slots with their DTRKC bit set (logic 1). The DTRKC bits are located in the RPSC Indirect Registers. When in T1 mode, the clock is always gapped during the framing bit position.

When the 56 kbit/s NxDS0 mode is selected, only the first 7 bits of the selected time slots are presented to the backplane and the 8th bit is gapped out. When

the 64 kbit/s NxDS0 mode is selected, all 8 bits of the selected time slots are presented to the backplane.

The 64 kbit/s NxDS0 with F-bit mode is intended to support ITU recommendation G.802 where 1.544 Mbit/s data is carried within a 2.048 Mbit/s data stream. This mode is only valid when the E1/T1B register bit is a logic 1 (E1 mode is selected). The operation is the same as the 64 NxDS0 mode, except that the framing bit is presented during the first bit of time slot 26. To properly extract a G.802 formatted T1, the DTRKC bits must be set to logic 0 for time slots 1 through 15 and 17 through 26, and the DTRKC bits must be set to logic 1 for time slots 27 through 31.

CMODE:

The clock mode (CMODE) bit determines whether the BRCLK pin is an input or output. When CMODE is a logic 0, clock master mode is selected and the BRCLK output is derived from the integral clock synthesizer. Depending on the mode of operation, BRCLK may have a burst frequency of up to 2.048 MHz and may be gapped to support sub-rate applications. In T1 mode, CMODE can only be logic 0 if the backplane rate is 1.544 Mbit/s (RATE[1:0]=00) and CMS=0. In E1 mode, CMODE can only be logic 0 if the backplane rate is 2.048 Mbit/s (RATE[1:0]=01) and CMS=0.

When CMODE is a logic 1, clock slave mode is selected and BRCLK is an input.

DE:

The data edge (DE) bit determines the edge of BRCLK on which BRPCM and BRSIG are generated. If DE is a logic 0, BRPCM and BRSIG are updated on the falling edge of BRCLK. If DE is a logic 1, BRPCM and BRSIG are updated on the rising edge of BRCLK.

FE:

The framing edge (FE) bit determines the edge of BRCLK on which the frame pulse (BRFP) pulse is sampled or updated. If FE is a logic 0, BRFP is sampled or updated on the falling edge of BRCLK. If FE is a logic 1, BRFP is sampled on the rising edge of BRCLK. In the case where FE is not equal to DE, BRFP is sampled or updated one clock edge before BRPCM and BRSIG.

CMS:

The clock mode select (CMS) bit determines the BRCLK frequency multiple. If CMS is a logic 0, BRCLK is at the backplane rate. If CMS is a logic 1, BRCLK is at twice the backplane rate.

RATE[1:0]:

The rate select (RATE[1:0]) bits determine the backplane rate according to the following table:

**Table 22 - Receive Backplane Rate**

| RATE[1] | RATE[0] | Backplane Rate |
|---|---|---|
| 0 | 0 | 1.544 Mbit/s |
| 0 | 1 | 2.048 Mbit/s |
| 1 | 0 | 4.096 Mbit/s |
| 1 | 1 | 8.192 Mbit/s |

The 4.096 Mbit/s and 8.192 Mbit/s rates are only supported in clock slave mode (CMODE logic 1) with RXELSTBYP logic 0.

The RATE[1:0] bits can only be set once after reset.

### Register 031H: BRIF Frame Pulse Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | MAP | 0 |
| Bit 6 | R/W | FPINV | 0 |
| Bit 5 | R/W | FPMODE | 1 |
| Bit 4 | R/W | ALTFDL | 0 |
| Bit 3 | R/W | ROHM | 0 |
| Bit 2 | R/W | BRXSMFP | 0 |
| Bit 1 | R/W | BRXCMFP | 0 |
| Bit 0 | R/W | ALTBRFP | 0 |

MAP:

The MAP bit determines the mapping of a 2.048 MHz backplane onto a 1.544 MHz line. This bit is ignored when in E1 mode (E1/T1B register bit is logic 1), when the backplane rate is 1.544 Mbit/s (RATE[1:0] = 'b00), or when in clock master mode (CMODE = 'b0).

When MAP is a logic 0, every fourth time slot is unused, starting with time slot 0. The framing bit is presented during bit 0 of time slot 0, so that only bits 1 to 7 of time slot 0 are unused.

When MAP is a logic 1, the first 24 time slots (0 to 23) are used. The framing bit is sampled during bit 7 of time slot 31 and the rest of the frame (time slots 24 to 30 and bits 0 to 6 of time slot 31) does not contain valid data.

FPINV:

The frame pulse inversion (FPINV) bit determines whether BRFP is inverted prior to sampling or presentation. If FPINV is a logic 0, BRFP is active high. If FPINV is a logic 1, BRFP is active low.

FPMODE:

The frame pulse mode (FPMODE) bit determines whether BRFP is an input or an output. When FPMODE is a logic 0, frame pulse master mode is selected, BRFP is an output and the ROHM, BRXSMFP, BRXCMFP and ALTBRFP bits determine what BRFP connotes.

When FPMODE is a logic 1, frame pulse slave mode is selected and BRFP is an input. When configured as an input, BRFP only has effect when the elastic store is in use (RXELSTBYP is logic 0); otherwise, it is ignored.

ALTFDL:

In T1 mode, the ALTFDL bit enables the framing bit position on the backplane PCM output to contain a copy of the FDL bit. When ALTFDL is set to logic 1, each M-bit value in the ESF-formatted stream is duplicated and replaces the subsequent CRC bit or F-bit in the output signal stream on BRPCM. When ALTFDL is set to logic 0, the output BRPCM stream contains the received M, CRC, or F bits in the framing bit position. Note that this function is only valid for ESF-formatted streams, ALTFDL should be set to logic 0 when other framing formats are being received.

This bit is ignored in E1 mode.

ALTBRFP:

The ALTBRFP bit suppresses every second output pulse on the backplane output BRFP. When ALTBRFP is set to logic 1 and BRXCMFP and BRXSMP bits are both logic 0, the output signal on BRFP pulses every 386 bits or 512 bits, indicating the first bit of every second frame. Under this condition, BRFP indicates the Signaling Alignment bits (S1-S6) for T1 SF, the data link bits for T1 ESF and the NFAS frames for E1. If the BRXCMFP or BRXSMFP bit is logic 1 when ALTBRFP is logic 1, the output signal on BRFP pulses every 24, 32 or 48 frames. In T1 mode, this latter setting (i.e. both ALTBRFP and BRXSMFP set to logic 1) is useful for converting SF formatted data to ESF formatted data between two COMET devices. When ALTBRFP is set to logic 0, the output signal on BRFP pulses in accordance to the ROHM, BRXCMFP and BRXSMP bit settings.

ALTBRFP has no effect if the FPMODE bit or the ROHM bit is a logic 1.

ROHM, BRXSMFP, BRXCMFP:

The ROHM, BRXSMFP and BRXCMFP bits select the output signal seen on the backplane output BRFP. These register bits only have effect if the FPMODE bit is a logic 0.

In T1 mode, only BRXSMFP has effect, the other two bits are ignored. When set to logic 1, the BRFP output pulses high during the first framing bit of the 12 frame SF or the 24 frame ESF (depending on the framing format selected in the T1-FRMR ). When BRXSMFP is set to logic 0, the BRFP output pulses high during each framing bit (i.e. every 193 bits).

The following table summarizes the configurations for E1 mode:

**Table 23 - E1 Receive Backplane Frame Pulse Configurations**

| ROHM | BRXSMFP | BRXCMFP | Result |
|---|---|---|---|
| 0 | 0 | 0 | Backplane receive frame pulse output:<br>BRFP pulses high for 1 BRCLK cycle during bit 1 of each 256-bit frame, indicating the frame alignment of the BRPCM data stream. |
| 0 | 0 | 1 | Backplane receive CRC multiframe output:<br>BRFP pulses high for 1 BRCLK cycle during bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the BRPCM data stream. (Even when CRC multiframing is disabled, the BRFP output continues to indicate the position of bit 1 of the FAS frame every 16th frame). |
| 0 | 1 | 0 | Backplane receive signaling multiframe output:<br>BRFP pulses high for 1 BRCLK cycle during bit 1 of frame 1 of the 16 frame signaling multiframe, indicating the signaling multiframe alignment of the BRPCM data stream. (Even when signaling multiframing is disabled, the BRFP output continues to indicate the position of bit 1 of every 16th frame.) |

| ROHM | BRXSMFP | BRXCMFP | Result |
|---|---|---|---|
| 0 | 1 | 1 | Backplane receive composite multiframe output:<br>BRFP goes high on the active BRCLK edge marking the beginning of bit 1 of frame 1 of every 16 frame signaling multiframe, indicating the signaling multiframe alignment of the BRPCM data stream, and returns low on the active BRCLK edge marking the end of bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the BRPCM data stream. This mode allows both multiframe alignments to be decoded externally from the single BRFP signal. Note that if the signaling and CRC multiframe alignments are coincident, BRFP will pulse high for 1 BRCLK cycle every 16 frames. |
| 1 | X | X | Backplane receive overhead output:<br>BRFP is high for timeslot 0 and timeslot 16 of each 256-bit frame, indicating the overhead of the BRPCM data stream. |

### Register 032H: BRIF Parity/F-bit Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | RPTYP | 0 |
| Bit 6 | R/W | RPTYE | 0 |
| Bit 5 | R/W | FIXF | 0 |
| Bit 4 | R/W | FIXPOL | 0 |
| Bit 3 | R/W | PTY_EXTD | 0 |
| Bit 2 | | Unused | X |
| Bit 1 | R/W | TRI[1] | 0 |
| Bit 0 | R/W | TRI[0] | 0 |

This register provides control of data integrity checking on the receive backplane interface. A single parity bit in the F-bit position represents parity over the previous frame (including the undefined bit positions). If a 2.048 Mbit/s backplane rate is selected, the parity calculation is performed over all bit positions, including the undefined positions. Signaling parity is similarly calculated over all bit positions. Parity checking and generation is not supported when the NxDS0 mode is active. Parity checking and generation is not supported when mapping a 1.544 Mbit/s signal onto a higher rate backplane in the format where the first 24 time slots are used, i.e., the RATE[1:0] bits in the BRIF Configuration register are not set to “00” and the MAP bit in the BRIF Frame Pulse Configuration register is logic 1.

RPTYP:

The receive parity type (RPTYP) bit sets even or odd parity in the receive streams. If RPTYP is a logic 0, the expected parity value in the F-bit position of BRPCM and BRSIG is even, thus it is a one if the number of ones in the previous frame is odd. If RPTYP is a logic 1, the expected parity value in the F-bit position if BRPCM and BRSIG is odd, thus it is a one if the number of ones in the previous frame is even. RPTYP only has effect if RPRTYE is a logic one.

RPRTYE:

The RPRTYE bit enables receive parity insertion. When set a logic one, parity is inserted into the F-bit position of the BRPCM and BRSIG streams. When set to logic zero, the F-bit passes through transparently.

FIXF:

If the RPRTYE bit is a logic 0, a logic 1 in the FIXF bit forces the first bit of the BRPCM frame (F-bit for T1) to the polarity specified by the FIXPOL bit.

If RPRTYE is a logic 1, FIXF has no effect. If RPRTYE and FIXF are both logic 0, the first bit of the frame passes from the line transparently.

FIXPOL:

This bit determines the logic level of the first bit of the BRPCM frame when the FIXF bit is a logic 1 and the RPRTYE bit is a logic 0. If FIXPOL is a logic 1, BRPCM will be high in the first bit of the frame. If FIXPOL is a logic 0, BRPCM will be low in the first bit of the frame.

PTY_EXTD:

The parity extend (PRY_EXTD) bit determines the scope of the parity calculation. When PTY_EXTD is logic 1, the parity is calculated over the previous frame plus the previous parity bit. When it is logic 0, the parity is calculated only over the previous frame.

TRI[1:0]:

The tri-state control bits determine when the BRPCM and BRSIG outputs are high impedance.

**Table 24 - Receive Backplane Tri-state Control**

| TRI[1] | TRI[0] | Effect |
|---|---|---|
| 0 | 0 | BRPCM and BRSIG are held high impedance. This default ensures the outputs are high impedance during reset and configuration |
| 0 | 1 | Totem-pole operation. BRPCM and BRSIG drive during the bit periods that contain valid data, i.e. every second or fourth byte for multiplexed operation. |
| 1 | 0 | Open-drain operation. BRPCM and BRSIG are driven low to indicate a zero. BRPCM and BRSIG are high impedance otherwise. |
| 1 | 1 | Reserved |

### Register 033H: BRIF Time Slot Offset

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | R/W | TSOFF[6] | 0 |
| Bit 5 | R/W | TSOFF[5] | 0 |
| Bit 4 | R/W | TSOFF[4] | 0 |
| Bit 3 | R/W | TSOFF[3] | 0 |
| Bit 2 | R/W | TSOFF[2] | 0 |
| Bit 1 | R/W | TSOFF[1] | 0 |
| Bit 0 | R/W | TSOFF[0] | 0 |

TSOFF[6:0]:

The time slot offset (TSOFF[6:0]) bits give a binary representation of the fixed byte offset between the backplane receive frame pulse (BRFP) and the start of the next frame on the backplane receive data signal (BRPCM). The seven bits can give an offset from 0 - 127 bytes. With a data rate of 2.048 Mbit/s, every byte on BRPCM is driven. With a data rate of 4.096 Mbit/s, every second byte on BRPCM is driven. With a data rate of 8.192 Mbit/s, every fourth byte on BRPCM is driven.

### Register 034H: BRIF Bit Offset

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | R/W | BOFF_EN | 0 |
| Bit 2 | R/W | BOFF[2] | 0 |
| Bit 1 | R/W | BOFF[1] | 0 |
| Bit 0 | R/W | BOFF[0] | 0 |

BOFF_EN:

The bit offset enable (BOFF_EN) bit is used to enable the bit offset bits. If BOFF_EN is a logic 0, the bit offset is disabled and there is no bit offset between the frame pulse and the first bit of the first time slot. In this case, the BOFF[2:0] bits are ignored. If BOFF_EN is a logic 1, the bit offset is enabled and the BOFF[2:0] bits operate as described below.

BOFF[2:0]:

The bit offset (BOFF[2:0]) bits gives a binary representation of the fixed offset between the backplane receive frame pulse (BRFP) and the start of the first bit of the first time slot. This binary representation is then used to determine the BRCLK edge, defined as CET (clock edge transmit) on which the first bit of the first time slot is sampled. For example, if CET is 4, the data on BRPCM and BRSIG is sampled on the fourth clock edge after BRFP is sampled (see Figure 11). The following tables show the relationship between BOFF[2:0], FE, DE and CER.

**Table 25 - Receive Backplane Bit Offset for CMS = 0**

| FE | DE | BOFF[2:0] | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 | |
| 0 | 0 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | |
| 0 | 1 | 3 | 5 | 7 | 9 | 11 | 13 | 15 | 17 | CET |
| 1 | 0 | 3 | 5 | 7 | 9 | 11 | 13 | 15 | 17 | |
| 1 | 1 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | |

**Table 26 - Receive Backplane Bit Offset for CMS = 1**

| FE | DE | BOFF[2:0] | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 | |
| 0 | 0 | 4 | 8 | 12 | 16 | 20 | 24 | 28 | 32 | |
| 0 | 1 | 3 | 7 | 11 | 15 | 19 | 23 | 27 | 31 | CET |
| 1 | 0 | 3 | 7 | 11 | 15 | 19 | 23 | 27 | 31 | |
| 1 | 1 | 4 | 8 | 12 | 16 | 20 | 24 | 28 | 32 | |

The above tables are consistent with the convention established by the Concentration Highway Interface (CHI) specification.

Note that in the case where FE is logic 0, DE is logic 1 and BRFP is configured for a superframe/multiframe mode, the maximum offset is one frame less two bits, rather than one frame less one bit as in all other configurations. In this configuration, the maximum offset is 191 bits at 1.544 Mbit/s, 254 bits at 2.048 Mbit/s, 510 bits at 4.096 Mbit/s and 1022 bits at 8.192 Mbit/s.

### Register 038H: TXCI Transmit Data Link 1 Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | DL1_EVEN | 0 |
| Bit 6 | R/W | DL1_ODD | 0 |
| Bit 5 | R/W | T1_DL_EN | 1 |
| Bit 4 | R/W | DL1_TS[4] | 0 |
| Bit 3 | R/W | DL1_TS[3] | 0 |
| Bit 2 | R/W | DL1_TS[2] | 0 |
| Bit 1 | R/W | DL1_TS[1] | 0 |
| Bit 0 | R/W | DL1_TS[0] | 0 |

This register, along with the TXCI Data Link 1 Bit Select register, controls the insertion of the data link generated by TDPR #1. Refer to the "Using the Internal HDLC Transmitters" description in the Operation section for details on terminating HDLC frames.

DL1_EVEN:

The data link 1 even select (DL1_EVEN) bit controls whether or not the first data link is inserted into the even frames of the receive data stream. If DL1_EVEN is a logic 0, the data link is not inserted into the even frames. If DL1_EVEN is a logic 1, the data link is inserted into the even frames. In E1 mode, the frames in an E1 CRC-4 multiframe are considered to be numbered from 0 to 15; in T1 mode, the frames in a superframe are considered to be numbered from 1 to 12 (or 1 to 24 in an extended superframe).

DL1_ODD:

The data link 1 odd select (DL1_ODD) bit controls whether or not the first data link is inserted into the odd frames of the receive data stream. If DL1_ODD is a logic 0, the data link is not inserted into the odd frames. If DL1_ODD is a logic 1, the data link is inserted into the odd frames.

T1_DL_EN:

The T1 data link enable bit allows the generation of the ESF or T1DM data links when in T1 mode. If T1_DL_EN is a logic 1, the ESF, FMS1 and FMS0 bits of the T1 FRMR Configuration register determine the bit locations into which the data link is inserted. When the T1_DL_EN bit is a logic 1, the DL1_EVEN and DL1_ODD bits must both be set to logic 0. This bit must be set to logic 0 when in E1 mode.

DL1_TS[4:0]:

The data link 1 time slot (DL1_TS[4:0]) bits gives a binary representation of the time slot/channel into which the data link is to be inserted. Note that T1 channels 1 to 24 are mapped to values 0 to 23. The DL1_TS[4:0] bits have no effect when DL1_EVEN and DL1_ODD are both a logic 0.

### Register 039H: TXCI Transmit Data Link 1 Bit Select

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | DL1_BIT[7] | 0 |
| Bit 6 | R/W | DL1_BIT[6] | 0 |
| Bit 5 | R/W | DL1_BIT[5] | 0 |
| Bit 4 | R/W | DL1_BIT[4] | 0 |
| Bit 3 | R/W | DL1_BIT[3] | 0 |
| Bit 2 | R/W | DL1_BIT[2] | 0 |
| Bit 1 | R/W | DL1_BIT[1] | 0 |
| Bit 0 | R/W | DL1_BIT[0] | 0 |

DL1_BIT[7:0]:

The data link 1 bit select (DL1_BIT[7:0]) bits controls into which bits of the time slot/channel data from TDPR #1 are to be inserted. If DL1_BIT[x] is a logic 1, the data link is inserted into that bit. To insert the data link into the entire time slot, all eight DL1_BIT[x] bits must be set to a logic 1. DL1_BIT[7] corresponds to the most significant bit (bit 1, the first bit transmitted) of the time slot and DL1_BIT[0] corresponds to the least significant bit (bit 8, the last bit transmitted) of the time slot. The DL1_BIT[7:0] bits have no effect when the DL1_EVEN and DL1_ODD bits of the TXCI Data Link 1 Control register are both logic 0.

### Register 03AH: TXCI Transmit Data Link 2 Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | DL2_EVEN | 0 |
| Bit 6 | R/W | DL2_ODD | 0 |
| Bit 5 | | Unused | X |
| Bit 4 | R/W | DL2_TS[4] | 0 |
| Bit 3 | R/W | DL2_TS[3] | 0 |
| Bit 2 | R/W | DL2_TS[2] | 0 |
| Bit 1 | R/W | DL2_TS[1] | 0 |
| Bit 0 | R/W | DL2_TS[0] | 0 |

This register, along with the TXCI Data Link 2 Bit Select register, controls the insertion of the data link generated by TDPR #2. Refer to the "Using the Internal HDLC Transmitters" description in the Operation section for details on terminating HDLC frames.

DL2_EVEN:

The data link 2 even select (DL2_EVEN) bit controls whether or not the second data link is inserted into the even frames of the receive data stream. If DL2_EVEN is a logic 0, the data link is not inserted into the even frames. If DL2_EVEN is a logic 1, the data link is inserted into the even frames. In E1 mode, the frames in an E1 CRC-4 multiframe are considered to be numbered from 0 to 15; in T1 mode, the frames in a superframe are considered to be numbered from 1 to 12 (or 1 to 24 in an extended superframe).

DL2_ODD:

The data link 2 odd select (DL2_ODD) bit controls whether or not the second data link is inserted into the odd frames of the receive data stream. If DL2_ODD is a logic 0, the data link is not inserted into the odd frames. If DL2_ODD is a logic 1, the data link is inserted into the odd frames.

DL2_TS[4:0]:

The data link 2 time slot (DL2_TS[4:0]) bits gives a binary representation of the time slot/channel into which the data link is to be inserted. Note that T1 channels 1 to 24 are mapped to values 0 to 23. The DL2_TS[4:0] bits have no effect when DL2_EVEN and DL2_ODD are both a logic 0.

### Register 03BH: TXCI Transmit Data Link 2 Bit Select

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | DL2_BIT[7] | 0 |
| Bit 6 | R/W | DL2_BIT[6] | 0 |
| Bit 5 | R/W | DL2_BIT[5] | 0 |
| Bit 4 | R/W | DL2_BIT[4] | 0 |
| Bit 3 | R/W | DL2_BIT[3] | 0 |
| Bit 2 | R/W | DL2_BIT[2] | 0 |
| Bit 1 | R/W | DL2_BIT[1] | 0 |
| Bit 0 | R/W | DL2_BIT[0] | 0 |

DL2_BIT[7:0]:

The data link 2 bit select (DL2_BIT[7:0]) bits controls into which bits of the time slot/channel data from TDPR #2 are to be inserted. If DL2_BIT[x] is a logic 1, the data link is inserted into that bit. To insert the data link into the entire time slot, all eight DL2_BIT[x] bits must be set to a logic 1. DL2_BIT[7] corresponds to the most significant bit (bit 1, the first bit transmitted) of the time slot and DL2_BIT[0] corresponds to the least significant bit (bit 8, the last bit transmitted) of the time slot. The DL2_BIT[7:0] bits have no effect when the DL2_EVEN and DL2_ODD bits of the TXCI Data Link 2 Control register are both logic 0.

### Register 03CH: TXCI Transmit Data Link 3 Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | DL3_EVEN | 0 |
| Bit 6 | R/W | DL3_ODD | 0 |
| Bit 5 | | Unused | X |
| Bit 4 | R/W | DL3_TS[4] | 0 |
| Bit 3 | R/W | DL3_TS[3] | 0 |
| Bit 2 | R/W | DL3_TS[2] | 0 |
| Bit 1 | R/W | DL3_TS[1] | 0 |
| Bit 0 | R/W | DL3_TS[0] | 0 |

This register, along with the TXCI Data Link 3 Bit Select register, controls the insertion of the data link generated by TDPR #3. Refer to the "Using the Internal HDLC Transmitters" description in the Operation section for details on terminating HDLC frames.

DL3_EVEN:

The data link 3 even select (DL3_EVEN) bit controls whether or not the third data link is inserted into the even frames of the receive data stream. If DL3_EVEN is a logic 0, the data link is not inserted into the even frames. If DL3_EVEN is a logic 1, the data link is inserted into the even frames. In E1 mode, the frames in an E1 CRC-4 multiframe are considered to be numbered from 0 to 15; in T1 mode, the frames in a superframe are considered to be numbered from 1 to 12 (or 1 to 24 in an extended superframe).

DL3_ODD:

The data link 3 odd select (DL3_ODD) bit controls whether or not the third data link is inserted into the odd frames of the receive data stream. If DL3_ODD is a logic 0, the data link is not inserted into the odd frames. If DL3_ODD is a logic 1, the data link is inserted into the odd frames.

DL3_TS[4:0]:

The data link 3 time slot (DL3_TS[4:0]) bits gives a binary representation of the time slot/channel into which the data link is to be inserted. Note that T1 channels 1 to 24 are mapped to values 0 to 23. The DL3_TS[4:0] bits have no effect when DL3_EVEN and DL3_ODD are both a logic 0.

### Register 03DH: TXCI Transmit Data Link 3 Bit Select

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | DL3_BIT[7] | 0 |
| Bit 6 | R/W | DL3_BIT[6] | 0 |
| Bit 5 | R/W | DL3_BIT[5] | 0 |
| Bit 4 | R/W | DL3_BIT[4] | 0 |
| Bit 3 | R/W | DL3_BIT[3] | 0 |
| Bit 2 | R/W | DL3_BIT[2] | 0 |
| Bit 1 | R/W | DL3_BIT[1] | 0 |
| Bit 0 | R/W | DL3_BIT[0] | 0 |

DL3_BIT[7:0]:

The data link 3 bit select (DL3_BIT[7:0]) bits controls into which bits of the time slot/channel data from TDPR #3 are to be inserted. If DL3_BIT[x] is a logic 1, the data link is inserted into that bit. To insert the data link into the entire time slot, all eight DL3_BIT[x] bits must be set to a logic 1. DL3_BIT[7] corresponds to the most significant bit (bit 1, the first bit transmitted) of the time slot and DL3_BIT[0] corresponds to the least significant bit (bit 8, the last bit transmitted) of the time slot. The DL3_BIT[7:0] bits have no effect when the DL3_EVEN and DL3_ODD bits of the TXCI Data Link 3 Control register are both logic 0.

### Register 040H: BTIF Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | NXDS0[1] | 0 |
| Bit 6 | R/W | NXDS0[0] | 0 |
| Bit 5 | R/W | CMODE | 1 |
| Bit 4 | R/W | DE | 1 |
| Bit 3 | R/W | FE | 1 |
| Bit 2 | R/W | CMS | 0 |
| Bit 1 | R/W | RATE[1] | 0 |
| Bit 0 | R/W | RATE[0] | 0 |

NXDS0[1:0]:

The NXDS0[1:0] bits determine the mode of operation when BTCLK clock master mode is selected (CMODE logic 0), as shown in the following table. Note that these bits are ignored when clock slave mode is selected (CMODE logic 1).

**Table 27 - Transmit Backplane NXDS0 Mode Selection**

| NXDS0[1] | NXDS0[0] | Operation |
|---|---|---|
| 0 | 0 | Full Frame |
| 0 | 1 | 56 kbit/s NxDS0 |
| 1 | 0 | 64 kbit/s NxDS0 |
| 1 | 1 | 64 kbit/s NxDS0 with F-bit (only valid for E1 mode) |

When in Full Frame mode, the entire frame (193 bits for T1 or 256 bits for E1) is sampled from the backplane.

When in any of the NxDS0 modes, only those time slots with their IDLE_DS0 bit cleared (logic 0) are sampled from the backplane. The other time slots, with their IDLE_DS0 bit set (logic 1), do not contain valid data and will be overwritten with the per-DS0 idle code. The IDLE_DS0 bits are located in the TPSC Indirect registers. When in T1 mode, the clock is always gapped during the framing bit position.

When the 56 kbit/s NxDS0 mode is selected, only the first 7 bits of the selected time slots are sampled from the backplane and the 8th bit is gapped out. When the 64 kbit/s NxDS0 mode is selected, all 8 bits of the selected time slots are sampled from the backplane.

The 64 kbit/s NxDS0 with F-bit mode is intended to support ITU recommendation G.802. This mode is only valid when the E1/T1B register bit is a logic 1 (E1 mode is selected). The operation is the same as the 64 kbit/s NxDS0 mode, except that the framing bit is sampled. The F-bit is always sampled during the first bit of time slot 26. The remaining seven bits of time slot 26 are not sampled. To properly insert a G.802 formatted T1, the IDLE_DS0 bits must be set to logic 0 for time slots 1 through 15 and 17 through 26, and the IDLE_DS0 bits must be set to logic 1 for time slots 27 through 31.

CMODE:

The clock mode (CMODE) bit determines whether the BTCLK pin is an input or output. When CMODE is a logic 0, clock master mode is selected and the BTCLK output is derived from the integral clock synthesizer. Depending on the mode of operation, BTCLK may have a burst frequency of up to 2.048 MHz and may be gapped to support sub-rate applications. In T1 mode, CMODE can only be logic 0 if the backplane rate is 1.544 Mbit/s (RATE[1:0]=00) and CMS=0. In E1 mode, CMODE can only be logic 0 if the backplane rate is 2.048 Mbit/s (RATE[1:0]=01) and CMS=0.

When CMODE is a logic 1, clock slave mode is selected and BTCLK is an input.

DE:

The data edge (DE) bit determines the edge of BTCLK on which BTPCM and BTSIG are sampled. If DE is a logic 0, BTPCM and BTSIG are sampled on the falling edge of BTCLK. If DE is a logic 1, BTPCM and BTSIG are sampled on the rising edge of BTCLK.

FE:

The framing edge (FE) bit determines the edge of BTCLK on which the frame pulse (BTFP) pulse is sampled or updated. If FE is a logic 0, BTFP is sampled or updated on the falling edge of BTCLK. If FE is a logic 1, BTFP is sampled or updated on the rising edge of BTCLK. In the case where FE is not equal to DE, BTFP is sampled one clock edge or updated three clock edges before BTPCM and BTSIG are sampled.

CMS:

The clock mode select (CMS) bit determines the BTCLK frequency multiple. If CMS is a logic 0, BTCLK is at the backplane rate. If CMS is a logic 1,

BTCLK is at twice the backplane rate. CMS must be programmed to logic 0 when CMODE=0.

RATE[1:0]:

The rate select (RATE[1:0]) bits determine the backplane rate according to the following table:

**Table 28 - Transmit Backplane Rate**

| RATE[1] | RATE[0] | Backplane Rate |
|---|---|---|
| 0 | 0 | 1.544 Mbit/s |
| 0 | 1 | 2.048 Mbit/s |
| 1 | 0 | 4.096 Mbit/s |
| 1 | 1 | 8.192 Mbit/s |

The 4.096 Mbit/s and 8.192 Mbit/s rates are only supported in clock slave mode (CMODE logic 1).

The RATE[1:0] bits can only be set once after reset.

### Register 041H: BTIF Frame Pulse Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | MAP | 0 |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | R/W | FPINV | 0 |
| Bit 2 | R/W | ESF_EN | 0 |
| Bit 1 | R/W | FPTYP | 0 |
| Bit 0 | R/W | FPMODE | 1 |

MAP:

The MAP bit determines the mapping of a 2.048 MHz backplane onto a 1.544 MHz line. This bit is ignored when in E1 mode (E1/T1B register bit is logic 1), when the backplane rate is 1.544 Mbit/s (RATE[1:0] = 'b00), or when in clock master mode (CMODE = 'b0).

When MAP is a logic 0, every fourth time slot is unused, starting with time slot 0. The framing bit is sampled during bit 0 of time slot 0, so that only bits 1 to 7 of time slot 0 are ignored.

When MAP is a logic 1, the first 24 time slots (0 to 23) are sampled. The framing bit is sampled during bit 7 of time slot 31 and the rest of the frame (time slots 24 to 30 and bits 0 to 6 of time slot 31) are ignored.

FPINV:

The frame pulse inversion (FPINV) bit determines whether BTFP is inverted prior to sampling. If FPINV is a logic 0, BTFP is active high. If FPINV is a logic 1, BTFP is active low. Frame pulse inversion cannot be used when BTFP is configured as an output (FPMODE is a logic 0).

ESF_EN:

The extended superframe enable (ESF_EN) bit determines which superframe alignment is used when in T1 mode and FPTYP is a logic 1. When ESF_EN is a logic 0, superframe alignment is chosen and BTFP pulses (FPMODE logic 0) or is expected (FPMODE logic 1) every 12 frames. When ESF_EN is a logic 1, extended superframe alignment is chosen and pulses (FPMODE logic 0) or is expected (FPMODE logic 1) every 24 frames.

This bit is ignored when in E1 mode or in T1 mode when FPTYP is a logic 0.

FPTYP:

The frame pulse type (FPTYP) bit determines the type of frame pulse on BTFP. When FPTYP is a logic 0, basic frame alignment is chosen and frame pulses occur every frame. When FPTYP is a logic 1, multiframe alignment is chosen.

In T1 mode, with multiframe alignment pulses (FPMODE logic 0) or is expected (FRMODE logic 1) every 12 or 24 frames as determined by the ESF_EN bit.

In E1 mode, with multiframe alignment when FPMODE is a logic 0, as an output BTFP pulses once every 16 frames to indicate both CRC and signaling multiframe alignment. When BTFP is configured as an input, must be brought high to mark bit 1 of frame 1 of every 16 frame signaling multiframe and brought low following bit 1 of frame 1 of every 16 frame CRC multiframe.

To properly initialize the transmit HDLC controllers in basic frame alignment mode (FPTYP is logic 0), multiframe alignment (FPTYP is logic 1) must be configured for at least one multiframe (i.e., for at least one multiframe period in frame pulse master mode or for at least one input frame pulse in frame pulse slave mode). After this initialization, the FPTYP can be set to any desired value.

FPMODE:

The frame pulse mode (FPMODE) bit determines whether BTFP is an input or an output. When FPMODE is a logic 0, frame pulse master mode is selected and BTFP is an output. When FPMODE is a logic 1, frame pulse slave mode is selected and BTFP is an input. Frame pulse master mode cannot be used with transmit backplane clock rates greater than 2.048 MHz.

### Register 042H: BTIF Parity Configuration and Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | TPTYP | 0 |
| Bit 6 | R/W | TPTYE | 0 |
| Bit 5 | R | TDI | X |
| Bit 4 | R | TSIGI | X |
| Bit 3 | R/W | PTY_EXTD | 0 |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | | Unused | X |

This register provides control and status reporting of data integrity checking on the transmit backplane interface. A single parity bit in the F-bit position represents parity over the previous frame (including the undefined bit positions). Parity checking and generation is not supported when the NxDS0 mode is active. Parity checking and generation is not supported when mapping a 1.544 Mbit/s signal onto a higher rate backplane in the format where the first 24 time slots are used, i.e., the RATE[1:0] bits in the BTIF Configuration register are not set to “00” and the MAP bit in the BTIF Frame Pulse Configuration register is logic 1.

TPTYP:

The transmit parity type (TPTYP) bit sets even or odd parity in the transmit streams. If TPTYP is a logic 0, the expected parity value in the F-bit position of BTPCM and BTSIG is even, thus it is a one if the number of ones in the previous frame is odd. If TPTYP is a logic 1, the expected parity value in the F-bit position if BTPCM and BTSIG is odd, thus it is a one if the number of ones in the previous frame is even.

TPTYE:

The transmit parity enable (TPTYE) bit enables transmit parity interrupts. When TPTYE is a logic 1, parity errors on the inputs BTPCM and BTSIG are indicated by the TDI and TSIGI bits, respectively, and by the assertion low of the INTB output. When TPTYE is a logic 0, parity errors are indicated by the TDI and TSIGI bits but are not indicated on the INTB output.

TDI:

The transmit data interrupt (TDI) bit indicates if a parity error has been detected on the BTPCM input. This bit is cleared when this register is read.

TSIGI:

The transmit signaling interrupt (TSIGI) bit indicated if a parity error has been detected on the BTSIG input. This bit is cleared when this register is read.

PTY_EXTD:

The parity extend (PRY_EXTD) bit causes the parity to be calculated over the previous frame plus the previous parity bit, instead of only the previous frame.

### Register 043H: BTIF Time Slot Offset

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | R/W | TSOFF[6] | 0 |
| Bit 5 | R/W | TSOFF[5] | 0 |
| Bit 4 | R/W | TSOFF[4] | 0 |
| Bit 3 | R/W | TSOFF[3] | 0 |
| Bit 2 | R/W | TSOFF[2] | 0 |
| Bit 1 | R/W | TSOFF[1] | 0 |
| Bit 0 | R/W | TSOFF[0] | 0 |

TSOFF[6:0]:

The time slot offset (TSOFF[6:0]) bits give a binary representation of the fixed byte offset between the backplane transmit frame pulse (BTFP) and the start of the next frame on the backplane transmit data signal (BTPCM). The seven bits can give an offset from 0 - 127 bytes. With a data rate of 2.048 Mbit/s, every byte on BTPCM is sampled. With a data rate of 4.096 Mbit/s, every second byte on BTPCM is sampled. With a data rate of 8.192 Mbit/s, every fourth byte on BTPCM is sampled.

### Register 044H: BTIF Bit Offset

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | R/W | BOFF_EN | 0 |
| Bit 2 | R/W | BOFF[2] | 0 |
| Bit 1 | R/W | BOFF[1] | 0 |
| Bit 0 | R/W | BOFF[0] | 0 |

BOFF_EN:

The bit offset enable (BOFF_EN) bit is used to enable the bit offset bits. If BOFF_EN is a logic 0, the bit offset is disabled and there is no bit offset between the frame pulse and the first bit of the first time slot. In this case, the BOFF[2:0] bits are ignored. If BOFF_EN is a logic 1, the bit offset is enabled and the BOFF[2:0] bits operate as described below.

BOFF[2:0]:

The bit offset (BOFF[2:0]) bits gives a binary representation of the fixed offset between the backplane transmit frame pulse (BTFP) and the start of the first bit of the first time slot. This binary representation is then used to determine the BTCLK edge, defined as CER (clock edge receive) on which the first bit of the first time slot is sampled. For example, if CER is 4, the data on BTPCM and BTSIG is sampled on the fourth clock edge after BTFP is sampled (see Figure 11). The following tables show the relationship between BOFF[2:0], FE, DE and CER.

**Table 29 - Transmit Backplane Bit Offset for CMS = 0**

| FE | DE | BOFF[2:0] | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 | |
| 0 | 0 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | |
| 0 | 1 | 3 | 5 | 7 | 9 | 11 | 13 | 15 | 17 | CER |
| 1 | 0 | 3 | 5 | 7 | 9 | 11 | 13 | 15 | 17 | |
| 1 | 1 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | |

**Table 30 - Transmit Backplane Bit Offset for CMS = 1**

| FE | DE | BOFF[2:0] | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 | |
| 0 | 0 | 6 | 10 | 14 | 18 | 22 | 26 | 30 | 34 | |
| 0 | 1 | 7 | 11 | 15 | 19 | 23 | 27 | 31 | 35 | CER |
| 1 | 0 | 7 | 11 | 15 | 19 | 23 | 27 | 31 | 35 | |
| 1 | 1 | 6 | 10 | 14 | 18 | 22 | 26 | 30 | 34 | |

The above tables are consistent with the convention established by the Concentration Highway Interface (CHI) specification.

### Register 048H: T1 FRMR Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | M2O[1] | 0 |
| Bit 6 | R/W | M2O[0] | 0 |
| Bit 5 | R/W | ESFFA | 0 |
| Bit 4 | R/W | ESF | 0 |
| Bit 3 | R/W | FMS1 | 0 |
| Bit 2 | R/W | FMS0 | 0 |
| Bit 1 | R/W | JPN | 0 |
| Bit 0 | | Unused | X |

When the E1/T1B bit of the Global Configuration register is a logic 1 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

This register selects the framing format and the frame loss criteria used by the T1-FRMR.

M2O[1:0]:

The M2O[1:0] bits select the ratio of errored to total framing bits before declaring out of frame in SF, SLC®96, and ESF framing formats. A logic 00 selects 2 of 4 framing bits in error; a logic 01 selects 2 of 5 bits in error; a logic 10 selects 2 of 6 bits in error. In T1DM framing format, the ratio of errored to total framing bits before declaring out of frame is always 4 out of 12. A logic 11 in the M2O[1:0] bits is reserved and should not be used.

ESFFA:

The ESFFA bit selects one of two framing algorithms for ESF frame search in the presence of mimic framing patterns in the incoming data. A logic 0 selects the ESF algorithm where the FRMR does not declare inframe while more than one framing bit candidate is following the framing pattern in the incoming data. A logic 1 selects the ESF algorithm where a CRC-6 calculation is performed on each framing bit candidate, and is compared against the CRC bits associated with the framing bit candidate to determine the most likely framing bit position.

ESF:

The ESF bit selects either extended superframe format or enables the Frame Mode Select bits to select either standard superframe, T1DM, or SLC®96

framing formats. A logic 1 in the ESF bit position selects ESF; a logic 0 bit enables FMS1 and FMS0 to select SF, T1DM, or SLC®96.

FMS1,FMS0:

The FMS1 and FMS0 bits select standard superframe, T1DM, or SLC®96 framing formats. A logic 00 in these bits enable the SF framing format; a logic 01 or 11 in these bit positions enable the T1DM framing format; a logic 10 in these bit positions enable the SLC®96 framing format. When ESF is selected (ESF bit set to logic 1), the FMS1 and FMS0 bits select the data rate and the source channel for the facility data link data. A logic 00 in these bits enable the FRMR to receive FDL data at the full 4 kHz rate from every odd frame. When ESF is selected, FMS1 and FMS0 settings other than logic 00 are reserved and should not be used.

The valid combinations of the ESF, FMS1, and FMS0 bits are summarized in the table below:

**Table 31 - T1 Framing Modes**

| ESF | FMS1 | FMS0 | Mode |
|---|---|---|---|
| 0 | 0 | 0 | Select SF framing format |
| 0 | 0 | 1 | Select T1DM framing format |
| 0 | 1 | 0 | Select SLC96 framing format |
| 0 | 1 | 1 | Select T1DM framing format |
| 1 | 0 | 0 | Select ESF framing format & 4 kHz FDL Data Rate |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

JPN:

The JPN bit enables Japanese variations of the standard framing formats. If the JPN bit is a logic 1 and the ESF format is selected (ESF bit is logic 1), the T1-FRMR complies to TTC JT-G704. If the JPN bit is a logic 1 and a non-ESF format is selected (ESF bit is logic 0), it is assumed the $12^{th}$ F-bit of the superframe carries a far end receive failure alarm. The alarm is extracted and the framing is modified to be robust when the alarm is active.

### Register 049H: T1 FRMR Interrupt Enable

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | R/W | Reserved | 0 |
| Bit 5 | R/W | COFAE | 0 |
| Bit 4 | R/W | FERE | 0 |
| Bit 3 | R/W | BEEE | 0 |
| Bit 2 | R/W | SFEE | 0 |
| Bit 1 | R/W | MFPE | 0 |
| Bit 0 | R/W | INFRE | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 1 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

This register selects which of the MFP, COFA, FER, BEE, SFE or INFR events generates an interrupt on the microprocessor INTB pin when their state changes or their event condition is detected.

Reserved:

The Reserved bit is used for production test purposes only. The Reserved bit must be programmed to logic 0 for normal operation.

COFAE:

The COFAE bit enables the generation of an interrupt when the frame find circuitry determines that frame alignment has been achieved and that the new alignment differs from the previous alignment. When COFAE is set to logic 1, the declaration of a change of frame alignment is allowed to generate an interrupt. When COFAE is set to logic 0, a change in the frame alignment does not generate an interrupt on the INTB pin.

FERE:

The FERE bit enables the generation of an interrupt when a framing bit error has been detected. When FERE is set to logic 1, the detection of a framing bit error is allowed to generate an interrupt. When FERE is set to logic 0, any error in the framing bits does not generate an interrupt on the INTB pin.

BEEE:

The BEEE bit enables the generation of an interrupt when a bit error event has been detected. A bit error event is defined as framing bit errors for SF formatted data, CRC-6 mismatch errors for ESF formatted data, Ft bit errors for SLC®96 formatted data, and either framing bit errors or sync word errors for T1DM formatted data. When BEEE is set to logic 1, the detection of a bit error event is allowed to generate an interrupt. When BEEE is set to logic 0, bit error events are disabled from generating an interrupt on the INTB pin.

SFEE:

The SFEE bit enables the generation of an interrupt when a severely errored framing event has been detected. A severely errored framing event is defined as 2 or more framing bit errors during the current superframe for SF, ESF, or SLC®96 formatted data, and 2 or more framing bit errors or sync word errors during the current superframe for T1DM formatted data. When SFEE is set to logic 1, the detection of a severely errored framing event is allowed to generate an interrupt. When SFEE is set to logic 0, severely errored framing events are disabled from generating an interrupt on the INTB pin.

MFPE:

The MFPE bit enables the generation of an interrupt when the frame find circuitry detects the presence of framing bit mimics. The occurrence of a mimic is defined as more than one framing bit candidate following the frame alignment pattern. When MFPE is set to logic 1, the assertion or deassertion of the detection of a mimic is allowed to generate an interrupt. When MFPE is set to logic 0, the detection of a mimic framing pattern is disabled from generating an interrupt on the INTB pin.

INFRE:

The INFRE bit enables the generation of an interrupt when the frame find circuitry determines that frame alignment has been achieved and that the framer is now "inframe". When INFRE is set to logic 1, the assertion or deassertion of the "inframe" state is allowed to generate an interrupt. When INFRE is set to logic 0, a change in the "inframe" state is disabled from generating an interrupt on the INTB pin.

Upon reset of the COMET, these bits are set to logic 0, disabling the generation of interrupts on the INTB pin.

### Register 04AH: T1 FRMR Interrupt Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | COFAI | 0 |
| Bit 6 | R | FERI | 0 |
| Bit 5 | R | BEEI | 0 |
| Bit 4 | R | SFEI | 0 |
| Bit 3 | R | MFPI | 0 |
| Bit 2 | R | INFRI | 0 |
| Bit 1 | R | MFP | 0 |
| Bit 0 | R | INFR | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 1 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

This register indicate whether a change of frame alignment, a framing bit error, a bit error event, or a severely errored framing event generated an interrupt. This register also indicates whether a mimic framing pattern was detected or whether there was a change in the "inframe" state of the frame circuitry.

COFAI, FERI, BEEI, SFEI:

A logic 1 in the status bit positions COFAI, FERI, BEEI and SFEI indicate that the occurrence of the corresponding event generated an interrupt; a logic 0 in the status bit positions COFAI, FERI, BEEI, and SFEI indicate that the corresponding event did not generate an interrupt.

MFPI:

A logic 1 in the MFPI status bit position indicates that the assertion or deassertion of the mimic detection indication has generated an interrupt; a logic 0 in the MFPI bit position indicates that no change in the state of the mimic detection indication occurred.

INFRI:

A logic 1 in the INFRI status bit position indicates that a change in the "inframe" state of the frame alignment circuitry generated an interrupt; a logic 0 in the INFRI status bit position indicates that no state change occurred.

MFP, INFR:

The bit position MFP and INFR indicate the current state of the mimic detection and of the frame alignment circuitry.

The interrupt and the status bit positions (COFAI, FERI, BEEI, SFEI, MFPI, and INFRI) are cleared to logic 0 when this register is read.

### Register 04CH: IBCD Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | Reserved | 0 |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | R/W | DSEL1 | 0 |
| Bit 2 | R/W | DSEL0 | 0 |
| Bit 1 | R/W | ASEL1 | 0 |
| Bit 0 | R/W | ASEL0 | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register provides the selection of the Activate and De-activate loopback code lengths (from 3 bits to 8 bits) as follows:

**Table 32 - Loopback Code Configurations**

| DEACTIVATE Code | | ACTIVATE Code | | |
|---|---|---|---|---|
| **DSEL1** | **DSEL0** | **ASEL1** | **ASEL0** | **CODE LENGTH** |
| 0 | 0 | 0 | 0 | 5 bits |
| 0 | 1 | 0 | 1 | 6 (or 3*) bits |
| 1 | 0 | 1 | 0 | 7 bits |
| 1 | 1 | 1 | 1 | 8 (or 4*) bits |

**Note:**

3-bit and 4-bit code sequences can be accommodated by configuring the IBCD for 6 or 8 bits and by programming two repetitions of the code sequence.

The Reserved bit is used for production test purposes only. The Reserved bit must be programmed to logic 0 for normal operation.

### Register 04DH: IBCD Interrupt Enable/Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | LBACP | 0 |
| Bit 6 | R | LBDCP | 0 |
| Bit 5 | R/W | LBAE | 0 |
| Bit 4 | R/W | LBDE | 0 |
| Bit 3 | R | LBAI | 0 |
| Bit 2 | R | LBDI | 0 |
| Bit 1 | R | LBA | 0 |
| Bit 0 | R | LBD | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

LBACP, LBDCP:

The LBACP and LBDCP bits indicate when the corresponding loopback code is present during a 39.8 ms interval.

LBAE:

The LBAE bit enables the assertion or deassertion of the inband Loopback Activate (LBA) detect indication to generate an interrupt on the microprocessor INTB pin. When LBAE is set to logic 1, any change in the state of the LBA detect indication generates an interrupt. When LBAE is set to logic 0, no interrupt is generated by changes in the LBA detect state.

LBDE:

The LBDE bit enables the assertion or deassertion of the inband Loopback Deactivate (LBD) detect indication to generate an interrupt on the microprocessor INTB pin. When LBDE is set to logic 1, any change in the state of the LBD detect indication generates an interrupt. When LBDE is set to logic 0, no interrupt is generated by changes in the LBD detect state.

LBAI, LBDI:

The LBAI and LBDI bits indicate which of the two expected loopback codes generated the interrupt when their state changed. A logic 1 in these bit positions indicate that a state change in that code has generated an interrupt; a logic 0 in these bit positions indicate that no state change has occurred.

LBA, LBD:

The LBA and LBD bits indicate the current state of the corresponding loopback code detect indication. A logic 1 in these bit positions indicate the presence of that code has been detected; a logic 0 in these bit positions indicate the absence of that code.

### Register 04EH: IBCD Activate Code

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | ACT7 | 0 |
| Bit 6 | R/W | ACT6 | 0 |
| Bit 5 | R/W | ACT5 | 0 |
| Bit 4 | R/W | ACT4 | 0 |
| Bit 3 | R/W | ACT3 | 0 |
| Bit 2 | R/W | ACT2 | 0 |
| Bit 1 | R/W | ACT1 | 0 |
| Bit 0 | R/W | ACT0 | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This 8-bit register selects the Activate code sequence that is to be detected. If the code sequence length is less than 8 bits, the first 8 bits of several repetitions of the code sequence must be used to fill the 8-bit register. For example, if code sequence is a repeating 00001, the first 8 bits of two repetitions (0000100001) is programmed into the register, i.e.00001000. Note that bit ACT7 corresponds to the first code bit received.

Upon reset of the COMET, the register contents are set to logic 0.

### Register 04FH: IBCD Deactivate Code

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | DACT7 | 0 |
| Bit 6 | R/W | DACT6 | 0 |
| Bit 5 | R/W | DACT5 | 0 |
| Bit 4 | R/W | DACT4 | 0 |
| Bit 3 | R/W | DACT3 | 0 |
| Bit 2 | R/W | DACT2 | 0 |
| Bit 1 | R/W | DACT1 | 0 |
| Bit 0 | R/W | DACT0 | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This 8-bit register selects the Deactivate code sequence that is to be detected. If the code sequence length is less than 8 bits, the first 8 bits of several repetitions of the code sequence must be used to fill the 8-bit register. For example, if code sequence is a repeating 001, the first 8 bits of three repetitions (001001001) is programmed into the register, i.e.00100100. Note that bit DACT7 corresponds to the first code bit received.

Upon reset of the COMET, the register contents are set to logic 0.

### Register 050H: SIGX Configuration Register (COSS = 0)

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | Reserved | 0 |
| Bit 6 | R/W | COSS | 0 |
| Bit 5 | R/W | SIGE | 0 |
| Bit 4 | R/W | Reserved | 0 |
| Bit 3 | R/W | Reserved | 0 |
| Bit 2 | R/W | ESF | 0 |
| Bit 1 | R/W | IND | 0 |
| Bit 0 | R/W | PCCE | 0 |

Reserved:

These bits must be a logic 0 for correct operation.

COSS:

The COSS bit allows the channels to be polled to determine in which channel(s) the signaling state has changed. When COSS is a logic 1, the SIGX register space is configured to allow the change of signaling state event bits to be read. When COSS is a logic 0, the SIGX register space is configured to allow indirect access to the configuration and signaling data for each of the 24 T1 or 30 E1 channels.

SIGE:

The SIGE bit enables a change of signaling state in any one of the 24 channels (T1 mode) or 30 channels for (E1 mode ) to generate an interrupt on the INTB output.

When SIGE is set to logic 1, a change of signaling state in any channel generates an interrupt. When SIGE is set to logic 0, the interrupt is disabled.

ESF:

The framing format in T1 mode is controlled by the ESF bit. A logic 1 in the ESF bit position selects ESF; a logic 0 bit selects SF, SLC®96 or T1DM. When in E1 mode, this bit is ignored.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. IND must be logic 1 for proper operation.

PCCE:

The per-timeslot/per-channel configuration enable bit, PCCE, enables the configuration data in the per-timeslot/per-channel registers to affect the BRSIG and BRPCM data streams. A logic 1 in the PCCE bit position enables the Per-Timeslot/Per-Channel Configuration Register bits in the indirect registers 40H through 5FH; a logic 0 disables the Per-Timeslot/Per-Channel Configuration Register bits in those registers. Please refer to the Per-timeslot/Per-Channel Configuration descriptions for configuration bit details. When the TSB is reset, the PCCE bit is set to logic 0, disabling the Per-Timeslot/Per-Channel Configuration Register bits.

### Register 050H: SIGX Change of Signaling State Register (COSS = 1)

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | R/W | COSS | 0 |
| Bit 5 | R | COSS[30] | X |
| Bit 4 | R | COSS[29] | X |
| Bit 3 | R | COSS[28] | X |
| Bit 2 | R | COSS[27] | X |
| Bit 1 | R | COSS[26] | X |
| Bit 0 | R | COSS[25] | X |

COSS[30:25]:

The COSS[30:25] bits will be set to logic 1 if a change of signaling state occurs on the corresponding E1 timeslot. COSS[30:25] are cleared after this register is read. COSS[30:25] are valid only if the E1/T1B register bit is a logic 1. The COSS bit allows the timeslot to be polled to determine in which timeslot(s) the signaling state has changed. When COSS is a logic 1, the SIGX register space is configured to allow the change of signaling state event bits to be read. When COSS is a logic 0, the SIGX register space is configured to allow indirect access to the configuration and signaling data for each of the 24 T1 or 30 E1 channels.

COSS[25] through COSS[30] correspond to timeslots 26 through 31.

### Register 051H: SIGX Timeslot Indirect Status (COSS = 0)

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | BUSY | 0 |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | | Unused | X |

The Timeslot Indirect Status Register is provided at SIGX read/write address 1.

BUSY:

The BUSY bit is set to logic 1 while the timeslot data is being retrieved or while the configuration data is being written. The bit is set to logic 0 when the read or write cycle has been completed. The BUSY signal holds off a microprocessor read or write access until the SIGX has completed the previous request. This register should be polled until the BUSY bit is logic 0. The bits in this register are valid only when COSS = 0.

### Register 051H: SIGX Change Of Signaling State Change (COSS=1)

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | COSS[24] | X |
| Bit 6 | R | COSS[23] | X |
| Bit 5 | R | COSS[22] | X |
| Bit 4 | R | COSS[21] | X |
| Bit 3 | R | COSS[20] | X |
| Bit 2 | R | COSS[19] | X |
| Bit 1 | R | COSS[18] | X |
| Bit 0 | R | COSS[17] | X |

COSS[24:17]:

The COSS[24:17] bits will be set to logic 1 if a change of signaling state occurs on the corresponding E1 timeslot OR T1 channel. COSS[24:17] are cleared after this register is read.

In E1 mode, COSS[17] through COSS[24] correspond to timeslots 18 through 25.

For the purposes of signaling extraction, the T1 channels are indexed 1 through 24.

### Register 052H: SIGX Timeslot Indirect Address/Control (COSS = 0)

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | RWB | 0 |
| Bit 6 | R/W | A[6] | 0 |
| Bit 5 | R/W | A[5] | 0 |
| Bit 4 | R/W | A[4] | 0 |
| Bit 3 | R/W | A[3] | 0 |
| Bit 2 | R/W | A[2] | 0 |
| Bit 1 | R/W | A[1] | 0 |
| Bit 0 | R/W | A[0] | 0 |

If the SIGX is enabled for direct microprocessor access, writing to and reading from the Timeslot Indirect Address Register will not generate any additional accesses.

A[6:0]:

If the SIGX is enabled for indirect microprocessor access, writing to the Timeslot Indirect Address Register initiates a microprocessor access request to one of the registers in segments 2 and 3. The desired register is addressed using the value written to bits A[6:0].

RWB:

The RWB bit indicates which operation is requested. If RWB is set to logic 1, a read is requested. After the request has been issued, the Timeslot Indirect Status register should be monitored to verify completion of the read. The desired register contents can then be found in the Timeslot Indirect Data Register. If RWB is set to logic 0, a write is requested. Data to be written to the microprocessor should first be placed in the Timeslot Indirect Data Register. For both read and write operations, the BUSY bit in the Timeslot Indirect Status Register should be monitored to ensure that the previous access has been completed.

Note: If the value written to A[6:0] addresses a segment 1 register, an access is not initiated.

### Register 052H: SIGX Change of Signaling State Register (COSS = 1)

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | COSS[16] | X |
| Bit 6 | R | COSS[15] | X |
| Bit 5 | R | COSS[14] | X |
| Bit 4 | R | COSS[13] | X |
| Bit 3 | R | COSS[12] | X |
| Bit 2 | R | COSS[11] | X |
| Bit 1 | R | COSS[10] | X |
| Bit 0 | R | COSS[9] | X |

COSS[16:9]:

The COSS[16:9] bits will be set to logic 1 if a change of signaling state occurs on the corresponding E1 timeslot or T1 channel. COSS[16:9] are cleared after this register is read.

In E1 mode, COSS[9] through COSS[15] correspond to timeslots 9 through 15 and COSS[16] corresponds to timeslot 17.

For the purposes of signaling extraction, the T1 channels are indexed 1 through 24.

### Register 053H: SIGX Timeslot Indirect Data Buffer (COSS = 0)

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | D[7] | X |
| Bit 6 | R/W | D[6] | X |
| Bit 5 | R/W | D[5] | X |
| Bit 4 | R/W | D[4] | X |
| Bit 3 | R/W | D[3] | X |
| Bit 2 | R/W | D[2] | X |
| Bit 1 | R/W | D[1] | X |
| Bit 0 | R/W | D[0] | X |

In the case of an indirect write, the Indirect Data Register holds the value that will be written to the desired register when a write is initiated via the Timeslot Indirect Address Register. In the case of an indirect read, the Indirect Data Register will hold the contents of the indirectly addressed register, when the read has been completed. Please refer below to the per-timeslot register descriptions for the expected bit formats.

**Register 053H: SIGX Change of Signaling State (COSS = 1)**

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | COSS[8] | X |
| Bit 6 | R | COSS[7] | X |
| Bit 5 | R | COSS[6] | X |
| Bit 4 | R | COSS[5] | X |
| Bit 3 | R | COSS[4] | X |
| Bit 2 | R | COSS[3] | X |
| Bit 1 | R | COSS[2] | X |
| Bit 0 | R | COSS[1] | X |

COSS[8:1]:

The COSS[8:1] bits will be set to logic 1 if a change of signaling state occurs on the corresponding E1 timeslot or T1 channel. COSS[8:1] are cleared after this register is read.

In E1 mode, COSS[1] through COSS[8] correspond to timeslots 1 through 8.

For the purposes of signaling extraction, the T1 channels are indexed 1 through 24.

### SIGX Indirect Registers

The signaling and per-timeslot functions are allocated within the indirect registers as follows:

**Table 33 - SIGX Indirect Register Map**

| Addr | Register |
|---|---|
| 10H | Current Signaling Data Register for Ch 1 and 17 |
| 11H | Current Signaling Data Register for TS1 and 17/Ch 2 and 18 |
| 12H | Current Signaling Data Register for TS2 and 18/Ch 3 and 19 |
| 13H | Current Signaling Data Register for TS3 and 19/Ch 4 and 20 |
| 14H | Current Signaling Data Register for TS4 and 20/Ch 5 and 21 |
| 15H | Current Signaling Data Register for TS5 and 21/Ch 6 and 22 |

| Addr | Register |
|---|---|
| 16H | Current Signaling Data Register for TS6 and 22/Ch 7 and 23 |
| 17H | Current Signaling Data Register for TS7 and 23/Ch 8 and 24 |
| 18H | Current Signaling Data Register for TS8 and 24/Ch 9 |
| 19H | Current Signaling Data Register for TS9 and 25/Ch 10 |
| 1AH | Current Signaling Data Register for TS10 and 26/Ch 11 |
| 1BH | Current Signaling Data Register for TS11 and 27/Ch 12 |
| 1CH | Current Signaling Data Register for TS12 and 28/Ch 13 |
| 1DH | Current Signaling Data Register for TS13 and 29/Ch 14 |
| 1EH | Current Signaling Data Register for TS14 and 30/Ch 15 |
| 1FH | Current Signaling Data Register for TS15 and 31/Ch 16 |
| 20H | Delayed Signaling Data Register for Ch 1 |
| 21H | Delayed Signaling Data Register for TS1/Ch 2 |
| 22H | Delayed Signaling Data Register for TS2/Ch 3 |
| • | • |
| • | • |
| • | • |
| 2FH | Delayed Signaling Data Register for TS15/Ch 16 |
| 30H | Delayed Signaling Data Register for Ch 17 |
| 31H | Delayed Signaling Data Register for TS17/Ch 18 |
| • | • |
| • | • |
| • | • |
| 37H | Delayed Signaling Data Register for TS23/Ch 24 |
| 38H | Delayed Signaling Data Register for TS24 |
| • | • |
| • | • |
| • | • |
| 3EH | Delayed Signaling Data Register for TS30 |
| 3FH | Delayed Signaling Data Register for TS31 |

| Addr | Register |
|---|---|
| 40H | TS0/Ch 1 Configuration Data |
| 41H | TS1/Ch 2 Configuration Data |
| • | • |
| • | • |
| • | • |
| 57H | TS23/Ch 24 Configuration Data |
| 58H | TS24 Configuration Data |
| • | • |
| • | • |
| • | • |
| 5EH | TS 30 Configuration Data |
| 5FH | TS 31 Configuration Data |

**Table 34 - SIGX Indirect Registers 10H - 1FH: Current Timeslot/Channel Signaling Data**

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | A TS/Ch ‘n’ | X |
| Bit 6 | R | B TS/Ch ‘n’ | X |
| Bit 5 | R | C TS/Ch ‘n’ | X |
| Bit 4 | R | D TS/Ch ‘n’ | X |
| Bit 3 | R | A TS/Ch ‘n+16’ | X |
| Bit 2 | R | B TS/Ch ‘n+16’ | X |
| Bit 1 | R | C TS/Ch ‘n+16’ | X |
| Bit 0 | R | D TS/Ch ‘n+16’ | X |

Timeslot (E1 mode) and Channel (T1 mode) signaling data can be read from the Timeslot/Channel Signaling Data registers. In E1 mode, TS0 and TS16 do not contain valid data and are not available for reading. The signaling data is termed “Current” here because it is available in the same signaling multi-frame that the COSS[x] indication is available. Note that the signaling data is stored in nibble format.

**Table 35 - SIGX Indirect Registers 20H - 3FH: Delayed Timeslot/Channel Signaling Data**

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | R | A TS/Ch ‘n’ | X |
| Bit 2 | R | B TS/Ch ‘n’ | X |
| Bit 1 | R | C TS/Ch ‘n’ | X |
| Bit 0 | R | D TS/Ch ‘n’ | X |

Timeslot (E1 mode) and Channel (T1 mode) signaling data can be read from the Timeslot/Channel Signaling Data registers. Addresses 20H - 37H are valid in T1 mode. Addresses 20H-3FH correspond to TS 0 - TS31. In E1 mode, TS0 and TS16 do not contain valid data. The signaling data is termed “Delayed” here because it is not available until one full signaling multi-frame after the COSS[x] indication is available.

**Table 36 - Indirect Registers 40H - 5FH: Per-Timeslot Configuration**

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | R/W | RINV[1] | X |
| Bit 2 | R/W | RINV[0]/RFIX | X |
| Bit 1 | R/W | RPOL | X |
| Bit 0 | R/W | RDEBE | X |

RINV[1:0] / RFIX:

In T1 mode, the RINV[1] and SIGNINV bit of the RPSC Data Control byte can be used to invert data as shown in Table 37:

**Table 37 - SIGX Per-Channel T1 Data Conditioning**

| RINV[1] | SIGNINV | Effect on PCM Channel Data |
|---|---|---|
| 0 | 0 | PCM Channel data is unchanged |
| 1 | 0 | All 8 bits of the received PCM channel data are inverted |
| 0 | 1 | Only the MSB of the received PCM channel data is inverted (SIGN bit inversion) |
| 1 | 1 | All bits EXCEPT the MSB of the received PCM channel data is inverted (Magnitude inversion) |

In E1 mode, the RINV[1:0] bits select bits within the timeslot are inverted. The bit mapping is as shown in Table 38.

**Table 38 - SIGX Per-Channel E1 Data Conditioning**

| RINV[1] | RINV[0] | Effect on PCM Channel Data |
|---|---|---|
| 0 | 0 | do not invert |
| 0 | 1 | invert even bits (2,4,6,8) |
| 1 | 0 | invert odd bits (1,3,5,7) |
| 1 | 1 | invert all bits |

Because of the distinct requirements for E1 and T1, the register bits have different definitions in the two modes. In E1 mode bit 2 is defined as RINV[0]; whereas in T1 it is RFIX. RINV[1] has a different effect for the two modes.

In T1 mode, RFIX controls whether the signaling bit (the least significant bit of the DS0 channel on BRPCM during signaling frames) is fixed to the polarity specified by the RPOL bit. A logic 1 in the RFIX position enables bit fixing; a logic 0 in the RFIX position disables bit fixing. Note that the RPSC functions (inversion, digital milliwatt code insertion, trunk conditioning, and PRBS detection or insertion) take place after bit fixing.

RPOL:

In T1 mode, the RPOL bit selects the logic level the signaling bit is fixed to when bit fixing is enabled. When RPOL is a logic 1, the signaling is fixed to logic 1. When RPOL is a logic 0, the signaling is fixed to logic 0.

RDEBE:

The RDEBE bit enables debouncing of timeslot/channel signaling bits. A logic 1 in this bit position enables signaling debouncing while a logic 0

disables it. When debouncing is selected, per-timeslot/per-channel signaling transitions are ignored until two consecutive, equal values are sampled. Debouncing is performed on a per signaling bit basis.

Data inversion, data trunk conditioning, and digital milliwatt insertion are performed independently of the received framing format. Digital milliwatt insertion takes precedence over data trunk conditioning which, in turn, takes precedence over the various data inversions.

To enable the RINV[1], RINV[0]/RFIX, RPOL, RDEBE bits, the PCCE bit in the SIGX Configuration Register must be set to logic 1.

### Register 054H: T1 XBAS Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | MTRK | 0 |
| Bit 6 | R/W | JPN | 0 |
| Bit 5 | R/W | B8ZS | 0 |
| Bit 4 | R/W | ESF | 0 |
| Bit 3 | R/W | FMS1 | 0 |
| Bit 2 | R/W | FMS0 | 0 |
| Bit 1 | R/W | ZCS1 | 0 |
| Bit 0 | R/W | ZCS0 | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

MTRK:

The MTRK bit forces trunk conditioning, idle code substitution and signaling conditioning, on all channels when MTRK is a logic 1. This has the same effect as setting the IDLE_DS0 bit in the PCM Control byte and the SIG0 bit in the SIGNALING Control byte for all channels.

JPN:

The JPN bit enables Japanese variations of the standard framing formats. If the JPN bit is a logic 1 and the ESF format is selected (ESF bit is logic 1), the XBAS complies to TTC JT-G704. If the JPN bit is a logic 1 and the SF format is selected, the framing bit of frame 12 is forced to logic 1 when a Yellow alarm is declared. Otherwise, bit 2 in all of the channels is forced to logic 0 to indicate Yellow alarm. Framing insertion must be enabled in order to transmit the alternate SF Yellow alarm.

B8ZS:

The B8ZS bit enables B8ZS line coding when it is a logic 1. When the B8ZS bit is a logic 0, AMI coding is used.

ESF, FMS1, FMS0:

The ESF bit selects either Extended Superframe format or enables the Frame Mode Select bits (FMS) to select either regular superframe, T1DM or SLC®96 framing formats. The mode is encoded as follows:

**Table 39 - T1 Framing Formats**

| ESF | FMS1 | FMS0 | MODE |
|---|---|---|---|
| 0 | 0 | 0 | SF framing format |
| 0 | 0 | 1 | T1DM framing format (R bit unaffected) |
| 0 | 1 | 0 | SLC®96 |
| 0 | 1 | 1 | T1DM framing format (FDL data replaces R bit) |
| 1 | 0 | 0 | ESF framing format - 4 kbit/s data link |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

ZCS[1:0]:

The ZCS[1:0] bits select the Zero Code Suppression format to be used. These bits are logically ORed with the ZCS[1:0] bits in the TPSC per-channel PCM Control byte. The bits are encoded as follows:

**Table 40 - T1 Zero Code Suppression Formats**

| ZCS1 | ZCS0 | Zero Code Suppression Format |
|---|---|---|
| 0 | 0 | None |
| 0 | 1 | GTE Zero Code Suppression (Bit 8 of an all zero channel byte is replaced by a one, except in signaling frames where bit 7 is forced to a one.) |
| 1 | 0 | DDS Zero Code Suppression (All zero data byte replaced with "10011000") |
| 1 | 1 | Bell Zero Code Suppression (Bit 7 of an all zero channel byte is replaced by a one.) |

### Register 055H: T1 XBAS Alarm Transmit

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | R/W | XYEL | 0 |
| Bit 0 | R/W | XAIS | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register controls the transmission of Yellow or AIS alarm.

XYEL

The XYEL bit enables the XBAS to generate a Yellow alarm in the appropriate framing format. When XYEL is set to logic 1, XBAS is enabled to set bit 2 of each channel to logic 0 for SF and SLC®96 formats, the Y-bit to logic 0 for T1DM format, and XBAS is enabled to transmit repetitions of 1111111100000000 (the Yellow Alarm BOC) on the FDL for ESF format. If the JPN bit of the T1-XBAS Configuration register is a logic 1 and the SF format is selected, the framing bit of frame 12 is forced to logic 1 when a Yellow alarm is enabled. When XYEL is set to logic 0, XBAS is disabled from generating the Yellow alarm.

XAIS:

The XAIS bit enables the XBAS to generate an unframed all-ones AIS alarm. When XAIS is set to logic 1, the XBAS bipolar outputs are forced to pulse alternately, creating an all-ones signal. When XAIS is set to logic 0, the XBAS bipolar outputs operate normally.

### Register 056H: T1 XIBC Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | EN | 0 |
| Bit 6 | R/W | UF | 0 |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | R/W | CL1 | 0 |
| Bit 0 | R/W | CL0 | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

EN:

The EN bit controls whether the Inband Code is transmitted or not. A logic 1 in the EN bit position enables transmission of inband codes; a logic 0 in the EN bit position disables inband code transmission.

UF:

The UF bit controls whether the code is transmitted framed or unframed. A logic 1 in the UF bit position selects unframed inband code transmission; a logic 0 in the UF bit position selects framed inband code transmission. Note: the UF register bit controls the XBAS directly and is not qualified by the EN bit. When UF is set to logic 1, the XBAS is disabled and no framing is inserted regardless of the setting of EN. The UF bit should only be written to logic 1 when the EN bit is set, and should be cleared to logic 0 when the EN bit is cleared.

CL1, CL0:

The bit positions CL1 and CL0 of this register indicate the length of the inband loopback code sequence, as follows:

**Table 41 - Transmit In-band Code Length**

| CL1 | CL0 | Code Length |
|---|---|---|
| 0 | 0 | 5 |

| CL1 | CL0 | Code Length |
|---|---|---|
| 0 | 1 | 6 |
| 1 | 0 | 7 |
| 1 | 1 | 8 |

Codes of 3 or 4 bits in length may be accommodated by treating them as half of a double-sized code (i.e., a 3-bit code would use the 6-bit code length setting).

### Register 057H: T1 XIBC Loopback Code

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | IBC7 | X |
| Bit 6 | R/W | IBC6 | X |
| Bit 5 | R/W | IBC5 | X |
| Bit 4 | R/W | IBC4 | X |
| Bit 3 | R/W | IBC3 | X |
| Bit 2 | R/W | IBC2 | X |
| Bit 1 | R/W | IBC1 | X |
| Bit 0 | R/W | IBC0 | X |

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register contains the inband loopback code pattern to be transmitted. The code is transmitted most significant bit ( IBC7) first, followed by IBC6 and so on. The code, regardless of the length, must be aligned with the MSB always in the IBC7 position (e.g., a 5-bit code would occupy the IBC7 through IBC2 bit positions). To transmit a 3-bit or a 4-bit code pattern, the pattern must be paired to form a double-sized code (i.e., the 3-bit code '011' would be written as the 6-bit code '011011').

When the COMET is reset, the contents of this register are not affected.

### Register 058H: PMON Interrupt Enable/Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | R/W | INTE | 0 |
| Bit 1 | R | XFER | 0 |
| Bit 0 | R | OVR | 0 |

This register contains status information indicating when counter data has been transferred into the holding registers and indicating whether the holding registers have been overrun.

INTE:

The INTE bit controls the generation of a microprocessor interrupt when the transfer clock has caused the counter values to be stored in the holding registers. A logic 1 bit in the INTE position enables the generation of an interrupt via the INTB output; a logic 0 bit in the INTE position disables the generation of an interrupt.

XFER:

The XFER bit indicates that a transfer of counter data has occurred. A logic 1 in this bit position indicates that a latch request, initiated by writing to one of the counter register locations or the Global PMON Update register, was received and a transfer of the counter values has occurred. A logic 0 indicates that no transfer has occurred. The XFER bit is cleared (acknowledged) by reading this register.

OVR:

The OVR bit is the overrun status of the holding registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFER being logic 1) has not been acknowledged before the next transfer clock has been issued and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. The OVR bit is cleared by reading this register.

### Registers 059-05FH: Latching Performance Data

The Performance Data registers for a single framer are updated as a group by writing to any of the PMON count registers (addresses 059H-05FH). A write to one (and only one) of these locations loads performance data located in the PMON into the internal holding registers. Alternatively, the Performance Data registers are updated by writing to the Revision/Chip ID/Global PMON Update register (address 00DH). The data contained in the holding registers can then be subsequently read by microprocessor accesses into the PMON count register address space. The latching of count data, and subsequent resetting of the counters, is synchronized to the internal event timing so that no events are missed.

The PMON is loaded with new performance data within 3.5 recovered clock periods of the latch performance data register write. With nominal line rates, the PMON registers should not be polled until 2.3 µsec have elapsed from the "latch performance data" register write.

When the COMET is reset, the contents of the PMON count registers are unknown until the first latching of performance data is performed.

### Register 059H: PMON Framing Bit Error Count

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | R | FER[6] | X |
| Bit 5 | R | FER[5] | X |
| Bit 4 | R | FER[4] | X |
| Bit 3 | R | FER[3] | X |
| Bit 2 | R | FER[2] | X |
| Bit 1 | R | FER[1] | X |
| Bit 0 | R | FER[0] | X |

FER[6:0]:

The FER[6:0] bits indicate the number of framing bit error events that occurred during the previous accumulation interval. The FER counts are suppressed when the framer has lost frame alignment (OOF in the E1-FRMR Framing Status register is logic 1 or INFR in the T1-FRMR Interrupt Status register is logic 0).

In T1 mode, a framing bit error is defined as an $F_e$-bit error in ESF, a framing bit error in SF, $F_T$-bit error in SLC®96, or an F-bit error in T1DM.

In E1 mode, the count is either the number of FAS (frame alignment signal) bits (default) or words in error. As an option, a zero in bit 2 of time slot 0 of non-frame alignment signal (NFAS) frames results in an increment of the framing error count. Refer to the Receive Options register.

### Register 05AH: PMON OOF/COFA/Far End Block Error Count LSB

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | OOF/FEBE[7] | X |
| Bit 6 | R | OOF/FEBE[6] | X |
| Bit 5 | R | OOF/FEBE[5] | X |
| Bit 4 | R | OOF/FEBE[4] | X |
| Bit 3 | R | OOF/FEBE[3] | X |
| Bit 2 | R | OOF/FEBE[2] | X |
| Bit 1 | R | OOF/FEBE[1] | X |
| Bit 0 | R | OOF/FEBE[0] | X |

### Register 05BH: PMON OOF/COFA/Far End Block Error Count MSB

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | R | OOF/FEBE[9] | X |
| Bit 0 | R | OOF/FEBE[8] | X |

OOF/FEBE[9:0]:

In T1 mode, the OOF[9:0] bits indicate the number Out Of Frame or Change Of Frame Alignment events that occurred during the previous accumulation interval, as specified by the CCOFA bit in the Receive Options register. If OOFs are being accumulated, the count is incremented each time a severely errored framing event forces a reframe. IF COFAs are being accumulated, the count is incremented if a new alignment differs from the previous alignment.

In E1 mode, the FEBE[9:0] bits indicate the number of far end block error events that occurred during the previous accumulation interval. The FEBE counts are suppressed when the E1 FRMR has lost frame alignment (OOF in the FRMR Framing Status register is set).

### Register 05CH: PMON Bit Error/CRC Error Count LSB

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | BEE/CRCE[7] | X |
| Bit 6 | R | BEE/CRCE[6] | X |
| Bit 5 | R | BEE/CRCE[5] | X |
| Bit 4 | R | BEE/CRCE[4] | X |
| Bit 3 | R | BEE/CRCE[3] | X |
| Bit 2 | R | BEE/CRCE[2] | X |
| Bit 1 | R | BEE/CRCE[1] | X |
| Bit 0 | R | BEE/CRCE[0] | X |

### Register 05DH: PMON Bit Error/CRC Error Count MSB

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | R | BEE/CRCE[9] | X |
| Bit 0 | R | BEE/CRCE[8] | X |

BEE/CRCE[9:0]:

In T1 mode, the BEE[9:0] bits contain the number of bit error events that occurred during the previous accumulation interval. A bit error event is defined as a CRC-6 error in ESF, a framing bit error in SF, an $F_T$-bit error in SLC®96, and an F-bit or sync bit error (there can be up to 7 bits in error per frame) in T1DM.

In E1 mode, the CRCE[9:0] bits indicate the number of CRC error events that occurred during the previous accumulation interval. CRC error events are suppressed when the E1 FRMR is out of CRC-4 multiframe alignment (OOCMF bit in the FRMR Framing Status register is set).

### Register 05EH: PMON LCV Count (LSB)

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | LCV[7] | X |
| Bit 6 | R | LCV[6] | X |
| Bit 5 | R | LCV[5] | X |
| Bit 4 | R | LCV[4] | X |
| Bit 3 | R | LCV[3] | X |
| Bit 2 | R | LCV[2] | X |
| Bit 1 | R | LCV[1] | X |
| Bit 0 | R | LCV[0] | X |

### Register 05FH: PMON LCV Count (MSB)

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R | LCV[12] | X |
| Bit 3 | R | LCV[11] | X |
| Bit 2 | R | LCV[10] | X |
| Bit 1 | R | LCV[9] | X |
| Bit 0 | R | LCV[8] | X |

LCV[12:0]:

The LCV[12:0] bits indicate the number of LCV error events that occurred during the previous accumulation interval. An LCV event is defined as the occurrence of a Bipolar Violation or Excessive Zeros. The counting of Excessive Zeros can be disabled by the BPV bit of the Receive Line Interface Configuration register.

### Register 060H: T1 ALMI Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R/W | ESF | 0 |
| Bit 3 | R/W | FMS1 | 0 |
| Bit 2 | R/W | FMS0 | 0 |
| Bit 1 | | Unused | X |
| Bit 0 | | Unused | X |

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register allows selection of the framing format and the data rate of the Facility Data Link in ESF to allow operation of the CFA detection algorithms.

ESF:

The ESF bit selects either extended superframe format or enables the frame mode select bits to select either regular superframe, T1DM, "alternate" T1DM, or SLC®96 framing formats. A logic 1 in the ESF bit position selects ESF; a logic 0 bit enables FMS1 and FMS0 to select SF, T1DM, "alternate" T1DM, or SLC®96.

FMS1,FMS0:

The FMS1 and FMS0 bits select standard superframe, T1DM, "alternate" T1DM, or SLC®96 framing formats. A logic 00 in these bits enable the SF framing format; a logic 01 in these bit positions enable the T1DM framing format; a logic 10 in these bit positions enable the SLC®96 framing format; and a logic 11 in these bit positions enable the "alternate" T1DM framing format. The "alternate" T1DM framing format configures the ALMI to process the Red alarm as if the SF, SLC®96, or ESF framing format were selected; the Yellow alarm is still processed as T1DM.

When ESF is selected (ESF bit set to logic 1), the FMS1 and FMS0 bits select the data rate and the source channel for the Facility Data Link (FDL) data. A logic 00 in these bits enables the ALMI to receive FDL data and validate the Yellow alarm at the full 4 kbit rate.

The valid combinations of the ESF, FMS1, and FMS0 bits are summarized in the table below:

**Table 42 - T1 Framing Modes**

| ESF | FMS1 | FMS0 | Mode |
|---|---|---|---|
| 0 | 0 | 0 | Select Superframe framing format |
| 0 | 0 | 1 | Select T1DM framing format |
| 0 | 1 | 0 | Select SLC-96 framing format |
| 0 | 1 | 1 | Select "alternate" T1DM mode |
| 1 | 0 | 0 | Select ESF framing format & 4 kbit FDL Data Rate |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

### Register 061H: T1 ALMI Interrupt Enable

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R/W | FASTD | 0 |
| Bit 3 | R/W | ACCEL | 0 |
| Bit 2 | R/W | YELE | 0 |
| Bit 1 | R/W | REDE | 0 |
| Bit 0 | R/W | AISE | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register selects which of the three CFA's can generate an interrupt when their logic state changes and enables the "fast" deassertion mode of operation.

FASTD:

The FASTD bit enables the "fast" deassertion of Red and AIS alarms. When FASTD is set to a logic 1, deassertion of Red alarm occurs within 120 ms of going in frame. Deassertion of AIS alarm occurs within 180 ms of either detecting a 60 ms interval containing 127 or more zeros, or going in frame. When FASTD is set to a logic 0, Red and AIS alarm deassertion times remain as defined in the ALMI description.

ACCEL:

The ACCEL bit is used for production test purposes only. THE ACCEL BIT MUST BE PROGRAMMED TO LOGIC 0 FOR NORMAL OPERATION.

YELE, REDE, AISE:

A logic 1 in the enable bit positions (YELE, REDE, AISE) enables a state change in the corresponding CFA to generate an interrupt; a logic 0 in the enable bit positions disables any state changes to generate an interrupt. The enable bits are independent; any combination of Yellow, Red, and AIS CFA's can be enabled to generate an interrupt.

Upon reset of the COMET, these bits are cleared to logic 0.

### Register 062H: T1 ALMI Interrupt Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | R | YELI | 0 |
| Bit 4 | R | REDI | 0 |
| Bit 3 | R | AISI | 0 |
| Bit 2 | R | YEL | 0 |
| Bit 1 | R | RED | 0 |
| Bit 0 | R | AIS | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register indicates which of the three Carry Failure Alarms (CFA's) generated an interrupt when their logic state changed in bit positions 5 through 3, and indicate the current state of each CFA in bit positions 2 through 0. A logic 1 in the status positions (YELI, REDI, AISI) indicate that a state change in the corresponding CFA has generated an interrupt; a logic 0 in the status positions indicates that no state change has occurred. Both the status bit positions (bits 5 through 3) and the interrupt generated because of the change in CFA state are cleared to logic 0 when the register containing then is read.

### Register 063H: T1 ALMI Alarm Detection Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | R | REDD | X |
| Bit 1 | R | YELD | X |
| Bit 0 | R | AISD | X |

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register indicates the presence or absence of one or more OOF occurrences within the last 40 ms; the presence or absence of the Yellow alarm signal over the last 40 ms; and indicate the presence or absence of the AIS alarm signal over the last 60 ms.

REDD:

When REDD is a logic 1, one or more out of frame events have occurred during the last 40 ms interval. When REDD is a logic 0, no out of frame events have occurred within the last 40 ms interval.

YELD:

When YELD is logic 1, a valid Yellow signal was present during the last 40 ms interval. When YELD is logic 0, the Yellow signal was absent during the last 40 ms interval. For each framing format, a valid Yellow signal is deemed to be present if:

bit 2 of each channel is not logic 0 for 16 or fewer times during the 40 ms interval for SF and SLC®96 framing formats;

the Y-bit is not logic 0 for 4 or fewer times during the 40 ms interval for T1DM framing format;

the 16-bit Yellow bit oriented code is received error-free 8 or more times during the interval for ESF framing format with a 4 kHz data link;

In a Japanese T1 mode, the 12th F-bit toggles between 1 and 0 signifying a Japanese Yellow alarm

AISD:

When AISD is logic 1, a valid AIS signal was present during the last 60 ms interval. When AISD is logic 0, the AIS signal was absent during the last 60 ms interval. A valid AIS signal is deemed to be present during a 60 ms interval if the out of frame condition has persisted for the entire interval and the received PCM data stream is not logic 0 for 126 or fewer times.

### Register 065H: T1 PDVD Interrupt Enable/Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R | PDV | 0 |
| Bit 3 | R | Z16DI | 0 |
| Bit 2 | R | PDVI | 0 |
| Bit 1 | R/W | Z16DE | 0 |
| Bit 0 | R/W | PDVE | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset. Also, this register is only available when the RUNI bit in the Receive Line Interface Configuration register is logic 0.

PDV:

The PDV bit indicates the current state of the pulse density violation indication. When PDV is a logic 1, a violation of the pulse density rule exists. When PDV is a logic 0, no violation of the pulse density rule exists. Note: the PDV indication persists for the duration of the pulse density violation. At its minimum, PDV may be asserted for only 1 bit time, therefore, reading this bit may not return a logic 1 even though a pulse density violation has occurred.

PDVI, Z16DI:

The PDVI and Z16DI bits identify the source of a generated interrupt. PDVI is a logic 1 whenever a change in the pulse density violation indication generated an interrupt. PDVI is cleared to 0 when this register is read. Z16DI is a logic 1 whenever 16 consecutive zeros are detected. Z16DI is cleared to 0 when this register is read. Note that the PDVI and Z16DI interrupt indications operate regardless of whether interrupts are enabled or disabled.

Z16DE:

The Z16DE bit enables an interrupt to be generated on the microprocessor INTB pin when 16 consecutive zeros are detected. When Z16DE is set to logic 1, interrupt is generation is enabled. When Z16DE is set to logic 0, interrupt generation is disabled.

PDVE:

The PDVE bit enables an interrupt to be generated on the microprocessor INTB pin when a change in the pulse density is detected. When PDVE is set to logic 1, an interrupt is generated whenever a pulse density violation occurs or when the pulse density ceases to exist. When PDVE is set to logic 0, interrupt generation by pulse density violations is disabled.

### Register 067H: T1 XBOC Code

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | R/W | BC[5] | 1 |
| Bit 4 | R/W | BC[4] | 1 |
| Bit 3 | R/W | BC[3] | 1 |
| Bit 2 | R/W | BC[2] | 1 |
| Bit 1 | R/W | BC[1] | 1 |
| Bit 0 | R/W | BC[0] | 1 |

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register enables the XBOC to generate a bit oriented code and selects the 6-bit code to be transmitted.

When this register is written with any 6-bit code other than 111111, that code will be transmitted repeatedly in the ESF Facility Data Link with the format 111111110[BC0][BC1][BC2][BC3][BC4][BC5]0, overwriting any HDLC packets currently being transmitted. When the register is written with 111111, the XBOC is disabled.

### Register 069H: T1 XPDE Interrupt Enable/Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | STUFE | 0 |
| Bit 6 | R/W | STUFF | 0 |
| Bit 5 | R | STUFI | 0 |
| Bit 4 | R | PDV | 0 |
| Bit 3 | R | Z16DI | 0 |
| Bit 2 | R | PDVI | 0 |
| Bit 1 | R/W | Z16DE | 0 |
| Bit 0 | R/W | PDVE | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

STUFE:

The STUFE bit enables the occurrence of pulse stuffing to generate an interrupt on INTB. When STUFE is set to logic 1, an interrupt is generated on the occurrence of a bit stuff. When STUFE is a logic 0, bit stuffing occurrences do not generate an interrupt on INTB.

STUFF:

The STUFF bit enables pulse stuffing to occur upon detection of a violation of the pulse density rule. Bit stuffing is performed in such a way that the resulting data stream no longer violates the pulse density rule. When STUFF is set to logic 1, bit stuffing is enabled and the STUFI bit indicates the occurrence of bit stuffs. When STUFF is a logic 0, bit stuffing is disabled and the PDVI bit indicates occurrences of pulse density violation. Also, when STUFF is a logic 0, PCM data passes through XPDE unaltered.

STUFI:

The STUFI bit is valid when pulse stuffing is active. This bit indicates when a bit stuff occurred to eliminate a pulse density violation and that an interrupt was generated due to the bit stuff (if STUFE is logic 1). When pulse stuffing is active, PDVI remains logic 0, indicating that the stuffing has removed the density violation. The STUFI bit is reset to logic 0 once this register is read. If the STUFE bit is also logic 1, the interrupt is also cleared once this register is read.

PDV:

The PDV bit indicates the current state of the pulse density violation indication. When PDV is a logic 1, a violation of the pulse density rule exists. When PDV is a logic 0, no violation of the pulse density rule exists. Note: the PDV indication persists for the duration of the pulse density violation. At its minimum, PDV may be asserted for only 1 bit time, therefore, reading this bit may not return a logic 1 even though a pulse density violation has occurred. When the XPDE is enabled for pulse stuffing, PDV remains logic 0.

PDVI, Z16DI:

The PDVI and Z16DI bits identify the source of a generated interrupt. PDVI is a logic 1 whenever a change in the pulse density violation indication generated an interrupt. PDVI is cleared to 0 when this register is read. Z16DI is a logic 1 whenever 16 consecutive zeros are detected. Z16DI is cleared to 0 when this register is read. Note that the PDVI and Z16DI interrupt indications operate regardless of whether the corresponding interrupt enables are enabled or disabled. When STUFF is set to logic 1, the PDVI and Z16DI bits are forced to logic 0.

Z16DE:

The Z16DE bit enables an interrupt to be generated on the microprocessor INTB pin when 16 consecutive zeros are detected. When Z16DE is set to logic 1, interrupt is generation is enabled. When Z16DE is set to logic 0, interrupt generation is disabled.

PDVE:

The PDVE bit enables an interrupt to be generated on the microprocessor INTB pin when a change in the pulse density is detected. When PDVE is set to logic 1, an interrupt is generated whenever a pulse density violation occurs or when the pulse density ceases to exist (if STUFE is logic 0). When PDVE is set to logic 0, interrupt generation by pulse density violations is disabled.

### Register 06AH: T1 RBOC Enable

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | R/W | IDLE | 0 |
| Bit 1 | R/W | AVC | 0 |
| Bit 0 | R/W | BOCE | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register selects the validation criteria to be used in determining a valid bit oriented code (BOC) and enables generation of an interrupt on a change in code status.

IDLE:

The IDLE bit position enables or disables the generation of an interrupt when there is a transition from a validated BOC to idle code. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation.

AVC:

The AVC bit position selects the validation criteria used in determining a valid BOC. A logic 1 in the AVC bit position selects the "alternate" validation criterion of 4 out of 5 matching BOCs; a logic 0 selects the 8 out of 10 matching BOC criterion.

BOCE:

The BOCE bit position enables or disables the generation of an interrupt on the microprocessor INTB pin when a valid BOC is detected. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation.

### Register 06BH: T1 RBOC Code Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | IDLEI | 0 |
| Bit 6 | R | BOCI | 0 |
| Bit 5 | R | BOC[5] | 1 |
| Bit 4 | R | BOC[4] | 1 |
| Bit 3 | R | BOC[3] | 1 |
| Bit 2 | R | BOC[2] | 1 |
| Bit 1 | R | BOC[1] | 1 |
| Bit 0 | R | BOC[0] | 1 |

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

BOC[5:0]:

The BOC[5:0] bits indicate the current state value of the received bit-oriented code.

IDLEI:

The IDLEI bit position indicates whether an interrupt was generated by the detection of the transition from a valid BOC to idle code. A logic 1 in the IDLEI bit position indicates that a transition from a valid BOC to idle code has generated an interrupt; a logic 0 in the IDLEI bit position indicates that no transition from a valid BOC to idle code has been detected. IDLEI is cleared to logic 0 when the register is read.

BOCI:

The BOCI bit position indicates whether an interrupt was generated by the detection of a valid BOC. A logic 1 in the BOCI bit position indicates that a validated BOC code has generated an interrupt; a logic 0 in the BOCI bit position indicates that no BOC has been detected. BOCI is cleared to logic 0 when the register is read.

### Register 06CH: TPSC Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | R/W | Reserved | 0 |
| Bit 1 | R/W | IND | 0 |
| Bit 0 | R/W | PCCE | 0 |

This register allows selection of the microprocessor read access type and output enable control for the Transmit Per-channel Serial Controller.

Reserved:

The Reserved bit must be programmed to logic 0 for normal operation.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the COMET is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the per-channel functions. When the PCCE bit is set to a logic 1, each channel's PCM Control byte, IDLE Code byte, and SIGNALING Control byte are passed on to the XBAS. When the PCCE bit is set to logic 0, the per-channel functions are disabled.

### Register 06DH: TPSC µP Access Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | BUSY | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | | Unused | X |

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 640 ns.

### Register 06EH: TPSC Channel Indirect Address/Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | R/WB | 0 |
| Bit 6 | R/W | A6 | 0 |
| Bit 5 | R/W | A5 | 0 |
| Bit 4 | R/W | A4 | 0 |
| Bit 3 | R/W | A3 | 0 |
| Bit 2 | R/W | A2 | 0 |
| Bit 1 | R/W | A1 | 0 |
| Bit 0 | R/W | A0 | 0 |

This register allows the µP to access the internal TPSC registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal TPSC register is requested; when R/WB is set to a logic 0, a write to the internal TPSC register is requested.

### Register 06FH: TPSC Channel Indirect Data Buffer

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | D7 | 0 |
| Bit 6 | R/W | D6 | 0 |
| Bit 5 | R/W | D5 | 0 |
| Bit 4 | R/W | D4 | 0 |
| Bit 3 | R/W | D3 | 0 |
| Bit 2 | R/W | D2 | 0 |
| Bit 1 | R/W | D1 | 0 |
| Bit 0 | R/W | D0 | 0 |

This register contains either the data to be written into the internal TPSC registers when a write request is initiated or the data read from the internal TPSC registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the byte to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data byte.

The internal TPSC registers control the per-channel functions on the Transmit PCM data, provide the per-channel Transmit IDLE Code, and provide the per-channel Transmit signaling control and the alternate signaling bits. The functions are allocated within the registers as follows:

**Table 43 - TPSC Indirect Register Map**

| Addr | Register |
|---|---|
| 20H | PCM Data Control byte for Timeslot 0 |
| 21H | PCM Data Control byte for Channel 1/Timeslot 1 |
| 22H | PCM Data Control byte for Channel 2/Timeslot 2 |
| . . | . . |
| 37H | PCM Data Control byte for Channel 23/Timeslot 23 |
| 38H | PCM Data Control byte for Channel 24/Timeslot 24 |

| Addr | Register |
|---|---|
| 39H | PCM Data Control byte for Timeslot 25 |
| • • • | • • • |
| 3EH | PCM Data Control byte for Timeslot 30 |
| 3FH | PCM Data Control byte for Timeslot 31 |
| 40H | IDLE Code byte for Timeslot 0 |
| 41H | IDLE Code byte for Channel 1/Timeslot 1 |
| 42H | IDLE Code byte for Channel 2/Timeslot 2 |
| • • • | • • • |
| 57H | IDLE Code byte for Channel 23/Timeslot 23 |
| 58H | IDLE Code byte for Channel 24/Timeslot 24 |
| 59H | IDLE Code byte for Timeslot 25 |
| • • • | • • • |
| 5EH | IDLE Code byte for Timeslot 30 |
| 5FH | IDLE Code byte for Timeslot 31 |
| 60H | E1 Control byte for Timeslot 0 |
| 61H | Signaling/E1 Control byte for Channel 1/Timeslot 1 |
| 62H | Signaling/E1 Control byte for Channel 2/Timeslot 2 |
| • • • | • • • |
| 77H | Signaling/E1 Control byte for Channel 23/Timeslot 23 |
| 78H | Signaling/E1 Control byte for Channel 24/Timeslot 24 |
| 79H | Signaling/E1 Control byte for Timeslot 25 |
| • • • | • • • |
| 7EH | Signaling/E1 Control byte for Timeslot 30 |
| 7FH | Signaling/E1 Control byte for Timeslot 31 |

The "Timeslot" designation refers to the E1 assignment. The "Channel" designation refers to the T1 assignment.

The bits within each control byte are allocated as follows:

**Table 44 - TPSC Indirect Registers 20H-3FH: PCM Data Control byte**

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | INVERT | X |
| Bit 6 | R/W | IDLE_DS0 | X |
| Bit 5 | R/W | DMW | X |
| Bit 4 | R/W | SIGNINV | X |
| Bit 3 | R/W | TEST | X |
| Bit 2 | R/W | LOOP | X |
| Bit 1 | R/W | ZCS0 | X |
| Bit 0 | R/W | ZCS1 | X |

INVERT:

When the INVERT bit is set to a logic 1, data from the BTPCM input is inverted for the duration of that channel.

The INVERT bit only has effect in T1 mode.

IDLE_DS0:

When the IDLE_DS0 bit is set to a logic 1, data from the IDLE Code Byte replaces the BTPCM input data for the duration of that channel. The IDLE_DS0 bit controls insertion of the IDLE Code Byte only in T1 mode.

When the NxDS0 mode is active, IDLE_DS0 also controls the generation of BTCLK. When IDLE_DS0 is a logic 0, data is inserted from the transmit backplane interface during that channel, and eight clock pulses are generated on BTCLK. When IDLE_DS0 is a logic 1, an IDLE code byte is inserted, and BTCLK is suppressed for the duration of that channel.

SIGNINV:

When the SIGNINV bit is set to a logic 1, the most significant bit from the BTPCM input is inverted for that channel.

The SIGNINV bit only has effect in T1 mode.

The INVERT and SIGNINV can be used to produce the following types of inversions:

**Table 45 - TPSC Transmit Data Conditioning**

| INVERT | SIGNINV | Effect on PCM Channel Data |
|---|---|---|
| 0 | 0 | PCM Channel data is unchanged |
| 1 | 0 | All 8 bits of the PCM channel data are inverted |
| 0 | 1 | Only the MSB of the PCM channel data is inverted (SIGN bit inversion) |
| 1 | 1 | All bits EXCEPT the MSB of the PCM channel data is inverted (Magnitude inversion) |

DMW:

When the DMW bit is set to a logic 1, the digital milliwatt pattern replaces the BTPCM input data for the duration of that channel.

The DMW bit only has effect in T1 mode.

TEST:

When the TEST bit is set to a logic 1, channel data from the BTPCM input is either overwritten with a test pattern from the PRGD block or is routed to the PRGD block and compared against an expected test pattern. The RXPATGEN bit in the Pattern Generator/Detector Positioning/Control register determines whether the transmit data is overwritten or compared as shown in the following table:

**Table 46 - Transmit Test Pattern Modes**

| TEST | RXPATGEN | Description |
|---|---|---|
| 0 | X | Channel data is not included in test pattern |
| 1 | 1 | Channel data is routed to PRGD and compared against expected test pattern |
| 1 | 0 | Channel data is overwritten with PRGD test pattern |

All the channels that are routed to the PRGD are concatenated and treated as a continuous stream in which pseudorandom are searched for. Similarly, all channels set to be overwritten with PRGD test pattern data are treated such that if the channels are subsequently extracted and concatenated, the PRBS appears in the concatenated stream. Pattern generation/detection can

be enabled to work on only the first 7 bits of a channel (for Nx56 kbps fractional T1) using the Nx56k_DET and Nx56k_GEN bits in the Pattern Generator/Detector Positioning/Control register. The PRGD can also be enabled to work on the entire DS1, including framing bits, using the UNF_GEN and UNF_DET bits in the Pattern Generator/Detector Positioning/Control register.

LOOP:

The LOOP bit enables the DS0 loopback. When the LOOP bit is set to a logic 1, transmit data is overwritten with the corresponding channel data from the receive line. When the Receive Elastic Store (RX-ELST) is bypassed, it is used to align the receive line data to the transmit frame. When RX-ELST is enabled, however, it is unavailable to facilitate per-DS0 loopbacks.

Data inversion, idle, loopback and test pattern insertion/checking are performed independent of the transmit framing format. DS0 loopback takes precedence over digital milliwatt pattern insertion. Next in priority is test pattern insertion, which, in turn, takes precedence over idle code insertion. Data inversion has the lowest priority. When test pattern checking is enabled, the transmit data is compared before DS0 loopback, digital milliwatt pattern insertion, idle code insertion or data inversion is performed. None of this prioritizing has any effect on the gapping of BTCLK in NxDS0 mode. That is, if both DS0 loopback and idle code insertion are enabled for a given channel while in NxDS0 mode, the DS0 will be looped-back, will not be overwritten with idle code, and BTCLK will be gapped out for the duration of the channel. Similarly, none of the prioritizing has any effect on the generation of test patterns from the PRGD, only on the insertion of that pattern. Thus, if both DMW and TEST are set for a given DS0, and RXPATGEN = 0, the test pattern from the PRGD will be overwritten with the digital milliwatt code. This same rule also applies to test patterns inserted via the UNF_GEN bit in the Pattern Generator/Detector Positioning/Control register.

ZCS0, ZCS1:

The ZCS0 and ZCS1 bits select the zero code suppression used as follows:

**Table 47 - Transmit Zero Code Suppression Formats**

| ZCS0 | ZCS1 | Description |
|---|---|---|
| 0 | 0 | No Zero Code Suppression |
| 0 | 1 | “Jammed bit 8" - Every bit 8 is forced to a one. This may be used for 56 kbit/s data service. This is the only code that should be inserted in E1 mode. |

| ZCS0 | ZCS1 | Description |
|---|---|---|
| 1 | 0 | GTE Zero Code Suppression (Bit 8 of an all zero channel byte is replaced by a one, except in signaling frames where bit 7 is forced to a one.) |
| 1 | 1 | Bell Zero Code Suppression (Bit 7 of an all zero channel byte is replaced by a one.) |

**Table 48 - TPSC Indirect Registers 40H-5FH: IDLE Code byte**

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | IDLE7 | X |
| Bit 6 | R/W | IDLE6 | X |
| Bit 5 | R/W | IDLE5 | X |
| Bit 4 | R/W | IDLE4 | X |
| Bit 3 | R/W | IDLE3 | X |
| Bit 2 | R/W | IDLE2 | X |
| Bit 1 | R/W | IDLE1 | X |
| Bit 0 | R/W | IDLE0 | X |

The contents of the IDLE Code byte register is substituted for the channel data on BTPCM when the IDLE_DS0 bit in the PCM Control Byte is set to a logic 1 in T1 mode or when the SUBS bit of the E1 Control Byte is logic 1 and the DS[0] bit of the E1 Control Byte is logic 0 in E1 mode. The IDLE Code is transmitted from MSB (IDLE7) to LSB (IDLE0).

**Table 49 - TPSC Indirect Registers 60H-7FH: Signaling/E1 Control byte**

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | SIGC[0]/SUBS | X |
| Bit 6 | R/W | SIGC[1]/DS[0] | X |
| Bit 5 | R/W | DS[1] | X |
| Bit 4 | R/W | SIGSRC | X |
| Bit 3 | R/W | A' | X |
| Bit 2 | R/W | B' | X |
| Bit 1 | R/W | C' | X |

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 0 | R/W | D' | X |

The significance of the bits in these registers is dependent on whether the operating mode is T1 or E1.

**E1 Mode**

SUBS, DS[1], and DS[0]:

The SUBS, DS[1], and DS[0] bits select one of the following data manipulations to be performed on the timeslot:

**Table 50 - Transmit Per-timeslot Data Manipulation**

| SUBS | DS[0] | DS[1] | Function |
|---|---|---|---|
| 0 | 0 | 0 | OFF - no change to PCM timeslot data |
| 0 | 0 | 1 | ADI - data inversion on timeslot bits 1, 3, 5, 7 |
| 0 | 1 | 0 | ADI - data inversion on timeslot bits 2, 4, 6, 8 |
| 0 | 1 | 1 | INV - data inversion on all timeslot bits |
| 1 | 0 | X | Data substitution on - IDLE code replaces BTPCM timeslot data |
| 1 | 1 | 0 | Data substitution on - A-Law digital pattern* replaces BTPCM timeslot data. |
| 1 | 1 | 1 | Data substitution on - µ-Law digital pattern* replaces BTPCM timeslot data. |

*Note: The A-Law digital milliwatt pattern used is that defined in Recommendation G.711 for A-law:

**Table 51 - A-Law Digital Milliwatt Pattern**

| Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 | Bit 8 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |

| Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 | Bit 8 |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |

*Note: The µ-Law digital milliwatt pattern used is that defined in Recommendation G.711 for µ-law:

**Table 52 - µ-Law Digital Milliwatt Pattern**

| Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 | Bit 8 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |

SIGSRC:

The SIGSRC bit is valid only if Channel Associated Signaling (CAS) is selected in the E1-TRAN Configuration Register; otherwise, it is ignored. When valid, the SIGSRC bit selects the source of the timeslot signaling bits: if SIGSRC is a logic 0, the signaling bits are taken from the incoming BTSIG stream in the format specified by the SIGEN and DLEN bits in the E1-TRAN Configuration Register; if SIGSRC is a logic 1, the signaling bits are taken from the A',B',C', and D' bit .

**T1 Mode**

Signaling insertion is controlled by the SIGC[1:0] bits. The source of the signaling bits is determined by SIGC0: when SIGC0 is set to a logic 1, signaling data is taken from the A', B', C', and D' bits; when SIGC0 is set to logic 0, signaling data is taken from the A,B,C, and D bit locations on the BTSIG input. Signaling insertion is controlled by SIGC1: when SIGC1 is set to a logic 1 and

ESF, SF, or SLC®96 transmit format is selected, insertion of signaling bits is enabled; when SIGC1 is set to logic 0, the insertion of signaling bits is disabled. For SF and SLC®96 formats, the C' and D' or C and D bits from Signaling Control byte or BTSIG, respectively, are inserted into the A and B signaling bit positions of every second superframe that is transmitted. It is assumed that C=A and D=B. The A',B',C', and D' bits do not pass through the Signaling Aligner block. When signaling insertion via the A',B',C', and D' bits is enabled, changing the signaling state by writing to the TPSC can cause the transmit stream to briefly (for one superframe or extended superframe) carry a signaling state that is neither the new or the old signaling state (e.g., may have the A bit from the new state but the B bit from the old state).

### Register 070H: RPSC Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | R/W | Reserved | 0 |
| Bit 1 | R/W | IND | 0 |
| Bit 0 | R/W | PCCE | 0 |

This register allows selection of the microprocessor read access type and output enable control for the Receive Per-channel Serial Controller.

Reserved:

The Reserved bit must be programmed to logic 0 for normal operation.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the COMET is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the per-channel functions. When the PCCE bit is set to a logic 1, the Data Trunk Conditioning Code byte and Signaling Trunk Conditioning Code byte are enabled to modify the received data and extracted signaling data streams (visible on BRPCM and BRSIG, if selected) under direction of each channel's PCM Control byte. When the PCCE bit is set to logic 0, the per-channel functions are disabled.

### Register 071H: RPSC µP Access Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | BUSY | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | | Unused | X |

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 640 ns.

### Register 072H: RPSC Channel Indirect Address/Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | R/WB | 0 |
| Bit 6 | R/W | A6 | 0 |
| Bit 5 | R/W | A5 | 0 |
| Bit 4 | R/W | A4 | 0 |
| Bit 3 | R/W | A3 | 0 |
| Bit 2 | R/W | A2 | 0 |
| Bit 1 | R/W | A1 | 0 |
| Bit 0 | R/W | A0 | 0 |

This register allows the µP to access the internal RPSC registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal RPSC register is requested; when R/WB is set to a logic 0, an write to the internal RPSC register is requested.

### Register 073H: RPSC Channel Indirect Data Buffer

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | D7 | 0 |
| Bit 6 | R/W | D6 | 0 |
| Bit 5 | R/W | D5 | 0 |
| Bit 4 | R/W | D4 | 0 |
| Bit 3 | R/W | D3 | 0 |
| Bit 2 | R/W | D2 | 0 |
| Bit 1 | R/W | D1 | 0 |
| Bit 0 | R/W | D0 | 0 |

This register contains either the data to be written into the internal RPSC registers when a write request is initiated or the data read from the internal RPSC registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the byte to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data byte.

The internal RPSC registers control the per-channel functions on the Receive PCM data provide the per-channel Data Trunk Conditioning Code and provide the per-channel Signaling Trunk Conditioning Code. The functions are allocated within the registers shown in Table 53:

**Table 53 - RPSC Indirect Register Map**

| Addr | Register |
|---|---|
| 20H | PCM Data Control byte for Timeslot 0 |
| 21H | PCM Data Control byte for Channel 1/Timeslot 1 |
| 22H | PCM Data Control byte for Channel 2/Timeslot 2 |
| . | . |
| . | . |
| 37H | PCM Data Control byte for Channel 23/Timeslot 23 |
| 38H | PCM Data Control byte for Channel 24/Timeslot 24 |

| Addr | Register |
|---|---|
| 39H | PCM Data Control byte for Timeslot 25 |
| • | • |
| • | • |
| 3EH | PCM Data Control byte for Timeslot 30 |
| 3FH | PCM Data Control byte for Timeslot 31 |
| 40H | Data Trunk Conditioning byte for Timeslot 0 |
| 41H | Data Trunk Conditioning byte for Channel 1/Timeslot 1 |
| 42H | Data Trunk Conditioning byte for Channel 2/Timeslot 2 |
| • | • |
| • | • |
| 57H | Data Trunk Conditioning byte for Channel 23/Timeslot 23 |
| 58H | Data Trunk Conditioning byte for Channel 24/Timeslot 24 |
| 59H | Data Trunk Conditioning byte for Timeslot 25 |
| • | • |
| • | • |
| 5EH | Data Trunk Conditioning byte for Timeslot 30 |
| 5FH | Data Trunk Conditioning byte for Timeslot 31 |
| 61H | Signaling Trunk Conditioning byte for Channel 1/Timeslot 1 |
| 62H | Signaling Trunk Conditioning byte for Channel 2/Timeslot 2 |
| • | • |
| • | • |
| 77H | Signaling Trunk Conditioning byte for Channel 23/Timeslot 23 |
| 78H | Signaling Trunk Conditioning byte for Channel 24/Timeslot 24 |
| 79H | Signaling Trunk Conditioning byte for Timeslot 25 |
| • | • |
| • | • |
| 7EH | Signaling Trunk Conditioning byte for Timeslot 30 |
| 7FH | Signaling Trunk Conditioning byte for Timeslot 31 |

The "Timeslot" designation refers to the E1 assignment. The "Channel" designation refers to the T1 assignment.

The bits within each control byte are allocated as follows:

**Table 54 - RPSC Indirect Registers 20H-3FH: PCM Data Control byte**

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | TEST | X |
| Bit 6 | R/W | DTRKC | X |
| Bit 5 | R/W | STRKC | X |
| Bit 4 | R/W | DMW | X |
| Bit 3 | R/W | DMWALAW | X |
| Bit 2 | R/W | SIGNINV | X |
| Bit 1 | | Unused | X |
| Bit 0 | | Unused | X |

TEST:

When the TEST bit is set to a logic 1, receive channel data is either overwritten with a test pattern from the PRGD block or is routed to the PRGD block and compared against an expected test pattern. The RXPATGEN bit in the Pattern Generator/Detector Positioning/Control register determines whether the transmit data is overwritten or compared as shown in the following table:

**Table 55 - Receive Test Pattern Modes**

| TEST | RXPATGEN | Description |
|---|---|---|
| 0 | X | Channel data is not included in test pattern |
| 1 | 0 | Channel data is routed to PRGD and compared against expected test pattern |
| 1 | 1 | Channel data is overwritten with PRGD test pattern |

All the channels that are routed to the PRGD are concatenated and treated as a continuous stream in which pseudorandom are searched for. Similarly, all channels set to be overwritten with PRGD test pattern data are treated such that if the channels are subsequently extracted and concatenated, the PRBS appears in the concatenated stream. Pattern generation/detection can be enabled to work on only the first 7 bits of a channel (for Nx56 kbps fractional T1) using the

Nx56k_DET and Nx56k_GEN bits in the Pattern Generator/Detector Positioning/Control register. The PRGD can also be enabled to work on the entire DS1, including framing bits, using the UNF_GEN and UNF_DET bits in the Pattern Generator/Detector Positioning/Control register.

DTRKC:

When the DTRKC bit is set to a logic 1, data from the Data Trunk Conditioning Code Byte contained within the RPSC indirect registers replaces the BRPCM output data for the duration of that channel.

When the Receive Backplane Configuration register selects a NxDS0 mode, the DTRKC bit also controls BRCLK generation. If DTRKC is a logic 1, BRCLK is held low for the duration of the channel.

STRKC:

When the STRKC bit is set to a logic 1, data from the Signaling Trunk Conditioning Code Byte contained within the RPSC indirect registers replaces the BRSIG output data for the duration of that channel.

DMW:

When the DMW bit is set to a logic 1, a digital milliwatt pattern replaces the BRPCM output data for the duration of that channel. The particular digital milliwatt pattern used, A-law or u-law, is selected by the DMWALAW bit of this register.

DMWALAW:

When the DMWALAW bit is set to a logic 1, the digital milliwatt pattern replacing the BRPCM output data for the duration of that channel is the A-law pattern (see Table 51). When the DMWALAW bit is set to a logic 0, the digital milliwatt pattern replacing the BRPCM output data for the duration of that channel is the µ-law pattern (see Table 52).

SIGNINV:

When the SIGNINV bit is set to a logic 1, the most significant bit of the data output on the BRPCM pin is the inverse of the received data most significant bit for that channel.

In T1 mode, the RINV[1] of the and SIGNINV bits can be used to invert data as shown in Table 37:

**Table 56 - RPSC Indirect Registers 40H-5FH: Data Trunk Conditioning Code byte**

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | DTRK7 | X |
| Bit 6 | R/W | DTRK6 | X |
| Bit 5 | R/W | DTRK5 | X |
| Bit 4 | R/W | DTRK4 | X |
| Bit 3 | R/W | DTRK3 | X |
| Bit 2 | R/W | DTRK2 | X |
| Bit 1 | R/W | DTRK1 | X |
| Bit 0 | R/W | DTRK0 | X |

The contents of the Data Trunk Conditioning Code byte register is substituted for the channel data on BRPCM when the DTRKC bit in the PCM Control Byte is set to a logic 1. The Data Trunk Conditioning Code is transmitted from MSB (DTRK7) to LSB (DTRK0).

**Table 57 - RPSC Indirect Registers 61H-7FH: Signaling Trunk Conditioning byte**

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | R/W | A' | X |
| Bit 2 | R/W | B' | X |
| Bit 1 | R/W | C' | X |
| Bit 0 | R/W | D' | X |

The contents of the Signaling Trunk Conditioning Code byte register is substituted for the channel signaling data on BRSIG when the STRKC bit is set to a logic 1. The Signaling Trunk Conditioning Code is placed in least significant nibble of the channel byte.

### Register 078H: T1 APRM Configuration/Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | R/W | R | 0 |
| Bit 4 | R/W | U1 | 0 |
| Bit 3 | R/W | U2 | 0 |
| Bit 2 | R/W | CONT_CRC | 0 |
| Bit 1 | R/W | INTE | 0 |
| Bit 0 | R/W | AUTOUPDATE | 0 |

AUTOUPDATE:

The AUTOUPDATE bit controls the automatic updating of the performance report on a per second basis. If this bit is set to a logic 1, the Performance Report Messages are generated and updated once a second. When AUTOUPDATE is set to a logic 0, the performance report is updated manually by toggling the MAN_LOAD register bit.

INTE:

The INTE bit enables the interrupt output pin. When INTE is set to a logic 1, a logic 1 in the INTR bit in the T1 APRM Interrupt Status register asserts the INTB output low. INTR is disabled from generating interrupts when INTE is set to a logic 0.

CONT_CRC:

The CONT_CRC is the Continuous CRC bit. When set to logic 1, the SE and G6 bits in the Performance Report are set to1 and G1, G2, G3, G4, G5 and FE are set to 0. When reset to logic 0, the Gn (n = [1..5]), FE and SE bits are set according to the received CRC errors.

U1, U2:

The U1, U2 bits are under study for synchronization. Their default value is 0. These bits require two updating cycles before they are included in the performance report.

R:

The R bit is a reserved bit in the performance report. The default value is 0. This bit requires two updating cycles before it is included in the performance report.

### Register 079H: T1 APRM Manual Load

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | R/W | MAN_LOAD | 0 |

MAN_LOAD:

The MAN_LOAD bit is used to load the next Performance Report into the holding registers. This bit is enabled when AUTOUPDATE is set to a logic 0. In manual PR generation mode, it is important to poll the MAN_LOAD bit to ensure that the previous Performance Report transmission has been transmitted. When the microprocessor requests a Performance Report, the MAN_LOAD bit is set high. When the last bit of the Performance Report has been transmitted, the MAN_LOAD bit is reset to a logic 0.

### Register 07AH: T1 APRM Interrupt Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | R | INTR | 0 |

INTR:

The interrupt (INTR) bit is set to logic 1 on one second boundaries, to signal that the one second data is ready. If the INTE bit is a logic 1, the INTB output is asserted low when INTR is logic 1. INTR is cleared when this register is read.

### Register 07BH: T1 APRM One Second Content Octet 2

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | SAPI[5] | 0 |
| Bit 6 | R/W | SAPI[4] | 0 |
| Bit 5 | R/W | SAPI[3] | 1 |
| Bit 4 | R/W | SAPI[2] | 1 |
| Bit 3 | R/W | SAPI[1] | 1 |
| Bit 2 | R/W | SAPI[0] | 0 |
| Bit 1 | R/W | C/R | 0 |
| Bit 0 | R/W | EA | 0 |

SAPI[5:0]:

The SAPI[5:0] represent the service access point identifier bits. The value of SAPI[5:0] in the performance report is constant i.e., SAPI = 14.

C/R:

The C/R bit is the Command/Response bit. The value of C/R from the CI is set to a logic 0 and the value of the C/R bit from the carrier is set to a logic 1.

EA:

The EA bit is the Extended Address bit in the second octet. The EA bit defaults to logic 0.

### Register 07CH: T1 APRM One Second Content Octet 3

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | TEI[6] | 0 |
| Bit 6 | R/W | TEI[5] | 0 |
| Bit 5 | R/W | TEI[4] | 0 |
| Bit 4 | R/W | TEI[3] | 0 |
| Bit 3 | R/W | TEI[2] | 0 |
| Bit 2 | R/W | TEI[1] | 0 |
| Bit 1 | R/W | TEI[0] | 0 |
| Bit 0 | R/W | EA | 1 |

TEI[6:0]:

The TEI[6:0] bits represent the terminal endpoint identifier. The TEI[6:0] default to logic 0.

EA:

The EA bit is the Extended Address bit in the third octet. The EA bit defaults to logic 1.

### Register 07DH: T1 APRM One Second Content Octet 4

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | CONTROL[7] | 0 |
| Bit 6 | R/W | CONTROL[6] | 0 |
| Bit 5 | R/W | CONTROL[5] | 0 |
| Bit 4 | R/W | CONTROL[4] | 0 |
| Bit 3 | R/W | CONTROL[3] | 0 |
| Bit 2 | R/W | CONTROL[2] | 0 |
| Bit 1 | R/W | CONTROL[1] | 1 |
| Bit 0 | R/W | CONTROL[0] | 1 |

CONTROL[7:0]:

This register set the value of the CONTROL field in the performance report and defaults to "00000011". It is inserted into the fourth octet of the performance report.

### Register 07EH: T1 APRM One Second Content MSB (Octet 5)

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | G3 | X |
| Bit 6 | R | LV | X |
| Bit 5 | R | G4 | X |
| Bit 4 | R | U1 | X |
| Bit 3 | R | U2 | X |
| Bit 2 | R | G5 | X |
| Bit 1 | R | SL | X |
| Bit 0 | R | G6 | X |

The contents of this register represent the values encoded in the latest performance report transmitted. This register is updated coincident with the assertion of the INTR bit of the T1 APRM Interrupt Status register.

G3:

This bit is set to a logic-1, if the number of CRC error events in a one second interval is greater than 5 and less than or equal to 10 (i.e., 5 < CRC error events ≤ 10).

LV:

This bit is set to a logic 1, if the number of Line code violation events in a one second interval is greater than or equal to 1 (i.e., LCV ≥ 1).

G4:

This bit is set to a logic 1, if the number of CRC error events in a one second interval is greater than 10 and less than or equal to 100 (i.e., 10 <CRC error events ≤ 100).

U1,U2:

Under Study For Synchronization. The default value is set by the U1 and U2 bits in the T1 APRM configuration register (register 078H).

G5:

This bit is set to a logic 1 if, the number of CRC error events is greater than 100 and less than or equal to 319 (i.e., 100 < CRC error events ≤ 319).

SL:

This bit is set to a logic 1 if, one or more controlled slip events occur in a one second interval i.e. (SL ≥ 1).

G6:

This bit is set to a logic 1 if the number of CRC error events in a one second interval is greater than or equal to 320 (i.e., CRC error events ≥ 320).

### Register 07FH: T1 APRM One Second Content LSB (Octet 6)

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | FE | X |
| Bit 6 | R | SE | X |
| Bit 5 | R | LB | X |
| Bit 4 | R | G1 | X |
| Bit 3 | R | R | X |
| Bit 2 | R | G2 | X |
| Bit 1 | R | Nm | X |
| Bit 0 | R | NI | X |

The contents of this register represent the values encoded in the latest performance report transmitted. This register is updated coincident with the assertion of the INTR bit of the T1 APRM Interrupt Status register.

FE:

This bit is set to a logic 1 if one or more Frame Synchronization Bit Error Event occurs in a 1 second window (SE =0). If more than one FE occurs in a 3 ms window, a SE is declared and the FE bit is set to 0.

SE:

This bit is set to a logic 1 if, Severely Errored Framing Event ≥ 1 (FE =0). If more than one FE occurs in a 3 ms window, a SE is declared and the FE bit is set to 0.

LB:

This bit is set to a logic 1 if the Payload Loopback is activated.

G1:

This bit is set to a logic 1 if the number of CRC error events in a one second interval is equal to 1 (i.e., CRC error events =1).

R:

Reserved. The default value is set by the R bit in the T1 APRM configuration register (register 078H).

G2:

This bit is set to a logic 1 if the number of CRC error events in a one second interval is greater than 1 and less than or equal to 5 (i.e., 1 <CRC error events ≤ 5).

NmNi:

One second Report Modulo 4 Counter. Every second, the value of NmNi is incremented by one for the most recent second. The values NmNi can take are shown in the table below:

**Table 58 - NmNi Settings**

| NmNi | Time |
|---|---|
| 00 | t (most recent second) |
| 11 | t-1 |
| 10 | t-2 |
| 01 | t-3 |

### Register 080H: E1 TRAN Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | AMI | 0 |
| Bit 6 | R/W | SIGEN | 1 |
| Bit 5 | R/W | DLEN | 1 |
| Bit 4 | R/W | GENCRC | 0 |
| Bit 3 | R/W | FDIS | 0 |
| Bit 2 | R/W | FEBEDIS | 0 |
| Bit 1 | R/W | INDIS | 0 |
| Bit 0 | R/W | XDIS | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 0, this register is held reset.

AMI:

The AMI bit enables AMI line coding when set to logic 1; when it is set to logic 0, the HDB3 line coding is enabled.

SIGEN, DLEN:

The SIGEN and DLEN bits select the signaling data source for Time Slot 16 (TS16) as follows:

**Table 59 - E1 Signaling Insertion Mode**

| SIGEN | DLEN | MODE |
|---|---|---|
| 0 | 0 | Signaling insertion disabled. TS16 data is taken directly from the input BTPCM TS16. |
| 0 | 1 | Reserved. |
| 1 | 0 | Reserved. |
| 1 | 1 | CAS enabled. TS16 data is taken from either BTSIG stream or from the TPSC SIGNALING/E1 Control byte as selected on a per-timeslot basis via the SIGSRC bit. The format of the BTSIG input data stream is shown in the "Functional Timing" section. |

When channel associated signaling (CAS) is enabled, the format of the input BTSIG stream is selected by the DLEN bit. A logic 1 in the DLEN bit position selects the PMC compatible format in which the BTSIG stream contains the signaling data nibble in the lower four bits of the time slot byte. A logic 0 in the DLEN bit position is reserved and should not be used.

GENCRC:

The GENCRC bit enables generation of the CRC multiframe when set to logic 1. When enabled, the E1-TRAN generates the CRC multiframe alignment signal, calculates and inserts the CRC bits, and if enabled by FEBEDIS, inserts the FEBE indication in the spare bit positions. The CRC bits transmitted during the first submultiframe (SMF) are indeterminate and should be ignored. The CRC bits calculated during the transmission of the $n^{th}$ SMF (SMF n) are transmitted in the following SMF (SMF n+1). When GENCRC is set to logic 0, the CRC generation is disabled. The CRC bits are then set to the logic value contained in the Si[1] bit position in the International/National Bit Control Register and bit 1 of the NFAS frames are set to the value of Si[0] bit if enabled by INDIS, or, if not enabled by INDIS, are taken directly from BTPCM. When BTPCM or Si[1] are transmitted in lieu of the calculated CRC bits, there is no delay of one SMF (i.e., the BTPCM bits received in SMF n are transmitted in the same SMF). The same applies when substituting Si[1] in place of the calculated CRC bits.

FDIS:

The FDIS bit value controls the generation of the framing alignment signal. A logic 1 in the FDIS bit position disables the generation of the framing pattern in TS0 and allows the incoming data on BTPCM to pass through the E1-TRAN transparently. A logic 0 in FDIS enables the generation of the framing pattern, replacing TS0 of frames 0, 2, 4, 6, 8, 10, 12 and 14 with the frame alignment signal, and if enabled by INDIS, replacing TS0 of frames 1, 3, 5, 7, 9, 11, 13 and 15 with the contents of the International Bits Control Register. When FDIS is a logic 1, framing is globally disabled and the values in control bits GENCRC, FEBEDIS, INDIS, and XDIS are ignored.

Note that the above is true only if the AIS bit in the E1-TRAN Transmit Alarm/Diagnostic Control register is a logic 0. If AIS is logic 1, the output bit stream becomes all-ones unconditionally.

INDIS, GENCRC and FEBEDIS:

The INDIS bit controls the insertion of the International and National bits into TS0. When INDIS is set to logic 0, the contents of the E1-TRAN International Bits Control register and the National bits are inserted into TS0 (note that only the national bits that are enabled in the E1-TRAN National Bits Codeword registers are inserted into TS0); when INDIS is a logic 1, the contents of the

E1-TRAN International Bits Control register and the E1-TRAN National bits are ignored and the values for those bit positions in the output stream are taken directly from the BTPCM stream. When INDIS and FDIS are logic 0, the bit values used for the International and National bits are dependent upon the values of the GENCRC and FEBEDIS configuration bits, as shown in the following table:

**Table 60 - E1 Timeslot 0 Bit 1 Insertion Control Summary**

| GENCRC | FEBEDIS | Source of International Bits |
|---|---|---|
| 0 | X | Bit position Si[1] in the International Bits Control register is used for the International bit in the frame alignment signal (FAS) frames and the Si[0] bit in the non-frame alignment signal (NFAS) frames if INDIS is logic 0. BTPCM replaces Si[1:0] if INDIS is logic 1. |
| 1 | 0 | The calculated CRC bits are used for the International bit in the FAS frames and the generated CRC multiframe alignment signal and the FEBE bits are used for the International bit in the NFAS frames. |
| 1 | 1 | The calculated CRC bits are used for the International bit in the FAS frames and the generated CRC multiframe alignment signal is used for the International bit in the NFAS frames, with the Si[1:0] bits in the International Bits Control register used for the spare bits. |

XDIS:

If FDIS is logic 0 and SIGEN is logic 1, the XDIS bit controls the insertion of the Extra bits in TS16 of frame 0 of the signaling multiframe as follows. When XDIS is set to a logic 0, the contents of the E1-TRAN Extra Bits Control Register are inserted into TS16, frame 0; when XDIS is a logic 1, the contents of the register are ignored and the values for those bits positions in the output stream are taken directly from the BTPCM stream. That is, when XDIS and FDIS are logic 0 and SIGEN is logic 1, the X1, X3 and X4 bit values from the E1-TRAN Extra Bits Control Register are used for the Extra bits in TS16 of frame 0 of the signaling multiframe.

When the COMET is reset, the contents of this register are set to logic 0, except SIGEN and DLEN which are set to logic 1.

### Register 081H: E1 TRAN Transmit Alarm/Diagnostic Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | MTRK | 0 |
| Bit 6 | R/W | FPATINV | 0 |
| Bit 5 | R/W | SPLRINV | 0 |
| Bit 4 | R/W | SPATINV | 0 |
| Bit 3 | R/W | RAI | 0 |
| Bit 2 | R/W | YBIT | 0 |
| Bit 1 | R/W | Reserved | 0 |
| Bit 0 | R/W | AIS | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 0, this register is held reset.

MTRK:

The MTRK bit forces trunk conditioning (i.e., idle code substitution and signaling substitution) when MTRK is a logic 1. This has the same effect as setting data substitution to IDLE code on time slots 1-15 and 17-31 (setting bits SUBS and DS[0] to binary 10 in time slots 1-15 and 17-31) and sourcing the signaling data from the TPCS stream, if SIGEN is logic 1. When SIGEN is logic 0, TS16 will be treated the same as time slots 1-15 and 17-31 and will contain data sourced from TIDL. TS0 data is determined by the control bits associated with it and is independent of the value of MTRK.

FPATINV:

The FPATINV bit is a diagnostic control bit. When set to logic 1, FPATINV forces the frame alignment signal (FAS) written into TS0 to be inverted (i.e., the correct FAS, 0011011, is substituted with 1100100); when set to logic 0, the FAS is unchanged.

SPLRINV:

The SPLRINV bit is a diagnostic control bit. When set to logic 1, SPLRINV forces the "spoiler bit" written into bit 2 of TS0 of NFAS frames to be inverted (i.e., the spoiler bit is forced to 0); when set to logic 0, the spoiler bit is unchanged.

SPATINV:

The SPATINV bit is a diagnostic control bit. When set to logic 1, SPATINV forces the signaling multiframe alignment signal written into bits 1-4 of TS16 of frame 0 of the signaling multiframe to be inverted (i.e., the correct signaling multiframe alignment signal, 0000, is substituted with 1111); when set to logic 0, the signaling multiframe alignment signal is unchanged.

RAI:

The RAI bit controls the transmission of the Remote Alarm Indication signal. A logic 1 in the RAI bit position causes bit 3 of NFAS frames to be forced to logic 1; otherwise, bit 3 of NFAS frames is a logic 0 unless the AUTOYELLOW register bit is set and a receive defect is present.

YBIT:

The YBIT bit controls the transmission of the signaling multiframe Alarm Indication Signal. A logic 1 in the YBIT bit position causes the Y-bit (bit 6) of TS16 of frame 0 of the signaling multiframe to be forced to logic 1; otherwise, the Y-bit is a logic 0.

Reserved:

This bit must be set to a logic 0 for correct operation.

AIS:

The AIS bit controls the transmission of the Alarm Indication Signal (unframed all-ones). A logic 1 in the AIS bit position forces the output streams to logic 1.

When the COMET is reset, the contents of this register are set to logic 0.

### Register 082H: E1 TRAN International/National Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | Si[1] | 1 |
| Bit 6 | R/W | Si[0] | 1 |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | | Unused | X |

When the E1/T1B bit of the Global Configuration register is a logic 0, this register is held reset.

Si[1:0]:

The bits Si[1] and Si[0] correspond to the International bits. The Si[1] and Si[0] bits can be programmed to any value and will be inserted into bit 1 of each FAS frame and NFAS frame, respectively, when the block is configured for frame generation, INDIS is set to logic 0, and CRC multiframe generation is disabled. When CRC multiframe generation is enabled, both Si[1] and Si[0] are ignored if FEBE indication is enabled; if FEBEDIS is a logic 1 and INDIS = 0, the values programmed in the Si[1] and Si[0] bit positions are inserted into the spare bit locations of frame 13 and frame 15, respectively, of the CRC multiframe. If both FEBEDIS and INDIS are logic 1, data from BTPCM replaces the Si[0] and Si[1] bits in the CRC multiframe.

The Si[1] and Si[0] bits should be programmed to a logic 1 when not being used to carry information.

When the COMET is reset, the contents of the register are set to logic 1.

### Register 083H: E1 TRAN Extra Bits Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | R/W | X[1] | 1 |
| Bit 2 | | Unused | X |
| Bit 1 | R/W | X[3] | 1 |
| Bit 0 | R/W | X[4] | 1 |

When the E1/T1B bit of the Global Configuration register is a logic 0, this register is held reset.

X[4:3,1]:

The X[1], X[3], and X[4] bits control the value programmed in the X[1], X[3], and X[4] bit locations (bits 5,7, and 8) in TS16 of frame 0 of the signaling multiframe, when enabled by XDIS. The X[1], X[3], and X[4] bits should be programmed to a logic 1 when not being used to carry information.

When the COMET is reset, the contents of the register are set to logic 1.

### Register 084H: E1 TRAN Interrupt Enable

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R/W | SIGMFE | 0 |
| Bit 3 | R/W | NFASE | 0 |
| Bit 2 | R/W | MFE | 0 |
| Bit 1 | R/W | SMFE | 0 |
| Bit 0 | R/W | FRME | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 0, this register is held reset.

FRME:

When FRME is set to logic 1, the interrupt generated by the FRMI interrupt register is propagated to the INTB output pin. When FRME is set to logic 0, the FRMI interrupt bit is masked.

SMFE:

When SMFE is set to logic 1, the interrupt generated by the SMFI interrupt register is propagated to the INTB output pin. When SMFE is set to logic 0, the SMFI interrupt bit is masked.

MFE:

When MFE is set to logic 1, the interrupt generated by the MFI interrupt register is propagated to the INTB output pin. When MFE is set to logic 0, the MFI interrupt bit is masked.

NFASE:

When NFASE is set to logic 1, the interrupt generated by the NFASI interrupt register is propagated to the INTB output pin. When NFASE is set to logic 0, the NFASI interrupt bit is masked.

SIGMFE:

When SIGMFE is set to logic 1, the interrupt generated by the SIGMFI interrupt register is propagated to the INTB output pin. When SIGMFE is set to logic 0, the SIGMFI interrupt bit is masked.

### Register 085H: E1 TRAN Interrupt Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R | SIGMFI | X |
| Bit 3 | R | NFASI | X |
| Bit 2 | R | MFI | X |
| Bit 1 | R | SMFI | X |
| Bit 0 | R | FRMI | X |

When the E1/T1B bit of the Global Configuration register is a logic 0, this register is held reset.

FRMI:

The FRMI interrupt bit is set to logic 1 on frame boundaries, it is set on timeslot 30, bit 7 of every frame in the transmit data stream. The contents of this register are cleared to logic 0 after the register is read.

SMFI:

The SMFI interrupt bit is set to logic 1 on CRC-4 sub multiframe boundaries, it is set on timeslot 30, bit 7 of frame 0 of the CRC submultiframe in the transmit data stream. The contents of this register are cleared to logic 0 after the register is read.

MFI:

The MFI interrupt bit is set to logic 1 on CRC-4 multiframe boundaries, it is set on timeslot 30, bit 7 of frame 0 of the CRC multiframe in the transmit data stream. The contents of this register are cleared to logic 0 after the register is read.

NFASI:

The NFASI interrupt bit is set to logic 1 on NFAS frame boundaries, it is set on timeslot 30, bit 7 of the NFAS frame in the transmit data stream. The contents of this register are cleared to logic 0 after the register is read.

SIGMFI:

The SIGMFI interrupt bit is set to logic 1 on signaling multiframe boundaries, it is set on timeslot 14, bit 1 of frame 0 of the signaling multiframe in the transmit data stream. The contents of this register are cleared to logic 0 after the register is read.

### Register 086H: E1 TRAN National Bits Codeword Select

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | SaSEL[2] | X |
| Bit 6 | R/W | SaSEL[1] | X |
| Bit 5 | R/W | SaSEL[0] | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | | Unused | X |

When the E1/T1B bit of the Global Configuration register is a logic 0, this register is held reset.

SaSEL[2:0]:

The SaSEL[2:0] bits select which National Bit codeword appears in the SaX[1:4] bits of the E1-TRAN National Bits Codeword register. These bits map to the codeword selection as follows:

**Table 61 - National Bits Codeword Select**

| SaSEL[2:0] | National Bit Codeword |
|---|---|
| 000 | Undefined |
| 001 | Undefined |
| 010 | Undefined |
| 011 | Sa4 |
| 100 | Sa5 |
| 101 | Sa6 |
| 110 | Sa7 |
| 111 | Sa8 |

### Register 087H: E1 TRAN National Bits Codeword

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | SaX_EN[1] | 0 |
| Bit 6 | R/W | SaX_EN[2] | 0 |
| Bit 5 | R/W | SaX_EN[3] | 0 |
| Bit 4 | R/W | SaX_EN[4] | 0 |
| Bit 3 | R/W | SaX[1] | 1 |
| Bit 2 | R/W | SaX[2] | 1 |
| Bit 1 | R/W | SaX[3] | 1 |
| Bit 0 | R/W | SaX[4] | 1 |

When the E1/T1B bit of the Global Configuration register is a logic 0, this register is held reset.

SaX[1:4]:

The code word SaX[1:4], (where X = 4, 5, 6, 7 or 8 as selected by the SaSEL[2:0] bits in the E1 TRAN National Bits Codeword Select register) appears in bit X (where X= 4, 5, 6, 7 or 8 as selected by the SaSEL[2:0] bits) of TS0 in frames 1, 3, 5 and 7 respectively (SMF I), or in frames 9, 11, 13 and 15 respectively (SMF II) of a G.704 CRC-4 multiframe. If X = 4, Sa4[1:4] bits appear in bit 4 of frames 1, 3, 5, and 7 respectively (SMF I) or in bit 4 of frames 9, 11, 13, and 15 (SMF II) of a G.704 CRC-4 multiframe. If X = 8, the codeword is inserted into bit 8 of TS 0 in frames 1, 3, 5 and 7 respectively (SMF I), or in frames 9, 11, 13 and 15 respectively (SMF II) of a G.704 CRC-4 multiframe.

The code word written in bits SaX[1:4] is latched internally and is updated every submultiframe. Therefore, if the code word is written into register 7 during SMF I of a G.704 CRC-4 multiframe, it will appear in the SaX[1:4] bits of SMF II of the same multiframe. If the code word is written into register 7 during SMF II of a multiframe, its contents will be latched internally and will appear in SMF I of the next multiframe.

Hence, a code written in SMF I of a multiframe is latched internally and appears in bit positions 4, 5, 6, 7, or 8 of TS0 in frames 9, 11, 13, and 15 of the CRC-4 multiframe. Also, a code word written during SMF II of a G.704 CRC-4 multiframe will appear in bit positions 4, 5, 6, 7, or 8 of TS0 in frames 1, 3, 5 and 7 of the subsequent CRC-4 multiframe.

Note that when Sa8[1:4] has been selected by the SaSEL[2:0] bits, the SaX[1:4] bits are mapped in this register in the reverse order as the SaX[1:4] bits, where X = 4, 5, 6 or 7. That is, Sa8[1] is mapped to bit 0 of this register, Sa8[2] is mapped to bit 1, Sa8[3] is mapped to bit 2, and Sa8[4] is mapped to bit 3.

SaX_EN[1:4]

Bits SaX_EN[1:4] enable the insertion of codeword bits SaX[1:4] (where X = 4, 5, 6, 7, or 8) respectively. If bits SaX_EN[1: 4] are set to logic 1, then the contents of bits SaX[1:4] are substituted into bit X of TS0 ( where X = 4, 5, 6, 7, or 8) of NFAS frames 1, 3, 5, and 7 of SMF I, or into NFAS frames 9, 11, 13, and 15 of SMF II. If any one or more of the SaX_EN[1:4] bits are set to logic 0, the respective SaX[1:4] register bit is disabled and will not be written into the G.704 CRC multiframe (i.e. the SaX bit that has been disabled will pass through transparently). The SaX_EN bits are valid only when the INDIS bit in the E1-TRAN Configuration register is set to logic 0.

### Register 090H: E1 FRMR Frame Alignment Options

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | CRCEN | 1 |
| Bit 6 | R/W | CASDIS | 0 |
| Bit 5 | R/W | C2NCIWCK | 0 |
| Bit 4 | | Unused | X |
| Bit 3 | R/W | Reserved | 0 |
| Bit 2 | R/W | REFR | 0 |
| Bit 1 | R/W | REFCRCEN | 1 |
| Bit 0 | R/W | REFRDIS | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

This register selects the various framing formats and framing algorithms supported by the FRMR block.

CRCEN:

The CRCEN bit enables the FRMR to frame to the CRC multiframe. When the CRCEN bit is logic 1, the FRMR searches for CRC multiframe alignment and monitors for errors in the alignment. A logic 0 in the CRCEN bit position disables searching for multiframe and suppresses the OOCMF, CRCE, CMFER, FEBE, CFEBE, RAICCRC, C2NCIW and ICMFPI FRMR status/interrupt bits, forcing them to logic 0.

CASDIS:

The CASDIS bit enables the FRMR to frame to the Channel Associated Signaling multiframe when set to a logic 0. When CAS is enabled, the FRMR searches for signaling multiframe alignment and monitors for errors in the alignment. A logic 1 in the CASDIS bit position disables searching for multiframe and suppresses the OOSMF and the SMFER FRMR outputs, forcing them to logic 0.

C2NCIWCK:

The C2NCIWCK bit enables the continuous checking for CRC multiframe in the CRC to non-CRC interworking mode of the E1 FRMR. If this bit is a logic 0, the E1-FRMR will cease searching for CRC multiframe alignment in CRC to non-CRC interworking mode. If this bit is a logic 1, the E1-FRMR will

continue searching for CRC multiframe alignment, even if CRC to non-CRC interworking has been declared.

Reserved:

The Reserved bit must be programmed to logic 0 for normal operation.

REFR:

A transition from logic 0 to logic 1 in the REFR bit position forces the re-synchronization to a new frame alignment. The bit must be cleared to logic 0, then set to logic 1 again to generate subsequent re-synchronizations.

REFCRCEN:

The REFCRCEN bit enables excessive CRC errors (≥ 915 errors in one second) to force a re-synchronization to a new frame alignment. Setting the REFCRCEN bit position to logic 1 enables reframe due to excessive CRC errors; setting the REFCRCEN bit to logic 0 disables CRC errors from causing a reframe.

REFRDIS:

The REFRDIS bit disables reframing under any error condition once frame alignment has been found; reframing can be initiated by software via the REFR bit. A logic 1 in the REFRDIS bit position causes the FRMR to remain "locked in frame" once initial frame alignment has been found. A logic 0 allows reframing to occur based on the various error criteria (FER, excessive CRC errors, etc.). Note that while the FRMR remains locked in frame due to REFRDIS=1, a received AIS will not be detected since the FRMR must be out-of-frame to detect AIS.

### Register 091H: E1 FRMR Maintenance Mode Options

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | R/W | BIT2C | 1 |
| Bit 5 | R/W | SMFASC | 0 |
| Bit 4 | R/W | TS16C | 0 |
| Bit 3 | R/W | RAIC | 0 |
| Bit 2 | | Unused | X |
| Bit 1 | R/W | AISC | 0 |
| Bit 0 | R | EXCRCERR | X |

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

BIT2C:

The BIT2C bit enables the additional criterion that loss of frame is declared when bit 2 in time slot 0 of NFAS frames has been received in error on 3 consecutive occasions: a logic 1 in the BIT2C position enables declaration of loss of frame alignment when bit 2 is received in error; a logic 0 in BIT2C enables declaration of loss of frame alignment based on the absence of FAS frames only.

SMFASC:

The SMFASC bit selects the criterion used to declare loss of signaling multiframe alignment signal: a logic 0 in the SMFASC bit position enables declaration of loss of signaling multiframe alignment when 2 consecutive multiframe alignment patterns have been received in error; a logic 1 in the SMFASC bit position enables declaration of loss of signaling multiframe when 2 consecutive multiframe alignment patterns have been received in error or when time slot 16 contains logic 0 in all bit positions for 1 or 2 multiframes based on the criterion selected by TS16C.

TS16C:

The TS16C bit selects the criterion used to declare loss of signaling multiframe alignment signal when enabled by the SMFASC: a logic 0 in the TS16C bit position enables declaration of loss of signaling multiframe alignment when time slot 16 contains logic 0 in all bit positions for 1 multiframe; a logic 1 in the TS16C bit position enables declaration of loss of

signaling multiframe when time slot 16 contains logic 0 in all bit positions for 2 consecutive signaling multiframes.

RAIC:

The RAIC bit selects the criterion used to declare a Remote Alarm Indication (RAI). If RAIC is logic 0, the RAIV indication is asserted upon reception of any A=1 (bit 3 of NFAS frames) and is deasserted upon reception of any A=0. If RAIC is logic 1, the RAIV indication is asserted if A=1 is received on 4 or more consecutive occasions, and is cleared upon reception of any A=0.

AISC :

The AISC bit selects the criterion used for determining AIS alarm indication. If AISC is logic 0, AIS is declared if there is a loss of frame (LOF) indication and a 512-bit period is received with less than 3 zeros. If AISC is a logic 1, AIS is declared if less than 3 zeros are detected in each of 2 consecutive 512-bit periods and is cleared when 3 or more zeros are detected in each of 2 consecutive 512-bit intervals.

EXCRCERR:

The EXCRCERR bit is an active high status bit indicating that excessive CRC evaluation errors (i.e., $\geq$ 915 errors in one second) have occurred, thereby initiating a reframe if enabled by the REFCRCNE bit of the E1 FRMR Frame Alignment Options register. The EXCRCERR bit is reset to logic 0 after the register is read.

### Register 092H: E1 FRMR Framing Status Interrupt Enable

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | C2NCIWE | 0 |
| Bit 6 | R/W | OOFE | 0 |
| Bit 5 | R/W | OOSMFE | 0 |
| Bit 4 | R/W | OOCMFE | 0 |
| Bit 3 | R/W | COFAE | 0 |
| Bit 2 | R/W | FERE | 0 |
| Bit 1 | R/W | SMFERE | 0 |
| Bit 0 | R/W | CMFERE | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

C2NCIWE, OOFE, OOSMFE and OOCMFE:

A logic one in bits C2NCIWE, OOFE, OOSMFE and OOCMFE enables the generation of an interrupt on a change of state of C2NCIWV, OOFV, OOSMFV and OOCMFV bits respectively of the E1 FRMR Framing Status register.

COFAE:

A logic one in the COFAE bit enables the generation of an interrupt when the position of the frame alignment has changed.

FERE:

A logic one in the FERE bit enables the generation of an interrupt when an error has been detected in the frame alignment signal.

SMFERE:

A logic one in the SMFERE bit enables the generation of an interrupt when an error has been detected in the signaling multiframe alignment signal.

CMFERE:

A logic one in the CMFERE bit enables the generation of an interrupt when an error has been detected in the CRC multiframe alignment signal.

### Register 093H: E1 FRMR Maintenance/Alarm Status Interrupt Enable

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | RAIE | 0 |
| Bit 6 | R/W | RMAIE | 0 |
| Bit 5 | R/W | AISDE | 0 |
| Bit 4 | R/W | Reserved | 0 |
| Bit 3 | R/W | REDE | 0 |
| Bit 2 | R/W | AISE | 0 |
| Bit 1 | R/W | FEBEE | 0 |
| Bit 0 | R/W | CRCEE | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

RAIE, RMAIE, AISDE, REDE and AISE:

A logic one in bits RAIE, RMAIE, AISDE, REDE or AISE enables the generation of an interrupt on a change of state of the RAIV, RMAIV, AISD, RED and AIS bits respectively of the E1 FRMR Maintenance/Alarm Status register.

Reserved:

This bit must be set to a logic 0 for correct operation.

FEBEE:

When the FEBEE bit is a logic one, an interrupt is generated when a logic zero is received in the Si bits of frames 13 or 15.

CRCEE:

When the CRCEE bit is a logic one, an interrupt is generated when calculated CRC differs from the received CRC remainder.

### Register 094H: E1 FRMR Framing Status Interrupt Indication

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | C2NCIWI | X |
| Bit 6 | R | OOFI | X |
| Bit 5 | R | OOSMFI | X |
| Bit 4 | R | OOCMFI | X |
| Bit 3 | R | COFAI | X |
| Bit 2 | R | FERI | X |
| Bit 1 | R | SMFERI | X |
| Bit 0 | R | CMFERI | X |

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

A logic 1 in any bit position of this register indicates which framing status generated an interrupt by changing state.

C2NCIWI, OOFI, OOSMFI, OOCMFI, and COFAI:

C2NCIWI, OOFI, OOSMFI, OOCMFI, and COFAI indicate when the corresponding status has changed state from logic 0 to logic 1 or vice-versa.

FERI, SMFERI, CMFERI:

FERI, SMFERI, CMFERI indicate when a framing error, signaling multiframe error or CRC multiframe error event has been detected; these bits will be set if one or more errors have occurred since the last register read.

The interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the state of the framer. The contents of this register are cleared to logic 0 after the register is read; the interrupt is also cleared if it was generated by any of the Framing Status outputs.

### Register 095H: E1 FRMR Maintenance/Alarm Status Interrupt Indication

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | RAII | X |
| Bit 6 | R | RMAII | X |
| Bit 5 | R | AISDI | X |
| Bit 4 | | Unused | X |
| Bit 3 | R | REDI | X |
| Bit 2 | R | AISI | X |
| Bit 1 | R | FEBEI | X |
| Bit 0 | R | CRCEI | X |

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

A logic 1 in any bit position of this register indicates which maintenance or alarm status generated an interrupt by changing state.

RAII, RMAII, AISDI, REDI, and AISI:

RAII, RMAII, AISDI, REDI, and AISI indicate when the corresponding FRMR Maintenance/Alarm Status register bit has changed state from logic 0 to logic 1 or vice-versa.

FEBEI:

The FEBEI bit becomes a logic one when a logic zero is received in the Si bits of frames 13 or 15.

CRCEI:

The CRCEI bit becomes a logic one when a calculated CRC differs from the received CRC remainder.

The bits in this register are set by a single error event.

The interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the state of the framer. The contents of this register are cleared to logic 0 after the register is read; the interrupt is also cleared if it was generated by one of the Maintenance/Alarm Status events.

### Register 096H: E1 FRMR Framing Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | C2NCIWV | X |
| Bit 6 | R | OOFV | X |
| Bit 5 | R | OOSMFV | X |
| Bit 4 | R | OOCMFV | X |
| Bit 3 | R | OOOFV | X |
| Bit 2 | R | RAICCRCV | X |
| Bit 1 | R | CFEBEV | X |
| Bit 0 | R | V52LINKV | X |

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

Reading this register returns the current state value of the C2NCIW, OOF, OOSMF, OOCMF, OOOF and RAICCRC FRMR framing statuses.

C2NCIWV:

The C2NCIWV bit is set to logic one while the FRMR is operating in CRC to non-CRC interworking mode. The C2NCIWV bit goes to a logic zero once when the FRMR exits CRC to non-CRC interworking mode.

OOFV:

The OOFV bit is a logic one when basic frame alignment has been lost. The OOFV bit goes to a logic zero once frame alignment has been regained.

OOSMFV:

The OOSMFV bit is a logic one when the signaling multiframe alignment has been lost. The OOSMFV bit becomes a logic zero once signaling multiframe has been regained.

OOCMFV:

The OOCMFV bit is a logic one when the CRC multiframe alignment has been lost. The OOCMFV bit becomes a logic zero once CRC multiframe has been regained.

OOOFV:

This bit indicates the current state of the out of offline frame (OOOF) indicator. OOOFV is asserted when the offline framer in the CRC multiframe find procedure is searching for frame alignment.

RAICCRCV:

This bit indicates the current state of the RAI and continuous CRC (RAICCRC) indicator. RAICCRCV is asserted when the remote alarm (A bit) is set high and the CRC error (E bit) is set low for a period of 10 ms.

CFEBEV:

This bit indicates the current state of the continuous FEBE (CFEBE) indicator. CFEBEV is asserted when the CRC error (E bit) is set high on more than 990 occasions in each second (out of 1000 possible occasions) for the last 5 consecutive seconds.

V52LINKV:

This bit indicates the current state of the V5.2 link (V52LINK) identification signal indicator. V52LINKV is asserted if 2 out of the last 3 received Sa7 bits are a logic 0.

### Register 097H: E1 FRMR Maintenance/Alarm Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | RAIV | X |
| Bit 6 | R | RMAIV | X |
| Bit 5 | R | AISD | X |
| Bit 4 | | Unused | X |
| Bit 3 | R | RED | X |
| Bit 2 | R | AIS | X |
| Bit 1 | | Unused | X |
| Bit 0 | | Unused | X |

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

Reading this register returns the current state value of the RAI, RMAI, AISD, RED, and AIS maintenance/alarm statuses.

RAIV:

The RAIV bit indicates the remote alarm indication (RAI) value. The RAIV bit is set to logic one when the "A" bit (bit 3 in time slot 0 of the non-frame alignment signal frame) has been logic one for an interval specified by the RAIC bit in the E1 FRMR Maintenance Mode Options register. When RACI is logic 1, RAIV is set when A=1 for 4 or more consecutive intervals, and is cleared upon reception of any A=0. When RACI is logic 0, RAI is set upon reception of any A=1, and is cleared upon reception of any A=0. The RAIV output is updated every two frames.

RMAIV:

The RMAIV bit indicates the remote multiframe alarm indication (RMAI) value. The RMAIV bit is set to logic one when the "Y" bit (bit 6 in time slot 16 in frame 0 of the signaling multiframes) has been a logic one for 3 consecutive signaling multiframes, and is cleared upon reception of any Y=0. The RMAIV bit is updated every 16 frames.

AISD:

The AISD bit indicates the alarm indication signal (AIS) detect value. The AISD bit is set to logic one when the incoming data stream has a low zero-bit density for an interval specified by the AISC bit in the E1 FRMR Maintenance

Mode Options register. When AISC is logic 0, AISD is asserted when 512-bit periods have been received with 2 or fewer zeros. The indication is cleared when a 512-bit period is received with 3 or more zeros. When AISC is logic 1, AISD is asserted when two consecutive 512 bit periods have been received with 2 or fewer zeros. The indication is cleared when 2 consecutive 512-bit periods are received, with each period containing 3 or more zeros. The AISD bit is updated once every 512-bit period.

RED:

The RED bit is a logic one if an out of frame condition has persisted for 100 ms. The RED bit returns to a logic zero when a out of frame condition has been absent for 100 ms.

AIS:

The AIS bit is a logic one when an out of frame all-ones condition has persisted for 100 ms. The AIS bit returns to a logic zero when the AIS condition has been absent for 100 ms.

### Register 098H: E1 FRMR Timeslot 0 International/National Bits

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | Si[1] | X |
| Bit 6 | R | Si[0] | X |
| Bit 5 | R | A | X |
| Bit 4 | R | Sa[4] | X |
| Bit 3 | R | Sa[5] | X |
| Bit 2 | R | Sa[6] | X |
| Bit 1 | R | Sa[7] | X |
| Bit 0 | R | Sa[8] | X |

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

This register returns the International and National bits from TS0 of incoming frames. The Si[1:0], A and Sa[4:8] bits map to TS0 frames as shown in Table 62.

**Table 62 - Timeslot 0 Bit Position Allocation**

| Frame | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| FAS | Si[1] | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| NFAS | Si[0] | 1 | A | Sa[4] | Sa[5] | Sa[6] | Sa[7] | Sa[8] |

Si [1]:

Reading the Si[1] bit returns the International bit in the last received FAS frame. This bit is updated upon generation of the IFPI interrupt on FAS frames.

Si[0]:

Reading the Si[0] bit returns the International bit in the last received NFAS frame. This bit is updated upon generation of the IFPI interrupt on NFAS frames.

A:

Reading the A bit position returns the Remote Alarm Indication (RAI) bit in the last received NFAS frame. This bit is updated upon generation of the IFPI interrupt on NFAS frames.

Sa[4:8]:

Reading these bits returns the National bit values in the last received NFAS frame. This bit is updated upon generation of the IFPI interrupt on NFAS frames.

### Register 099H: E1 FRMR CRC Error Counter - LSB

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | CRCERR[7] | X |
| Bit 6 | R | CRCERR[6] | X |
| Bit 5 | R | CRCERR [5] | X |
| Bit 4 | R | CRCERR [4] | X |
| Bit 3 | R | CRCERR [3] | X |
| Bit 2 | R | CRCERR [2] | X |
| Bit 1 | R | CRCERR [1] | X |
| Bit 0 | R | CRCERR [0] | X |

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

CRCERR[7:0]:

The CRCERR[7:0] register bits contain the least significant byte of the 10-bit CRC error counter value, which is updated every second.

### Register 09AH: E1 FRMR CRC Error Counter – MSB/Timeslot 16 Extra Bits

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | OVR | 0 |
| Bit 6 | R | NEWDATA | 0 |
| Bit 5 | R | X[3] | X |
| Bit 4 | R | Y | X |
| Bit 3 | R | X[1] | X |
| Bit 2 | R | X[0] | X |
| Bit 1 | R | CRCERR [9] | X |
| Bit 0 | R | CRCERR [8] | X |

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

This register contains the most significant two bits of the 10-bit CRC error counter value, updated every second.

NEWDATA:

The NEWDATA flag bit indicates that the CRCERR counter register contents have been updated with a new count value accumulated over the last 1 second interval. It is set to logic 1 when the CRC error counter data is transferred into the counter registers, and is reset to logic 0 when this register is read. This bit can be polled to determine the 1 second timing boundary used by the FRMR.

OVR:

The OVR flag bit indicates that the CRCERR counter register contents have not been read within the last 1 second interval, and therefore have been over-written. It is set to logic 1 if CRC error counter data is transferred into the counter registers before the previous data has been read out, and is reset to logic 0 when this register is read.

X[3], Y, X[1], X[0]:

Reading these bits returns the value of the Extra bits (X[3] and X1:0]) and the Remote Signaling Multiframe Alarm bit (Y) in Frame 0, Timeslot 16 of the last received signaling multiframe. These bits are updated upon generation of the IFPI interrupt on NFAS frames. They map to timeslot 16 as shown in Table

63. Note that the contents of this register are not updated while the E1-FRMR is out of frame.

**Table 63 - Signaling Multiframe Timeslot 16, Frame 0 Bit Positions**

| Bit | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | X[3] | Y | X[1] | X[0] |

CRCERR[9:8]:

The CRCERR[9:8] register bits contain the two most significant bits of the 10-bit CRC error counter value, which is updated every second.

This CRC error count is distinct from that of PMON because it is guaranteed to be an accurate count of the number of CRC errors in one second; whereas, PMON relies on externally initiated transfers which may not be one second apart.

### Register 09BH: E1 FRMR National Bit Codeword Interrupt Enables

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | SaSEL[2] | 0 |
| Bit 6 | R/W | SaSEL[1] | 0 |
| Bit 5 | R/W | SaSEL[0] | 0 |
| Bit 4 | R/W | Sa4E | 0 |
| Bit 3 | R/W | Sa5E | 0 |
| Bit 2 | R/W | Sa6E | 0 |
| Bit 1 | R/W | Sa7E | 0 |
| Bit 0 | R/W | Sa8E | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

SaSEL[2:0]:

The SaSEL[2:0] bits selects which National Bit Codeword appears in the SaX[1:4] bits of the National Bit Codeword register. These bits map to the codeword selection as shown in Table 64:

**Table 64 - E1 FRMR Codeword Select**

| SaSEL[2:0] | National Bit Codeword |
|---|---|
| 001 | Undefined |
| 010 | Undefined |
| 011 | Undefined |
| 100 | Sa4 |
| 101 | Sa5 |
| 110 | Sa6 |
| 111 | Sa7 |
| 000 | Sa8 |

Sa4E, Sa5E, Sa6E, Sa7E, Sa8E:

The National Use interrupt enables allow changes in Sa code word values to generate an interrupt. If SaXE is a logic 1, a logic 1 in the corresponding SaXI bit of the E1 FRMR National Bit Codeword Interrupts register will result in the assertion low of the INTB output.

The interrupt enable should be logic 0 for any bit receiving a HDLC datalink.

### Register 09CH: E1 FRMR National Bit Codeword Interrupts

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R | Sa4I | X |
| Bit 3 | R | Sa5I | X |
| Bit 2 | R | Sa6I | X |
| Bit 1 | R | Sa7I | X |
| Bit 0 | R | Sa8I | X |

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

Sa4I, Sa5I, Sa6I, Sa7I, Sa8I:

The National Use interrupt status bits indicate if the debounced version of the individual bits has changed since the last time this register has been read. A logic 1 in one of the bit positions indicates a new nibble codeword is available in the associated SaX[1:4] bits in the National Bit Codeword registers, where N is 4 through 8. If the associated SaXE bit in the E1 FRMR National Bit Interrupt Enables register is a logic 1, a logic 1 in the SaXI results in the assertion of the INTB output.

### Register 09DH: E1 FRMR National Bit Codeword

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | R | SaX[1] | X |
| Bit 2 | R | SaX[2] | X |
| Bit 1 | R | SaX[3] | X |
| Bit 0 | R | SaX[4] | X |

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

SaX[1:4]:

Reading these bits returns the SaX nibble code word extracted from the submultiframe, where 'X' corresponds to the National bit selected by the SaSEL[2:0] bits in the E1 FRMR National Bit Codeword Interrupt Enables register. SaX[1] is from the first SaX bit of the submultiframe; SaX[4] is from the last. A change in the codeword values sets the SaI[X] bit of the E1 FRMR National Bits Codeword Interrupts register.

### Register 09EH: E1 FRMR Frame Pulse/Alarm/V5.2 Link ID Interrupt Enables

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | OOOFE | 0 |
| Bit 6 | R/W | RAICCRCE | 0 |
| Bit 5 | R/W | CFEBEE | 0 |
| Bit 4 | R/W | V52LINKE | 0 |
| Bit 3 | R/W | IFPE | 0 |
| Bit 2 | R/W | ICSMFPE | 0 |
| Bit 1 | R/W | ICMFPE | 0 |
| Bit 0 | R/W | ISMFPE | 0 |

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

OOOFE:

A logic one in the OOOFE bit enables the generation of an interrupt when the out of offline frame interrupt (OOOFI) is asserted.

RAICCRCE:

A logic one in the RAICCRCE bit enables the generation of an interrupt when a RAI and Continuous CRC condition has been detected in the incoming data stream.

CFEBEE:

A logic one in the CFEBEE bit enables the generation of an interrupt when continuous FEBEs have been detected in the incoming data stream.

V52LINKE:

A logic one in the V52LINKE bit enables the generation of an interrupt when a V5.2 link identification has been detected in the Sa7 bits.

IFPE:

The input frame pulse interrupt enable bit allows interrupts to be generated on each basic frame pulse. If IFPE is a logic 1, a logic 1 in the IFPI bit of the Frame Pulse Interrupts register will result in the assertion low of the INTB output.

ICSMFPE:

The input frame pulse interrupt enable bit allows interrupts to be generated on each CRC submultiframe pulse. If ICSMFPE is a logic 1, a logic 1 in the ICSMFPI bit of the Frame Pulse Interrupts register will result in the assertion low of the INTB output.

ICMFPE:

The input frame pulse interrupt enable bit allows interrupts to be generated on each CRC multiframe pulse. If ISMFPE is a logic 1, a logic 1 in the ISMFPI bit of the Frame Pulse Interrupts register will result in the assertion low of the INTB output.

ISMFPE:

The input frame pulse interrupt enable bit allows interrupts to be generated on each signalling multiframe pulse. If ISMFPE is a logic 1, a logic 1 in the ISMFPI bit of the Frame Pulse Interrupts register will result in the assertion low of the INTB output.

### Register 09FH: E1 FRMR Frame Pulse/Alarm Interrupts

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | OOOFI | X |
| Bit 6 | R | RAICCRCI | X |
| Bit 5 | R | CFEBEI | X |
| Bit 4 | R | V52LINKI | X |
| Bit 3 | R | IFPI | X |
| Bit 2 | R | ICSMFPI | X |
| Bit 1 | R | ICMFPI | X |
| Bit 0 | R | ISMFPI | X |

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

OOOFI:

The OOOFI bit indicates when the out of offline frame indicator (OOOFV) changes state.

RAICCRCI:

The RAICCRCI bit indicates when a RAI and Continuous CRC condition has been detected in the incoming data stream. This interrupt is triggered when the remote alarm (A bit) is set high and the CRC error (E bit) is set low for a period of 10 ms.

CFEBEI:

The CFEBEI bit indicates when continuous FEBEs have been detected in the incoming data stream. This interrupt is triggered when the CRC error (E bit) is set high on more than 990 occasions in each second (out of 1000 possible occasions) for 5 consecutive seconds.

V52LINKI:

V52LINKI indicates when a V5.2 link identification signal has been detected or lost in the Sa7 bits. This bit will toggle any time the V52LINKV bit changes state.

IFPI:

The input frame pulse interrupt status bit is asserted at timeslot 1, bit position 1 of the frame in the incoming data stream.

ICSMFPI:

The input CRC submultiframe alignment frame pulse interrupt status bit is asserted at timeslot 1, bit position 1 of frame 0 of the CRC submultiframe in the incoming data stream.

ICMFPI:

The input CRC multiframe alignment frame pulse interrupt status bit is asserted at timeslot 1, bit position 1 of frame 0 of the CRC multiframe in the incoming data stream.

ISMFPI:

The input signaling multiframe alignment frame pulse interrupt status bit is asserted at timeslot 17, bit position 1 of frame 0 of the signaling multiframe in the incoming data stream.

### Register 0A8H (#1), 0B0H (#2), 0B8H (#3): TDPR Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | FLGSHARE | 1 |
| Bit 6 | R/W | FIFOCLR | 0 |
| Bit 5 | R/W | PREN | 0 |
| Bit 4 | | Unused | X |
| Bit 3 | R/W | EOM | 0 |
| Bit 2 | R/W | ABT | 0 |
| Bit 1 | R/W | CRC | 1 |
| Bit 0 | R/W | EN | 0 |

EN:

The EN bit enables the TDPR functions. When EN is set to logic 1, the TDPR is enabled and flag sequences are sent until data is written into the TDPR Transmit Data register. When the EN bit is set to logic 0, the TDPR is disabled and overwrites the incoming backplane data with an all 1's pattern.

CRC:

The CRC enable bit controls the generation of the CCITT_CRC frame check sequence (FCS). Setting the CRC bit to logic 1 enables the CCITT-CRC generator and appends the 16-bit FCS to the end of each message. When the CRC bit is set to logic 0, the FCS is not appended to the end of the message. The CRC type used is the CCITT-CRC with generator polynomial $x^{16} + x^{12} + x^5 + 1$. The high order bit of the FCS word is transmitted first. . CRC FCS is also appended to the performance report data transmitted from the T1-APRM if CRC is set to logic 1.

ABT:

The Abort (ABT) bit controls the sending of the 7 consecutive ones HDLC abort code. Setting the ABT bit to a logic 1 causes the 11111110 code (the 0 is transmitted first) to be transmitted after the last byte from the TDPR FIFO is transmitted. The FIFO is then reset. All data in the FIFO will be lost. Aborts are continuously sent and the FIFO is held in reset until this bit is reset to a logic 0. At least one Abort sequence will be sent when the ABT bit transitions from logic 0 to logic 1. Note that T1-APRM performance report insertion takes precedence over the ABT register bit. When a performance report frame is available, the TDPR will transmit 2 flag sequences before, and 1 or 2 flag

sequences (depending on the FLGSHARE bit setting) after the performance report frame. If the ABT bit is still set, the TDPR will then transmit the Abort sequence again.

EOM:

The EOM bit indicates that the last byte of data written in the Transmit Data register is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated. The EOM bit is cleared upon a write to the TDPR Transmit Data register.

PREN:

The PREN bit enables performance reports from the T1-APRM to be transmitted. When PREN is a logic 1, the message arbitrator circuit will insert the T1-APRM performance report as soon as it is finished any packet whose transmission is already in progress and the delimiting flags. When PREN is a logic 0, the message arbitrator circuit will ignore requests from the T1-APRM.

This bit has no effect for TDPR #2 and TDPR #3.

FIFOCLR:

The FIFOCLR bit resets the TDPR FIFO. When set to logic 1, FIFOCLR will cause the TDPR FIFO to be cleared. There is a maximum delay of one T1 or E1 clock cycle between the setting of this register bit and the execution of the FIFO clear operation.

FLGSHARE:

The FLGSHARE bit configures the TDPR to share the opening and closing flags between successive frames. If FLGSHARE is logic 1, the opening and closing flags between successive frames are shared. If FLGSHARE is logic 0, separate closing and opening flags are inserted between successive frames.

### Register 0A9H (#1), 0B1H (#2), 0B9H (#3): TDPR Upper Transmit Threshold

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | R/W | UTHR[6] | 1 |
| Bit 5 | R/W | UTHR[5] | 0 |
| Bit 4 | R/W | UTHR[4] | 0 |
| Bit 3 | R/W | UTHR[3] | 0 |
| Bit 2 | R/W | UTHR[2] | 0 |
| Bit 1 | R/W | UTHR[1] | 0 |
| Bit 0 | R/W | UTHR[0] | 0 |

UTHR[6:0]:

The UTHR[6:0] bits define the TDPR FIFO fill level which will automatically cause the bytes stored in the TDPR FIFO to be transmitted. Once the fill level exceeds the UTHR[6:0] value, transmission will begin. Transmission will not stop until the last complete packet is transmitted and the TDPR FIFO fill level is below UTHR[6:0] + 1.

The value of UTHR[6:0] must always be greater than the value of LINT[6:0] unless both values are equal to 00H.

### Register 0AAH (#1), 0B2H (#2), 0BAH (#3): TDPR Lower Interrupt Threshold

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | R/W | LINT[6] | 0 |
| Bit 5 | R/W | LINT[5] | 0 |
| Bit 4 | R/W | LINT[4] | 0 |
| Bit 3 | R/W | LINT[3] | 0 |
| Bit 2 | R/W | LINT[2] | 1 |
| Bit 1 | R/W | LINT[1] | 1 |
| Bit 0 | R/W | LINT[0] | 1 |

LINT[6:0]:

The LINT[6:0] bits define the TDPR FIFO fill level which causes an internal interrupt (LFILLI) to be generated. Once the TDPR FIFO level decrements to empty or to a value less than LINT[6:0], LFILLI and BLFILL will be set to logic 1. LFILLI will cause an interrupt on INTB if LFILLE is set to logic 1.

The value of LINT[6:0] must always be less than the value of UTHR[6:0] unless both values are equal to 00H.

### Register 0ABH (#1), 0B3H (#2), 0BBH (#3): TDPR Interrupt Enable

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R/W | PRINTE | 0 |
| Bit 3 | R/W | FULLE | 0 |
| Bit 2 | R/W | OVRE | 0 |
| Bit 1 | R/W | UDRE | 0 |
| Bit 0 | R/W | LFILLE | 0 |

LFILLE:

If LFILLE is a logic 1, a transition to logic 1 on LFILLI will generate an interrupt on INTB.

UDRE:

If UDRE is a logic 1, a transition to logic 1 on UDRI will generate an interrupt on INTB.

OVRE:

If OVRE is a logic 1, a transition to logic 1 on OVRI will generate an interrupt on INTB.

FULLE:

If FULLE is a logic 1, a transition to logic 1 on FULLI will generate an interrupt on INTB.

PRINTE:

If PRINTE is a logic 1, a transition to logic 1 on PRINTI will generate an interrupt on INTB.

### Register 0ACH (#1), 0B4H (#2), 0BCH (#3): TDPR Interrupt Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | R | FULL | X |
| Bit 5 | R | BLFILL | X |
| Bit 4 | R | PRINTI | X |
| Bit 3 | R | FULLI | X |
| Bit 2 | R | OVRI | X |
| Bit 1 | R | UDRI | X |
| Bit 0 | R | LFILLI | X |

Writing to this register will clear the underrun condition if it has occurred.

Consecutive writes to the TDPR Configuration and TDPR Transmit Data register and reads of the TDPR Interrupt Status register should not occur at rates greater than that of TCLKO.

LFILLI:

The LFILLI bit will transition to logic 1 when the TDPR FIFO level transitions to empty or falls below the value of LINT[6:0] programmed in the TDPR Lower Interrupt Threshold register. LFILLI will assert INTB if it is a logic 1 and LFILLE is programmed to logic 1. LFILLI is cleared when this register is read.

UDRI:

The UDRI bit will transition to 1 when the TDPR FIFO underruns. That is, the TDPR was in the process of transmitting a packet when it ran out of data to transmit. UDRI will assert INTB if it is a logic 1 and UDRE is programmed to logic 1. UDRI is cleared when this register is read.

OVRI:

The OVRI bit will transition to 1 when the TDPR FIFO overruns. That is, the TDPR FIFO was already full when another data byte was written to the TDPR Transmit Data register. OVRI will assert INTB if it is a logic 1 and OVRE is programmed to logic 1. OVRI is cleared when this register is read.

FULLI:

The FULLI bit will transition to logic 1 when the TDPR FIFO is full. FULLI will assert INTB if it is a logic 1 and FULLE is programmed to logic 1. FULLI is cleared when this register is read.

PRINTI:

The PRINTI bit will transition to logic 1 when a performance report is ready to be transmitted from the T1-APRM. PRINTI will assert INTB if it is a logic 1 and PRINTE is programmed to logic 1. PRINTI is cleared when this register is read.

BLFILL:

The BLFILL bit is set to logic 1 if the current FIFO fill level is below the LINT[7:0] level or is empty.

FULL:

The FULL bit reflects the current condition of the TDPR FIFO. If FULL is a logic 1, the TDPR FIFO already contains 128-bytes of data and can accept no more.

### Register 0ADH (#1), 0B5H (#2), 0BDH (#3): TDPR Transmit Data

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | TD[7] | X |
| Bit 6 | R/W | TD[6] | X |
| Bit 5 | R/W | TD[5] | X |
| Bit 4 | R/W | TD[4] | X |
| Bit 3 | R/W | TD[3] | X |
| Bit 2 | R/W | TD[2] | X |
| Bit 1 | R/W | TD[1] | X |
| Bit 0 | R/W | TD[0] | X |

Consecutive writes to the TDPR Configuration and TDPR Transmit Data register and reads of the TDPR Interrupt Status register should not occur at rates greater than that of TCLKO

TD[7:0]:

The TD[7:0] bits contain the data to be transmitted on the data link. Data written to this register is serialized and transmitted (TD[0] is transmitted first).

### Registers 0C0H (#1), 0C8H (#2), 0D0H (#3): RDLC Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R/W | Reserved | 0 |
| Bit 3 | R/W | MEN | 0 |
| Bit 2 | R/W | MM | 0 |
| Bit 1 | R/W | TR | 0 |
| Bit 0 | R/W | EN | 0 |

EN:

The enable (EN) bit controls the overall operation of the RDLC. When EN is set to logic 1, RDLC is enabled; when set to logic 0, RDLC is disabled. When the RDLC is disabled, the FIFO buffer and interrupts are all cleared. When the RDLC is enabled, it will immediately begin looking for flags.

TR:

Setting the terminate reception (TR) bit to logic 1 forces the RDLC to immediately terminate the reception of the current data frame, empty the FIFO buffer, clear the interrupts, and begin searching for a new flag sequence. The RDLC handles a terminate reception event in the same manner as it would the toggling of the EN bit from logic 1 to logic 0 and back to logic 1. Thus, the RDLC state machine will begin searching for flags. An interrupt will be generated when the first flag is detected. The TR bit will reset itself to logic 0 after a rising and falling edge have occurred on the CLK input, once the write strobe (CBI[9]) goes high. If the Configuration Register is read after this time, the TR bit value returned will be logic 0.

MEN:

Setting the Match Enable (MEN) bit to logic 1 enables the detection and storage in the FIFO of only those packets whose first data byte matches either of the bytes written to the Primary or Secondary Match Address Registers, or the universal all ones address. When the MEN bit is logic 0, all packets received are written into the FIFO.

MM:

Setting the Match Mask (MM) bit to logic 1 ignores the PA[1:0] bits of the Primary Address Match Register, the SA[1:0] bits of the Secondary Address Match Register, and the two least significant bits of the universal all ones address when performing the address comparison.

Reserved:

This bit must be set to logic 0 for correct operation.

### Registers 0C1H (#1), 0C9H (#2), 0D1H (#3): RDLC Interrupt Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | INTE | 0 |
| Bit 6 | R/W | INTC[6] | 0 |
| Bit 5 | R/W | INTC[5] | 0 |
| Bit 4 | R/W | INTC[4] | 0 |
| Bit 3 | R/W | INTC[3] | 0 |
| Bit 2 | R/W | INTC[2] | 0 |
| Bit 1 | R/W | INTC[1] | 0 |
| Bit 0 | R/W | INTC[0] | 0 |

The contents of the Interrupt Control Register should only be changed when the EN bit in the Configuration Register is logic 0. This prevents any erroneous interrupt generation.

INTC[6:0]:

These bits control the assertion of FIFO fill level set point interrupts. A value of 0 in INTC[6:0] is interpreted as decimal 128.

INTE:

The Interrupt Enable bit (INTE) must be set to logic 1 to allow the internal interrupt status to be propagated to the INTB output.

### Registers 0C2H (#1), 0CAH (#2), 0D2H (#3): RDLC Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | FE | X |
| Bit 6 | R | OVR | X |
| Bit 5 | R | COLS | X |
| Bit 4 | R | PKIN | X |
| Bit 3 | R | PBS[2] | X |
| Bit 2 | R | PBS[1] | X |
| Bit 1 | R | PBS[0] | X |
| Bit 0 | R | INTR | X |

INTR:

The interrupt (INTR) bit is logic 1 if the RDLC has an active interrupt status. An RDLC interrupt is generated

1) when the number of bytes specified by the INTC[6:0] bits of the RDLC Interrupt Control register have been received on the data link and have been written into the FIFO,
2) immediately upon detection of a FIFO buffer overrun, as indicated by the OVR in this register,
3) immediately upon writing the last byte of a packet into the FIFO,
4) immediately upon writing the last byte of an aborted packet, or
5) immediately upon detection of the transition from receiving all ones to flags, as indicated by a “001” code in PBS[2:0].

If INTR is logic 1, follow the procedure described in section 14.3: Using the Internal HDLC Receivers

PBS[2:0]

The packet byte status (PBS[2:0]) bits indicate the status of the data last read from the FIFO. The bits are encoded as follows:

**Table 65 - Receive Packet Byte Status**

| PBS[2:0] | Significance |
|---|---|
| 000 | Data byte read from the FIFO is not special |

| PBS[2:0] | Significance |
|---|---|
| 001 | The data byte read from the FIFO is the dummy byte that was written into the FIFO when the first HDLC flag sequence (01111110) was detected. This indicates that the data link became active. |
| 010 | The data byte read from the FIFO is the dummy byte that was written into the FIFO when the HDLC abort sequence (01111111) was detected. This indicates that the data link became inactive. |
| 011 | Reserved |
| 100 | The data byte read from the FIFO is the last byte of a normally terminated packet with no CRC error and the packet received had an integer number of bytes. |
| 101 | The data byte read from the FIFO must be discard because there was a non-integer number of bytes in the packet. |
| 110 | The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error. The packet was received in error. |
| 111 | The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error and a non-integer number of bytes. The packet was received in error. |

PKIN:

The Packet In (PKIN) bit is logic 1 when the last byte of a non-aborted packet is written into the FIFO. The PKIN bit is cleared to logic 0 after the Status Register is read.

COLS:

The Change of Link Status (COLS) bit is set to logic 1 if the RDLC has detected the HDLC flag sequence (01111110) or HDLC abort sequence (01111111) in the data. This indicates that there has been a change in the data link status. The COLS bit is cleared to logic 0 by reading this register or by clearing the EN bit in the Configuration Register. For each change in link status, a byte is written into the FIFO. If the COLS bit is found to be logic 1 then the FIFO must be read until empty. The status of the data link is determined by the PBS bits associated with the data read from the FIFO.

OVR:

The overrun (OVR) bit is set to logic 1 when data is written over unread data in the FIFO buffer. This bit is not reset to logic 0 until after the Status

Register is read. While the OVR bit is logic 1, the RDLC and FIFO buffer are held in the reset state, causing the COLS and PKIN bits to be reset to logic 0.

FE:

The FIFO buffer empty (FE) bit is set to logic 1 when the last FIFO buffer entry is read. The FE bit goes to logic 0 when the FIFO is loaded with new data.

### Registers 0C3H (#1), 0CBH (#2), 0D3H (#3): RDLC Data

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | RD[7] | X |
| Bit 6 | R | RD[6] | X |
| Bit 5 | R | RD[5] | X |
| Bit 4 | R | RD[4] | X |
| Bit 3 | R | RD[3] | X |
| Bit 2 | R | RD[2] | X |
| Bit 1 | R | RD[1] | X |
| Bit 0 | R | RD[0] | X |

RD[0] corresponds to the first bit of the serial byte received on the DATA input.

This register is actually a 128-byte FIFO buffer. If data is available, the FE bit in the FIFO Input Status Register is logic 0.

When an overrun is detected, an interrupt is generated and the FIFO buffer is held cleared until the FIFO Input Status Register is read.

### Registers 0C4H (#1), 0CCH (#2), 0D4H (#3): RDLC Primary Address Match

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | PA[7] | 1 |
| Bit 6 | R/W | PA[6] | 1 |
| Bit 5 | R/W | PA[5] | 1 |
| Bit 4 | R/W | PA[4] | 1 |
| Bit 3 | R/W | PA[3] | 1 |
| Bit 2 | R/W | PA[2] | 1 |
| Bit 1 | R/W | PA[1] | 1 |
| Bit 0 | R/W | PA[0] | 1 |

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. PA[0] corresponds to the first bit of the serial byte received on the DATA input. The MM bit in the Configuration Register is used mask off PA[1:0] during the address comparison.

### Registers 0C5H (#1), 0CDH (#2), 0D5H (#3): RDLC Secondary Address Match

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | SA[7] | 1 |
| Bit 6 | R/W | SA[6] | 1 |
| Bit 5 | R/W | SA[5] | 1 |
| Bit 4 | R/W | SA[4] | 1 |
| Bit 3 | R/W | SA[3] | 1 |
| Bit 2 | R/W | SA[2] | 1 |
| Bit 1 | R/W | SA[1] | 1 |
| Bit 0 | R/W | SA[0] | 1 |

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. SA[0] corresponds to the first bit of the serial byte received on the DATA input. The MM bit in the Configuration Register is used mask off SA[1:0] during the address comparison.

### Register 0D6H: CSU Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | CSU_RESET | 0 |
| Bit 6 | R/W | IDDQ_EN | 0 |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | R | CSU_LOCK | X |
| Bit 2 | R/W | MODE[2] | 0 |
| Bit 1 | R/W | MODE[1] | 0 |
| Bit 0 | R/W | MODE[0] | 0 |

MODE[2:0]:

The MODE[2:0] selects the mode of the CSU. Table 66 indicates the required XCLK frequency, and output frequencies for each mode.

Table 66 - Clock Synthesis Mode

| MODE[2:0] | XCLK frequency | TCLKO frequency |
|---|---|---|
| 000 | 2.048 MHz | 2.048 MHz |
| 001 | 1.544 MHz | 1.544 MHz |
| 01X | Reserved | Reserved |
| 10X | Reserved | Reserved |
| 110 | Reserved | Reserved |
| 111 | 2.048 MHz | 1.544 MHz |

CSU_LOCK:

The CSU_LOCK bit may indicate whether or not the embedded clock synthesis unit (CSU) has achieved phase and frequency lock to XCLK. CSU_LOCK is a logic 1 if the divided down synthesized clock frequency is within 244 ppm of the XCLK frequency. A persistent logic 0 in this bit position may indicate a mismatch between the actual and expected XCLK frequency or a problem with the analog supplies (TAVS4 and TAVD4).

IDDQ_EN:

The IDDQ enable bit (IDDQ_EN) is used to configure the embedded CSU for IDDQ tests. When IDDQ_EN is a logic 1, or the IDDQEN bit in the Master Test register (00BH) is a logic 1, the digital outputs of the CSU are pulled to ground. When either the IDDQ_EN bit or IDDQEN bit is set to logic 1, the HIGHZ bit in the XLPG Line Driver Configuration register must also be set to logic 1.

CSU_RESET:

Setting the CSU_RESET bit to logic 1 causes the embedded CSU to be forced to a frequency much lower than normal operation.

### Register 0D8H: RLPS Equalization Indirect Data

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | EQ_DATA[31] | 0 |
| Bit 6 | R/W | EQ_DATA[30] | 0 |
| Bit 5 | R/W | EQ_DATA[29] | 0 |
| Bit 4 | R/W | EQ_DATA[28] | 0 |
| Bit 3 | R/W | EQ_DATA[27] | 0 |
| Bit 2 | R/W | EQ_DATA[26] | 0 |
| Bit 1 | R/W | EQ_DATA[25] | 0 |
| Bit 0 | R/W | EQ_DATA[24] | 0 |

When the RUNI bit of the Receive Line Interface Configuration register is a logic 1, this register is held reset.

EQ_DATA[31:24]:

This register consists of 2-parts: read-only and write-only. Writing this register affects the most significant byte of the input-data to the equalization RAM. Reading it returns the MSB of the RAM location indexed by register 0FCH.

### Register 0D9H: RLPS Equalization Indirect Data

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | EQ_DATA[23] | 0 |
| Bit 6 | R/W | EQ_DATA[22] | 0 |
| Bit 5 | R/W | EQ_DATA[21] | 0 |
| Bit 4 | R/W | EQ_DATA[20] | 0 |
| Bit 3 | R/W | EQ_DATA[19] | 0 |
| Bit 2 | R/W | EQ_DATA[18] | 0 |
| Bit 1 | R/W | EQ_DATA[17] | 0 |
| Bit 0 | R/W | EQ_DATA[16] | 0 |

When the RUNI bit of the Receive Line Interface Configuration register is a logic 1, this register is held reset.

EQ_DATA[23:16]:

This register consists of 2-parts: read-only and write-only. Writing this register affects the second most significant byte of the input-data to the equalization RAM. Reading it returns the second MSB of the RAM location indexed by register 0FCH.

### Register 0DAH: RLPS Equalization Indirect Data

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | EQ_DATA[15] | 0 |
| Bit 6 | R/W | EQ_DATA[14] | 0 |
| Bit 5 | R/W | EQ_DATA[13] | 0 |
| Bit 4 | R/W | EQ_DATA[12] | 0 |
| Bit 3 | R/W | EQ_DATA[11] | 0 |
| Bit 2 | R/W | EQ_DATA[10] | 0 |
| Bit 1 | R/W | EQ_DATA[9] | 0 |
| Bit 0 | R/W | EQ_DATA[8] | 0 |

When the RUNI bit of the Receive Line Interface Configuration register is a logic 1, this register is held reset.

EQ_DATA[15:8]:

This register consists of 2-parts: read-only and write-only. Writing this register affects the second least significant byte of the input-data to the equalization RAM. Reading it returns the corresponding bits of the RAM location indexed by register 0FCH.

### Register 0DBH: RLPS Equalization Indirect Data

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | EQ_DATA[7] | 0 |
| Bit 6 | R/W | EQ_DATA[6] | 0 |
| Bit 5 | R/W | EQ_DATA[5] | 0 |
| Bit 4 | R/W | EQ_DATA[4] | 0 |
| Bit 3 | R/W | EQ_DATA[3] | 0 |
| Bit 2 | R/W | EQ_DATA[2] | 0 |
| Bit 1 | R/W | EQ_DATA[1] | 0 |
| Bit 0 | R/W | EQ_DATA[0] | 0 |

When the RUNI bit of the Receive Line Interface Configuration register is a logic 1, this register is held reset.

EQ_DATA[7:0]:

This register consists of 2-parts: read-only and write-only. Writing this register affects the least significant byte of the input-data to the equalization RAM. Reading it returns the LSB of the RAM location indexed by register 0FCH.

### Register 0DCH: RLPS Equalizer Voltage Reference

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | R/W | EQ_VREF[5] | 0 |
| Bit 4 | R/W | EQ_VREF[4] | 0 |
| Bit 3 | R/W | EQ_VREF[3] | 0 |
| Bit 2 | R/W | EQ_VREF[2] | 0 |
| Bit 1 | R/W | EQ_VREF[1] | 0 |
| Bit 0 | R/W | EQ_VREF[0] | 0 |

When the RUNI bit of the Receive Line Interface Configuration register is a logic 1, this register is held reset.

EQ_VREF[5:0]:

This register sets the voltage reference of the analog receiver's equalizer. For T1 mode, the EQ_VREF[5:0] bits must be programmed to 2CH ('b101100). For E1 mode, the EQ_VREF[5:0] bits must be programmed to 34H ('b110100).

### Register 0E0H: PRGD Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | PDR[1] | 0 |
| Bit 6 | R/W | PDR[0] | 0 |
| Bit 5 | R/W | QRSS | 0 |
| Bit 4 | R/W | PS | 0 |
| Bit 3 | R/W | TINV | 0 |
| Bit 2 | R/W | RINV | 0 |
| Bit 1 | R/W | AUTOSYNC | 1 |
| Bit 0 | R/W | MANSYNC | 0 |

PDR[1:0]:

The PDR[1:0] bits select the content of the four pattern detector registers to be any one of the pattern receive registers, the error count holding registers, or the bit count holding registers. The selection is shown in the following table:

**Table 67 - Pattern Detector Register Configurations**

| PDR[1:0] | PDR#1 | PDR#2 | PDR#3 | PDR#4 |
|---|---|---|---|---|
| 00, 01 | Pattern Receive (LSB) | Pattern Receive | Pattern Receive | Pattern Receive (MSB) |
| 10 | Error Count (LSB) | Error Count | Error Count | Error Count (MSB) |
| 11 | Bit Count (LSB) | Bit Count | Bit Count | Bit Count (MSB) |

QRSS:

The quasi-random signal source (QRSS) bit enables the zero suppression feature required when generating a QRSS sequence. More specifically, a one is forced in the transmit stream when QRSS is a logic 1 and the following 14 bit positions in the transmit bit stream generator are all zeros. When QRSS is a logic 0, the zero suppression feature is disabled. Note that the QRSS bit is also interpreted by the PRGD receiver. Accordingly, the receiver

will expect appropriately placed zero suppression bits when QRSS is a logic 1.

PS:

The PS bit selects the pattern type. When PS is a logic 1, a repetitive pattern is generated. When PS is a logic 0, a pseudo-random pattern is generated/detected. The PS bit must be programmed to the desired setting before programming any other PRGD registers, otherwise the transmitted pattern may be corrupted. Any time the setting of the PS bit is changed, the rest of the PRGD registers should be reprogrammed.

TINV:

The TINV bit controls the logical inversion of the generated pattern. When TINV is a logic 1, the data generated is inverted.

RINV:

The RINV bit controls the logical inversion of the received stream. When RINV is a logic 1, the received data is inverted before being processed by the pattern detector.

AUTOSYNC:

The AUTOSYNC bit enables the automatic resynchronization of the pattern detector. The automatic resynchronization is activated when 10 or more bit errors are detected in a fixed 48-bit window. When AUTOSYNC is a logic 1, the auto resync feature is enabled. When AUTOSYNC is a logic 0, the auto sync feature is disabled, and pattern resynchronization is accomplished using the MANSYNC bit.

MANSYNC:

The MANSYNC bit is used to initiate a manual resynchronization of the pattern detector. A low to high transition on MANSYNC initiates the resynchronization.

### Register 0E1H: PRGD Interrupt Enable/Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | SYNCE | 0 |
| Bit 6 | R/W | BEE | 0 |
| Bit 5 | R/W | XFERE | 0 |
| Bit 4 | R | SYNCV | X |
| Bit 3 | R | SYNCI | X |
| Bit 2 | R | BEI | X |
| Bit 1 | R | XFERI | X |
| Bit 0 | R | OVR | X |

SYNCE:

The SYNCE bit enables the generation of an interrupt when the pattern detector changes synchronization state. When SYNCE is set to logic 1, the interrupt is enabled.

BEE:

The BEE bit enables the generation of an interrupt when a bit error is detected in the receive data. Bit errors are not flagged unless the pattern detector is synchronized. Loss of synchronization may result in the generation of a bit error interrupt. When BEE is set to logic 1, the interrupt is enabled.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the receive pattern registers, the bit counter holding registers, and the error counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

SYNCV:

The SYNCV bit indicates the synchronization state of the pattern detector. When SYNCV is a logic 1 the pattern detector is synchronized (the pattern detector has observed at least 48 consecutive error free bit periods). When SYNCV is a logic 0, the pattern detector is out of sync (the pattern detector has detected 10 or more bit errors in a fixed 48-bit window).

SYNCI:

The SYNCI bit indicates that the detector has changed synchronization state since the last time this register was read. If SYNCI is logic 1, the pattern detector has gained or lost synchronization at least once. SYNCI is set to logic 0 when this register is read.

BEI:

The BEI bit indicates that one or more bit errors have been detected since the last time this register was read. When BEI is set to logic 1, at least one bit error has been detected. BEI is set to logic 0 when this register is read.

XFERI:

The XFERI bit indicates that a transfer of pattern detector data has occurred. A logic 1 in this bit position indicates that the pattern receive registers, the bit counter holding registers and the error counter holding registers have been updated. This update is initiated by writing to one of the pattern detector register locations, or by writing to the Revision/Chip ID/Global PMON Update register. XFERI is set to logic 0 when this register is read.

OVR:

The OVR bit is the overrun status of the pattern detector registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred and that the contents of the pattern receive registers, the bit counter holding registers and the error counter holding registers have been overwritten. OVR is set to logic 0 when this register is read.

### Register 0E2H: PRGD Shift Register Length

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R/W | PL[4] | 0 |
| Bit 3 | R/W | PL[3] | 0 |
| Bit 2 | R/W | PL[2] | 0 |
| Bit 1 | R/W | PL[1] | 0 |
| Bit 0 | R/W | PL[0] | 0 |

PL[4:0]:

PL[4:0] determine the length of the generated pseudo random or repetitive pattern. The pattern length is equal to the value of PL[4:0] + 1.

### Register 0E3H: PRGD Tap

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R/W | PT[4] | 0 |
| Bit 3 | R/W | PT[3] | 0 |
| Bit 2 | R/W | PT[2] | 0 |
| Bit 1 | R/W | PT[1] | 0 |
| Bit 0 | R/W | PT[0] | 0 |

PT[4:0]:

PT[4:0] determine the feedback tap position of the generated pseudo random pattern. The feedback tap position is equal to the value of PT[4:0] + 1.

Refer to the Operation section for commonly programmed feedback taps and shift register lengths.

### Register 0E4H: PRGD Error Insertion

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | R/W | EVENT | 0 |
| Bit 2 | R/W | EIR[2] | 0 |
| Bit 1 | R/W | EIR[1] | 0 |
| Bit 0 | R/W | EIR[0] | 0 |

EVENT:

A low to high transition on the EVENT bit causes a single bit error to be inserted in the generated pattern. This bit must be cleared and set again for a subsequent error to be inserted.

EIR[2:0]:

The EIR[2:0] bits control the insertion of a programmable bit error rate as indicated in Table 68.

**Table 68 - Error Insertion Rates**

| EIR[2:0] | Generated Bit Error Rate |
|---|---|
| 000 | No errors inserted |
| 001 | $10^{-1}$ |
| 010 | $10^{-2}$ |
| 011 | $10^{-3}$ |
| 100 | $10^{-4}$ |
| 101 | $10^{-5}$ |
| 110 | $10^{-6}$ |
| 111 | $10^{-7}$ |

### Register 0E8H: PRGD Pattern Insertion #1

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | PI[7] | 0 |
| Bit 6 | R/W | PI[6] | 0 |
| Bit 5 | R/W | PI[5] | 0 |
| Bit 4 | R/W | PI[4] | 0 |
| Bit 3 | R/W | PI[3] | 0 |
| Bit 2 | R/W | PI[2] | 0 |
| Bit 1 | R/W | PI[1] | 0 |
| Bit 0 | R/W | PI[0] | 0 |

### Register 0E9H: PRGD Pattern Insertion #2

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | PI[15] | 0 |
| Bit 6 | R/W | PI[14] | 0 |
| Bit 5 | R/W | PI[13] | 0 |
| Bit 4 | R/W | PI[12] | 0 |
| Bit 3 | R/W | PI[11] | 0 |
| Bit 2 | R/W | PI[10] | 0 |
| Bit 1 | R/W | PI[9] | 0 |
| Bit 0 | R/W | PI[8] | 0 |

### Register 0EAH: PRGD Pattern Insertion #3

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | PI[23] | 0 |
| Bit 6 | R/W | PI[22] | 0 |
| Bit 5 | R/W | PI[21] | 0 |
| Bit 4 | R/W | PI[20] | 0 |
| Bit 3 | R/W | PI[19] | 0 |
| Bit 2 | R/W | PI[18] | 0 |
| Bit 1 | R/W | PI[17] | 0 |
| Bit 0 | R/W | PI[16] | 0 |

### Register 0EBH: PRGD Pattern Insertion #4

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | PI[31] | 0 |
| Bit 6 | R/W | PI[30] | 0 |
| Bit 5 | R/W | PI[29] | 0 |
| Bit 4 | R/W | PI[28] | 0 |
| Bit 3 | R/W | PI[27] | 0 |
| Bit 2 | R/W | PI[26] | 0 |
| Bit 1 | R/W | PI[25] | 0 |
| Bit 0 | R/W | PI[24] | 0 |

PI[31:0]:

PI[31:0] contain the data that is loaded in the pattern generator each time a new pattern (pseudo random or repetitive) is to be generated. When a pseudo random pattern is to be generated, PI[31:0] should be set to FFFFFFFFH. The data is loaded each time pattern insertion register #4 is written. Pattern insertion registers #1 - #3 should be loaded with the desired data before pattern register #4 is written. When a repetitive pattern is transmitted, PI[31] is transmitted first, followed by the remaining bits in sequence down to PI[0]. Subsequently, PI [pattern_length-1] down to PI[0] will be repetitively transmitted, where pattern_length is the decimal value stored in the PRGD length register.

### Register 0ECH: PRGD Pattern Detector #1

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | PD[7] | X |
| Bit 6 | R | PD[6] | X |
| Bit 5 | R | PD[5] | X |
| Bit 4 | R | PD[4] | X |
| Bit 3 | R | PD[3] | X |
| Bit 2 | R | PD[2] | X |
| Bit 1 | R | PD[1] | X |
| Bit 0 | R | PD[0] | X |

### Register 0EDH: PRGD Pattern Detector #2

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | PD[15] | X |
| Bit 6 | R | PD[14] | X |
| Bit 5 | R | PD[13] | X |
| Bit 4 | R | PD[12] | X |
| Bit 3 | R | PD[11] | X |
| Bit 2 | R | PD[10] | X |
| Bit 1 | R | PD[9] | X |
| Bit 0 | R | PD[8] | X |

### Register 0EEH: PRGD Pattern Detector #3

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | PD[23] | X |
| Bit 6 | R | PD[22] | X |
| Bit 5 | R | PD[21] | X |
| Bit 4 | R | PD[20] | X |
| Bit 3 | R | PD[19] | X |
| Bit 2 | R | PD[18] | X |
| Bit 1 | R | PD[17] | X |
| Bit 0 | R | PD[16] | X |

### Register 0EFH: PRGD Pattern Detector #4

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | PD[31] | X |
| Bit 6 | R | PD[30] | X |
| Bit 5 | R | PD[29] | X |
| Bit 4 | R | PD[28] | X |
| Bit 3 | R | PD[27] | X |
| Bit 2 | R | PD[26] | X |
| Bit 1 | R | PD[25] | X |
| Bit 0 | R | PD[24] | X |

PD[31:0]:

Reading PD[31:0] returns the contents of the pattern detector data register selected by the PDR[1:0] bits in the control register. All three detector data registers are updated during an accumulation interval.

When PDR[1:0] is set to 00 or 01, reading PD[31:0] returns the contents of the pattern receive register. The 32 bits received immediately before the last accumulation interval are present on PD[31:0]. PD[0] contains the bit received immediately prior to the last accumulation.

When PDR[1:0] is set to 10, reading PD[31:0] returns the contents of the error counter holding register. The value in this register represents the number of bit errors that were accumulated during the last accumulation interval, up to a maximum (saturation) value of $2^{32}$-1. Note that bit errors are not accumulated while the pattern detector is out of sync.

When PDR[1:0] is set to 11, reading PD[31:0] returns the contents of the bit counter holding register. The value in this register represents the total number of bits that were received during the last accumulation interval, up to a maximum (saturation) value of $2^{32}$-1. Note that bits are not counted while the pattern detector is out of synchronization.

Writing to any of these registers or the Global PMON Update Register causes them to be updated, and the internal counters reset. The XFERI bit in PRGD Enable/Status register will go high once the update is complete, and an interrupt will be generated if enabled.

### Register 0F0H: XLPG Line Driver Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | HIGHZ | 1 |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R/W | SCALE[4] | 0 |
| Bit 3 | R/W | SCALE[3] | 0 |
| Bit 2 | R/W | SCALE[2] | 0 |
| Bit 1 | R/W | SCALE[1] | 0 |
| Bit 0 | R/W | SCALE[0] | 0 |

When the TUNI bit of the Transmit Line Interface Configuration register is a logic 1, this register is held reset.

HIGHZ:

The HIGHZ bit controls if the TXTIP and TXRING outputs are to be tri-stated or not. When the HIGHZ bit is set to a logic 0, the outputs are enabled. When the HIGHZ bit is set to a logic 1 then the outputs are put into high impedance. Setting HIGHZ to logic 1 has the same effect as setting SCALE[4:0] to 00H.

SCALE[4:0]:

The SCALE[4:0] bits control the amplitude of the D/A output waveform. The full scale output amplitude is increased by increments of 11.14 mA. A value of 0 (00H) tristates the output while the maximum value of 21 (15H) sets the full scale current to 234 mA.

**Table 69 - Transmit Output Amplitude**

| SCALE[4:0] | Output Amplitude |
|---|---|
| 0<br>00000 | 0 mA (tristate) |
| 1-20<br>00001-10100 | Increments of 11.14 mA for each D/A step |
| 21<br>10101 | 234 mA total |
| >21<br>10110-11111 | Reserved |

### Register 0F1H: XLPG Control/Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | R | OVRFLW | X |
| Bit 1 | R/W | Reserved | 0 |
| Bit 0 | R/W | Reserved | 1 |

When the TUNI bit of the Transmit Line Interface Configuration register is a logic 1, this register is held reset.

OVRFLW:

The overflow detection value bit (OVRFLW) indicates the presence or absence of an overflow condition in the waveform computation pipeline. An overflow occurs when the sum of the five unit interval (UI) samples exceeds the maximum D/A value. The XLPG detects overflows and saturates the output value to minimize their impact on the output signal. Overflows can easily be eliminated by changing the waveform programming. This status bit is set to logic 1 when an overflow condition is detected and it is reset to logic 0 only when this register is read. It is suggested to read this register twice after the programming of a new waveform and transmission of data to ensure the maximum output amplitude is never exceeded.

Reserved:

The Reserved bits must remain in their default state for correct operation.

### Register 0F2H: XLPG Pulse Waveform Storage Write Address

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | SAMPLE[4] | 0 |
| Bit 6 | R/W | SAMPLE[3] | 0 |
| Bit 5 | R/W | SAMPLE[2] | 0 |
| Bit 4 | R/W | SAMPLE[1] | 0 |
| Bit 3 | R/W | SAMPLE[0] | 0 |
| Bit 2 | R/W | UI[2] | 0 |
| Bit 1 | R/W | UI[1] | 0 |
| Bit 0 | R/W | UI[0] | 0 |

When the TUNI bit of the Transmit Line Interface Configuration register is a logic 1, this register is held reset.

UI[2:0]:

The pulse waveform write address is composed of a unit interval selector and a sample selector. The unit interval selector (UI[2:0]) selects which unit interval is being written for a given sample. There are 5 unit intervals, numbered from 0 to 4. UI[2:0] can take the values 0H, 1H, 2H, 3H and 4H. The values 5H, 6H and 7H are undefined.

SAMPLE[4:0]:

The pulse waveform write address is composed of a unit interval selector and a sample selector. The sample selector (SAMPLE[4:0]) selects which sample is being written for a given unit interval. There are 24 samples, numbered from 0 to 23. SAMPLE[4:0] can thus have any value from 00H to 17H. The values from 18H to 1FH are undefined.

See the Operation section for more details on setting up waveform templates.

### Register 0F3H: XLPG Pulse Waveform Storage Data

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | W | WDAT[6] | X |
| Bit 5 | W | WDAT[5] | X |
| Bit 4 | W | WDAT[4] | X |
| Bit 3 | W | WDAT[3] | X |
| Bit 2 | W | WDAT[2] | X |
| Bit 1 | W | WDAT[1] | X |
| Bit 0 | W | WDAT[0] | X |

When the TUNI bit of the Transmit Line Interface Configuration register is a logic 1, this register is held reset.

WDAT[6:0]:

This register allows software to program the contents of any one of the 120 internal waveform template registers, addressed by the UI[2:0] and SAMPLE[4:0] bits in the Pulse Waveform Storage Write Address register. When accessing the internal waveform storage registers, the address of the desired register must first be written to the Indirect Address register (the XLPG Pulse Waveform Storage Write Address register). Then, by writing the Indirect Data register (the XLPG Pulse Waveform Storage Data register), the microprocessor can write the data to the selected write address.

The value written to the internal pulse waveform storage registers is contained in the signed WDAT[6:0] bits. A signed representation is used (by opposition to a two's complement representation) to make the programming easier. WDAT[6] is the sign bit, WDAT[5] is the most significant data bit and WDAT[0] is the least significant data bit. The data value thus can range from -62 to +63 (-63 is not a valid value due to subsequent conversion into a two's complement representation).

See the Operation section for more details on setting up custom waveform templates.

### Register 0F4H: XLPG Analog Test Negative Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | R/W | TNC[6] | 0 |
| Bit 5 | R/W | TNC[5] | 0 |
| Bit 4 | R/W | TNC[4] | 0 |
| Bit 3 | R/W | TNC[3] | 0 |
| Bit 2 | R/W | TNC[2] | 0 |
| Bit 1 | R/W | TNC[1] | 0 |
| Bit 0 | R/W | TNC[0] | 0 |

When the TUNI bit of the Transmit Line Interface Configuration register is a logic 1, this register is held reset.

TNC[6:0]:

This register controls the nDAC absolute current (both “blowing” the fuses and the software override of the fuses) of the analog transmit line interface unit. TNC[1:5] adjust the offset in steps of 0.78125%, TNC[6] controls the direction (0 is positive, 1 is negative) and TNC[0] is the enable (active low). When TNC[0] is logic 0 and the TRIMF input pin is high, the fuse(s) (as indicated by TNC[1:6]) will be blown. Note that the device must be in analog test mode to enable this control. When TRIMF is low and TNC[0] is logic 0, then TNC[1:6] override the fuses (note this is independent of being in analog test mode).

### Register 0F5H: XLPG Analog Test Positive Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | R/W | TPC[6] | 0 |
| Bit 5 | R/W | TPC[5] | 0 |
| Bit 4 | R/W | TPC[4] | 0 |
| Bit 3 | R/W | TPC[3] | 0 |
| Bit 2 | R/W | TPC[2] | 0 |
| Bit 1 | R/W | TPC[1] | 0 |
| Bit 0 | R/W | TPC[0] | 0 |

When the TUNI bit of the Transmit Line Interface Configuration register is a logic 1, this register is held reset.

TPC[6:0]:

This register controls the pDAC absolute current (both “blowing” the fuses and the software override of the fuses) of the analog transmit line interface unit. TPC[1:5] adjust the offset in steps of 0.78125%, TPC[6] controls the direction (0 is positive, 1 is negative) and TPC[0] is the enable (active low). When TPC[0] is logic 0 and the TRIMF input pin is high, the fuse(s) (as indicated by TPC[1:6]) will be blown. Note that the device must be in analog test mode to enable this control. When TRIMF is low and TPC[0] is logic 0, then TPC[1:6] override the fuses (note this is independent of being in analog test mode).

### Register 0F6H: XLPG Fuse Data Select

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | R/W | FDSB | 0 |

When the TUNI bit of the Transmit Line Interface Configuration register is a logic 1, this register is held reset.

FDSB:

This register selects between microprocessor data (FDSB is logic 1) or the value burned into the fuses of the transmit line interface unit (FDSB is logic 0) as the inputs to the XLPG Analog Test Negative Control Register and the XLPG Analog Test Positive Control Register. To write the fuse data into the XLPG Analog Test Negative Control Register and the XLPG Analog Test Positive Control Register, TPC[0] and TNC[0], respectively, must be set to logic 1 and the XLPG Analog Test Negative Control Register and the XLPG Analog Test Positive Control Register must each be written to twice consecutively. (The first write is to activate the outputs of the transmit line interface unit valid, and the second write copies the fuse data into the register.) TPC[0] and TNC[0] should be cleared to lower the likelihood of fuse re-growth.

### Register 0F8H: RLPS Configuration and Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | ALOSI | X |
| Bit 6 | R | ALOSV | X |
| Bit 5 | R/W | ALOSE | 0 |
| Bit 4 | R/W | SQUELCHE | 0 |
| Bit 3 | R/W | IDDQ_EN | 0 |
| Bit 2 | R/W | DB_VALID | X |
| Bit 1 | | Unused | X |
| Bit 0 | R/W | Reserved | 1 |

When the RUNI bit of the Receive Line Interface Configuration register is a logic 1, this register is held reset.

Reserved:

The Reserved bit must be programmed to logic 1 for correct operation.

DB_VALID:

The DB_VALID bit indicates if the adaptive equalizer has stabilized. This bit is set if the CABLELOSS signal has not changed by more than 2dB (or +/-8 steps in the RAM table) in more than the count of sampling periods selected by the VALID_PER[1:0] bits of the RLPS Equalizer Configuration register.

IDDQ_EN:

The IDDQ enable bit (IDDQ_EN) is used to configure the analog receiver for IDDQ tests. When IDDQ_EN is a logic 1, or the IDDQEN bit in the Master Test register (00BH) is a logic 1, the digital outputs of the analog receiver are pulled to ground.

SQUELCHE:

The output data squelch enable (SQUELCHE) allows control of data squelching in response to an analog LOS of signal condition. When SQUELCHE is set to logic 1, the recovered data are forced to all-zeros if the ALOSV register bit is asserted. When SQUELCHE is set to logic 0, squelching is disabled.

ALOSE:

The loss of signal interrupt enable bit (ALOSE) enables the generation of device level interrupt on a change of Loss of Signal status. When ALOSE is a logic 1, an interrupt is generated by asserting INTB low when there is a change of the ALOSV status. When ALOSE is set to logic 0, interrupts are disabled.

ALOSV:

The loss of signal value bit (ALOSV) indicates the loss of signal alarm state. This status bit is available for both short haul mode and long haul modes of operation.

ALOSI:

The loss of signal interrupt bit (ALOSI) is a logic 1 whenever the Loss of Signal indicator state (ALOSV) changes from a logic 0 to a logic 1. This bit is cleared when this register is read.

### Register 0F9H: RLPS ALOS Detection/Clearance Threshold

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | R/W | CLR_THR[2] | 0 |
| Bit 5 | R/W | CLR_THR[1] | 0 |
| Bit 4 | R/W | CLR_THR[0] | 0 |
| Bit 3 | | Unused | X |
| Bit 2 | R/W | DET_THR[2] | 0 |
| Bit 1 | R/W | DET_THR[1] | 0 |
| Bit 0 | R/W | DET_THR[0] | 0 |

When the RUNI bit of the Receive Line Interface Configuration register is a logic 1, this register is held reset.

**Table 70 - ALOS Detection/Clearance Thresholds**

| THR | Signal level (dB) | Detection/ Clearance |
|---|---|---|
| 000 | 9 | Clearance |
| 001 | 14.5 | |
| 010 | 20 | Detection and Clearance |
| 011 | 22 | |
| 100 | 25 | |
| 101 | 30 | Detection and Clearance |
| 110 | 31 | |
| 111 | 35 | Detection |

DET_THR[2:0]:

DET_THR[2:0] references one of the threshold settings in Table 70 as the ALOS detection criteria. If the incoming signal level is less than or equal to that threshold for N consecutive pulse period, (where N = 16 * the value stored in the RLPS ALOS Detection Period Register) ALOS is declared and interrupt is set. The DET_THR[2:0] bits must be programmed to the same value as the CLR_THR[2:0] bits.

CLR_THR[2:0]:

CLR_THR[2:0] references one of the threshold settings listed in Table 70 as the ALOS clearance criteria. ALOS is cleared when the incoming signal level is greater than or equal to  dB below nominal for N consecutive pulse intervals, where N = 16 * CLR_PER stored in the RLPS ALOS Clearance Period Register.  The CLR_THR[2:0] bits must be programmed to the same value as the DET_THR[2:0] bits.

### Register 0FAH: RLPS ALOS Detection Period

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | DET_PER[7] | 0 |
| Bit 6 | R/W | DET_PER[6] | 0 |
| Bit 5 | R/W | DET_PER[5] | 0 |
| Bit 4 | R/W | DET_PER[4] | 0 |
| Bit 3 | R/W | DET_PER[3] | 0 |
| Bit 2 | R/W | DET_PER[2] | 0 |
| Bit 1 | R/W | DET_PER[1] | 0 |
| Bit 0 | R/W | DET_PER[0] | 1 |

When the RUNI bit of the Receive Line Interface Configuration register is a logic 1, this register is held reset.

DET_PER[7:0]:

This register specifies the time duration that the incoming signal level has to remain below the detection threshold in order for the ALOS to be issued. This duration is equal to DET_PER * 16 number of pulse intervals, the resulting range is from 16 to 4080 and thus compliant with all the presently available E1/T1 ALOS detection standards/ recommendations.

### Register 0FBH: RLPS ALOS Clearance Period

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | CLR_PER[7] | 0 |
| Bit 6 | R/W | CLR_PER[6] | 0 |
| Bit 5 | R/W | CLR_PER[5] | 0 |
| Bit 4 | R/W | CLR_PER[4] | 0 |
| Bit 3 | R/W | CLR_PER[3] | 0 |
| Bit 2 | R/W | CLR_PER[2] | 0 |
| Bit 1 | R/W | CLR_PER[1] | 0 |
| Bit 0 | R/W | CLR_PER[0] | 1 |

When the RUNI bit of the Receive Line Interface Configuration register is a logic 1, this register is held reset.

CLR_PER[7:0]:

This register specifies the time duration that the incoming signal level has to remain above the clearance threshold in order for the ALOS to be cleared. This duration is equal to CLR_PER * 16 number of pulse intervals resulting in a range from 16 to 4080 and thus compliant with all the presently available E1/T1 ALOS clearance standards/ recommendations.

### Register 0FCH: RLPS Equalization Indirect Address

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | EQ_ADDR[7] | 0 |
| Bit 6 | R/W | EQ_ADDR[6] | 0 |
| Bit 5 | R/W | EQ_ADDR[5] | 0 |
| Bit 4 | R/W | EQ_ADDR[4] | 0 |
| Bit 3 | R/W | EQ_ADDR[3] | 0 |
| Bit 2 | R/W | EQ_ADDR[2] | 0 |
| Bit 1 | R/W | EQ_ADDR[1] | 0 |
| Bit 0 | R/W | EQ_ADDR[0] | 0 |

When the RUNI bit of the Receive Line Interface Configuration register is a logic 1, this register is held reset.

EQ_ADDR [7:0]:

Writing to this register initiates an internal uP access request cycle to the RAM. Depending on the setting of the RWB bit inside register 0FDH, a read or a write will be performed.

During a write cycle, the indirect data bits located in registers 0D8H to 0DBH is written into the RAM. For a read request, the content of the addressed RAM location is written into registers 0D8H to 0DBH. This register should be the last register to be written for a uP access.

A waiting period of three line rate cycles is needed between the time this register is written to the time the next indirect data bits in registers 0D8H to 0DBH are written.

### Register 0FDH: RLPS Equalization Read/WriteB Select

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | RWB | 1 |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | | Unused | X |

When the RUNI bit of the Receive Line Interface Configuration register is a logic 1, this register is held reset.

RWB:

This bit selects the operation to be performed on the RAM: when RWB is ‘1’, a read from the equalization RAM is requested; when RWB is set to ‘0’, a write to the RAM is desired.

### Register 0FEH: RLPS Equalizer Loop Status and Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | LOCATION[7] | 0 |
| Bit 6 | R/W | LOCATION[6] | 0 |
| Bit 5 | R/W | LOCATION[5] | 0 |
| Bit 4 | R/W | LOCATION[4] | 0 |
| Bit 3 | R/W | LOCATION[3] | 0 |
| Bit 2 | R/W | LOCATION[2] | 0 |
| Bit 1 | R/W | LOCATION[1] | 0 |
| Bit 0 | R/W | LOCATION[0] | 0 |

When the RUNI bit of the Receive Line Interface Configuration register is a logic 1, this register is held reset.

LOCATION[7:0]:

Writing to this register overwrites a counter which serves as the read address to the equalization RAM. Reading this register returns the current value of the counter

### Register 0FFH: RLPS Equalizer Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | VALID_PER[1] | 0 |
| Bit 6 | R/W | VALID_PER[0] | 0 |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | R/W | Reserved | 0 |
| Bit 2 | R/W | EQ_FREQ2] | 0 |
| Bit 1 | R/W | EQ_FREQ[1] | 1 |
| Bit 0 | R/W | EQ_FREQ[0] | 1 |

When the RUNI bit of the Receive Line Interface Configuration register is a logic 1, this register is held reset.

EQ_FREQ[2:0]:

The EQ_FREQ[2:0] field selects the frequency of the EQ feedback loop as indicated by Table 71.

**Table 71 - Equalization Feedback Frequencies**

| EQ_FREQ[2:0] | EQ Feedback Frequency | |
|---|---|---|
| | T1 mode | E1 mode |
| 000 | 24.125 kHz | 32.000 kHz |
| 001 | 12.063 kHz | 16.000 kHz |
| 010 | 8.0417 kHz | 10.667 kHz |
| 011 | 6.0313 kHz | 8.0000 kHz |
| 100 | 4.8250 kHz | 6.40 kHz |
| 101 | 4.0208 kHz | 5.333 kHz |
| 110 | 3.4464 kHz | 4.5714 kHz |
| 111 | 3.0156 kHz | 4.0 kHz |

Reserved:

The Reserved bit must be programmed to logic 1 for correct operation. Note that this bit defaults to logic 0.

VALID_PER[1:0]:

The VALID_PER[1:0] bits select the length of time that the dB loss counter must be stable before DB_VALID is asserted. The duration is measured in number of periods of the EQ feedback loop (specified by the EQ_FREQ bits) as indicated by Table 72.

**Table 72 - Valid Period**

| VALID_PER | Number of periods |
|---|---|
| 00 | 32 |
| 01 | 64 |
| 10 | 128 |
| 11 | 256 |

# 12 TEST FEATURES DESCRIPTION

Simultaneously asserting the CSB, RDB and WRB inputs causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the COMET. Test mode registers (as opposed to normal mode registers) are mapped into addresses 100H-1FFH.

Test mode registers may also be used for board testing. When all of the constituent Telecom System Blocks within the COMET are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

**Notes on Test Mode Register Bits:**

1. Writing values into unused register bits has no effect. Reading unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

### Register 00BH: COMET Master Test

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | W | IDDQEN | X |
| Bit 5 | W | PMCATST | X |
| Bit 4 | W | PMCTST | X |
| Bit 3 | W | DBCTRL | 0 |
| Bit 2 | R/W | IOTST | 0 |
| Bit 1 | W | HIZDATA | 0 |
| Bit 0 | R/W | HIZIO | 0 |

This register is used to select COMET test features. All bits, except for PMCTST, PMCATST and IDDQEN, are reset to zero by a hardware reset of the COMET; a software reset of the COMET does not affect the state of the bits in this register.

IDDQEN:

The IDDQEN bit is used to configure the COMET for IDDQ tests. IDDQEN is cleared when CSB is high and RSTB is low or when IDDQEN is written as logic 0. When the IDDQEN bit is set to logic 1, the HIGHZ bit in the XLPG Line Driver Configuration register must also be set to logic 1.

PMCATST:

The PMCATST bit is used to configure the analog portion of the COMET for PMC's manufacturing tests. PMCATST is cleared when CSB is high and RSTB is low or when PMCATST is written as logic 0.

PMCTST:

The PMCTST bit is used to configure the COMET for PMC's manufacturing tests. When PMCTST is set to logic 1, the COMET microprocessor port becomes the test access port used to run the PMC manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and is cleared by setting CSB high.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin

high causes the COMET to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each block in the COMET for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in this section).

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the COMET . While the HIZIO bit is a logic 1, all output pins of the COMET except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

## 12.1 Test Mode 0

In test mode 0, the COMET allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface.

To enable test mode 0, the IOTST bit in the Master Test Register (register 00BH) must be set to logic 1 and the following addresses must be written with 00H: 101H, 111H, 115H, 119H, 11DH, 121H, 125H, 129H, 131H, 139H, 141H, 149H, 14DH, 151H, 155H, 157H, 159H, 161H, 165H, 167H, 169H, 16BH, 16DH, 171H, 179H, 181H, 18DH, 191H, 1A9H, 1B1H, 1B9H, 1C1H, 1C9H, 1D1H, 1D7H, 1E1H, 1F1H and 1F9H. All other registers must be in their default (i.e., reset) state, except as noted below.

Reading the following address locations returns the values for the indicated inputs:

**Table 73 - Observing Inputs in Test Mode 0**

| Addr | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| 114H | | | | | | RCLKI[1] | | RDAT[1] |
| 118H | | | | | | TCLKI[2] | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 133H | | | | | | | | BRFP |
| 134H | | | BRCLK | | | | | |
| 143H | | | | | BTCLK | BTFP | BTSIG | BTPCM |
| 1D6H | | | | | | | | XCLK |
| 1F0H | | | TRIMF | | | | | |

Writing the following address locations forces the outputs to the value in the corresponding bit position:

**Table 74 - Controlling Outputs in Test Mode 0**

| Addr | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| 100H | RSYNC | | | | | | | |
| 118H | | | | | | | TFP[3] | TDAT[3] |
| 11AH | | | | | | TCLKO[3] | | |
| 133H | BRPCM | BRSIG | BRPCM (OEB) | BRSIG (OEB) | BRFP | BRFP (OEB) | BRCLK | BRCLK (OEB) |
| 143H | | INT[4] | | | | | | |
| 144H | | | | | BTCLK (OEB) | BTCLK | BTFP (OEB) | BTFP |

**Notes:**

1. To observe the value of RCLKI or RDAT, the RUNI bit in the Receive Line Interface Configuration register must be set to logic 1 and the RJATBYP bit in the Receive Options register must be set to logic 0. Additionally, the value on RDAT must be clocked in by RCLKI (one clock pulse) in order to be read.

2. To observe the value of TCLKI, the PLLREF1 and PLLREF0 bits in the Transmit Timing Options register must both be set to logic 1.

3. To control the TFP, TDAT and TCLKO outputs, the TJATBYP bit in the Transmit Options register must be set to logic 0 and the TUNI bit in the Transmit Line Interface Configuration register must be set to logic 1. Additionally, the value written to the TDAT and TFP bits do not propagate to the TDAT and TFP outputs, respectively, until the TCLKO output is toggled twice (i.e., by setting the TCLKO bit to logic 0, logic 1, logic 0, logic 1 and back to logic 0).

4. Writing a logic 1 to the block interrupt signal INT at address 143H, asserts the INTB output low. In order to force INTB to the high impedance state, registers, 110H to 1FFH must be initialized to 00H.

5. The “signal_name (OEB)” signals will set the corresponding output signal, “signal_name”, to high impedance when set high.

6. The “signal_name (OEB)” signals will set the corresponding bidirectional signal, “signal_name”, to an output when set low.

## 12.2 JTAG Test Port

The COMET JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

### Instruction Register

### Length - 3 bits

| Instructions | Selected Register | Instruction Codes, IR[2:0] |
|---|---|---|
| EXTEST | Boundary Scan | 000 |
| IDCODE | Identification | 001 |
| SAMPLE | Boundary Scan | 010 |
| BYPASS | Bypass | 011 |
| BYPASS | Bypass | 100 |
| STCTEST | Boundary Scan | 101 |
| BYPASS | Bypass | 110 |
| BYPASS | Bypass | 111 |

### Identification Register

Length - 32 bits

Version number – 5H for Rev G and F, 4H for Rev E

Part Number - 4351H

Manufacturer's identification code - 0CDH

Device identification - 543510CDH for Rev. G and F, 443510CDH for Rev. E

**Table 75 - Boundary Scan Register**

**Length - 59 bits**

| Pin/ Enable | Scan Register Bit | Pin/ Enable | Scan Register Bit | Pin/ Enable | Scan Register Bit |
|---|---|---|---|---|---|
| HIZ [3,4] | 58 | D1_OEB [1] | 38 | A7 | 18 |
| XCLK | 57 | D2 | 37 | A8 | 17 |
| TCLKI | 56 | D2_OEB [1] | 36 | ALE | 16 |
| TCLKO | 55 | D3 | 35 | BRFP | 15 |
| TDAT | 54 | D3_OEB [1] | 34 | BRFP_OEB [1] | 14 |
| TFP | 53 | D4 | 33 | BRSIG | 13 |
| BTCLK | 52 | D4_OEB [1] | 32 | BRSIG_OEB | 12 |
| BTCLK_OEB [1] | 51 | D5 | 31 | BRPCM | 11 |
| BTPCM | 50 | D5_OEB [1] | 30 | BRPCM_OEB [2] | 10 |
| BTSIG | 49 | D6 | 29 | BRCLK | 9 |
| BTFP | 48 | D6_OEB [1] | 28 | BRCLK_OEB [1] | 8 |
| BTFP_OEB [1] | 47 | D7 | 27 | RSYNC | 7 |
| CSB | 46 | D7_OEB [1] | 26 | RCLKI | 6 |
| RSTB | 45 | A0 | 25 | RCLKI_OEB [1] | 5 |
| RDB | 44 | A1 | 24 | RDAT | 4 |
| WRB | 43 | A2 | 23 | RDAT_OEB [1] | 3 |
| INTB | 42 | A3 | 22 | TRIMF | 2 |
| D0 | 41 | A4 | 21 | NC | 1 |
| DO_OEB [1] | 40 | A5 | 20 | NC_OEB | 0 |
| D1 | 39 | A6 | 19 | | |

**Notes:**

1. These OEB signals, when set low, will set the corresponding bidirectional signal to an output.
2. These OEB signals, when set high, will set the corresponding output to high impedance.
3. When set high, TCLKO, TDAT, TFP, and RSYNC will be set to high impedance.
4. HIZ is the first bit in the boundary scan chain.

# 13 FUNCTIONAL TIMING

## 13.1 Transmit Backplane Interface

By convention, the first bit transmitted in each timeslot is designated bit 0; the last is bit 7.

**Figure 13 - Transmit Backplane: CMS=0, FE=1, DE=1, BTFP is Input**

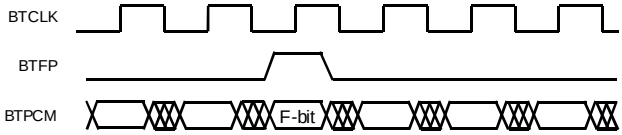



**Figure 14 - Transmit Backplane: CMS=0, FE=1, DE=0, BTFP is Input**

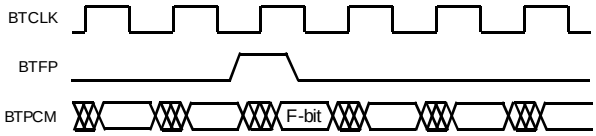



**Figure 15 - Transmit Backplane: CMS=1, FE=1, DE=1, BTFP is Input**

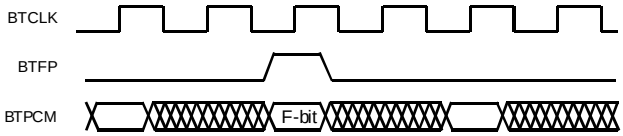



**Figure 16 - Transmit Backplane:  CMS=1, FE=0, DE=1, BTFP is Input**

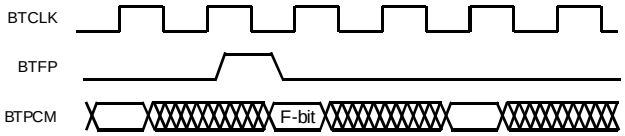



Figure 13, Figure 14, Figure 15, and Figure 16 above indicate the relationship between BTCLK, BTFP, and BTPCM with various settings for the BTIF's CMS, FE, and DE register bits in T1 mode with BTFP configured as an input (FPMODE=1). When FE and DE have the same value, the frame pulse is sampled on the same clock edge as the data. When FE and DE have opposite values, the frame pulse is sampled one clock edge before the data. In the above figures, the TSOFF[6:0], BOFF_EN and BOFF[2:0] register bits are logic zero.

**Figure 17 - Transmit Backplane: CMS=0, FE=1, DE=1, BTFP is Output**

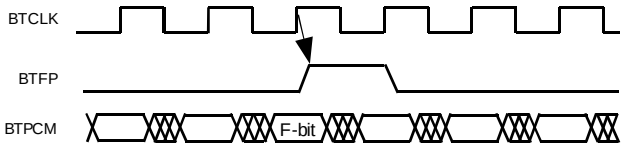



**Figure 18 - Transmit Backplane: CMS=0, FE=1, DE=0, BTFP is Output**

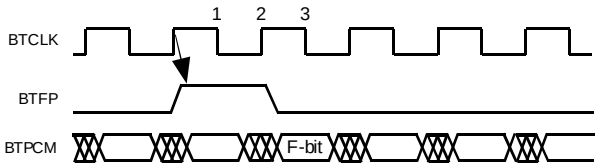
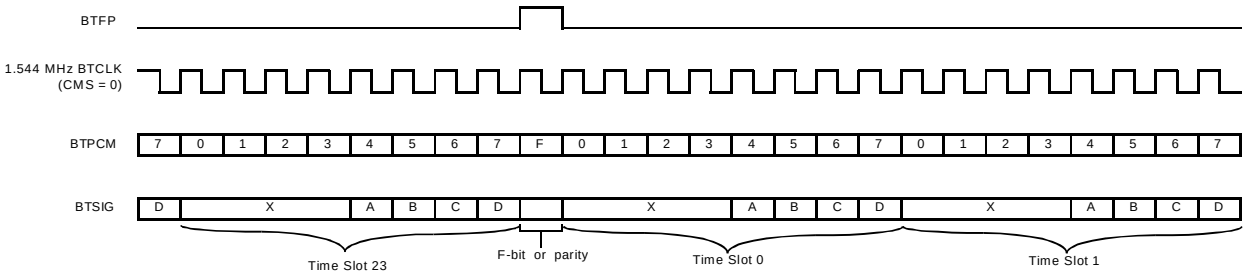



Figure 17 and Figure 18 above indicate the relationship between BTCLK, BTFP, and BTPCM with two settings for the BTIF's CMS, FE, and DE register bits in T1 mode with BTFP configured as an output (FPMODE=0). When FE and DE have the same value, the frame pulse is updated on the same clock edge as the data is sampled. When FE and DE have opposite values, the frame pulse is updated three clock edge before the data is sampled. In the above figures, the TSOFF[6:0], BOFF_EN and BOFF[2:0] register bits are logic zero.

**Figure 19 - Transmit Backplane at 1.544 Mbit/s (T1 mode)**



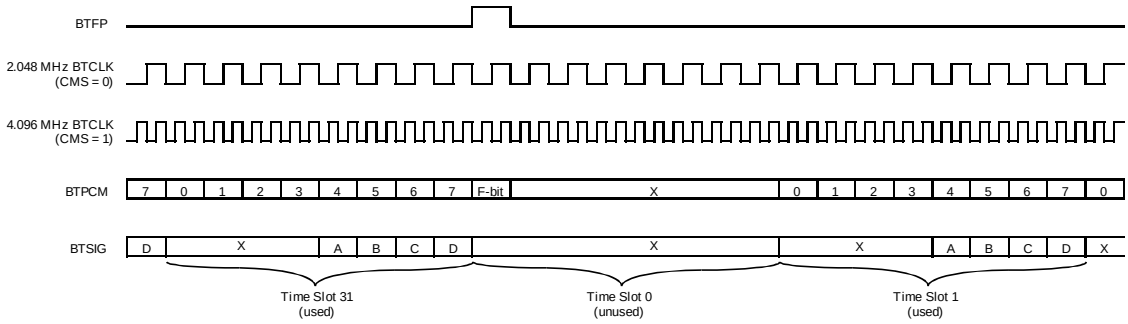

A 1.544 Mbit/s backplane in T1 mode is configured by setting RATE[1:0] of the Transmit Backplane Configuration register to 'b00 and the E1/T1B bit of the Global Configuration register to a logic 0. In Figure 19, BTFP, BTPCM and BTSIG are configured to be updated on the falling edge of BTCLK by setting FE and DE bits of the Transmit Backplane Configuration register to logic 0. The TSOFF[6:0], BOFF_EN and BOFF[2:0] register bits are all logic 0, therefore BTFP is expected to be aligned to the first bit of the frame.

A 1.544 Mbit/s backplane in T1 mode is configured by setting the RATE[1:0] bits of the Transmit Backplane Configuration register to 'b00 and the E1/T1B bit of

the Global Configuration register to a logic 0. Once the RATE[1:0] bits are set, a reset is required to change to a new RATE[1:0].

In Figure 19, BTPCM and BTFP are configured to be sampled on the falling edge of BTCLK by setting the DE and FE bits of the Transmit Backplane Configuration register to a logic 0. The TSOFF[6:0], BOFF_EN and BOFF[2:0] register bits are all logic zero; therefore, BTFP is expected to be aligned to the F-bit position.

**Figure 20 - Transmit Backplane at 2.048 Mbit/s (T1 mode)**

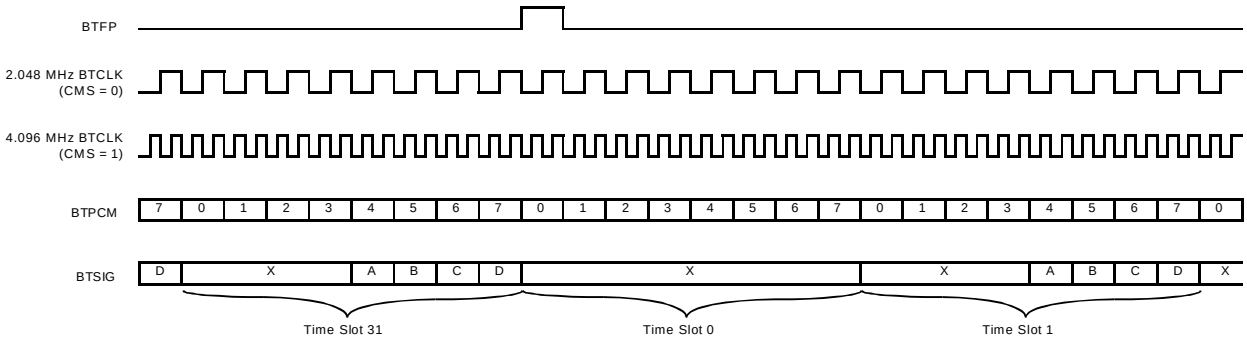



A 2.048 Mbit/s backplane in T1 mode is configured by setting the RATE[1:0] bits of the Transmit Backplane Configuration register to 'b01 and the E1/T1B bit of the Global Configuration register to a logic 0. In Figure 20, BTFP, BTPCM and BTSIG are configured to be sampled on the rising edge of BTCLK by setting the FE and DE bits of the Transmit Backplane Configuration register to logic 1. Once the RATE[1:0] bits are set, a reset is required to change to a new RATE[1:0].

In Figure 20, the MAP bit of the Transmit Backplane Frame Pulse Configuration register is a logic 0. Therefore, every fourth time slot is unused, starting with timeslot 0. The framing bit is sampled during bit 0 of time slot 0, so that only bits 1 to 7 of time slot 0 are ignored. If MAP is logic 1, the 24 T1 channels would be aligned to the first 24 timeslots with the F-bit located in the last bit of the 32$^{nd}$ timeslot.

The TSOFF[6:0], BOFF_EN and BOFF[2:0] register bits are all logic zero; therefore, BTFP is expected to be aligned to the F-bit position.

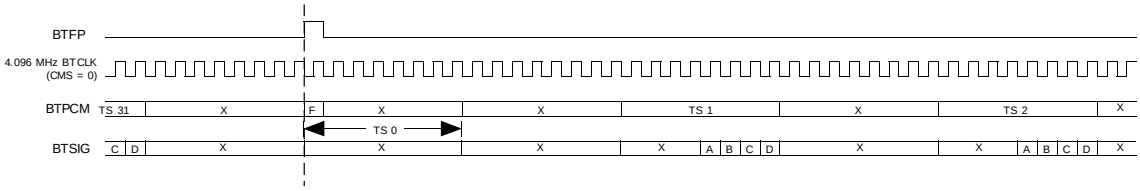
**Figure 21 - Transmit Backplane at 2.048 Mbit/s (E1 mode)**




A 2.048 Mbit/s backplane in E1 mode is configured by setting the RATE[1:0] bits of the Transmit Backplane Configuration register to 'b01 and the E1/T1B bit of the Global Configuration register to a logic 1. In Figure 21, BTFP, BTPCM and BTSIG are configured to be sampled on the rising edge of BTCLK by setting the FE and DE bits of the Transmit Backplane Configuration register to logic 1. Once the RATE[1:0] bits are set, a reset is required to change to a new RATE[1:0].

The TSOFF[6:0], BOFF_EN and BOFF[2:0] register bits are all logic zero; therefore, BTFP is expected to be aligned to the first bit of the frame.

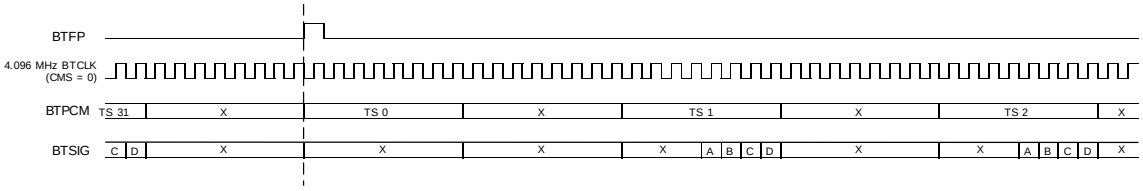
**Figure 22 - Transmit Backplane at 4.096 Mbit/s (T1 mode)**




A 4.096 Mbit/s backplane in T1 mode is configured by setting the RATE[1:0] bits of the Transmit Backplane Configuration register to 'b10 and the E1/T1B bit of the Global Configuration register to a logic 0. In Figure 20, BTFP, BTPCM and BTSIG are configured to be sampled on the rising edge of BTCLK by setting the FE and DE bits of the Transmit Backplane Configuration register to logic 1. TSOFF[6:0] is set to 'b0000000 so that the first of the two interleaved bytes is sampled. Once the RATE[1:0] bits are set, a reset is required to change to a new RATE[1:0].

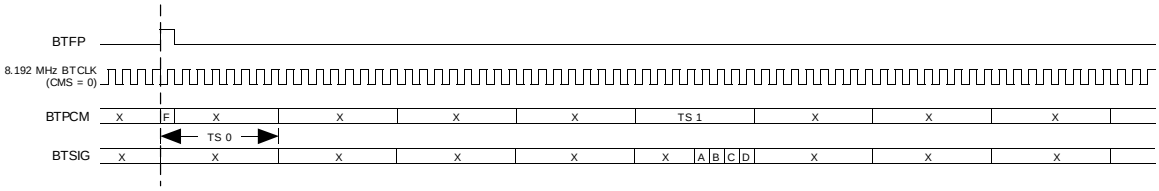
In Figure 20, the MAP bit of the Transmit Backplane Frame Pulse Configuration register is a logic 0. Therefore, every fourth time slot is unused, starting with timeslot 0. The framing bit is sampled during bit 0 of time slot 0, so that only bits 1 to 7 of time slot 0 are ignored. If MAP is logic 1, the 24 T1 channels would be aligned to the first 24 timeslots with the F-bit located in the last bit of the 32$^{nd}$ timeslot.

**Figure 23 - Transmit Backplane at 4.096 Mbit/s (E1 mode)**




A 4.096 Mbit/s backplane in E1 mode is configured by setting the RATE[1:0] bits of the Transmit Backplane Configuration register to 'b10 and the E1/T1B bit of the Global Configuration register to a logic 1. In Figure 23, BTFP, BTPCM and BTSIG are configured to be sampled on the rising edge of BTCLK by setting the FE and DE bits of the Transmit Backplane Configuration register to logic 1. TSOFF[6:0] is set to 'b0000000 so that the first of the two interleaved bytes is sampled.

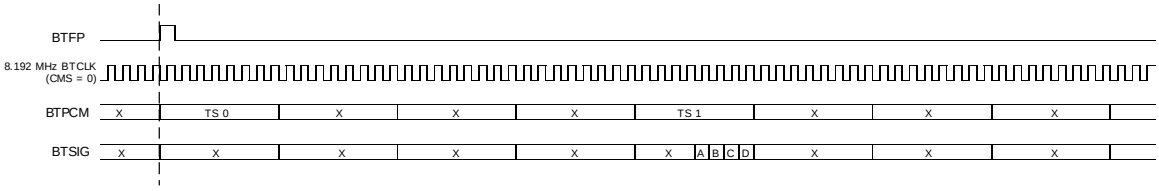
**Figure 24 - Transmit Backplane at 8.192 Mbit/s (T1 mode)**




A 8.192 Mbit/s backplane in T1 mode is configured by setting the RATE[1:0] bits of the Transmit Backplane Configuration register to 'b11 and the E1/T1B bit of the Global Configuration register to a logic 0. In Figure 24, BTFP, BTPCM and BTSIG are configured to be sampled on the rising edge of BTCLK by setting the FE and DE bits of the Transmit Backplane Configuration register to logic 1. TSOFF[6:0] is set to 'b0000000 so that the first of the four interleaved bytes is sampled. Once the RATE[1:0] bits are set, a reset is required to change to a new RATE[1:0].

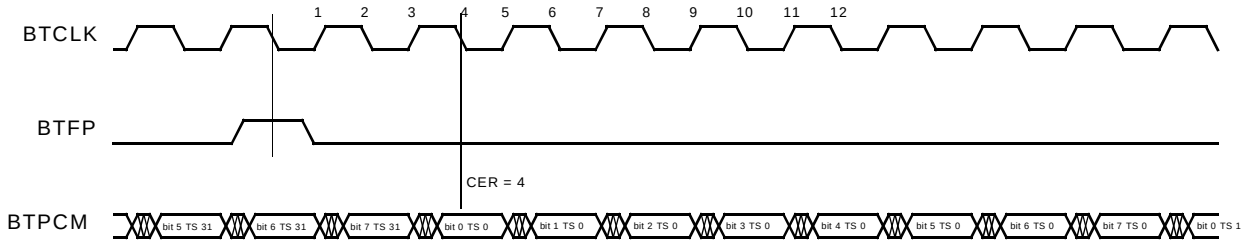
In Figure 24, the MAP bit of the Transmit Backplane Frame Pulse Configuration register is a logic 0. Therefore, every fourth time slot is unused, starting with timeslot 0. The framing bit is sampled during bit 0 of time slot 0, so that only bits 1 to 7 of time slot 0 are ignored. If MAP is logic 1, the 24 T1 channels would be aligned to the first 24 timeslots with the F-bit located in the last bit of the 32$^{nd}$ timeslot.

**Figure 25 - Transmit Backplane at 8.192 Mbit/s (E1 mode)**



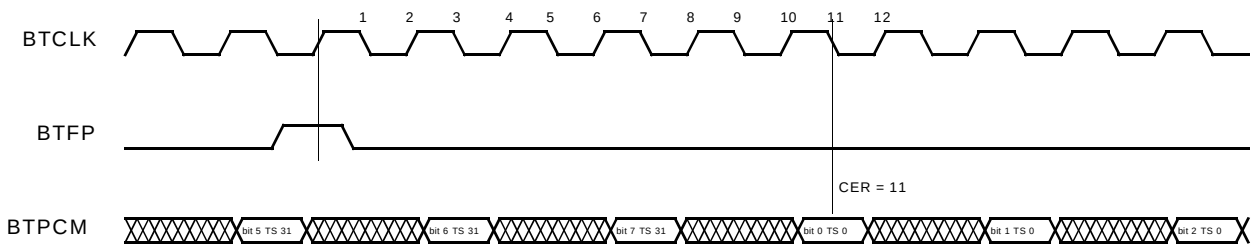

A 8.192 Mbit/s backplane in E1 mode is configured by setting the RATE[1:0] bits of the Transmit Backplane Configuration register to 'b11 and the E1/T1B bit of the Global Configuration register to a logic 1. In Figure 25, BTFP, BTPCM and BTSIG are configured to be sampled on the rising edge of BTCLK by setting the FE and DE bits of the Transmit Backplane Configuration register to logic 1. TSOFF[6:0] is set to 'b0000000 so that the first of the four interleaved bytes is sampled.

**Figure 26 - Concentration Highway Interface Timing, Example 1**




CHI timing is configured by setting the BOFF_EN bit of the Transmit Backplane Bit Offset register to a logic 1. In Figure 26, the DE and FE register bits are set to logic 0 so that BTPCM, BTSIG and BTFP are sampled on the falling edge of BTCLK. CMS is set to logic 0 so that the clock rate is equal to the data rate. BOFF[2:0] is set to 'b000 so that the receive clock edge (CER) is equal to 4 (as determined by the table in the Transmit Backplane Bit Offset register description of BOFF[2:0]) and BTPCM is sampled 4 clock edges after BTFP is sampled. TSOFF is set to 'b0000000 so that there is no time slot offset.

**Figure 27 - Concentration Highway Interface Timing, Example 2**

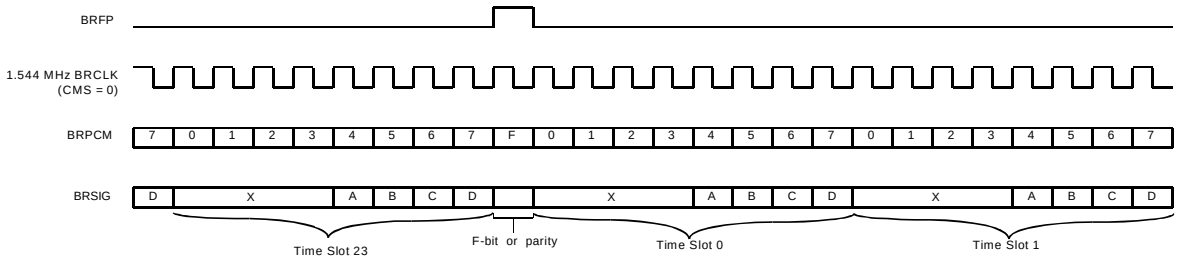


CHI timing is configured by setting the BOFF_EN bit of the Transmit Backplane Bit Offset register to a logic 1. In Figure 27, the FE register bit is set to logic 1 so that BTFP is sampled on the rising edge of BTCLK. The DE register bit is set to logic 0 so that BTPCM is sampled on the falling edge of BTCLK. CMS is set to logic 1 so that the clock rate is equal to two times the data rate. BOFF[2:0] is set to 'b001 so that the receive clock edge (CER) is equal to 11 (as determined by the table in the Transmit Backplane Bit Offset register description of BOFF[2:0]) and BTPCM is sampled 11 clock edges after BTFP is sampled. TSOFF is set to 'b0000000 so that there is no time slot offset.

## 13.2 Receive Backplane Interface

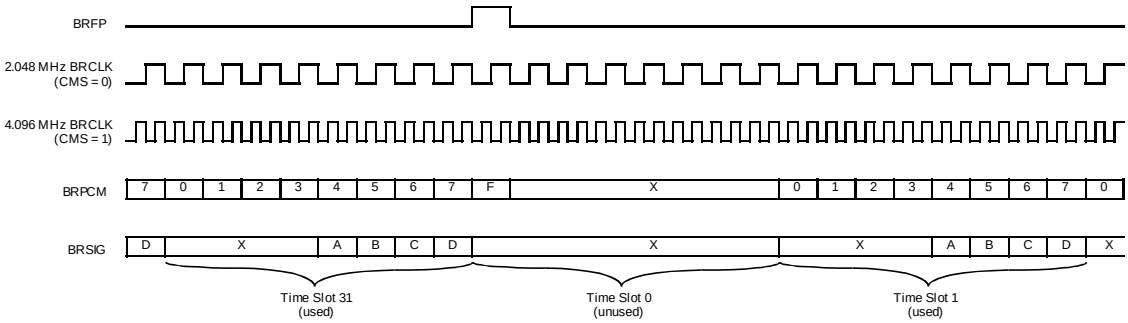
By convention, the first bit transmitted in each timeslot shall be designated bit 0; the last shall be bit 7.

**Figure 28 - Receive Backplane at 1.544 Mbit/s (T1 Mode)**




A 1.544 Mbit/s backplane in T1 mode is configured by setting the RATE[1:0] bits of the Receive Backplane Configuration register to 'b00 and the E1/T1B bit of the Global Configuration register to a logic 0. In Figure 28, BRFP, BRPCM and BRSIG are configured to be sampled on the falling edge of BRCLK by setting the FE and DE bits of the Receive Backplane Configuration register to logic 0. The TSOFF[6:0], BOFF_EN and BOFF[2:0] register bits are all logic zero; therefore, BRFP is aligned to the first bit of the frame. Once the RATE[1:0] bits are set, a reset is required to change to a new RATE[1:0].

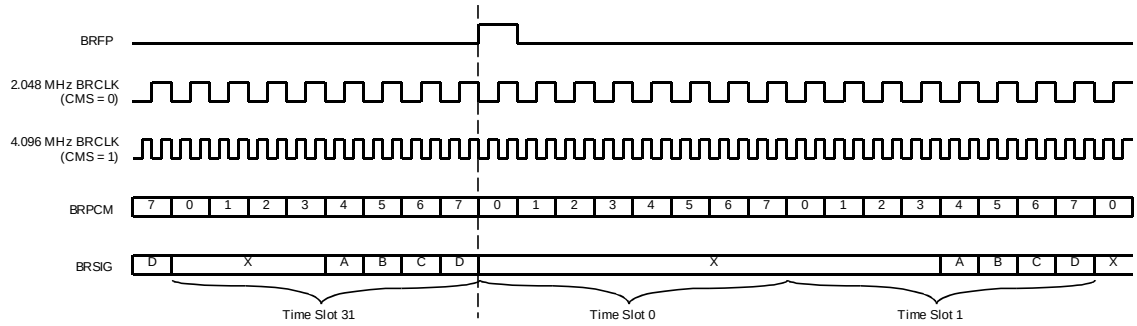
**Figure 29 - Receive Backplane at 2.048 Mbit/s (T1 Mode)**




A 2.048 Mbit/s backplane in T1 mode is configured by setting the RATE[1:0] bits of the Receive Backplane Configuration register to 'b01 and the E1/T1B bit of the Global Configuration register to a logic 0. In Figure 29, BRFP, BRPCM and BRSIG are configured to be updated on the falling edge of BRCLK by setting the FE and DE bits of the Receive Backplane Configuration register to logic 0. Once the RATE[1:0] bits are set, a reset is required to change to a new RATE[1:0].

In Figure 29, the MAP register bit is logic 0. As shown, every fourth time slot is unused, starting with the first. If MAP is a logic 1, time slots 0 through 23 would be used. The framing bit is presented during bit 0 of time slot 0, so that only bits 1 to 7 of time slot 0 are ignored. The TSOFF[6:0], BOFF_EN and BOFF[2:0] register bits are all logic zero; therefore, BRFP is expected to be aligned to the first bit of the frame.

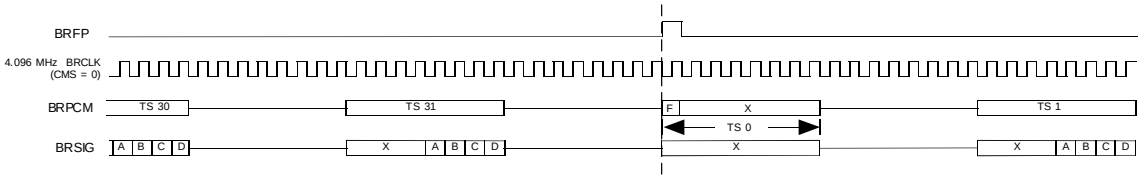
**Figure 30 - Receive Backplane at 2.048 Mbit/s (E1 Mode)**




A 2.048 Mbit/s backplane in E1 mode is configured by setting the RATE[1:0] bits of the Receive Backplane Configuration register to 'b01 and E1/T1B bit of the Global Configuration register to logic 1. In Figure 30, BRFP, BRPCM and BRSIG are configured to be updated on the falling edge of BRCLK by setting the FE and DE bits of the Receive Backplane Configuration register to logic 0. The TSOFF[6:0], BOFF_EN and BOFF[2:0] register bits are all logic zero; therefore,

BRFP is expected to be aligned to the first bit of the frame. Once the RATE[1:0] bits are set, a reset is required to change to a new RATE[1:0].

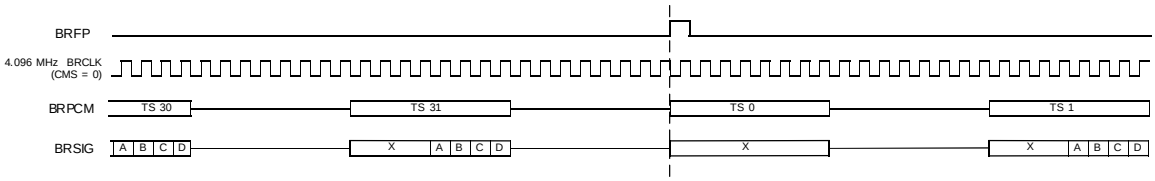
**Figure 31 - Receive Backplane at 4.096 Mbit/s (T1 Mode)**




A 4.096 Mbit/s backplane in T1 mode is configured by setting the RATE[1:0] bits of the Receive Backplane Configuration register to 'b10 and the E1/T1B bit of the Global Configuration register to logic 0. In Figure 31, BRFP, BRPCM and BRSIG are configured to be updated on the falling edge of BRCLK by setting the FE and DE bits of the Receive Backplane Configuration register to logic 0. TSOFF[6:0] is set to 'b0000000 so that the first of the two interleaved bytes is sampled. Once the RATE[1:0] bits are set, a reset is required to change to a new RATE[1:0].

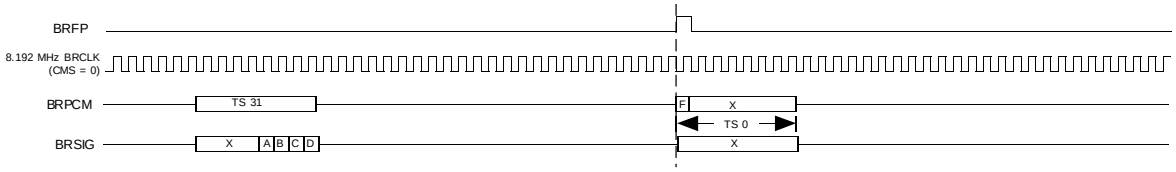
In Figure 31, the MAP register bit is logic 0. As shown, every fourth time slot is unused, starting with the first. If MAP is a logic 1, time slots 0 through 23 would be used. The framing bit is presented during bit 0 of time slot 0, so that only bits 1 to 7 of time slot 0 are ignored. The TSOFF[6:0], BOFF_EN and BOFF[2:0] register bits are all logic zero; therefore, BRFP is expected to be aligned to the first bit of the frame.

**Figure 32 - Receive Backplane at 4.096 Mbit/s (E1 Mode)**




A 4.096 Mbit/s backplane in E1 mode is configured by setting the RATE[1:0] bits of the Receive Backplane Configuration register to 'b10 and the E1/T1B bit of the Global Configuration register to logic 1. In Figure 32, BRFP, BRPCM and BRSIG are configured to be updated on the falling edge of BRCLK by setting the FE and DE bits of the Receive Backplane Configuration register to logic 0. TSOFF[6:0] is set to 'b0000000 so that the first of the two interleaved bytes is sampled. Once the RATE[1:0] bits are set, a reset is required to change to a new RATE[1:0].

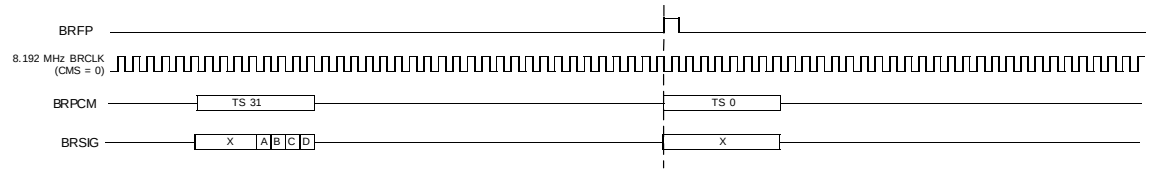
**Figure 33 - Receive Backplane at 8.192 Mbit/s (T1 Mode)**




A 8.192 Mbit/s backplane in T1 mode by setting the RATE[1:0] bits of the Receive Backplane Configuration register to 'b11 and the E1/T1B bit of the Global Configuration register to a logic 0. In Figure 24, BRFP, BRPCM and BRSIG are configured to be updated on the falling edge of BRCLK by setting the FE and DE bits of the Receive Backplane Configuration register to logic 0. TSOFF[6:0] is set to 'b0000000 so that the first of the four interleaved bytes is sampled. Once the RATE[1:0] bits are set, a reset is required to change to a new RATE[1:0].

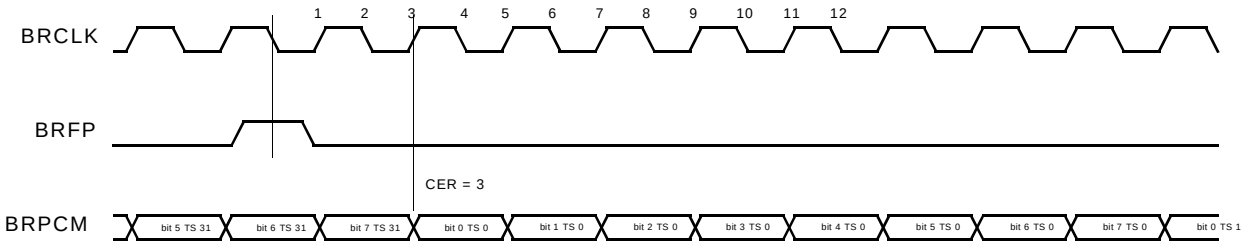
In Figure 24, the MAP register bit is logic 0. As shown, every fourth time slot is unused, starting with the first. If MAP is a logic 1, time slots 0 through 23 would be used. The framing bit is presented during bit 0 of time slot 0, so that only bits 1 to 7 of time slot 0 are ignored. The TSOFF[6:0], BOFF_EN and BOFF[2:0] register bits are all logic zero; therefore, BRFP is expected to be aligned to the first bit of the frame.

**Figure 34 - Receive Backplane at 8.192 Mbit/s (E1 Mode)**



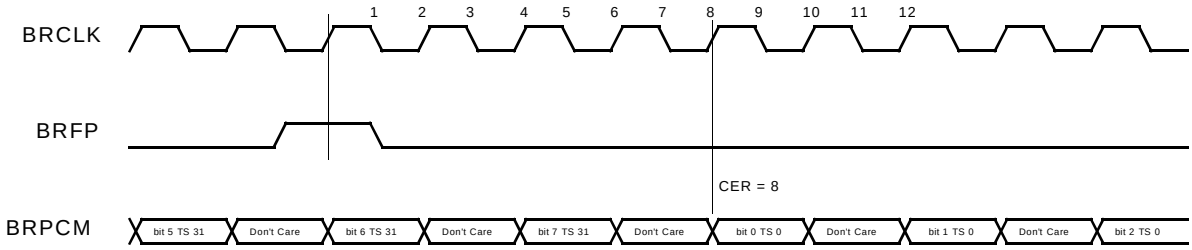

A 8.192 Mbit/s backplane in E1 mode by setting the RATE[1:0] bits of the Receive Backplane Configuration register to 'b11 and the E1/T1B bit of the Global Configuration register to a logic 1. In Figure 34, BRFP, BRPCM and BRSIG are configured to be updated on the falling edge of BRCLK by setting the FE and DE bits of the Receive Backplane Configuration register to logic 0. TSOFF[6:0] is set to 'b0000000 so that the first of the four interleaved bytes is sampled.

**Figure 35 - Concentration Highway Interface Timing, Example 1**




CHI timing is configured by setting the BOFF_EN bit of the Receive Backplane Configuration register to a logic 1. In Figure 35, FE is set to logic 0 so that BRFP is sampled on the falling edge of BRCLK. DE is set to logic 1 so that BRPCM is updated on the rising edge of BRCLK. CMS is set to logic 0 so that the clock rate is equal to the data rate. BOFF[2:0] is set to 'b000 so that the transmit clock edge (CET) is equal to 3 (as determined by the table in the register description of BOFF[2:0]) and BRPCM is updated 3 clock edges after BRFP is sampled. TSOFF is set to 'b0000000 so that there is no time slot offset.

**Figure 36 - Concentration Highway Interface Timing, Example 2**




CHI timing is configured by setting BOFF_EN to a logic 1. In Figure 36, FE is set to logic 1 so that BRFP is sampled on the rising edge of BRCLK. DE is set to logic 1 so that BRPCM is updated on the rising edge of BRCLK. CMS is set to logic 1 so that the clock rate is equal to two times the data rate. BOFF[2:0] is set to 'b001 so that the transmit clock edge (CET) is equal to 8 (as determined by the table in the register description of BOFF[2:0]) and BRPCM is updated 8 clock edges after BRFP is updated. TSOFF is set to 'b0000000 so that there is no time slot offset.

# 14 OPERATION

## 14.1 Configuring the COMET from Reset

After a system reset (either via the RSTB pin or via the RESET register bit), the COMET will default to the following settings:

**Table 76 - Default Settings**

| Setting | Receiver Section | Transmitter Section |
|---|---|---|
| Framing Format | T1 SF | T1 SF |
| Line Code | B8ZS | AMI |
| Line interface | Pins RXTIP and RXRING active short haul analog inputs | TXTIP[1:0], TXRING[1:0], TCLKO, TDAT and TFP held low |
| System Backplane | • 1.544 Mbit/s data rate<br>• BRPCM, BRSIG high impedance<br>• BRFP and BRCLK configured as inputs | • 1.544 Mbit/s data rate<br>• BTPCM active<br>• BTSIG inactive<br>• BTFP and BTCLK configured as inputs |
| Data Link | disabled | disabled |
| Options | • RX-ELST not bypassed<br>• PMON accumulates OOFs (not COFAs) | • TX-ELST bypassed<br>• Signaling alignment disabled<br>• F, CRC, FDL bit bypass disabled |
| Timing Options | Not applicable | Jitter attenuation enabled, with TCLKO referenced to BTCLK |
| Diagnostics | All diagnostic modes disabled | All diagnostic modes disabled |

To configure the COMET for ESF framing format, after a reset, the following registers should be written with the indicated values:

**Table 77 - ESF Frame Format**

| Action | Addr | Data | Effect |
|---|---|---|---|
| Write CDRC Configuration Register | 10H | 00H | Select B8ZS line code for receiver |
| Write RX-ELST Configuration Register | 1CH | 00H | Select 193-bit frame format. |
| Write TX-ELST Configuration Register | 20H | 00H | Select 193-bit frame format. |
| Write T1 XBAS Configuration Register | 54H | 3XH | Select B8ZS, enable for ESF in transmitter (bits defined by 'X' determine the FDL data rate & Zero Code suppression algorithm used) |
| Write T1 FRMR Configuration Register | 48H | 1XH or<br>5XH or<br>9XH | Select ESF, 2 of 4 OOF threshold<br>Select ESF, 2 of 5 OOF threshold<br>Select ESF, 2 of 6 OOF threshold<br>(bits defined by 'X' determine the FDL data rate, should be same as those written to XBAS) |
| Write RBOC Enable Register | 6AH | 00H or 02H | Enable 8 out of 10 validation<br>Enable 4 out of 5 validation |
| Write ALMI Configuration Register | 60H | 1XH | Select ESF (bits defined by 'X' determine the ESF Yellow data rate, should be same as those written to T1 FRMR) |
| Write IBCD Configuration Register | 4CH | 00H | Enable Inband Code detection |
| Write IBCD Activate Code Register | 4EH | 08H | Program Loopback Activate Code pattern |
| Write IBCD Deactivate Code Register | 4FH | 44H | Program Loopback Deactivate Code pattern |
| Write SIGX Configuration Register | 50H | 04H | Select ESF |

To configure the COMET for SLC®96 framing format, after a reset, the following registers should be written with the indicated values:

**Table 78 - SLC®96 Frame Format**

| Action | Addr | Data | Effect |
|---|---|---|---|
| Write CDRC Configuration Register | 10H | 80H | Select AMI line code for receiver |
| Write RX -ELST Configuration Register | 1CH | 00H | Select 193-bit frame format. |
| Write TX-ELST Configuration Register | 20H | 00H | Select 193-bit frame format. |
| Write T1 XBAS Configuration Register | 54H | 08H | Select AMI, enable for SLC®96 in transmitter |
| Write T1 FRMR Configuration Register | 48H | 08H<br>or<br>48H<br>or<br>88H | Select SLC®96, 2 of 4 OOF threshold<br>Select SLC®96, 2 of 5 OOF threshold<br>Select SLC®96, 2 of 6 OOF threshold |
| Write ALMI Configuration Register | 60H | 08H | Select SLC®96 |
| Write IBCD Configuration Register | 4CH | 00H | Enable Inband Code detection |
| Write IBCD Activate Code Register | 4EH | 08H | Program Loopback Activate Code pattern |
| Write IBCD Deactivate Code Register | 4FH | 44H | Program Loopback Deactivate Code pattern |
| Write SIGX Configuration Register | 50H | 00H | Select SLC®96 |

To configure the COMET for SF framing format, after a reset, the following registers should be written with the indicated values:

**Table 79 - SF Frame Format**

| Action | Addr | Data | Effect |
|---|---|---|---|
| Write CDRC Configuration Register | 10H | 80H | Select AMI line code for receiver |
| Write RX-ELST Configuration Register | 1CH | 00H | Select 193-bit frame format. |
| Write TX-ELST Configuration Register | 20H | 00H | Select 193-bit frame format. |
| Write T1 XBAS Configuration Register | 54H | 00H | Select AMI, enable for SF in transmitter |
| Write T1 FRMR Configuration Register | 48H | 00H or<br>40H or<br>80H | Select SF, 2 of 4 OOF threshold<br>Select SF, 2 of 5 OOF threshold<br>Select SF, 2 of 6 OOF threshold |
| Write ALMI Configuration Register | 60H | 00H | Select SF |
| Write IBCD Configuration Register | 4CH | 00H | Enable Inband Code detection |
| Write IBCD Activate Code Register | 4EH | 08H | Program Loopback Activate Code pattern |
| Write IBCD Deactivate Code Register | 4FH | 44H | Program Loopback Deactivate Code pattern |
| Write SIGX Configuration Register | 50H | 00H | Select SF |

To configure the COMET for T1DM framing format, after a reset, the following registers should be written with the indicated values:

**Table 80 - T1DM Frame Format**

| Action | Addr | Data | Effect |
|---|---|---|---|
| Write CDRC Configuration Register | 10H | 80H | Select AMI line code for receiver |

| Action | Addr | Data | Effect |
|---|---|---|---|
| Write RX-ELST Configuration Register | 1CH | 00H | Select 193-bit frame format. |
| Write TX-ELST Configuration Register | 20H | 00H | Select 193-bit frame format. |
| Write T1 XBAS Configuration Register | 54H | 04H or 0CH | Select AMI, enable for T1DM in transmitter |
| Write T1 FRMR Configuration Register | 48H | 04H | Select T1DM, 4 of 12 OOF threshold |
| Write ALMI Configuration Register | 60H | 04H or<br>0CH | Select T1DM with standard Red integration<br>Select T1DM with alternate Red integration |
| Write IBCD Configuration Register | 4CH | 00H | Enable Inband Code detection |
| Write IBCD Activate Code Register | 4EH | 08H | Program Loopback Activate Code pattern |
| Write IBCD Deactivate Code Register | 4FH | 44H | Program Loopback Deactivate Code pattern |
| Write SIGX Configuration Register | 50H | 00H | Select T1DM |

**Table 81 - E1 Frame Format**

| Action | Addr | Data | Effect |
|---|---|---|---|
| Write Global Configuration Register | 00H | 01H | Select E1 mode. |
| Write RXCE Receive Data Link 1 Control Register | 028H | 00H | Disable extraction of T1 data link for HDLC receiver #1. |
| Write TXCI Transmit Data Link 1 Control Register | 038H | 00H | Disable insertion of T1 data link from HDLC transmitter #1. |
| Write E1 TRAN Configuration Register | 80H | 70H | Enable CRC multiframe generation |
| Write E1 FRMR Frame Alignment Options Register | 90H | 80H | Enable CRC multiframe search algorithm |

To access the Performance Monitor Registers, the following polling sequence should be used:

**Table 82 - PMON Polling Sequence**

| Action | Addr Offset | Data | Effect |
|---|---|---|---|
| Write PMON Framing Bit Error Count Register | 59H | 00H | Latch performance data into PMON registers |
| Read Framing Bit Error Count | 59H | | Read Framing bit error count |
| Read OOF/COFA/FEBE (LSB) Count Register | 5AH | | Read least significant byte out-of-frame event count, change of frame alignment event count if CCOFA bit in COMET Receive Options Register is set, or FEBE if E1 |
| Read OOF/COFA/FEBE (MSB) Count Register | 5BH | | Read most significant byte out-of-frame event count, change of frame alignment event count if CCOFA bit in COMET Receive Options Register is set, or FEBE if E1 |
| Read BEE/CRCE Count (LSB) Register | 5CH | | Read least significant byte of bit error event or CRC error count |
| Read BEE/CRCE Count (MSB) Register | 5DH | | Read most significant byte of bit error event or CRC error count |
| Read LCV Count (LSB) Register | 5EH | | Read least significant byte of line code violation count |
| Read LCV Count (MSB) Register | 5FH | | Read most significant byte of line code violation count |

To configure the COMET to utilize the internal HDLC transmitter and receiver for processing the ESF facility data link, the following registers should be written with the indicated values:

**Table 83 - ESF FDL Processing**

| Action | Addr | Data | Effect |
|---|---|---|---|
| Write RXCE Receive Data Link 1 Control Register | 028H | 20H | Select extraction of ESF Facility Data Link for HDLC receiver #1. (COMET must be set up for ESF frame format.) |
| Write TXCI Transmit Data Link 1 Control Register | 038H | 20H | Select insertion of ESF Facility Data Link from HDLC transmitter #1. (COMET must be set up for ESF frame format.) |

## 14.2 Using the Internal HDLC Transmitters

It is important to note that the access rate to the TDPR registers is limited by the rate of the transmit clock. The TDPR registers should be accessed at a rate no faster than that of the transmit system clock.

To properly initialize the transmit HDLC controllers in transmit basic frame alignment mode (FPTYP is logic 0), transmit multiframe alignment (FPTYP is logic 1) must be configured for at least one multiframe (i.e., for at least one multiframe period in frame pulse master mode or for at least one input frame pulse in frame pulse slave mode). After this initialization, the FPTYP can be set to any desired value.

Upon reset, the TDPR should be disabled by setting the EN bit in the TDPR Configuration Register to logic 0 (default value). After making all initial configurations to the TDPR, the EN bit should be set to logic 1 to enable the TDPR and then the FIFOCLR bit should be set and then cleared to initialize the TDPR FIFO. The TDPR is now ready to transmit.

To initialize the TDPR, the TDPR Configuration Register must be properly set. If FCS generation is desired, the CRC bit should be set to logic 1. If the block is to be used in interrupt driven mode, then interrupts should be enabled by setting the FULLE, OVRE, UDRE, and LFILLE bits in the TDPR Interrupt Enable register to logic 1. The TDPR operating parameters in the TDPR Upper Transmit Threshold and TDPR Lower Interrupt Threshold registers should be set to the desired values. The TDPR Upper Transmit Threshold sets the value at which the TDPR automatically begins the transmission of HDLC packets, even if no complete packets are in the FIFO. Transmission will continue until the current packet is transmitted and the number of bytes in the TDPR FIFO falls to, or below, this threshold level. The TDPR will always transmit all complete HDLC

packets (packets with EOM attached) in its FIFO. Finally, the TDPR can be enabled by setting the EN bit to logic 1. If no message is sent after the EN bit is set to logic 1, continuous flags will be sent.

The TDPR can be used in a polled or interrupt driven mode for the transfer of packet data. In the polled mode the processor controlling the TDPR must periodically read the TDPR Interrupt Status register to determine when to write to the TDPR Transmit Data register. In the interrupt driven mode, the processor controlling the TDPR uses the INTB output to identify the interrupts which determine when writes can or must be done to the TDPR Transmit Data register.

### 14.2.1 Automatic transmission mode using interrupts:

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold. The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 1 so an interrupt on INTB is generated upon detection of a FIFO full state, a FIFO depth below the lower limit threshold, a FIFO overrun, or a FIFO underrun. The following procedure should be followed to transmit HDLC packets:

1. Wait for data to be transmitted. Once data is available to be transmitted, go to step 2.

2. Write the data byte to the TDPR Transmit Data register.

3. If all bytes in the packet have been sent, set the EOM bit in the TDPR Configuration register to logic 1. Go to step 1.

4. If there are more bytes in the packet to be sent, go to step 2.

While performing steps 1 to 4, the processor should monitor for interrupts generated by the TDPR. When an interrupt is detected, the TDPR Interrupt Routine should be executed.

The TDPR will force transmission of the packet information when the FIFO depth exceeds the threshold programmed with the UTHR[6:0] bits in the TDPR Upper Transmit Threshold register. Transmission will not stop until the last byte of all complete packets is transmitted and the FIFO depth is at or below the threshold limit. The user should watch the FULLI and LFILLI interrupts to prevent overruns and underruns.

### 14.2.2 TDPR Interrupt Routine:

The following procedure should be carried out when an interrupt is detected on INT:

1. Read the TDPR Interrupt Status register.

2. If UDRI=1, then the FIFO has underrun and the last packet transmitted has been corrupted and needs to be retransmitted. When the UDRI bit transitions to logic 1, one Abort sequence and continuous flags will be transmitted. The TDPR FIFO is held in reset state. To re-enable the TDPR FIFO and to clear the underrun, the TDPR Interrupt Status/UDR Clear register should be written with any value.

3. If OVRI=1, then the FIFO has overflowed. The packet which the last byte written into the FIFO belongs to has been corrupted and must be retransmitted. Other packets in the FIFO are not affected. Either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

   If the FIFO overflows on the packet currently being transmitted (packet is greater than 128 bytes long), an Abort signal is scheduled to be transmitted, the FIFO is emptied, and then flags are continuously sent until there is data to be transmitted. The FIFO is held in reset until a write to the TDPR Transmit Data register occurs. This write contains the first byte of the next packet to be transmitted.

4. If OVRI=1, then the FIFO has overflowed. The packet which the last byte written into the FIFO belongs to has been corrupted and must be retransmitted. Other packets in the FIFO are not affected. When an overflow occurs, the OVR output signal is set. Either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit. The OVR output signal remains set until the next write to the TDPR Transmit Data register. This write contains the first byte of the next packet to be transmitted.

   If the FIFO overflows on the packet currently being transmitted (packet is greater than 128 bytes long), the OVR output signal is set, an Abort signal is scheduled to be transmitted, the FIFO is emptied, and then flags are continuously sent until there is data to be transmitted. The FIFO is held in reset until a write to the TDPR Transmit Data register occurs. This write contains the first byte of the next packet to be transmitted.

5. If FULLI=1 and FULL=1, then the TDPR FIFO is full and no further bytes can be written. When in this state, either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

   If FULLI=1 and FULL=0, then the TDPR FIFO had reached the FULL state earlier, but has since emptied out some of its data bytes and now has space available in its FIFO for more data.

6. If LFILLI=1 and BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. If there is more data to transmit, then it should be written to the TDPR Transmit Data register before an underrun occurs. If there is no more data to transmit, then an EOM should be set at the end of the last packet byte. Flags will then be transmitted once the last packet has been transmitted.

   If LFILLI=1 and BLFILL=0, then the TDPR FIFO had fallen below the lower-threshold state earlier, but has since been refilled to a level above the lower-threshold level.

### 14.2.3 Automatic transmission mode using polling:

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold. The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 0 since packet transmission is set to work with a periodic polling procedure. The following procedure should be followed to transmit HDLC packets:

1. Wait until data is available to be transmitted, then go to step 2.

2. Read the TDPR Interrupt Status register.

3. If FULL=1, the TDPR FIFO is full and no further bytes can be written. Continue polling the TDPR Interrupt Status register until either FULL=0 or BLFILL=1. Then, go to either step 4 or 5 depending on implementation preference.

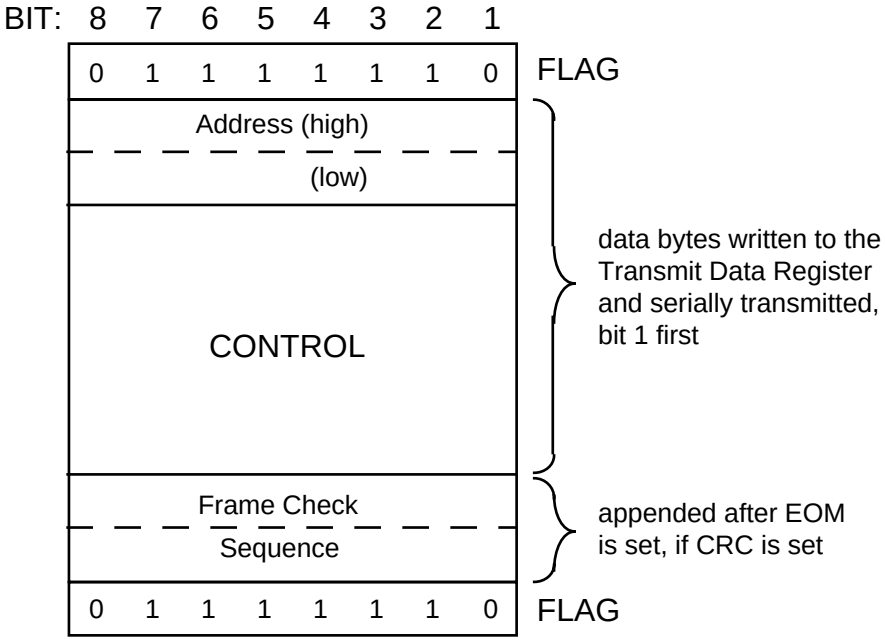
4. If BLFILL=1, the TDPR FIFO depth is below its lower threshold limit. Write the data into the TDPR Transmit Data register. Go to step 6.

5. If FULL=0, the TDPR FIFO has room for at least 1 more byte to be written. Write the data into the TDPR Transmit Data register. Go to step 6.

6. If more data bytes are to be transmitted in the packet, go to step 2.

7. If all bytes in the packet have been sent, set the EOM bit in the TDPR Configuration register to logic 1. Go to step 1.

**Figure 37 - Typical Data Frame**




## 14.3 Using the Internal HDLC Receivers

On power up of the system, the RDLC should be disabled by setting the EN bit in the Configuration Register to logic 0. The Interrupt Control Register should then be initialized to enable the INTB output and to select the FIFO buffer fill level at which an interrupt will be generated. If the INTE bit is not set to logic 1, the Status Register must be continuously polled to check the interrupt status (INTR) bit.

After the Interrupt Control Register has been written, the RDLC can be enabled at any time by setting the EN bit in the Configuration Register to logic 1. When the RDLC is enabled, it will assume the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated, and a dummy byte will be written into the FIFO buffer. This is done to provide alignment of link up status with the data read from the FIFO.

When an abort character is received, another dummy byte and link down status is written into the FIFO. This is done to provide alignment of link down status with the data read from the FIFO. It is up to the controlling processor to check the COLS Status Register bit for a change in the link status. If the COLS Status Register bit is set to logic 1, the FIFO must be emptied to determine the current link status. The first flag and abort status encoded in the PBS bits is used to set and clear a Link Active software flag.

When the last byte of a properly terminated packet is received, an interrupt is generated. When the Status Register is read the PKIN bit will be logic 1. This can be a signal to the external processor to empty the bytes remaining in the FIFO or to just increment a number-of-packets-received count and wait for the FIFO to fill to a programmable level. Once the Status Register is read, the PKIN bit is cleared to logic 0 . If the Status Register is read immediately after the last packet byte is read from the FIFO, the PBS[2] bit will be logic 1 and the CRC and non-integer byte status can be checked by reading the PBS[1:0] bits.

When the FIFO fill level is exceeded, an interrupt is generated. The FIFO must be emptied to remove this source of interrupt.

The RDLC can be used in a polled or interrupt driven, or DMA-controlled mode for the transfer of frame data. In the polled mode, the INTB output is not used, and the processor controlling the RDLC must periodically read the Status Register of the RDLC to determine when to read the Data Register. In the interrupt driven mode, the processor controlling the RDLC uses the INTB output to determine when to read the Data Register.

In the case of interrupt driven data transfer from the RDLC to the processor, the INTB output of the RDLC is connected to the interrupt input of the processor. Once the processor has determined the RDLC is the source of the interrupt, the interrupt service routine should process the data in the following order:

1. RDLC Status Register Read. If INTR=1 then proceed to step 2 else find the interrupt source elsewhere.

2. If OVR = 1, discard last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

3. If COLS = 1, set the EMPTY FIFO software flag.

4. If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will be delayed until the FIFO fill level is exceeded.

5. Data Register Read.

6. Status Register Read.

7. If OVR = 1, discard last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

8. If COLS = 1, set the EMPTY FIFO software flag.

9. If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will be delayed until the FIFO fill level is exceeded.

10. Start the processing of FIFO data. Use the PBS[2:0] packet byte status bits to decide what is to be done with the FIFO data.

    a) If PBS[2:0] = 001, discard data byte read in step 5 and set the LINK ACTIVE software flag.

    b) If PBS[2:0] = 010, discard the data byte read in step 5 and clear the LINK ACTIVE software flag.

    c) If PBS[2:0] = 1XX, store the last byte of the packet, decrement the PACKET COUNT, and check the PBS[1:0] bits for CRC or NVB errors before deciding whether or not to keep the packet.

    d) If PBS[2:0] = 000, store the packet data.

11. If FE = 0 and INTR = 1 or FE = 0 and EMPTY FIFO = 1, go to step 5 else clear the EMPTY FIFO software flag and leave this interrupt service routine to wait for the next interrupt.

The link state is typically a local software variable. The link state is inactive if the RDLC is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RDLC is receiving flags or data.

If the RDLC data transfer is operating in the polled mode, processor operation is exactly as shown above for the interrupt driven mode, except that the entry to the service routine is from a timer, rather than an interrupt.

## 14.4 T1 Automatic Performance Report Format

**Table 84 - Performance Report Message Structure and Contents**

| Octet No. | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 |
|---|---|---|---|---|---|---|---|---|
| 1 | FLAG | | | | | | | |
| 2 | SAPI | | | | | | C/R | EA |
| 3 | TEI | | | | | | | EA |
| 4 | CONTROL | | | | | | | |
| 5 | G3 | LV | G4 | U1 | U2 | G5 | SL | G6 |
| 6 | FE | SE | LB | G1 | R | G2 | Nm | NI |
| 7 | G3 | LV | G4 | U1 | U2 | G5 | SL | G6 |
| 8 | FE | SE | LB | G1 | R | G2 | Nm | NI |
| 9 | G3 | LV | G4 | U1 | U2 | G5 | SL | G6 |
| 10 | FE | SE | LB | G1 | R | G2 | Nm | NI |
| 11 | G3 | LV | G4 | U1 | U2 | G5 | SL | G6 |
| 12 | FE | SE | LB | G1 | R | G2 | Nm | NI |
| 13 | FCS | | | | | | | |
| 14 | FCS | | | | | | | |
| 15 | FLAG | | | | | | | |

**Notes:**

1. The order of transmission of the bits is LSB (Bit 1) to MSB (Bit 8).

**Table 85 - Performance Report Message Structure Notes**

| Octet No. | Octet Contents | Interpretation |
|---|---|---|
| 1 | 01111110 | Opening LAPD Flag |
| 2 | 00111000<br>00111010 | From CI: SAPI=14, C/R=0, EA=0<br>From carrier: SAPI=14,C/R=1,EA=0 |
| 3 | 00000001 | TEI=0,EA=1 |
| 4 | 00000011 | Unacknowledged Frame |
| 5,6 | Variable | Data for latest second (T') |
| 7,8 | Variable | Data for Previous Second(T'-1) |

| Octet No. | Octet Contents | Interpretation |
|---|---|---|
| 9,10 | Variable | Data for earlier Second(T'-2) |
| 11,12 | Variable | Data for earlier Second(T'-3) |
| 13,14 | Variable | CRC16 Frame Check Sequence |
| 15 | 01111110 | Closing LAPD flag |

**Table 86 - Performance Report Message Contents**

| Bit Value | Interpretation |
|---|---|
| G1=1 | CRC ERROR EVENT =1 |
| G2=1 | 1<CRC ERROR EVENT ≤5 |
| G3=1 | 5<CRC ERROR EVENT ≤10 |
| G4=1 | 10<CRC ERROR EVENT ≤100 |
| G5=1 | 100<CRC ERROR EVENT ≤319 |
| G6=1 | CRC ERROR EVENT ≥ 320 |
| SE=1 | Severely Errored Framing Event ≥ 1(FE shall =0) |
| FE=1 | Frame Synchronization Bit Error Event ≥1 (SE shall=0 ) |
| LV=1 | Line code violation event ≥1 |
| SL=1 | Slip Event ≥ 1 |
| LB=1 | Payload Loopback Activated |
| U1,U2=0 | Under Study For Synchronization. |
| R=0 | Reserved ( Default Value =0) |
| NmNI=00,01,10, 11 | One second Report Modulo 4 Counter |

## 14.5 Using the Transmit Line Pulse Generator

The internal D/A pulse waveform template registers, accessible via the microprocessor bus, can be used to create a custom waveform. These 120 pulse waveform storage registers are accessed indirectly through XLPG Pulse Waveform Storage Write Address and XLPG Pulse Waveform Storage Data register. The values written into the pulse waveform storage registers correspond to one of 127 quantized levels. 24 samples are output during every transmit clock cycle.

The waveform being programmed is completely arbitrary and programming must be done properly in order to meet the various T1 and E1 template specifications. The SCALE[4:0] bits of Line Driver Configuration Register bits are used to obtain a proper output amplitude. It must also be noted that since samples from the 5 UI are added before driving the DAC, it is possible to create arithmetic overflows. The XLPG detects overflows and saturates the resulting value to -62 or +62 as appropriate. However, it is recommended that the pulse amplitude be programmed such that overflows are avoided. It is possible to verify if an overflow condition occurred by reading the OVRFLV register bit after programming a new waveform and transmission of data.

The following tables contain the waveform values to be programmed for different situations. Table 87 to Table 96 specify waveform values typically used for T1 long haul and short haul transmission. Table 97 to Table 103 specify waveform values for compliance to the AT&T TR62411 ACCUNET T1.5 pulse template. This is particularly useful where compliance to the jitter specification of TR62411 is desired. Table 104 and Table 105 specify waveform values for E1 transmission.

**Table 87 - Transmit Waveform Values for T1 Long Haul (LBO 0 dB):**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 44 | 00 | 00 | 00 |
| 2 | 0A | 44 | 00 | 00 | 00 |
| 3 | 20 | 43 | 00 | 00 | 00 |
| 4 | 32 | 43 | 00 | 00 | 00 |
| 5 | 3E | 42 | 00 | 00 | 00 |
| 6 | 3D | 42 | 00 | 00 | 00 |
| 7 | 3C | 41 | 00 | 00 | 00 |
| 8 | 3B | 41 | 00 | 00 | 00 |
| 9 | 3A | 00 | 00 | 00 | 00 |
| 10 | 39 | 00 | 00 | 00 | 00 |
| 11 | 39 | 00 | 00 | 00 | 00 |
| 12 | 38 | 00 | 00 | 00 | 00 |
| 13 | 37 | 00 | 00 | 00 | 00 |
| 14 | 36 | 00 | 00 | 00 | 00 |
| 15 | 34 | 00 | 00 | 00 | 00 |

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 16 | 29 | 00 | 00 | 00 | 00 |
| 17 | 4F | 00 | 00 | 00 | 00 |
| 18 | 4C | 00 | 00 | 00 | 00 |
| 19 | 4A | 00 | 00 | 00 | 00 |
| 20 | 49 | 00 | 00 | 00 | 00 |
| 21 | 47 | 00 | 00 | 00 | 00 |
| 22 | 47 | 00 | 00 | 00 | 00 |
| 23 | 46 | 00 | 00 | 00 | 00 |
| 24 | 46 | 00 | 00 | 00 | 00 |

Note: SCALE[4:0] programmed to 0CH.

**Table 88 - Transmit Waveform Values for T1 Long Haul (LBO 7.5 dB):**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 10 | 00 | 00 | 00 |
| 2 | 01 | 0E | 00 | 00 | 00 |
| 3 | 02 | 0C | 00 | 00 | 00 |
| 4 | 04 | 0A | 00 | 00 | 00 |
| 5 | 08 | 08 | 00 | 00 | 00 |
| 6 | 0C | 06 | 00 | 00 | 00 |
| 7 | 10 | 04 | 00 | 00 | 00 |
| 8 | 16 | 02 | 00 | 00 | 00 |
| 9 | 1A | 01 | 00 | 00 | 00 |
| 10 | 1E | 00 | 00 | 00 | 00 |
| 11 | 22 | 00 | 00 | 00 | 00 |
| 12 | 26 | 00 | 00 | 00 | 00 |
| 13 | 2A | 00 | 00 | 00 | 00 |
| 14 | 2B | 00 | 00 | 00 | 00 |
| 15 | 2C | 00 | 00 | 00 | 00 |
| 16 | 2D | 00 | 00 | 00 | 00 |

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 17 | 2C | 00 | 00 | 00 | 00 |
| 18 | 28 | 00 | 00 | 00 | 00 |
| 19 | 24 | 00 | 00 | 00 | 00 |
| 20 | 20 | 00 | 00 | 00 | 00 |
| 21 | 1C | 00 | 00 | 00 | 00 |
| 22 | 18 | 00 | 00 | 00 | 00 |
| 23 | 14 | 00 | 00 | 00 | 00 |
| 24 | 12 | 00 | 00 | 00 | 00 |

Note: SCALE[4:0] programmed to 07H.

**Table 89 - Transmit Waveform Values for T1 Long Haul (LBO 15 dB):**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 2A | 09 | 01 | 00 |
| 2 | 00 | 28 | 08 | 01 | 00 |
| 3 | 00 | 26 | 08 | 01 | 00 |
| 4 | 00 | 24 | 07 | 01 | 00 |
| 5 | 01 | 22 | 07 | 01 | 00 |
| 6 | 02 | 20 | 06 | 01 | 00 |
| 7 | 04 | 1E | 06 | 01 | 00 |
| 8 | 07 | 1C | 05 | 00 | 00 |
| 9 | 0A | 1B | 05 | 00 | 00 |
| 10 | 0D | 19 | 05 | 00 | 00 |
| 11 | 10 | 18 | 04 | 00 | 00 |
| 12 | 14 | 16 | 04 | 00 | 00 |
| 13 | 18 | 15 | 04 | 00 | 00 |
| 14 | 1B | 13 | 03 | 00 | 00 |
| 15 | 1E | 12 | 03 | 00 | 00 |
| 16 | 21 | 10 | 03 | 00 | 00 |
| 17 | 24 | 0F | 03 | 00 | 00 |

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 18 | 27 | 0D | 03 | 00 | 00 |
| 19 | 2A | 0D | 02 | 00 | 00 |
| 20 | 2D | 0B | 02 | 00 | 00 |
| 21 | 30 | 0B | 02 | 00 | 00 |
| 22 | 30 | 0A | 02 | 00 | 00 |
| 23 | 2E | 0A | 02 | 00 | 00 |
| 24 | 2C | 09 | 02 | 00 | 00 |

Note: SCALE[4:0] programmed to 03H.

**Table 90 - Transmit Waveform Values for T1 Long Haul (LBO 22.5 dB):**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 1F | 16 | 06 | 01 |
| 2 | 00 | 20 | 15 | 05 | 01 |
| 3 | 00 | 21 | 15 | 05 | 01 |
| 4 | 00 | 22 | 14 | 05 | 01 |
| 5 | 00 | 22 | 13 | 04 | 00 |
| 6 | 00 | 23 | 12 | 04 | 00 |
| 7 | 01 | 23 | 12 | 04 | 00 |
| 8 | 01 | 24 | 11 | 03 | 00 |
| 9 | 01 | 23 | 10 | 03 | 00 |
| 10 | 02 | 23 | 10 | 03 | 00 |
| 11 | 03 | 22 | 0F | 03 | 00 |
| 12 | 05 | 22 | 0E | 03 | 00 |
| 13 | 07 | 21 | 0E | 02 | 00 |
| 14 | 09 | 20 | 0D | 02 | 00 |
| 15 | 0B | 1E | 0C | 02 | 00 |
| 16 | 0E | 1D | 0C | 02 | 00 |
| 17 | 10 | 1B | 0B | 02 | 00 |
| 18 | 13 | 1B | 0A | 02 | 00 |

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 19 | 15 | 1A | 0A | 02 | 00 |
| 20 | 17 | 19 | 09 | 01 | 00 |
| 21 | 19 | 19 | 08 | 01 | 00 |
| 22 | 1B | 18 | 08 | 01 | 00 |
| 23 | 1D | 17 | 07 | 01 | 00 |
| 24 | 1E | 17 | 06 | 01 | 00 |

Note: SCALE[4:0] programmed to 02H.

**Table 91 - Transmit Waveform Values for T1 Short Haul (0 - 110 ft.):**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 45 | 00 | 00 | 00 |
| 2 | 0A | 44 | 00 | 00 | 00 |
| 3 | 20 | 43 | 00 | 00 | 00 |
| 4 | 3F | 43 | 00 | 00 | 00 |
| 5 | 3F | 42 | 00 | 00 | 00 |
| 6 | 3F | 42 | 00 | 00 | 00 |
| 7 | 3C | 41 | 00 | 00 | 00 |
| 8 | 3B | 41 | 00 | 00 | 00 |
| 9 | 3A | 00 | 00 | 00 | 00 |
| 10 | 39 | 00 | 00 | 00 | 00 |
| 11 | 39 | 00 | 00 | 00 | 00 |
| 12 | 38 | 00 | 00 | 00 | 00 |
| 13 | 37 | 00 | 00 | 00 | 00 |
| 14 | 36 | 00 | 00 | 00 | 00 |
| 15 | 34 | 00 | 00 | 00 | 00 |
| 16 | 29 | 00 | 00 | 00 | 00 |
| 17 | 59 | 00 | 00 | 00 | 00 |
| 18 | 55 | 00 | 00 | 00 | 00 |
| 19 | 50 | 00 | 00 | 00 | 00 |

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 20 | 4D | 00 | 00 | 00 | 00 |
| 21 | 4A | 00 | 00 | 00 | 00 |
| 22 | 48 | 00 | 00 | 00 | 00 |
| 23 | 46 | 00 | 00 | 00 | 00 |
| 24 | 46 | 00 | 00 | 00 | 00 |

Note: SCALE[4:0] programmed to 0CH.

**Table 92 - Transmit Waveform Values for T1 Short Haul (110 – 220 ft.):**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 44 | 00 | 00 | 00 |
| 2 | 0A | 44 | 00 | 00 | 00 |
| 3 | 3F | 43 | 00 | 00 | 00 |
| 4 | 3F | 43 | 00 | 00 | 00 |
| 5 | 36 | 42 | 00 | 00 | 00 |
| 6 | 34 | 42 | 00 | 00 | 00 |
| 7 | 30 | 41 | 00 | 00 | 00 |
| 8 | 2F | 41 | 00 | 00 | 00 |
| 9 | 2E | 00 | 00 | 00 | 00 |
| 10 | 2D | 00 | 00 | 00 | 00 |
| 11 | 2C | 00 | 00 | 00 | 00 |
| 12 | 2B | 00 | 00 | 00 | 00 |
| 13 | 2A | 00 | 00 | 00 | 00 |
| 14 | 28 | 00 | 00 | 00 | 00 |
| 15 | 26 | 00 | 00 | 00 | 00 |
| 16 | 4A | 00 | 00 | 00 | 00 |
| 17 | 68 | 00 | 00 | 00 | 00 |
| 18 | 54 | 00 | 00 | 00 | 00 |
| 19 | 4F | 00 | 00 | 00 | 00 |
| 20 | 4A | 00 | 00 | 00 | 00 |

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 21 | 49 | 00 | 00 | 00 | 00 |
| 22 | 47 | 00 | 00 | 00 | 00 |
| 23 | 47 | 00 | 00 | 00 | 00 |
| 24 | 46 | 00 | 00 | 00 | 00 |

Note: SCALE[4:0] programmed to 10H.

**Table 93 - Transmit Waveform Values for T1 Short Haul (220 – 330 ft.):**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 44 | 00 | 00 | 00 |
| 2 | 0A | 44 | 00 | 00 | 00 |
| 3 | 3F | 43 | 00 | 00 | 00 |
| 4 | 3A | 43 | 00 | 00 | 00 |
| 5 | 3A | 42 | 00 | 00 | 00 |
| 6 | 38 | 42 | 00 | 00 | 00 |
| 7 | 30 | 41 | 00 | 00 | 00 |
| 8 | 2F | 41 | 00 | 00 | 00 |
| 9 | 2E | 00 | 00 | 00 | 00 |
| 10 | 2D | 00 | 00 | 00 | 00 |
| 11 | 2C | 00 | 00 | 00 | 00 |
| 12 | 2B | 00 | 00 | 00 | 00 |
| 13 | 2A | 00 | 00 | 00 | 00 |
| 14 | 29 | 00 | 00 | 00 | 00 |
| 15 | 23 | 00 | 00 | 00 | 00 |
| 16 | 4A | 00 | 00 | 00 | 00 |
| 17 | 6C | 00 | 00 | 00 | 00 |
| 18 | 60 | 00 | 00 | 00 | 00 |
| 19 | 4F | 00 | 00 | 00 | 00 |
| 20 | 4A | 00 | 00 | 00 | 00 |
| 21 | 49 | 00 | 00 | 00 | 00 |

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 22 | 47 | 00 | 00 | 00 | 00 |
| 23 | 47 | 00 | 00 | 00 | 00 |
| 24 | 46 | 00 | 00 | 00 | 00 |

Note: SCALE[4:0] programmed to 11H.

**Table 94 - Transmit Waveform Values for T1 Short Haul (330 – 440 ft.):**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 44 | 00 | 00 | 00 |
| 2 | 0A | 44 | 00 | 00 | 00 |
| 3 | 3F | 43 | 00 | 00 | 00 |
| 4 | 3F | 43 | 00 | 00 | 00 |
| 5 | 3F | 42 | 00 | 00 | 00 |
| 6 | 3F | 42 | 00 | 00 | 00 |
| 7 | 2F | 41 | 00 | 00 | 00 |
| 8 | 2E | 41 | 00 | 00 | 00 |
| 9 | 2D | 00 | 00 | 00 | 00 |
| 10 | 2C | 00 | 00 | 00 | 00 |
| 11 | 2B | 00 | 00 | 00 | 00 |
| 12 | 2A | 00 | 00 | 00 | 00 |
| 13 | 29 | 00 | 00 | 00 | 00 |
| 14 | 28 | 00 | 00 | 00 | 00 |
| 15 | 19 | 00 | 00 | 00 | 00 |
| 16 | 4A | 00 | 00 | 00 | 00 |
| 17 | 7F | 00 | 00 | 00 | 00 |
| 18 | 60 | 00 | 00 | 00 | 00 |
| 19 | 4F | 00 | 00 | 00 | 00 |
| 20 | 4A | 00 | 00 | 00 | 00 |
| 21 | 49 | 00 | 00 | 00 | 00 |
| 22 | 47 | 00 | 00 | 00 | 00 |

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 23 | 47 | 00 | 00 | 00 | 00 |
| 24 | 46 | 00 | 00 | 00 | 00 |

Note: SCALE[4:0] programmed to 12H.

**Table 95 - Transmit Waveform Values for T1 Short Haul (440 – 550 ft.):**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 44 | 00 | 00 | 00 |
| 2 | 0A | 44 | 00 | 00 | 00 |
| 3 | 3F | 43 | 00 | 00 | 00 |
| 4 | 3F | 43 | 00 | 00 | 00 |
| 5 | 3F | 42 | 00 | 00 | 00 |
| 6 | 3F | 42 | 00 | 00 | 00 |
| 7 | 30 | 41 | 00 | 00 | 00 |
| 8 | 2B | 41 | 00 | 00 | 00 |
| 9 | 2A | 00 | 00 | 00 | 00 |
| 10 | 29 | 00 | 00 | 00 | 00 |
| 11 | 28 | 00 | 00 | 00 | 00 |
| 12 | 27 | 00 | 00 | 00 | 00 |
| 13 | 26 | 00 | 00 | 00 | 00 |
| 14 | 26 | 00 | 00 | 00 | 00 |
| 15 | 24 | 00 | 00 | 00 | 00 |
| 16 | 4A | 00 | 00 | 00 | 00 |
| 17 | 7F | 00 | 00 | 00 | 00 |
| 18 | 7F | 00 | 00 | 00 | 00 |
| 19 | 4F | 00 | 00 | 00 | 00 |
| 20 | 4A | 00 | 00 | 00 | 00 |
| 21 | 49 | 00 | 00 | 00 | 00 |
| 22 | 47 | 00 | 00 | 00 | 00 |
| 23 | 47 | 00 | 00 | 00 | 00 |

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 24 | 46 | 00 | 00 | 00 | 00 |

Note: SCALE[4:0] programmed to 14H.

**Table 96 - Transmit Waveform Values for T1 Short Haul (550 – 660 ft.):**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 44 | 00 | 00 | 00 |
| 2 | 0A | 44 | 00 | 00 | 00 |
| 3 | 3F | 43 | 00 | 00 | 00 |
| 4 | 3F | 43 | 00 | 00 | 00 |
| 5 | 3F | 42 | 00 | 00 | 00 |
| 6 | 3F | 42 | 00 | 00 | 00 |
| 7 | 3F | 41 | 00 | 00 | 00 |
| 8 | 30 | 41 | 00 | 00 | 00 |
| 9 | 2A | 00 | 00 | 00 | 00 |
| 10 | 29 | 00 | 00 | 00 | 00 |
| 11 | 28 | 00 | 00 | 00 | 00 |
| 12 | 27 | 00 | 00 | 00 | 00 |
| 13 | 26 | 00 | 00 | 00 | 00 |
| 14 | 25 | 00 | 00 | 00 | 00 |
| 15 | 24 | 00 | 00 | 00 | 00 |
| 16 | 4A | 00 | 00 | 00 | 00 |
| 17 | 7F | 00 | 00 | 00 | 00 |
| 18 | 7F | 00 | 00 | 00 | 00 |
| 19 | 5F | 00 | 00 | 00 | 00 |
| 20 | 50 | 00 | 00 | 00 | 00 |
| 21 | 49 | 00 | 00 | 00 | 00 |
| 22 | 47 | 00 | 00 | 00 | 00 |
| 23 | 47 | 00 | 00 | 00 | 00 |
| 24 | 46 | 00 | 00 | 00 | 00 |

Note: SCALE[4:0] programmed to 15H.

**Table 97 - TR62411 Transmit Waveform Values for T1 Long Haul (LBO 0 dB):**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 00 | 00 | 00 | 00 |
| 2 | 0A | 00 | 00 | 00 | 00 |
| 3 | 20 | 00 | 00 | 00 | 00 |
| 4 | 32 | 00 | 00 | 00 | 00 |
| 5 | 3E | 00 | 00 | 00 | 00 |
| 6 | 3D | 00 | 00 | 00 | 00 |
| 7 | 3C | 00 | 00 | 00 | 00 |
| 8 | 3B | 00 | 00 | 00 | 00 |
| 9 | 3A | 00 | 00 | 00 | 00 |
| 10 | 39 | 00 | 00 | 00 | 00 |
| 11 | 39 | 00 | 00 | 00 | 00 |
| 12 | 38 | 00 | 00 | 00 | 00 |
| 13 | 37 | 00 | 00 | 00 | 00 |
| 14 | 36 | 00 | 00 | 00 | 00 |
| 15 | 34 | 00 | 00 | 00 | 00 |
| 16 | 29 | 00 | 00 | 00 | 00 |
| 17 | 4F | 00 | 00 | 00 | 00 |
| 18 | 4C | 00 | 00 | 00 | 00 |
| 19 | 4A | 00 | 00 | 00 | 00 |
| 20 | 46 | 00 | 00 | 00 | 00 |
| 21 | 44 | 00 | 00 | 00 | 00 |
| 22 | 42 | 00 | 00 | 00 | 00 |
| 23 | 00 | 00 | 00 | 00 | 00 |
| 24 | 00 | 00 | 00 | 00 | 00 |

Note: SCALE[4:0] programmed to 0CH.

**Table 98 - TR62411 Transmit Waveform Values for T1 Short Haul (0 - 110 ft.):**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 00 | 00 | 00 | 00 |
| 2 | 0A | 00 | 00 | 00 | 00 |
| 3 | 20 | 00 | 00 | 00 | 00 |
| 4 | 3F | 00 | 00 | 00 | 00 |
| 5 | 3F | 00 | 00 | 00 | 00 |
| 6 | 3F | 00 | 00 | 00 | 00 |
| 7 | 3C | 00 | 00 | 00 | 00 |
| 8 | 3B | 00 | 00 | 00 | 00 |
| 9 | 3A | 00 | 00 | 00 | 00 |
| 10 | 39 | 00 | 00 | 00 | 00 |
| 11 | 39 | 00 | 00 | 00 | 00 |
| 12 | 38 | 00 | 00 | 00 | 00 |
| 13 | 37 | 00 | 00 | 00 | 00 |
| 14 | 36 | 00 | 00 | 00 | 00 |
| 15 | 34 | 00 | 00 | 00 | 00 |
| 16 | 29 | 00 | 00 | 00 | 00 |
| 17 | 4C | 00 | 00 | 00 | 00 |
| 18 | 4A | 00 | 00 | 00 | 00 |
| 19 | 48 | 00 | 00 | 00 | 00 |
| 20 | 46 | 00 | 00 | 00 | 00 |
| 21 | 44 | 00 | 00 | 00 | 00 |
| 22 | 42 | 00 | 00 | 00 | 00 |
| 23 | 00 | 00 | 00 | 00 | 00 |
| 24 | 00 | 00 | 00 | 00 | 00 |

Note: SCALE[4:0] programmed to 0CH.

**Table 99 - TR62411 Transmit Waveform Values for T1 Short Haul (110 – 220 ft.):**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 00 | 00 | 00 | 00 |
| 2 | 0A | 00 | 00 | 00 | 00 |
| 3 | 3F | 00 | 00 | 00 | 00 |
| 4 | 3F | 00 | 00 | 00 | 00 |
| 5 | 36 | 00 | 00 | 00 | 00 |
| 6 | 34 | 00 | 00 | 00 | 00 |
| 7 | 30 | 00 | 00 | 00 | 00 |
| 8 | 2F | 00 | 00 | 00 | 00 |
| 9 | 2E | 00 | 00 | 00 | 00 |
| 10 | 2D | 00 | 00 | 00 | 00 |
| 11 | 2C | 00 | 00 | 00 | 00 |
| 12 | 2B | 00 | 00 | 00 | 00 |
| 13 | 2A | 00 | 00 | 00 | 00 |
| 14 | 28 | 00 | 00 | 00 | 00 |
| 15 | 26 | 00 | 00 | 00 | 00 |
| 16 | 4A | 00 | 00 | 00 | 00 |
| 17 | 68 | 00 | 00 | 00 | 00 |
| 18 | 4A | 00 | 00 | 00 | 00 |
| 19 | 48 | 00 | 00 | 00 | 00 |
| 20 | 46 | 00 | 00 | 00 | 00 |
| 21 | 44 | 00 | 00 | 00 | 00 |
| 22 | 42 | 00 | 00 | 00 | 00 |
| 23 | 00 | 00 | 00 | 00 | 00 |
| 24 | 00 | 00 | 00 | 00 | 00 |

Note: SCALE[4:0] programmed to 10H.

**Table 100 - TR62411 Transmit Waveform Values for T1 Short Haul (220 – 330 ft.):**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 00 | 00 | 00 | 00 |
| 2 | 0A | 00 | 00 | 00 | 00 |
| 3 | 3F | 00 | 00 | 00 | 00 |
| 4 | 3A | 00 | 00 | 00 | 00 |
| 5 | 3A | 00 | 00 | 00 | 00 |
| 6 | 38 | 00 | 00 | 00 | 00 |
| 7 | 30 | 00 | 00 | 00 | 00 |
| 8 | 2F | 00 | 00 | 00 | 00 |
| 9 | 2E | 00 | 00 | 00 | 00 |
| 10 | 2D | 00 | 00 | 00 | 00 |
| 11 | 2C | 00 | 00 | 00 | 00 |
| 12 | 2B | 00 | 00 | 00 | 00 |
| 13 | 2A | 00 | 00 | 00 | 00 |
| 14 | 29 | 00 | 00 | 00 | 00 |
| 15 | 23 | 00 | 00 | 00 | 00 |
| 16 | 4A | 00 | 00 | 00 | 00 |
| 17 | 6C | 00 | 00 | 00 | 00 |
| 18 | 4A | 00 | 00 | 00 | 00 |
| 19 | 48 | 00 | 00 | 00 | 00 |
| 20 | 46 | 00 | 00 | 00 | 00 |
| 21 | 44 | 00 | 00 | 00 | 00 |
| 22 | 42 | 00 | 00 | 00 | 00 |
| 23 | 00 | 00 | 00 | 00 | 00 |
| 24 | 00 | 00 | 00 | 00 | 00 |

Note: SCALE[4:0] programmed to 11H.

**Table 101 - TR62411 Transmit Waveform Values for T1 Short Haul (330 – 440 ft.):**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 00 | 00 | 00 | 00 |
| 2 | 0A | 00 | 00 | 00 | 00 |
| 3 | 3F | 00 | 00 | 00 | 00 |
| 4 | 3F | 00 | 00 | 00 | 00 |
| 5 | 3F | 00 | 00 | 00 | 00 |
| 6 | 3F | 00 | 00 | 00 | 00 |
| 7 | 2F | 00 | 00 | 00 | 00 |
| 8 | 2E | 00 | 00 | 00 | 00 |
| 9 | 2D | 00 | 00 | 00 | 00 |
| 10 | 2C | 00 | 00 | 00 | 00 |
| 11 | 2B | 00 | 00 | 00 | 00 |
| 12 | 2A | 00 | 00 | 00 | 00 |
| 13 | 29 | 00 | 00 | 00 | 00 |
| 14 | 28 | 00 | 00 | 00 | 00 |
| 15 | 19 | 00 | 00 | 00 | 00 |
| 16 | 4A | 00 | 00 | 00 | 00 |
| 17 | 7F | 00 | 00 | 00 | 00 |
| 18 | 54 | 00 | 00 | 00 | 00 |
| 19 | 48 | 00 | 00 | 00 | 00 |
| 20 | 46 | 00 | 00 | 00 | 00 |
| 21 | 44 | 00 | 00 | 00 | 00 |
| 22 | 42 | 00 | 00 | 00 | 00 |
| 23 | 00 | 00 | 00 | 00 | 00 |
| 24 | 00 | 00 | 00 | 00 | 00 |

Note: SCALE[4:0] programmed to 12H.

**Table 102 - TR62411 Transmit Waveform Values for T1 Short Haul (440 – 550 ft.):**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 00 | 00 | 00 | 00 |
| 2 | 0A | 00 | 00 | 00 | 00 |
| 3 | 3F | 00 | 00 | 00 | 00 |
| 4 | 3F | 00 | 00 | 00 | 00 |
| 5 | 3F | 00 | 00 | 00 | 00 |
| 6 | 3F | 00 | 00 | 00 | 00 |
| 7 | 30 | 00 | 00 | 00 | 00 |
| 8 | 2B | 00 | 00 | 00 | 00 |
| 9 | 2A | 00 | 00 | 00 | 00 |
| 10 | 29 | 00 | 00 | 00 | 00 |
| 11 | 28 | 00 | 00 | 00 | 00 |
| 12 | 27 | 00 | 00 | 00 | 00 |
| 13 | 26 | 00 | 00 | 00 | 00 |
| 14 | 26 | 00 | 00 | 00 | 00 |
| 15 | 24 | 00 | 00 | 00 | 00 |
| 16 | 4A | 00 | 00 | 00 | 00 |
| 17 | 7F | 00 | 00 | 00 | 00 |
| 18 | 7F | 00 | 00 | 00 | 00 |
| 19 | 4A | 00 | 00 | 00 | 00 |
| 20 | 46 | 00 | 00 | 00 | 00 |
| 21 | 44 | 00 | 00 | 00 | 00 |
| 22 | 42 | 00 | 00 | 00 | 00 |
| 23 | 00 | 00 | 00 | 00 | 00 |
| 24 | 00 | 00 | 00 | 00 | 00 |

Note: SCALE[4:0] programmed to 14H.

**Table 103 - TR62411 Transmit Waveform Values for T1 Short Haul (550 – 660 ft.):**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 00 | 00 | 00 | 00 |
| 2 | 0A | 00 | 00 | 00 | 00 |
| 3 | 3F | 00 | 00 | 00 | 00 |
| 4 | 3F | 00 | 00 | 00 | 00 |
| 5 | 3F | 00 | 00 | 00 | 00 |
| 6 | 3F | 00 | 00 | 00 | 00 |
| 7 | 3F | 00 | 00 | 00 | 00 |
| 8 | 30 | 00 | 00 | 00 | 00 |
| 9 | 2A | 00 | 00 | 00 | 00 |
| 10 | 29 | 00 | 00 | 00 | 00 |
| 11 | 28 | 00 | 00 | 00 | 00 |
| 12 | 27 | 00 | 00 | 00 | 00 |
| 13 | 26 | 00 | 00 | 00 | 00 |
| 14 | 25 | 00 | 00 | 00 | 00 |
| 15 | 24 | 00 | 00 | 00 | 00 |
| 16 | 4A | 00 | 00 | 00 | 00 |
| 17 | 7F | 00 | 00 | 00 | 00 |
| 18 | 7F | 00 | 00 | 00 | 00 |
| 19 | 5F | 00 | 00 | 00 | 00 |
| 20 | 50 | 00 | 00 | 00 | 00 |
| 21 | 49 | 00 | 00 | 00 | 00 |
| 22 | 44 | 00 | 00 | 00 | 00 |
| 23 | 42 | 00 | 00 | 00 | 00 |
| 24 | 00 | 00 | 00 | 00 | 00 |

Note: SCALE[4:0] programmed to 15H.

**Table 104 - Transmit Waveform Values for E1 120 Ohm:**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 00 | 00 | 00 | 00 |
| 2 | 00 | 00 | 00 | 00 | 00 |
| 3 | 0A | 00 | 00 | 00 | 00 |
| 4 | 3F | 00 | 00 | 00 | 00 |
| 5 | 3F | 00 | 00 | 00 | 00 |
| 6 | 39 | 00 | 00 | 00 | 00 |
| 7 | 38 | 00 | 00 | 00 | 00 |
| 8 | 36 | 00 | 00 | 00 | 00 |
| 9 | 36 | 00 | 00 | 00 | 00 |
| 10 | 35 | 00 | 00 | 00 | 00 |
| 11 | 35 | 00 | 00 | 00 | 00 |
| 12 | 35 | 00 | 00 | 00 | 00 |
| 13 | 35 | 00 | 00 | 00 | 00 |
| 14 | 35 | 00 | 00 | 00 | 00 |
| 15 | 35 | 00 | 00 | 00 | 00 |
| 16 | 2D | 00 | 00 | 00 | 00 |
| 17 | 00 | 00 | 00 | 00 | 00 |
| 18 | 00 | 00 | 00 | 00 | 00 |
| 19 | 00 | 00 | 00 | 00 | 00 |
| 20 | 00 | 00 | 00 | 00 | 00 |
| 21 | 00 | 00 | 00 | 00 | 00 |
| 22 | 00 | 00 | 00 | 00 | 00 |
| 23 | 00 | 00 | 00 | 00 | 00 |
| 24 | 00 | 00 | 00 | 00 | 00 |

Note: SCALE[4:0] programmed to 0CH.

**Table 105 - Transmit Waveform Values for E1 75 Ohm:**

| Sample number | UI #0 | UI #1 | UI #2 | UI #3 | UI #4 |
|---|---|---|---|---|---|
| 1 | 00 | 00 | 00 | 00 | 00 |
| 2 | 00 | 00 | 00 | 00 | 00 |
| 3 | 0A | 00 | 00 | 00 | 00 |
| 4 | 3E | 00 | 00 | 00 | 00 |
| 5 | 3E | 00 | 00 | 00 | 00 |
| 6 | 3E | 00 | 00 | 00 | 00 |
| 7 | 3C | 00 | 00 | 00 | 00 |
| 8 | 3C | 00 | 00 | 00 | 00 |
| 9 | 3A | 00 | 00 | 00 | 00 |
| 10 | 3A | 00 | 00 | 00 | 00 |
| 11 | 3A | 00 | 00 | 00 | 00 |
| 12 | 3A | 00 | 00 | 00 | 00 |
| 13 | 3A | 00 | 00 | 00 | 00 |
| 14 | 3A | 00 | 00 | 00 | 00 |
| 15 | 3A | 00 | 00 | 00 | 00 |
| 16 | 35 | 00 | 00 | 00 | 00 |
| 17 | 00 | 00 | 00 | 00 | 00 |
| 18 | 00 | 00 | 00 | 00 | 00 |
| 19 | 00 | 00 | 00 | 00 | 00 |
| 20 | 00 | 00 | 00 | 00 | 00 |
| 21 | 00 | 00 | 00 | 00 | 00 |
| 22 | 00 | 00 | 00 | 00 | 00 |
| 23 | 00 | 00 | 00 | 00 | 00 |
| 24 | 00 | 00 | 00 | 00 | 00 |

Note: SCALE[4:0] programmed to 0BH.

## 14.6 Using the Line Receiver

The line receiver must be properly initialized for correct operation. Several register bits must be programmed, and a RAM table must be initialized.

Note that two registers must be programmed to non-default values. The Reserved bit of the RLPS Equalizer Configuration register must be set to logic 1. The EQ_VREF[5:0] bits of the RLPS Equalizer Voltage Reference register must be programmed to 2CH (‘b101100) for T1 mode or 34H (‘b110100) for E1 mode.

Since the line receiver supports both E1 and T1 standards over either short haul or long haul cables, the line receiver has two normal modes of operation, as selected by the T1/E1B bit of the Global Configuration register. Table 107 and Table 108 contain the values to be programmed into the equalizer RAM for T1 and E1 mode, respectively.

The RLPS equalizer RAM content is programmed by the RLPS Equalization Indirect Data registers (0D8H to 0DBH) for each address location. The address location is given by the quadrant’s RLPS Equalization Indirect Address register (0FCH). A read or write request is done by setting the RWB bit in the quadrant’s RLPS Equalization Read/WriteB Select register (0FDH). Table 106 below summarizes the values the RLPS registers are to contain.

**Table 106 - RLPS Register Programming**

| Data Value | | Register Address | Register Name |
|---|---|---|---|
| **Binary** | **Hex** | | |
| XX000XX1 | 01H | 0F8H | RLPS Configuration and Status |
| X000X000 | 00H | 0F9H | RLPS ALOS Detection/ Clearance Threshold |
| 00000001 | 01H | 0FAH | RLPS ALOS Detection Period |
| 00000001 | 01H | 0FBH | RLPS ALOS Clearance Time |
| 00000000 | 00H | 0FCH | RLPS Equalization Indirect Address |
| 1XXXXXXX | 80H | 0FDH | RLPS Equalization RAM Read/WriteB Select |
| 00000000 | 00H | 0FEH | RLPS Equalizer Loop Status and Control |

| | | | |
|---|---|---|---|
| 00001011 | 0BH | 0FFH | RLPS Equalizer Configuration |
| * | * | 0D8H | RLPS Equalization Indirect Data[31:24] |
| * | * | 0D9H | RLPS Equalization Indirect Data[23:16] |
| * | * | 0DAH | RLPS Equalization Indirect Data[15:8] |
| * | * | 0DBH | RLPS Equalization Indirect Data[7:0] |
| XX101100<br>XX110100 | 2CH<br>34H | 0DCH | RLPS Equalizer Voltage Reference<br>(T1 mode)<br>(E1 mode) |

Access to the Equalizer RAM is provided by means of Registers FCH, FDH, D8H, D9H, FAH, and FBH. A typical programming sequence follows. This programming sequence is repeated for each of the 256 Equalizer RAM Addresses.

```
WRITE D8H  <31 – 24 Bits of Data>

WRITE D9H  <23 – 16 Bits of Data>

WRITE DAH  <15 – 8 Bits of Data>

WRITE DBH  <7 – 0 Bits of Data>

ACTION FDH  <A=80H for “read”; A=00H for “write”
action>

WRITE FCH  <address register from 0 to 255>

PAUSE  <wait 3 line rate clock cycles>
```

**Table 107 - RLPS Equalizer RAM Table (T1 mode)**

| RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) |
|---|---|---|---|
| 00D | 03 FE 18 40H | 128D | 97 5E 7A C0H |
| 01D | 03 F6 18 40H | 129D | 97 5E 7A C0H |

| RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) |
|---|---|---|---|
| 02D | 03 EE 18 40H | 130D | 97 5E 7A C0H |
| 03D | 03 E6 18 40H | 131D | 9F 5E 8A C0H |
| 04D | 03 DE 18 40h | 132D | 9F 5E 8A C0H |
| 05D | 03 D6 18 40H | 133D | 9F 5E 8A C0H |
| 06D | 03 D6 18 40H | 134D | 9F 5E 8A C0H |
| 07D | 03 D6 18 40H | 135D | 9F 5E 8A C0H |
| 08D | 03 CE 18 40H | 136D | A7 56 9A C0H |
| 09D | 03 CE 18 40H | 137D | A7 56 9A C0H |
| 10D | 03 CE 18 40H | 138D | A7 56 9A C0H |
| 11D | 03 CE 18 40H | 139D | A7 56 9A C0H |
| 12D | 03 C6 18 40H | 140D | A7 56 AA C0H |
| 13D | 03 C6 18 40H | 141D | A7 56 AA C0H |
| 14D | 03 C6 18 40H | 142D | A7 56 AA C0H |
| 15D | 0B BE 18 40H | 143D | AF 4E AA C0H |
| 16D | 0B BE 18 40H | 144D | AF 4E AA C0H |
| 17D | 0B BE 18 40H | 145D | AF 4E AA C0H |
| 18D | 0B BE 18 40H | 146D | AF 4E AA C0H |
| 19D | 0B B6 18 40H | 147D | AF 4E AA C0H |
| 20D | 0B B6 18 40H | 148D | B7 46 AA C0H |
| 21D | 0B B6 18 40H | 149D | B7 46 AA C0H |
| 22D | 0B B6 18 40H | 150D | B7 46 AA C0H |
| 23D | 13 AE 18 38H | 151D | B7 46 AA C0H |
| 24D | 13 AE 18 3CH | 152D | B7 46 AA C0H |
| 25D | 13 AE 18 40H | 153D | B7 46 AA C0H |
| 26D | 13 AE 18 40H | 154D | B7 46 AA C0H |
| 27D | 13 AE 18 40H | 155D | B7 46 BA C0H |
| 28D | 13 AE 18 40H | 156D | B7 46 BA C0H |
| 29D | 1B B6 18 B8H | 157D | B7 46 BA C0H |
| 30D | 1B AE 18 B8H | 158D | BF 4E BB 40H |
| 31D | 1B AE 18 BCH | 159D | BF 4E BB 40H |
| 32D | 1B AE 18 C0H | 160D | BF 4E BB 40H |

| RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) |
|---|---|---|---|
| 33D | 1B AE 18 C0H | 161D | BF 4E BB 40H |
| 34D | 23 A6 18 C0H | 162D | BF 4E BB 40H |
| 35D | 23 A6 18 C0H | 163D | BF 4E BB 40H |
| 36D | 23 A6 18 C0H | 164D | BF 4E BB 40H |
| 37D | 23 A6 18 C0H | 165D | BF 4E BB 40H |
| 38D | 23 A6 18 C0H | 166D | BF 4E BB 40H |
| 39D | 23 9E 18 C0H | 167D | BE 46 CB 40H |
| 40D | 23 9E 18 C0H | 168D | BE 46 CB 40H |
| 41D | 23 9E 18 C0H | 169D | BE 46 CB 40H |
| 42D | 23 9E 18 C0H | 170D | BE 46 CB 40H |
| 43D | 23 9E 18 C0H | 171D | BE 46 CB 40H |
| 44D | 2B 96 18 C0H | 172D | BE 46 CB 40H |
| 45D | 2B 96 18 C0H | 173D | BE 46 DB 40H |
| 46D | 2B 96 18 C0H | 174D | BE 46 DB 40H |
| 47D | 33 96 19 40H | 175D | BE 46 DB 40H |
| 48D | 37 96 19 40H | 176D | C6 3E CB 40H |
| 49D | 37 96 19 40H | 177D | C6 3E CB 40H |
| 50D | 37 96 19 40H | 178D | C6 3E DB 40H |
| 51D | 3F 9E 19 C0H | 179D | C6 3E DB 40H |
| 52D | 3F 9E 19 C0H | 180D | C6 3E DB 40H |
| 53D | 3F 9E 19 C0H | 181D | C6 44 DB 40H |
| 54D | 3F A6 1A 40H | 182D | C6 44 DB 40H |
| 55D | 3F A6 1A 40H | 183D | C6 44 DB 40H |
| 56D | 3F A6 1A 40H | 184D | C6 44 DB 40H |
| 57D | 3F A6 1A 40H | 185D | C6 3C DB 40H |
| 58D | 3F 96 19 C0H | 186D | C6 3C DB 40H |
| 59D | 3F 96 19 C0H | 187D | C6 3C DB 40H |
| 60D | 3F 96 19 C0H | 188D | C6 3C DB 40H |
| 61D | 3F 96 19 C0H | 189D | D6 34 DB 40H |
| 62D | 47 9E 1A 40H | 190D | D6 34 DB 40H |
| 63D | 47 9E 1A 40H | 191D | D6 34 DB 40H |

| RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) |
|---|---|---|---|
| 64D | 47 9E 1A 40H | 192D | D6 34 DB 40H |
| 65D | 47 96 1A 40H | 193D | D6 34 DB 40H |
| 66D | 47 96 1A 40H | 194D | DE 2C DB 3CH |
| 67D | 47 96 1A 40H | 195D | DE 2C DB 3CH |
| 68D | 47 96 1A 40H | 196D | DE 2C DB 3CH |
| 69D | 4F 8E 1A 40H | 197D | E6 2C DB 40H |
| 70D | 4F 8E 1A 40H | 198D | E6 2C DB 40H |
| 71D | 4F 8E 1A 40H | 199D | E6 2C DB 40H |
| 72D | 4F 8E 1A 40H | 200D | E6 2C DB 40H |
| 73D | 4F 8E 1A 40H | 201D | E6 2C DB 40H |
| 74D | 57 86 1A 40H | 202D | E6 2C EB 40H |
| 75D | 57 86 1A 40H | 203D | E6 2C EB 40H |
| 76D | 57 86 1A 40H | 204D | E6 2C EB 40H |
| 77D | 57 86 1A 40H | 205D | EE 2C FB 40H |
| 78D | 57 86 1A 40H | 206D | EE 2C FB 40H |
| 79D | 5F 86 1A C0H | 207D | EE 2C FB 40H |
| 80D | 5F 86 1A C0H | 208D | EE 2D 0B 40H |
| 81D | 5F 86 1A C0H | 209D | EE 2D 0B 40H |
| 82D | 5F 86 1A C0H | 210D | EE 2D 0B 40H |
| 83D | 5F 86 1A C0H | 211D | EE 2D 0B 40H |
| 84D | 5F 86 1A C0H | 212D | EE 2D 0B 40H |
| 85D | 5F 7E 1A C0H | 213D | F5 25 0B 38H |
| 86D | 5F 7E 1A C0H | 214D | F5 25 0B 3CH |
| 87D | 5F 7E 1A C0H | 215D | F5 25 0B 40H |
| 88D | 5F 7E 1A C0H | 216D | F5 25 1B 40H |
| 89D | 5F 7E 1A C0H | 217D | F5 25 1B 40H |
| 90D | 67 7E 2A C0H | 218D | F5 25 1B 40H |
| 91D | 67 7E 2A C0H | 219D | F5 25 1B 40H |
| 92D | 67 7E 2A C0H | 220D | F5 25 1B 40H |
| 93D | 67 7E 2A C0H | 221D | FD 25 2B 40H |
| 94D | 67 76 2A C0H | 222D | FD 25 2B 40H |

| RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) |
|---|---|---|---|
| 95D | 67 76 2A C0H | 223D | FD 25 2B 40H |
| 96D | 67 76 2A C0H | 224D | FD 25 2B 40H |
| 97D | 67 76 2A C0H | 225D | FD 25 27 40H |
| 98D | 67 76 2A C0H | 226D | FD 25 27 40H |
| 99D | 6F 6E 2A C0H | 227D | FD 25 27 40H |
| 100D | 6F 6E 2A C0H | 228D | FD 25 23 40H |
| 101D | 6F 6E 2A C0H | 229D | FD 25 23 40H |
| 102D | 6F 6E 2A C0H | 230D | FD 25 23 40H |
| 103D | 77 6E 3A C0H | 231D | FD 25 33 40H |
| 104D | 77 6E 3A C0H | 232D | FD 25 33 40H |
| 105D | 77 6E 3A C0H | 233D | FD 25 33 40H |
| 106D | 77 6E 3A C0H | 234D | FD 25 33 40H |
| 107D | 7F 66 3A C0H | 235D | FD 25 33 40H |
| 108D | 7F 66 3A C0H | 236D | FD 25 33 40H |
| 109D | 7F 66 4A C0H | 237D | FC 25 33 40H |
| 110D | 7F 66 4A C0H | 238D | FC 25 33 40H |
| 111D | 7F 66 4A C0H | 239D | FC 25 43 40H |
| 112D | 7F 66 4A C0H | 240D | FC 25 43 40H |
| 113D | 87 66 5A C0H | 241D | FC 25 43 40H |
| 114D | 87 66 5A C0H | 242D | FC 25 43 44H |
| 115D | 87 66 5A C0H | 243D | FC 25 43 48H |
| 116D | 87 66 5A C0H | 244D | FC 25 43 4CH |
| 117D | 87 66 5A C0H | 245D | FC 25 43 BCH |
| 118D | 87 5E 5A C0H | 246D | FC 25 43 C0H |
| 119D | 87 5E 5A C0H | 247D | FC 25 43 C0H |
| 120D | 87 5E 5A C0H | 248D | FC 23 43 C0H |
| 121D | 87 5E 5A C0H | 249D | FC 23 43 C0H |
| 122D | 87 5E 5A C0H | 250D | FC 23 43 C0H |
| 123D | 8F 5E 6A C0H | 251D | FC 21 43 C0H |
| 124D | 8F 5E 6A C0H | 252D | FC 21 43 C0H |
| 125D | 8F 5E 6A C0H | 253D | FC 21 53 C0H |

| RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) |
|---|---|---|---|
| 126D | 8F 5E 6A C0H | 254D | FC 21 53 C0H |
| 127D | 97 5E 7A C0H | 255D | FC 21 53 C0H |

**Table 108 - RLPS Equalizer RAM Table (E1 mode)**

| RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) |
|---|---|---|---|
| 00D | 07 DE 18 2CH | 128D | 97 4E AF 2CH |
| 01D | 07 DE 18 2CH | 129D | 97 4E AF 2CH |
| 02D | 07 D6 18 2CH | 130D | 97 4E AB 2CH |
| 03D | 07 D6 18 2CH | 131D | 97 4E AB 2CH |
| 04D | 07 D6 18 2CH | 132D | 97 4E AB 2CH |
| 05D | 07 CE 18 2CH | 133D | 9F 4E AB 2CH |
| 06D | 07 CE 18 2CH | 134D | 9F 4E BB 2CH |
| 07D | 07 CE 18 2CH | 135D | 9F 4E BB 2CH |
| 08D | 07 C6 18 2CH | 136D | 9F 4E BB 2CH |
| 09D | 07 C6 18 2CH | 137D | 9F 4E CB 2CH |
| 10D | 07 C6 18 2CH | 138D | A7 4E CB 2CH |
| 11D | 07 BE 18 2CH | 139D | A7 4E CB 2CH |
| 12D | 07 BE 18 2CH | 140D | A7 46 CB 2CH |
| 13D | 07 BE 18 2CH | 141D | A7 46 CB 2CH |
| 14D | 07 BE 18 2CH | 142D | A7 46 CB 2CH |
| 15D | 07 BE 18 2CH | 143D | A7 46 DB 2CH |
| 16D | 07 B6 18 2CH | 144D | AF 46 DB 2CH |
| 17D | 07 B6 18 2CH | 145D | AF 46 EB 2CH |
| 18D | 07 B6 18 2CH | 146D | AF 46 EB 2CH |
| 19D | 07 B6 18 2CH | 147D | AF 4E EB 2CH |
| 20D | 07 B6 18 2CH | 148D | AE 4E EB 2CH |
| 21D | 07 AE 18 2CH | 149D | AE 4E EB 2CH |
| 22D | 07 AE 18 2CH | 150D | B5 46 FB 2CH |
| 23D | 07 AE 18 2CH | 151D | B5 54 FB 2CH |
| 24D | 07 AE 18 2CH | 152D | B5 4C FB 2CH |
| 25D | 07 AE 18 2CH | 153D | B5 54 FB 2CH |

| RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) |
|---|---|---|---|
| 26D | 07 B6 18 ACH | 154D | B5 54 FB 2CH |
| 27D | 07 AE 18 ACH | 155D | BD 54 FB 2CH |
| 28D | 07 AE 18 ACH | 156D | BD 4C FB 2CH |
| 29D | 07 AE 18 ACH | 157D | BD 4C FB 2CH |
| 30D | 07 AE 18 ACH | 158D | BD 4C FB 2CH |
| 31D | 07 A6 18 ACH | 159D | BD 44 EB 2CH |
| 32D | 07 A6 18 ACH | 160D | C5 44 FB 2CH |
| 33D | 07 A6 18 ACH | 161D | C5 44 FB 2CH |
| 34D | 07 A6 18 ACH | 162D | C5 44 FB 2CH |
| 35D | 07 9E 18 ACH | 163D | C5 45 0B 2CH |
| 36D | 07 A6 19 2CH | 164D | C5 45 0B 2CH |
| 37D | 07 A6 19 2CH | 165D | C5 45 0B 2CH |
| 38D | 07 A6 19 2CH | 166D | CD 45 0B 2CH |
| 39D | 0F A6 19 2CH | 167D | CD 45 0B 2CH |
| 40D | 0F A6 19 2CH | 168D | CD 3D 0B 2CH |
| 41D | 0F 9E 19 2CH | 169D | CD 3D 0B 2CH |
| 42D | 0F 9E 19 2CH | 170D | CD 3D 0B 2CH |
| 43D | 0F 9E 19 2CH | 171D | D5 3D 0B 2CH |
| 44D | 17 9E 19 2CH | 172D | D5 3D 0B 2CH |
| 45D | 17 A6 19 ACH | 173D | D5 3D 1B 2CH |
| 46D | 17 9E 19 ACH | 174D | D5 3D 1B 2CH |
| 47D | 17 9E 19 ACH | 175D | D5 3D 1B 2CH |
| 48D | 17 96 19 ACH | 176D | DD 3D 1B 2CH |
| 49D | 1F 96 19 ACH | 177D | DD 3D 1B 2CH |
| 50D | 1F 96 19 ACH | 178D | DD 35 1B 2CH |
| 51D | 1F 8E 19 ACH | 179D | DD 35 1B 2CH |
| 52D | 1F 8E 19 ACH | 180D | DD 35 1B 2CH |
| 53D | 1F 8E 19 ACH | 181D | E5 35 1B 2CH |
| 54D | 27 8E 19 ACH | 182D | E5 35 1B 2CH |
| 55D | 27 8E 1A 2CH | 183D | E5 2D 1B 2CH |
| 56D | 27 8E 1A 2CH | 184D | E5 2D 1B 2CH |

| RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) |
|---|---|---|---|
| 57D | 27 8E 1A 2CH | 185D | E5 2D 3B 2CH |
| 58D | 27 8E 1A 2CH | 186D | ED 2D 4B 2CH |
| 59D | 2F 86 1A 2CH | 187D | ED 2D 1B A8H |
| 60D | 2F 86 1A 2CH | 188D | ED 2D 1B ACH |
| 61D | 2F 86 1A 2CH | 189D | ED 2D 17 ACH |
| 62D | 2F 7E 1A 2CH | 190D | ED 2D 17 ACH |
| 63D | 2F 7E 1A 2CH | 191D | ED 2D 27 ACH |
| 64D | 2F 7E 1A 2CH | 192D | F5 2D 27 ACH |
| 65D | 37 7E 1A 2CH | 193D | F5 2D 27 ACH |
| 66D | 37 7E 1A ACH | 194D | F5 2D 2B ACH |
| 67D | 37 7E 1A ACH | 195D | F5 2D 2B ACH |
| 68D | 37 7E 1A ACH | 196D | F5 2D 2B ACH |
| 69D | 37 7E 1A ACH | 197D | FD 2D 2B ACH |
| 70D | 3F 7E 2A ACH | 198D | FD 2B 2B ACH |
| 71D | 3F 7E 2A ACH | 199D | FD 2B 2B ACH |
| 72D | 3F 76 2A ACH | 200D | FD 2B 2B ACH |
| 73D | 3F 86 2B 2CH | 201D | FD 2B 2B ACH |
| 74D | 3F 7E 2B 2CH | 202D | FD 23 2B ACH |
| 75D | 47 7E 2B 2CH | 203D | FD 23 2B ACH |
| 76D | 47 7E 2F 2CH | 204D | FD 23 2B ACH |
| 77D | 47 7E 2F 2CH | 205D | FD 21 2B ACH |
| 78D | 47 7E 2F 2CH | 206D | FD 21 2B ACH |
| 79D | 47 76 2F 2CH | 207D | FD 29 2B ACH |
| 80D | 4F 76 2F 2CH | 208D | FD 29 2B ACH |
| 81D | 4F 76 2F 2CH | 209D | FD 29 27 ACH |
| 82D | 4F 6E 2F 2CH | 210D | FD 29 37 ACH |
| 83D | 4F 6E 2F 2CH | 211D | FD 29 23 ACH |
| 84D | 4F 6E 2F 2CH | 212D | FD 29 23 ACH |
| 85D | 57 6E 2F 2CH | 213D | FD 29 23 ACH |
| 86D | 57 6E 2F 2CH | 214D | FD 29 23 ACH |
| 87D | 57 6E 3F 2CH | 215D | FD 21 23 ACH |

| RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) |
|---|---|---|---|
| 88D | 57 6E 3F 2CH | 216D | FD 21 23 ACH |
| 89D | 57 6E 3F 2CH | 217D | FD 21 23 ACH |
| 90D | 5F 6E 3F 2CH | 218D | FD 21 33 ACH |
| 91D | 5F 6E 4F 2CH | 219D | FD 21 33 ACH |
| 92D | 5F 6E 4F 2CH | 220D | FD 21 33 ACH |
| 93D | 5F 6E 4F 2CH | 221D | FD 21 43 ACH |
| 94D | 5F 66 4F 2CH | 222D | FD 21 43 ACH |
| 95D | 67 66 4F 2CH | 223D | FD 21 43 ACH |
| 96D | 67 66 4F 2CH | 224D | FC 21 43 ACH |
| 97D | 67 5E 4F 2CH | 225D | FC 21 43 ACH |
| 98D | 67 5E 4F 2CH | 226D | FC 19 43 ACH |
| 99D | 67 66 4F 2CH | 227D | FC 19 43 ACH |
| 100D | 67 66 4F 2CH | 228D | FC 19 43 ACH |
| 101D | 67 66 5F 2CH | 229D | FC 19 43 ACH |
| 102D | 6F 6E 5F 2CH | 230D | FC 19 53 ACH |
| 103D | 6F 6E 6F 2CH | 231D | FC 19 53 ACH |
| 104D | 6F 6E 6F 2CH | 232D | FC 19 53 ACH |
| 105D | 6F 6E 7F 2CH | 233D | FC 19 53 ACH |
| 106D | 6F 6E 7F 2CH | 234D | FC 19 63 ACH |
| 107D | 6F 6E 7F 2CH | 235D | FC 19 63 ACH |
| 108D | 77 66 7F 2CH | 236D | FC 19 63 ACH |
| 109D | 77 66 7F 2CH | 237D | FC 19 73 ACH |
| 110D | 77 5E 6F 2CH | 238D | FC 19 73 ACH |
| 111D | 77 5E 7F 2CH | 239D | FC 19 73 ACH |
| 112D | 77 5E 7F 2CH | 240D | FC 19 73 ACH |
| 113D | 7F 5E 7F 2CH | 241D | FC 19 73 ACH |
| 114D | 7F 5E 8F 2CH | 242D | FC 19 83 ACH |
| 115D | 7F 5E 8F 2CH | 243D | FC 19 83 ACH |
| 116D | 7F 5E 8F 2CH | 244D | FC 19 83 ACH |
| 117D | 87 56 8F 2CH | 245D | FC 19 83 ACH |
| 118D | 87 56 8F 2CH | 246D | FC 19 83 ACH |

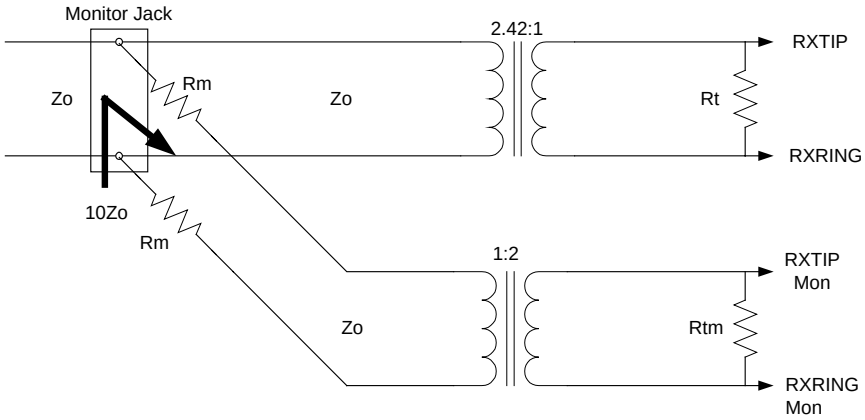
| RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) |
|---|---|---|---|
| 119D | 87 56 8F 2CH | 247D | FC 19 93 ACH |
| 120D | 87 4E 8F 2CH | 248D | FC 19 93 ACH |
| 121D | 87 4E 8F 2CH | 249D | FC 19 93 ACH |
| 122D | 87 4E 8F 2CH | 250D | FC 19 A3 ACH |
| 123D | 8F 4E 9F 2CH | 251D | FC 19 A3 ACH |
| 124D | 8F 4E 9F 2CH | 252D | FC 19 B3 ACH |
| 125D | 8F 4E AF 2CH | 253D | FC 19 B3 ACH |
| 126D | 8F 4E AF 2CH | 254D | FC 19 B3 ACH |
| 127D | 8F 4E AF 2CH | 255D | FC 19 B3 ACH |

The Analog Loss Of Signal feature is available for short haul and ISDN signal levels only. (Other LOS variants are always available via the CDRC Interrupt Status and Alternate Loss of Signal registers.) For short haul and ISDN signal levels, the receiver monitors if the received signal exceeds a predefined peak amplitude and the ALOSV bit is set when this condition is not meet. The change in ALOSV state sets the ALOSI bit and can be enabled to assert the INTB.

The RLPS is able to squelch the data in response to an assertion of ALOS. Since this action is not mandatory, it is not enabled by default. However it can be desirable to do so in which case data squelching can be enabled by setting the SQUELCHE register bit to logic 1.

### 14.6.1 T1 Performance Monitor Mode

The PM4351 COMET can operate in T1 Performance Monitor mode by programming the Equalizer to operate receiving a signal with a 20 dB flat loss from nominal as shown.




Rm = (10Zo - Zo)/2 = 450ohms(T1)
Rt = 18.7Ohms
Rtm = Zo*2^2 = 400Ohms(T1)
Zo = 100ohms

The RLPS receiver values to program the equalizer for T1 Performance Monitor Mode are contained in the below table.

**Table 109 - RLPS Equalizer Lookup Table for T1 Performance Monitor Mode**

| RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) |
|---|---|---|---|---|---|---|---|
| 00D | 03 FE 18 40H | 64D | 03 BE 18 40H | 128D | 03 76 18 40H | 192D | 03 36 18 40H |
| 01D | 03 FE 18 40H | 65D | 03 BE 18 40H | 129D | 03 76 18 40H | 193D | 03 36 18 40H |
| 02D | 03 FE 18 40H | 66D | 03 BE 18 40H | 130D | 03 76 18 40H | 194D | 03 36 18 40H |
| 03D | 03 FE 18 40H | 67D | 03 BE 18 40H | 131D | 03 76 18 40H | 195D | 03 36 18 40H |
| 04D | 03 FE 18 40H | 68D | 03 BE 18 40H | 132D | 03 76 18 40H | 196D | 03 36 18 40H |
| 05D | 03 FE 18 40H | 69D | 03 BE 18 40H | 133D | 03 76 18 40H | 197D | 03 36 18 40H |
| 06D | 03 FE 18 40H | 70D | 03 BE 18 40H | 134D | 03 76 18 40H | 198D | 03 36 18 40H |
| 07D | 03 FE 18 40H | 71D | 03 BE 18 40H | 135D | 03 76 18 40H | 199D | 03 36 18 40H |
| 08D | 03 F6 18 40H | 72D | 03 B6 18 40H | 136D | 03 6E 18 40H | 200D | 03 2E 18 40H |
| 09D | 03 F6 18 40H | 73D | 03 B6 18 40H | 137D | 03 6E 18 40H | 201D | 03 2E 18 40H |
| 10D | 03 F6 18 40H | 74D | 03 B6 18 40H | 138D | 03 6E 18 40H | 202D | 03 2E 18 40H |
| 11D | 03 F6 18 40H | 75D | 03 B6 18 40H | 139D | 03 6E 18 40H | 203D | 03 2E 18 40H |
| 12D | 03 F6 18 40H | 76D | 03 B6 18 40H | 140D | 03 6E 18 40H | 204D | 03 2E 18 40H |
| 13D | 03 F6 18 40H | 77D | 03 B6 18 40H | 141D | 03 6E 18 40H | 205D | 03 2E 18 40H |
| 14D | 03 F6 18 40H | 78D | 03 B6 18 40H | 142D | 03 6E 18 40H | 206D | 03 2E 18 40H |

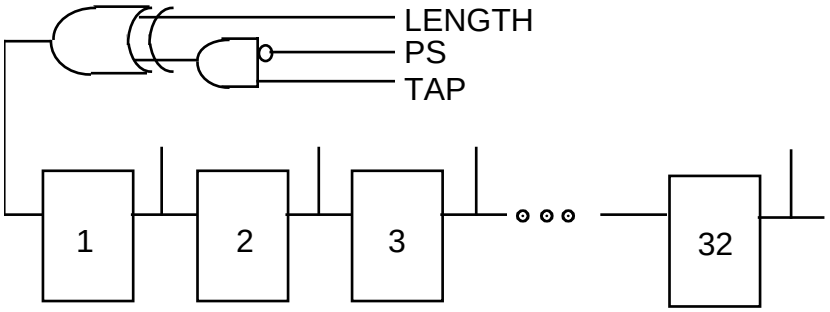
| RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) |
|---|---|---|---|---|---|---|---|
| 15D | 03 F6 18 40H | 79D | 03 B6 18 40H | 143D | 03 6E 18 40H | 207D | 03 2E 18 40H |
| 16D | 03 EE 18 40H | 80D | 03 A6 18 40H | 144D | 03 66 18 40H | 208D | 03 26 18 40H |
| 17D | 03 EE 18 40H | 81D | 03 A6 18 40H | 145D | 03 66 18 40H | 209D | 03 26 18 40H |
| 18D | 03 EE 18 40H | 82D | 03 A6 18 40H | 146D | 03 66 18 40H | 210D | 03 26 18 40H |
| 19D | 03 EE 18 40H | 83D | 03 A6 18 40H | 147D | 03 66 18 40H | 211D | 03 26 18 40H |
| 20D | 03 EE 18 40H | 84D | 03 A6 18 40H | 148D | 03 66 18 40H | 212D | 03 26 18 40H |
| 21D | 03 EE 18 40H | 85D | 03 A6 18 40H | 149D | 03 66 18 40H | 213D | 03 26 18 40H |
| 22D | 03 EE 18 40H | 86D | 03 A6 18 40H | 150D | 03 66 18 40H | 214D | 03 26 18 40H |
| 23D | 03 EE 18 40H | 87D | 03 A6 18 40H | 151D | 03 66 18 40H | 215D | 03 26 18 40H |
| 24D | 03 E6 18 40H | 88D | 03 9E 18 40H | 152D | 03 5E 18 40H | 216D | 03 1E 18 40H |
| 25D | 03 E6 18 40H | 89D | 03 9E 18 40H | 153D | 03 5E 18 40H | 217D | 03 1E 18 40H |
| 26D | 03 E6 18 40H | 90D | 03 9E 18 40H | 154D | 03 5E 18 40H | 218D | 03 1E 18 40H |
| 27D | 03 E6 18 40H | 91D | 03 9E 18 40H | 155D | 03 5E 18 40H | 219D | 03 1E 18 40H |
| 28D | 03 E6 18 40H | 92D | 03 9E 18 40H | 156D | 03 5E 18 40H | 220D | 03 1E 18 40H |
| 29D | 03 E6 18 40H | 93D | 03 9E 18 40H | 157D | 03 5E 18 40H | 221D | 03 1E 18 40H |
| 30D | 03 E6 18 40H | 94D | 03 9E 18 40H | 158D | 03 5E 18 40H | 222D | 03 1E 18 40H |
| 31D | 03 E6 18 40H | 95D | 03 9E 18 40H | 159D | 03 5E 18 40H | 223D | 03 1E 18 40H |
| 32D | 03 DE 18 40H | 96D | 03 96 18 40H | 160D | 03 56 18 40H | 224D | 03 16 18 40H |
| 33D | 03 DE 18 40H | 97D | 03 96 18 40H | 161D | 03 56 18 40H | 225D | 03 16 18 40H |
| 34D | 03 DE 18 40H | 98D | 03 96 18 40H | 162D | 03 56 18 40H | 226D | 03 16 18 40H |
| 35D | 03 DE 18 40H | 99D | 03 96 18 40H | 163D | 03 56 18 40H | 227D | 03 16 18 40H |
| 36D | 03 DE 18 40H | 100D | 03 96 18 40H | 164D | 03 56 18 40H | 228D | 03 16 18 40H |
| 37D | 03 DE 18 40H | 101D | 03 96 18 40H | 165D | 03 56 18 40H | 229D | 03 16 18 40H |
| 38D | 03 DE 18 40H | 102D | 03 96 18 40H | 166D | 03 56 18 40H | 230D | 03 16 18 40H |
| 39D | 03 DE 18 40H | 103D | 03 96 18 40H | 167D | 03 56 18 40H | 231D | 03 16 18 40H |
| 40D | 03 D6 18 40H | 104D | 03 8E 18 40H | 168D | 03 4E 18 40H | 232D | 03 0E 18 40H |
| 41D | 03 D6 18 40H | 105D | 03 8E 18 40H | 169D | 03 4E 18 40H | 233D | 03 0E 18 40H |
| 42D | 03 D6 18 40H | 106D | 03 8E 18 40H | 170D | 03 4E 18 40H | 234D | 03 0E 18 40H |
| 43D | 03 D6 18 40H | 107D | 03 8E 18 40H | 171D | 03 4E 18 40H | 235D | 03 0E 18 40H |
| 44D | 03 D6 18 40H | 108D | 03 8E 18 40H | 172D | 03 4E 18 40H | 236D | 03 0E 18 40H |
| 45D | 03 D6 18 40H | 109D | 03 8E 18 40H | 173D | 03 4E 18 40H | 237D | 03 0E 18 40H |
| 46D | 03 D6 18 40H | 110D | 03 8E 18 40H | 174D | 03 4E 18 40H | 238D | 03 0E 18 40H |

| RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) | RAM Address | Content (MSB..LSB) |
|---|---|---|---|---|---|---|---|
| 47D | 03 D6 18 40H | 111D | 03 8E 18 40H | 175D | 03 4E 18 40H | 239D | 03 0E 18 40H |
| 48D | 03 CE 18 40H | 112D | 03 86 18 40H | 176D | 03 46 18 40H | 240D | 03 0E 18 40H |
| 49D | 03 CE 18 40H | 113D | 03 86 18 40H | 177D | 03 46 18 40H | 241D | 03 06 18 40H |
| 50D | 03 CE 18 40H | 114D | 03 86 18 40H | 178D | 03 46 18 40H | 242D | 03 06 18 40H |
| 51D | 03 CE 18 40H | 115D | 03 86 18 40H | 179D | 03 46 18 40H | 243D | 03 06 18 40H |
| 52D | 03 CE 18 40H | 116D | 03 86 18 40H | 180D | 03 46 18 40H | 244D | 03 06 18 40H |
| 53D | 03 CE 18 40H | 117D | 03 86 18 40H | 181D | 03 46 18 40H | 245D | 03 06 18 40H |
| 54D | 03 CE 18 40H | 118D | 03 86 18 40H | 182D | 03 46 18 40H | 246D | 03 06 18 40H |
| 55D | 03 CE 18 40H | 119D | 03 86 18 40H | 183D | 03 46 18 40H | 247D | 03 06 18 40H |
| 56D | 03 C6 18 40H | 120D | 03 7E 18 40H | 184D | 03 3E 18 40H | 248D | 03 06 18 40H |
| 57D | 03 C6 18 40H | 121D | 03 7E 18 40H | 185D | 03 3E 18 40H | 249D | 03 06 18 40H |
| 58D | 03 C6 18 40H | 122D | 03 7E 18 40H | 186D | 03 3E 18 40H | 250D | 03 06 18 40H |
| 59D | 03 C6 18 40H | 123D | 03 7E 18 40H | 187D | 03 3E 18 40H | 251D | 03 06 18 40H |
| 60D | 03 C6 18 40H | 124D | 03 7E 18 40H | 188D | 03 3E 18 40H | 252D | 03 06 18 40H |
| 61D | 03 C6 18 40H | 125D | 03 7E 18 40H | 189D | 03 3E 18 40H | 253D | 03 06 18 40H |
| 62D | 03 C6 18 40H | 126D | 03 7E 18 40H | 190D | 03 3E 18 40H | 254D | 03 06 18 40H |
| 63D | 03 C6 18 40H | 127D | 03 7E 18 40H | 191D | 03 3E 18 40H | 255D | 03 06 18 40H |

## 14.7 Using the Test Pattern Generator

The pattern generator can be configured to generate pseudo random patterns or repetitive patterns as shown in the figure below:

**Figure 38 - Pattern Generator Structure**



The pattern generator consists of a 32-bit shift register and a single XOR gate. The XOR gate output is fed into the first stage of the shift register. The XOR gate inputs are determined by values written to the length register (PL[4:0]) and the tap register (PT[4:0], when the PS bit is low). When PS is high, the pattern detector functions as a recirculating shift register, with length determined by PL[4:0].

### 14.7.1 Common Test Patterns

The PRGD can be configured to monitor the standardized pseudo random and repetitive patterns described in ITU-T O.151, O.152 and O.153. The register configurations required to generate these patterns and others are indicated in the two tables below:

**Table 110 - Pseudo-Random Pattern Generation (PS bit = 0)**

| Pattern Type | PT | PL | PI#1 | PI#2 | PI#3 | PI#4 | TINV | RINV |
|---|---|---|---|---|---|---|---|---|
| $2^3$ -1 | 00 | 02 | FF | FF | FF | FF | 0 | 0 |
| $2^4$ -1 | 00 | 03 | FF | FF | FF | FF | 0 | 0 |
| $2^5$-1 | 01 | 04 | FF | FF | FF | FF | 0 | 0 |
| $2^6$ -1 | 04 | 05 | FF | FF | FF | FF | 0 | 0 |
| $2^7$ -1 | 00 | 06 | FF | FF | FF | FF | 0 | 0 |
| $2^7$ -1 (Fractional T1 LB Activate) | 03 | 06 | FF | FF | FF | FF | 0 | 0 |
| $2^7$ -1 (Fractional T1 LB Deactivate) | 03 | 06 | FF | FF | FF | FF | 1 | 1 |
| $2^9$ -1 (O.153) | 04 | 08 | FF | FF | FF | FF | 0 | 0 |
| $2^{10}$ -1 | 02 | 09 | FF | FF | FF | FF | 0 | 0 |
| $2^{11}$ -1 (O.152, O.153) | 08 | 0A | FF | FF | FF | FF | 0 | 0 |

| Pattern Type | PT | PL | PI#1 | PI#2 | PI#3 | PI#4 | TINV | RINV |
|---|---|---|---|---|---|---|---|---|
| $2^{15}$ -1 (O.151) | 0D | 0E | FF | FF | FF | FF | 1 | 1 |
| $2^{17}$ -1 | 02 | 10 | FF | FF | FF | FF | 0 | 0 |
| $2^{18}$ -1 | 06 | 11 | FF | FF | FF | FF | 0 | 0 |
| $2^{20}$ -1 (O.153) | 02 | 13 | FF | FF | FF | FF | 0 | 0 |
| $2^{20}$ -1 (O.151 QRSS bit=1) | 10 | 13 | FF | FF | FF | FF | 0 | 0 |
| $2^{21}$ -1 | 01 | 14 | FF | FF | FF | FF | 0 | 0 |
| $2^{22}$ -1 | 00 | 15 | FF | FF | FF | FF | 0 | 0 |
| $2^{23}$ -1 (O.151) | 11 | 16 | FF | FF | FF | FF | 1 | 1 |
| $2^{25}$ -1 | 02 | 18 | FF | FF | FF | FF | 0 | 0 |
| $2^{28}$ -1 | 02 | 1B | FF | FF | FF | FF | 0 | 0 |
| $2^{29}$ -1 | 01 | 1C | FF | FF | FF | FF | 0 | 0 |
| $2^{31}$ -1 | 02 | 1E | FF | FF | FF | FF | 0 | 0 |

**Table 111 - Repetitive Pattern Generation (PS bit = 1)**

| Pattern Type | PT | PL | PI#1 | PI#2 | PI#3 | PI#4 | TINV | RINV |
|---|---|---|---|---|---|---|---|---|
| All ones | 00 | 00 | FF | FF | FF | FF | 0 | 0 |
| All zeros | 00 | 00 | FE | FF | FF | FF | 0 | 0 |
| Alternating ones/zeros | 00 | 01 | FE | FF | FF | FF | 0 | 0 |
| Double alternating ones/zeros | 00 | 03 | FC | FF | FF | FF | 0 | 0 |
| 3 in 24 | 00 | 17 | 22 | 00 | 20 | FF | 0 | 0 |
| 1 in 16 | 00 | 0F | 01 | 00 | FF | FF | 0 | 0 |
| 1 in 8 | 00 | 07 | 01 | FF | FF | FF | 0 | 0 |

| Pattern Type | PT | PL | PI#1 | PI#2 | PI#3 | PI#4 | TINV | RINV |
|---|---|---|---|---|---|---|---|---|
| 1 in 4 | 00 | 03 | F1 | FF | FF | FF | 0 | 0 |
| Inband loopback activate | 00 | 04 | F0 | FF | FF | FF | 0 | 0 |
| Inband loopback deactivate | 00 | 02 | FC | FF | FF | FF | 0 | 0 |

**Notes for the Pseudo Random and Repetitive Pattern Generation Tables**

1. The PS bit and the QRSS bit are contained in the PRGD Control register
2. PT = Tap Register
3. PL = Shift Register Length Register
4. PI#1 = PRGD Pattern Insertion #1 Register
5. PI#2 = PRGD Pattern Insertion #2 Register
6. PI#3 = PRGD Pattern Insertion #3 Register
7. PI#4 = PRGD Pattern Insertion #4 Register
8. The TINV bit and the RINV bit are contained in the PRGD Control register

## 14.8 Using the Loopback Modes

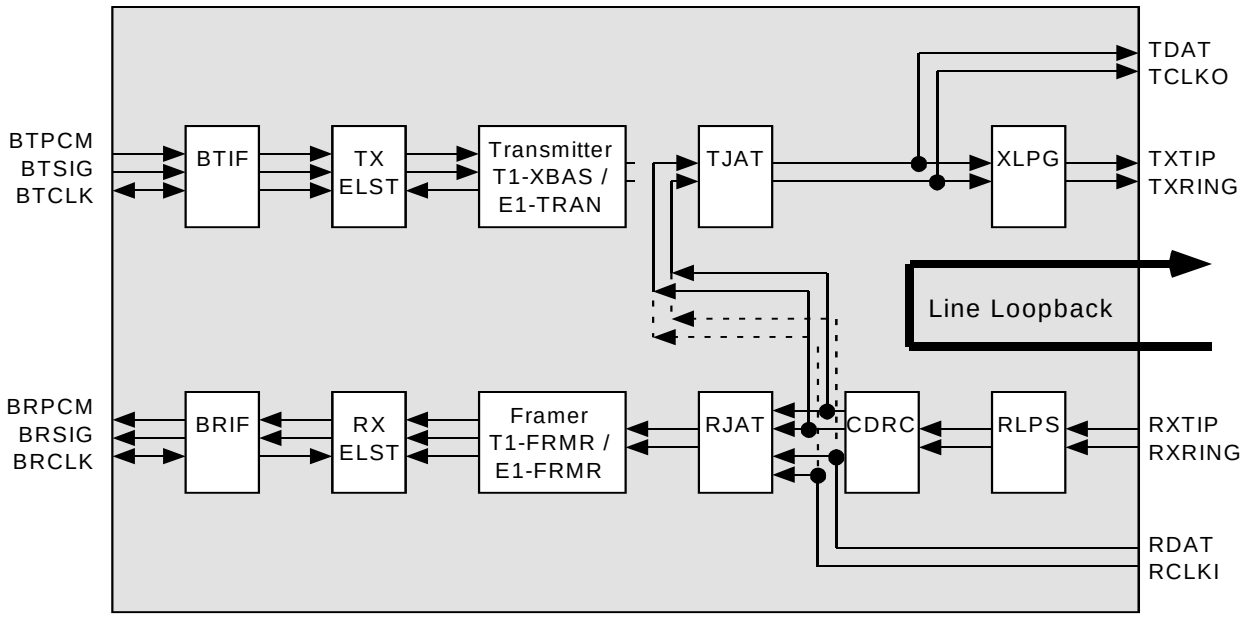
The COMET provides four loopback modes to aid in network and system diagnostics. The network loopbacks (Payload and Line) can be initiated at any time via the µP interface, but are usually initiated once an inband loopback activate code is detected. The system Diagnostic Digital loopback can be initiated at any time by the system via the µP interface to check the path of system data through the framer. The Per-DS0 loopback permits the payload to be looped-back on a per-DS0 basis to allow network testing without taking an entire link off-line.

### 14.8.1 Line Loopback

When LINE loopback (LINELB) is initiated by setting the LINELB bit in the Master Diagnostics Register (00AH) to logic 1, the COMET is configured to internally connect the recovered data to the transmit jitter attenuator, TJAT. In analog mode (RUNI is logic 0), the data sent to the TJAT is the recovered data

from the output of the CDRC block. In digital mode (RUNI is logic 1), the data sent to the TJAT is a sampled version of the RDAT digital input. Note that when line loopback is enabled, the contents of the TJAT Reference Clock Divisor and Output Clock Divisor registers should be programmed to 2FH in T1 or FFH in E1 to correctly attenuate the jitter on the receive clock. Conceptually, the data flow through the COMET in this loopback mode is illustrated in Figure 39. In this figure, the dashed lines represent connections in digital mode (RUNI is logic 1).

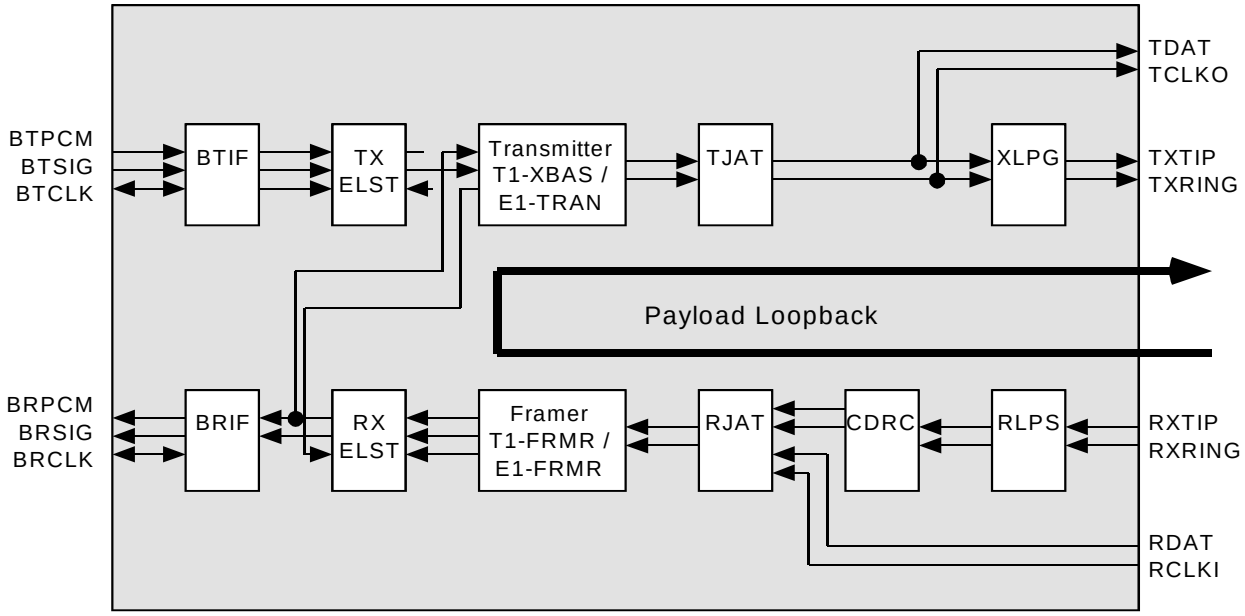
**Figure 39 - Line Loopback**




## 14.8.2 Payload Loopback

When PAYLOAD loopback (PAYLB) is initiated by setting the PAYLB bit in the Master Diagnostics Register (00AH) to logic 1, the COMET is configured to internally connect the output of its RX-ELST to the PCM input of its transmitter block. The data read out of RX-ELST is timed to the transmitter clock, and the transmit frame alignment indication is used to synchronize the output frame alignment of RX-ELST. The transmit frame alignment is either arbitrary (when the TX-ELST is used) or is specified by the BTFP input (when the TX-ELST is bypassed). Conceptually, the data flow through the COMET in this loopback mode is illustrated in Figure 40. Note that because the transmit and receive streams are not superframe aligned, any robbed-bit signaling in the receive stream will not fall in the correct frame once looped back and that transmit robbed-bit signaling will overwrite the looped back data if signaling insertion is enabled.

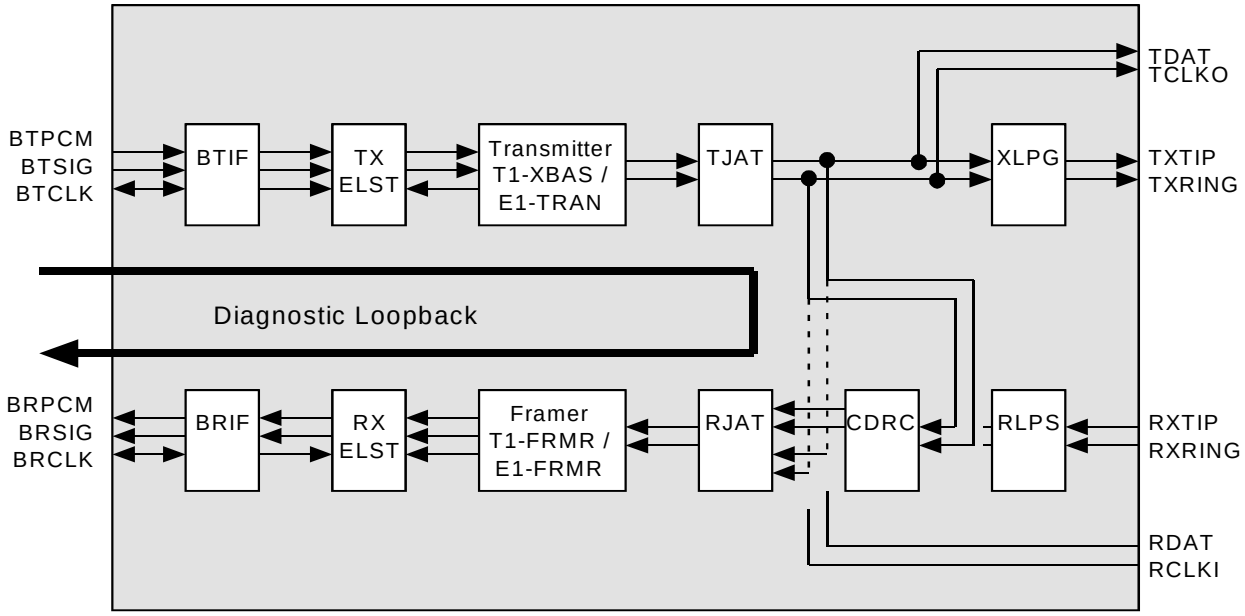
**Figure 40 - Payload Loopback**




### 14.8.3 Diagnostic Digital Loopback

When Diagnostic Digital loopback (DDLB) mode is initiated by setting the DDLB bit in the Master Diagnostics Register (00AH) to logic 1, the COMET is configured to internally direct the output of the TJAT to the inputs of the receiver section. In analog mode (RUNI is logic 0), the dual-rail RZ outputs of the TJAT are directed to the dual-rail inputs of the CDRC. In digital mode (RUNI is logic 1), the single-rail NRZ outputs of the TJAT are directed to the inputs of the RJAT. When configured for diagnostic digital loopback, the TUNI and RUNI bits must be set to the same value. Conceptually, the data flow through the COMET in this loopback condition is illustrated in Figure 41. In this figure, the dashed lines represent connections in digital mode (RUNI is logic 1).

**Figure 41 - Diagnostic Digital Loopback**




### 14.8.4 Per-Channel Loopback

The T1 or E1 payload may be looped back on a per-channel or per-timeslot basis through the use of the TPSC. If all channels are looped back, the result is very similar to Payload Loopback. In order for per-channel loopback to operated correctly, the receive elastic store, RX-ELST, must be bypassed by setting the RXELSTBYP bit to logic 1 and the backplane receive interface must be set to clock master by setting the CMODE bit in the BRIF Receive Backplane Configuration register to logic 0. The LOOP bit must be set to logic 1 in the TPSC Internal Registers for each channel/timeslot desired to be looped back, and the PCCE bit in the TPSC Configuration register must be set to logic 1. When all these parameters are configured, the incoming receive channels/timeslots selected will overwrite their corresponding outgoing transmit channels/timeslots; the remaining transmit channels will pass through intact. Note that because the transmit and receive streams are not superframe aligned, any robbed-bit signaling in the receive stream will not fall in the correct frame once looped back and that transmit robbed-bit signaling will overwrite the looped back channel data if signaling insertion is enabled.

## 14.9 Using the Per-Channel Serial Controllers

### 14.9.1 Initialization

Before the TPSC (RPSC) block can be used, a proper initialization of the internal registers must be performed to eliminate erroneous control data from being produced on the block outputs. The output control streams should be disabled by setting the PCCE bit in the TPSC (RPSC) Configuration Register to logic 0. Then, all 96 locations of the TPSC (RPSC) must be filled with valid data. Finally, the output streams can be enabled by setting the PCCE bit in the TPSC (RPSC) Configuration Register to logic 1.

### 14.9.2 Direct Access Mode

Direct access mode to the TPSC or RPSC is not used in the COMET. However, direct access mode is selected by default whenever the COMET is reset. The IND bit within the TPSC and RPSC Configuration Registers must be set to logic 1 after a reset is applied.

### 14.9.3 Indirect Access Mode

Indirect access mode is selected by setting the IND bit in the TPSC or RPSC Configuration Register to logic 1. When using the indirect access mode, the status of the BUSY indication bit should be polled to determine the status of the microprocessor access: when the BUSY bit is logic 1, the TPSC or RPSC is processing an access request; when the BUSY bit is logic 0, the TPSC or RPSC has completed the request.

The indirect write programming sequence for the TPSC (RPSC) is as follows:

1. Check that the BUSY bit in the TPSC (RPSC) µP Access Status Register is logic 0.

2. Write the channel data to the TPSC (RPSC) Channel Indirect Data Buffer register.

3. Write RWB=0 and the channel address to the TPSC (RPSC) Channel Indirect Address/Control Register.

4. Poll the BUSY bit until it goes to logic 0. The BUSY bit will go to logic 1 immediately after step 3 and remain at logic 1 until the request is complete.

5. If there is more data to be written, go back to step 1.

The indirect read programming sequence for the TPSC (RPSC) is as follows:

1. Check that the BUSY bit in the TPSC (RPSC) µP Access Status Register is logic 0.

2. Write RWB=1 and the channel address to the TPSC (RPSC) Channel Indirect Address/Control Register.

3. Poll the BUSY bit, waiting until it goes to a logic 0. The BUSY bit will go to logic 1 immediately after step 2 and remain at logic 1 until the request is complete.

4. Read the requested channel data from the TPSC (RPSC) Channel Indirect Data Buffer register.

5. If there is more data to be read, go back to step 1.

## 14.10 Isolating an Interrupt

When the INTB pin goes low, the following procedure may be used to isolate the interrupt source.

1. Read the Interrupt Source Registers (Registers 007H, 008H and 009H). The bit corresponding to any block with an outstanding interrupt will be set to logic 1 in these registers.

2. Read the register(s) containing the interrupt status bits of the interrupting block in order to determine the event causing the interrupt. A typical block interrupt has two related bits: an enable bit (EVENTE for instance) and an interrupt status bit (EVENTI for instance). EVENTI will go to logic 1 when the triggering event occurs, and goes low when the register containing it is read; the setting of EVENTE has no effect on the value of EVENTI. However, a chip interrupt will only be caused if EVENTE is logic 1 and EVENTI is logic 1. Thus, both the interrupt status bit(s) and their respective enables may need to be read in order to determine which event caused an interrupt. Specific interrupt setups may differ from this model, however.

## 14.11 Using the Performance Monitor Counter Values

All PMON event counters are of sufficient length so that the probability of counter saturation over a one second interval is very small (less than 0.001%). The odds of any one of the counters saturating during a one second sampling interval go up as the bit error rate (BER) increases. At some point, the probability of counter saturation reaches 50%. This point varies, depending upon the framing format and the type of event being counted. The BER at which the probability of

counter saturation reaches 50% is shown for various counters in Table 112 for E1 mode, and in Table 113 for T1 mode.

**Table 112 - PMON Counter Saturation Limits (E1 mode)**

| Counter | BER |
|---|---|
| LCV | $4.0 \times 10^{-3}$ |
| FER | $4.0 \times 10^{-3}$ |
| CRCE | cannot saturate |
| FEBE | cannot saturate |

**Table 113 - PMON Counter Saturation Limits (T1 mode)**

| Counter | Format | BER |
|---|---|---|
| LCV | all | $5.3 \times 10^{-3}$ |
| FER | SF | $1.6 \times 10^{-3}$ |
| | T1DM | $1.6 \times 10^{-3}$ |
| | SLC®96 | $3.2 \times 10^{-2}$ |
| | ESF | $6.4 \times 10^{-2}$ |
| CRCE | SF | $1.28 \times 10^{-1}$ |
| | T1DM | $1.83 \times 10^{-2}$ |
| | SLC®96 | $2.56 \times 10^{-1}$ |
| | ESF | cannot saturate |

Below these 50% points, the relationship between the BER and the counter event count (averaged over many one second samples) is essentially linear. Above the 50% point, the relationship between BER and the average counter event count is highly non-linear due to the likelihood of counter saturation. The following figures show this relationship for various counters and framing formats. These graphs can be used to determine the BER, given the average event count. In general, if the BER is above $10^{-3}$, the average counter event count cannot be used to determine the BER without considering the statistical effect of occasional counter saturation.

The following figures illustrate the expected count values for a range of Bit Error Ratios in E1 mode.

**Figure 42 - LCV Count vs. BER (E1 mode)**

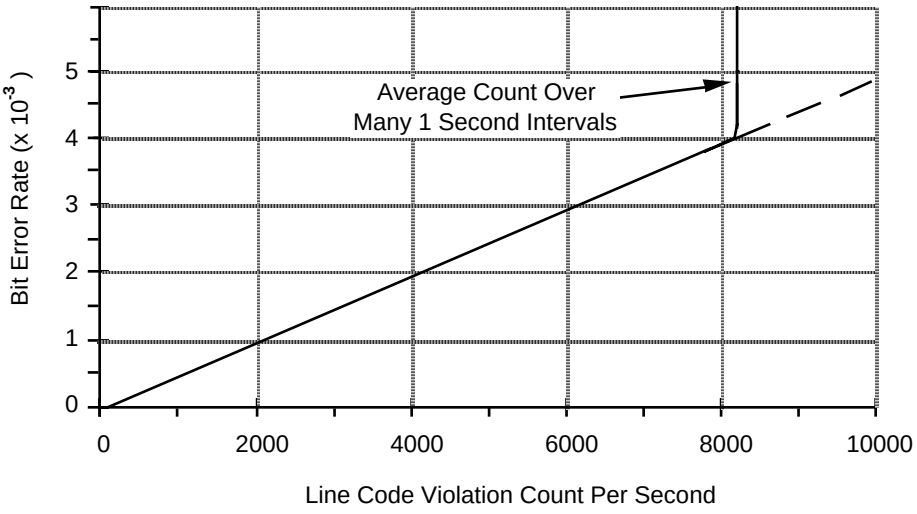
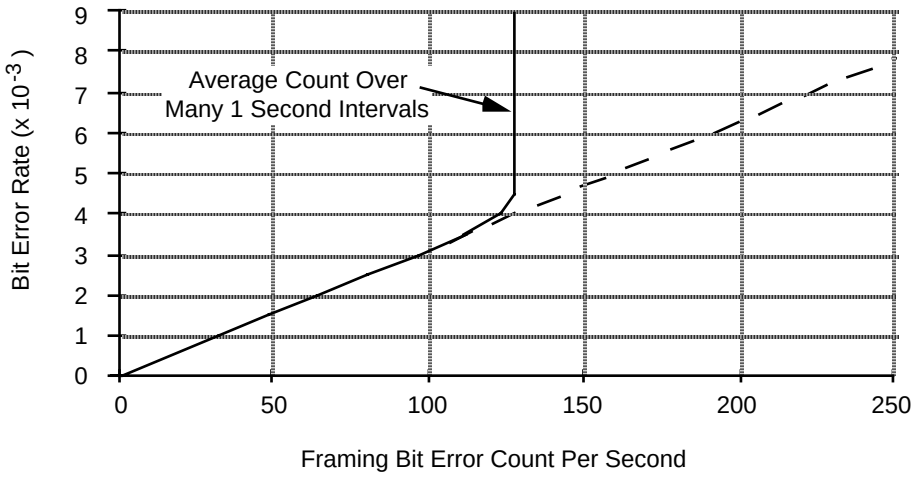



**Figure 43 - FER Count vs. BER (E1 mode)**



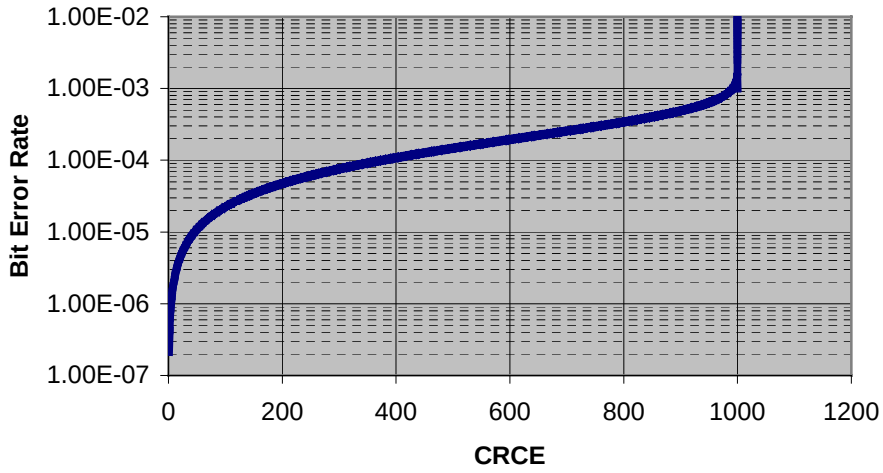

Since the maximum number of CRC sub-multiframes that can occur in one second is 1000, the 10-bit FEBE and CRCE counters cannot saturate in one second. Despite this, there is not a linear relationship between BER and CRC-4 block errors due to the nature of the CRC-4 calculation. At BERs below $10^{-4}$, there tends to be no more than one bit error per sub-multiframe, so the number of CRC-4 errors is generally equal to the number of bit errors, which is directly related to the BER. However, at BERs above $10^{-4}$, each CRC-4 error is often

due to more than one bit error. Thus, the relationship between BER and CRCE count becomes non-linear above a $10^{-4}$ BER. This must be taken into account when using CRC-4 counts to determine the BER. Since FEBEs are indications of CRCEs at the far end, and are accumulated identically to CRCEs, the same explanation holds for the FEBE event counter.

The bit error rate for E1 can be calculated from the one-second PMON CRCE count by the following equation:

$$\textbf{Bit Error Rate} = 1 - 10^{\left(\frac{\log\left(1-\frac{8}{8000}CRCE\right)}{8*256}\right)}$$

**Figure 44 - CRCE Count vs. BER (E1 mode)**




The following figures illustrate the expected count values for a range of Bit Error Ratios in T1 mode.

**Figure 45 - LCV Count vs. BER (T1 mode)**

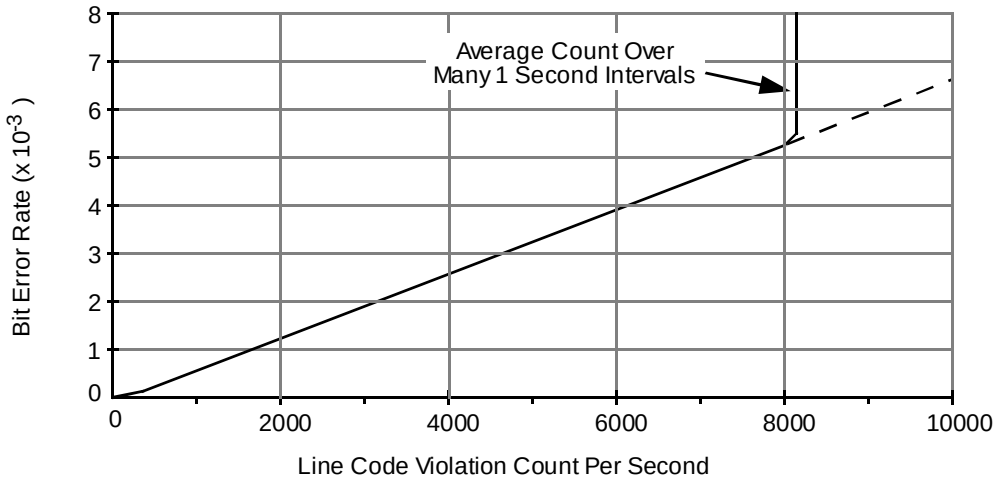
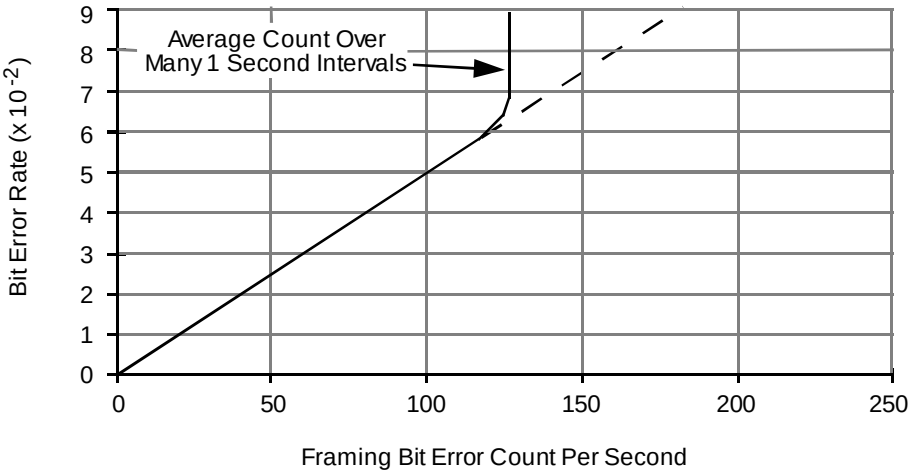



**Figure 46 - FER Count vs. BER (T1 ESF mode)**

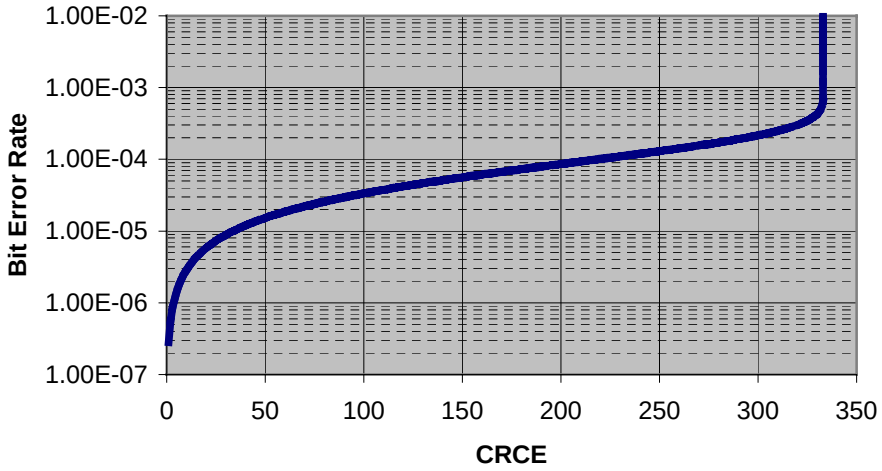



Since the maximum number of ESF superframes that can occur in one second is 333, the 9-bit BEE counter cannot saturate in one second in ESF framing format. Despite this, there is not a linear relationship between BER and BEE count, due to the nature of the CRC-6 calculation. At BERs below $10^{-4}$, there tends to be no more than one bit error per superframe, so the number of CRC-6 errors is generally equal to the number of bit errors, which is directly related to the BER. However, at BERs above $10^{-4}$, each CRC-6 error is often due to more than one bit error. Thus, the relationship between BER and BEE count becomes non-linear above a $10^{-4}$ BER. This must be taken into account when using ESF CRC-6 counts to determine the BER.

The bit error rate for T1 ESF can be calculated from the one-second PMON CRCE count by the following equation:

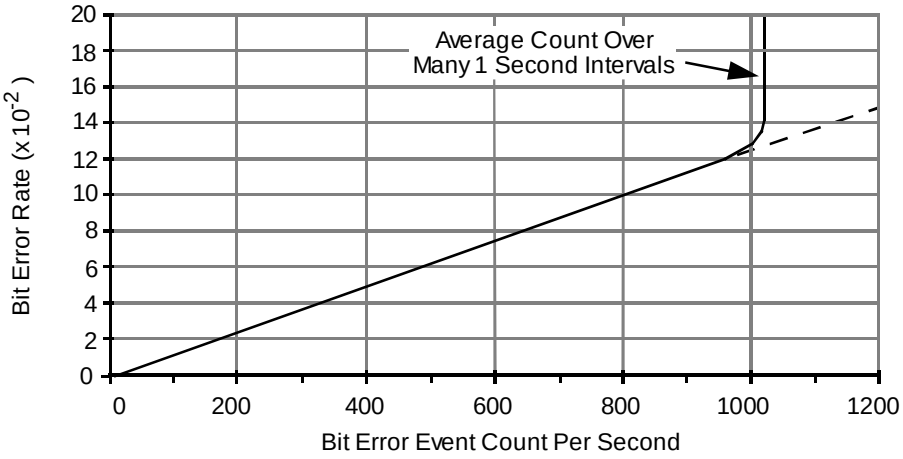
$$\text{Bit Error Rate} = 1 - 10^{\left(\frac{\log\left(1-\frac{24}{8000}BEE\right)}{24*193}\right)}$$

**Figure 47 - CRCE Count vs. BER (T1 ESF mode)**




For T1 SF format, the CRCE and FER counts are identical, but the FER counter is smaller and should be ignored.

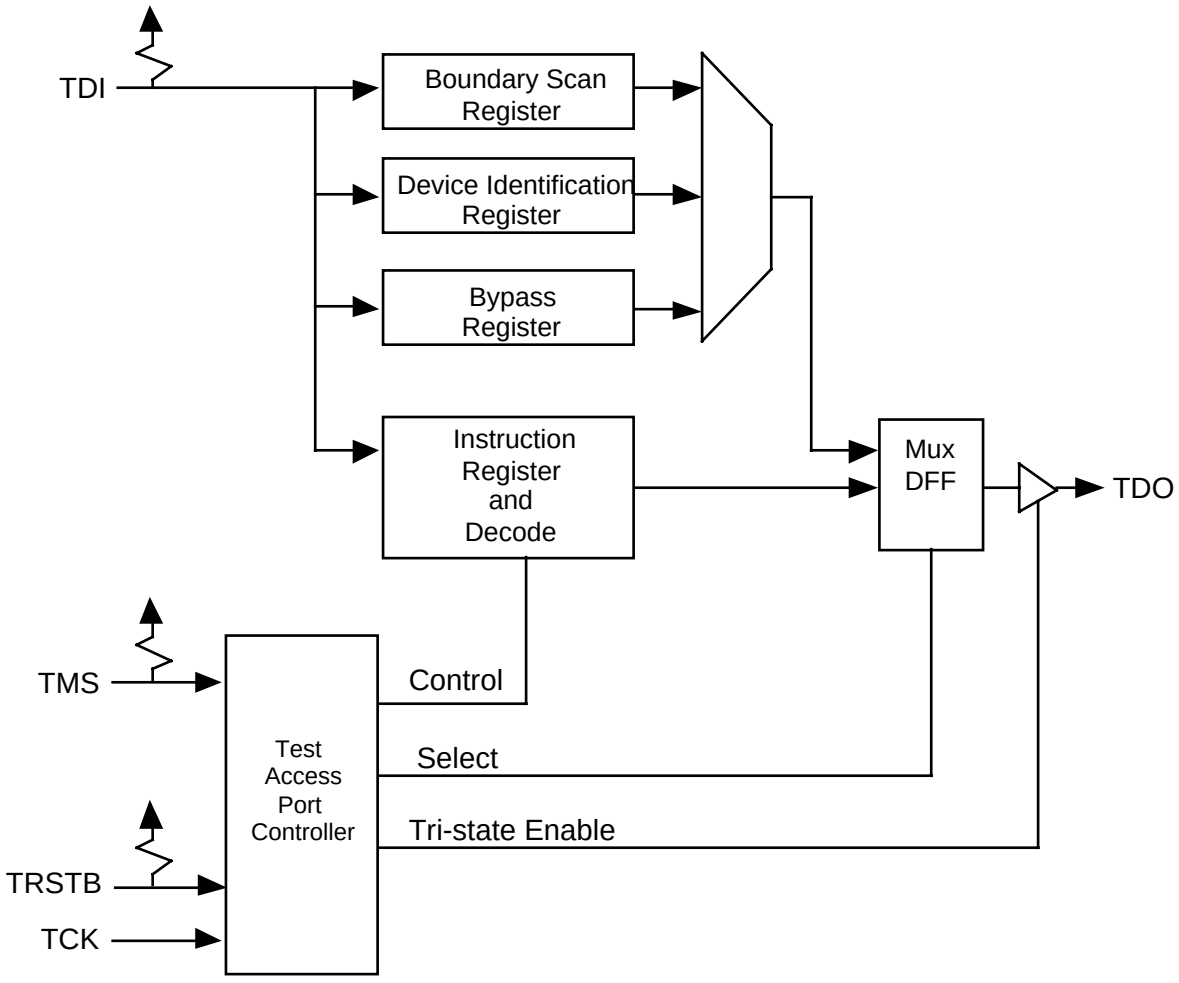
**Figure 48 - CRCE Count vs. BER (T1 SF mode)**



## 14.12 JTAG Support

The COMET supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown in Figure 49.

**Figure 49 - Boundary Scan Architecture**




The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register

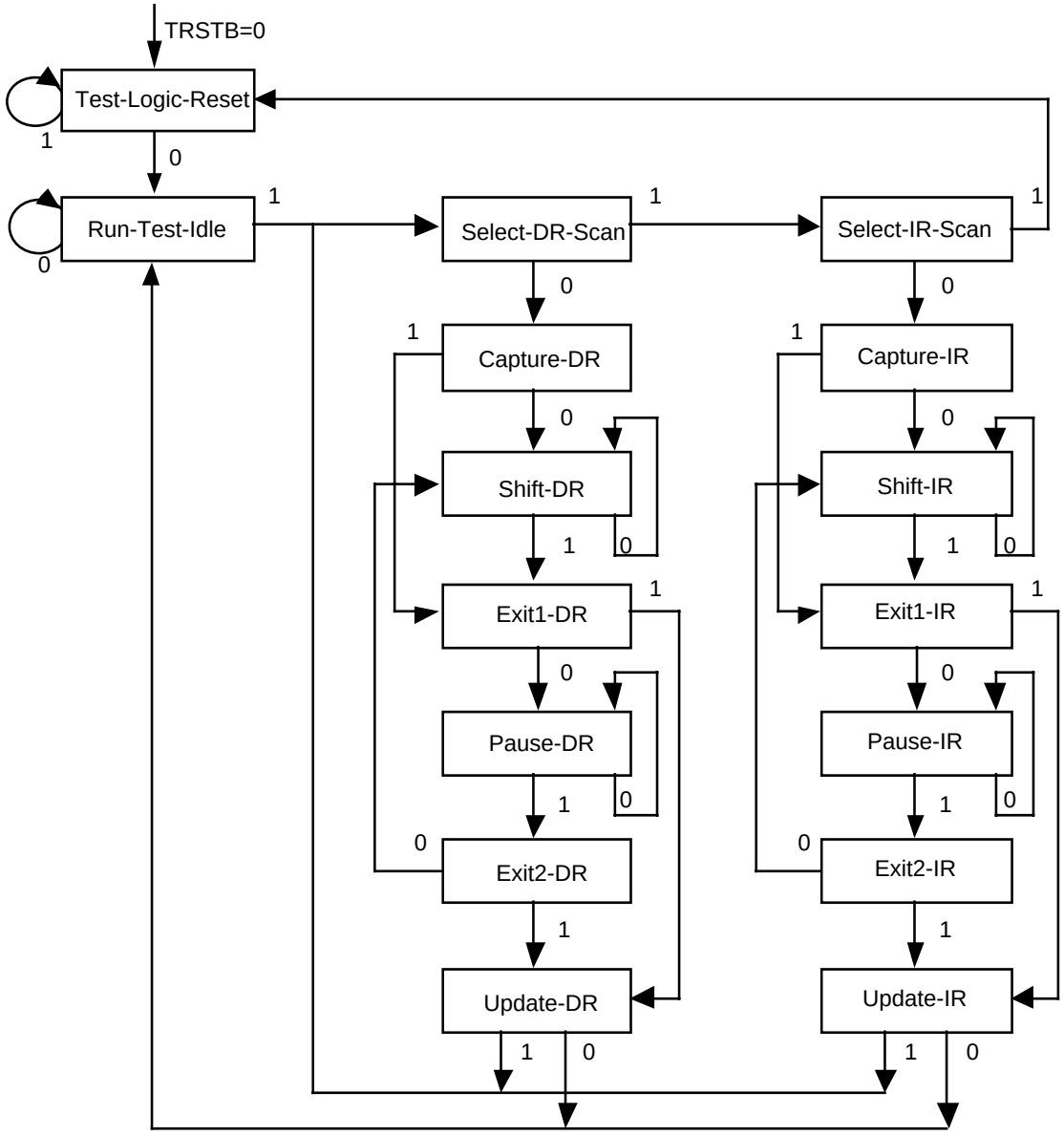
and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input TDI to primary output TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output TDO. In addition, patterns can be shifted in on primary input TDI and forced onto all digital outputs.

## TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary TMS. The finite state machine is shown in Figure 50.

**Figure 50 - TAP Controller Finite State Machine**




## Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP

controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

**Run-Test-Idle**

The run test/idle state is used to execute tests.

**Capture-DR**

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

**Shift-DR**

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

**Update-DR**

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

**Capture-IR**

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

**Shift-IR**

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

**Update-IR**

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

## Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects an serial test data register path between input TDI and output TDO.

### BYPASS

The bypass instruction shifts data from input TDI to output TDO with one TCK clock period delay. The instruction is used to bypass the device.

### EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

### SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

### IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

### STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and

TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out TDO using the Shift-DR state.

## Boundary Scan Register

The boundary scan register is made up of 59 boundary scan cells, divided into input observation (in_cell), output (out_cell), and bidirectional (io_cell) cells. These cells are detailed in the pages which follow. The first 32 cells (58 down to 27) form the ID code register, and carry the code 443510CD for revision E COMET devices and 543510CD for revision F COMET devices. The remaining cells also have values which may be captured during the idcode instruction and shifted out if desired; these are included in brackets for reference. The cells are arranged as follows:

### Table 114 - Boundary Scan Register

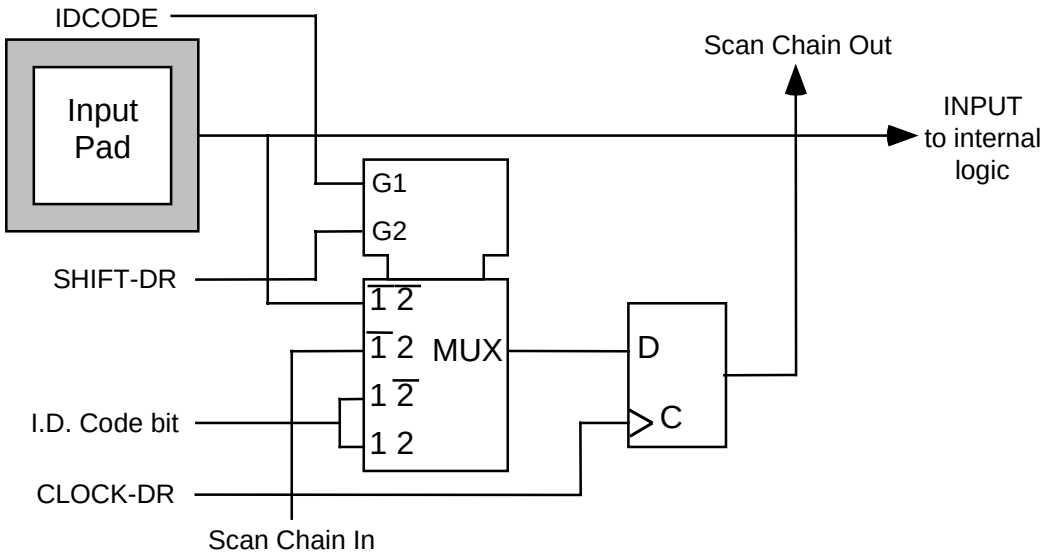
| Pin/ Enable | Register Bit | Cell Type | I.D Bit. | Pin/ Enable | Register Bit | Cell Type | I.D. Bit |
|---|---|---|---|---|---|---|---|
| HIZ[3,4] | 58 | OUT_CELL | 0 [5] | D6_OEB [1] | 28 | OUT_CELL | 0 |
| XCLK | 57 | IN_CELL | 1 [5] | D7 | 27 | IO_CELL | 1 |
| TCLKI | 56 | IN_CELL | 0 [5] | D7_OEB [1] | 26 | OUT_CELL | (0) |
| TCLKO | 55 | OUT_CELL | 0 [5] | A0 | 25 | IN_CELL | (0) |
| TDAT | 54 | OUT_CELL | 0 | A1 | 24 | IN_CELL | (0) |
| TFP | 53 | OUT_CELL | 1 | A2 | 23 | IN_CELL | (0) |
| BTCLK | 52 | IO_CELL | 0 | A3 | 22 | IN_CELL | (0) |
| BTCLK_OEB [1] | 51 | OUT_CELL | 0 | A4 | 21 | IN_CELL | (0) |
| BTPCM | 50 | IN_CELL | 0 | A5 | 20 | IN_CELL | (0) |
| BTSIG | 49 | IN_CELL | 0 | A6 | 19 | IN_CELL | (0) |
| BTFP | 48 | IO_CELL | 1 | A7 | 18 | IN_CELL | (0) |
| BTFP_OEB [1] | 47 | OUT_CELL | 1 | A8 | 17 | IN_CELL | (0) |
| CSB | 46 | IN_CELL | 0 | ALE | 16 | IN_CELL | (0) |
| RSTB | 45 | IN_CELL | 1 | BRFP | 15 | IO_CELL | (0) |
| RDB | 44 | IN_CELL | 0 | BRFP_OEB [1] | 14 | OUT_CELL | (0) |
| WRB | 43 | IN_CELL | 1 | BRSIG | 13 | OUT_CELL | (0) |
| INTB | 42 | OUT_CELL | 0 | BRSIG_OEB [2] | 12 | OUT_CELL | (0) |
| D0 | 41 | IO_CELL | 0 | BRPCM | 11 | OUT_CELL | (0) |
| D0_OEB [1] | 40 | OUT_CELL | 0 | BRPCM_OEB [2] | 10 | OUT_CELL | (0) |
| D1 | 39 | IO_CELL | 1 | BRCLK | 9 | IO_CELL | (0) |

| Pin/ Enable | Register Bit | Cell Type | I.D Bit. | Pin/ Enable | Register Bit | Cell Type | I.D. Bit |
|---|---|---|---|---|---|---|---|
| D1_OEB [1] | 38 | OUT_CELL | 0 | BRCLK_OEB [1] | 8 | OUT_CELL | (0) |
| D2 | 37 | IO_CELL | 0 | RSYNC | 7 | OUT_CELL | (0) |
| D2_OEB [1] | 36 | OUT_CELL | 0 | RLCKI | 6 | IO_CELL | (0) |
| D3 | 35 | IO_CELL | 0 | RCLKI_OEB [1] | 5 | OUT_CELL | (0) |
| D3_OEB [1] | 34 | OUT_CELL | 1 | RDAT | 4 | IO_CELL | (0) |
| D4 | 33 | IO_CELL | 1 | RDAT_OEB [1] | 3 | OUT_CELL | (0) |
| D4_OEB [1] | 32 | OUT_CELL | 0 | TRIMF | 2 | IN_CELL | (0) |
| D5 | 31 | IO_CELL | 0 | NC | 1 | IO_CELL | (0) |
| D5_OEB [1] | 30 | OUT_CELL | 1 | NC_OEB | 0 | OUT_CELL | (0) |
| D6 | 29 | IO_CELL | 1 | | | | |

**Notes:**

1. These OEB signals, when set low, will set the corresponding bidirectional signal to an output.
2. These OEB signals, when set high, will set the corresponding output to high impedance.
3. When set high, TCLKO, TDAT, TFP, and RSYNC will be set to high impedance.
4. HIZ is the first bit in the boundary scan chain.
5. Bits 59:56 represent the revision identification code. “0100” indicates revision E. “0101” indicates revision F.

**Figure 51 - Input Observation Cell (IN_CELL)**




In this diagram and those that follow, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the centre of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the table above.

**Figure 52 - Output Cell (OUT_CELL)**

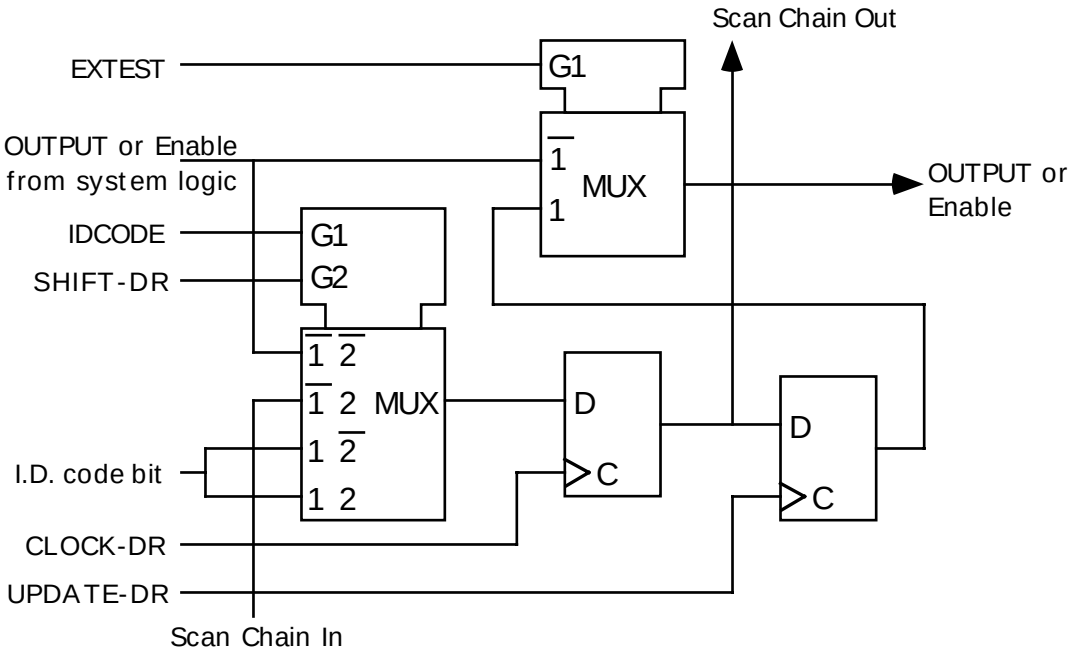



**Figure 53 - Bidirectional Cell (IO_CELL)**

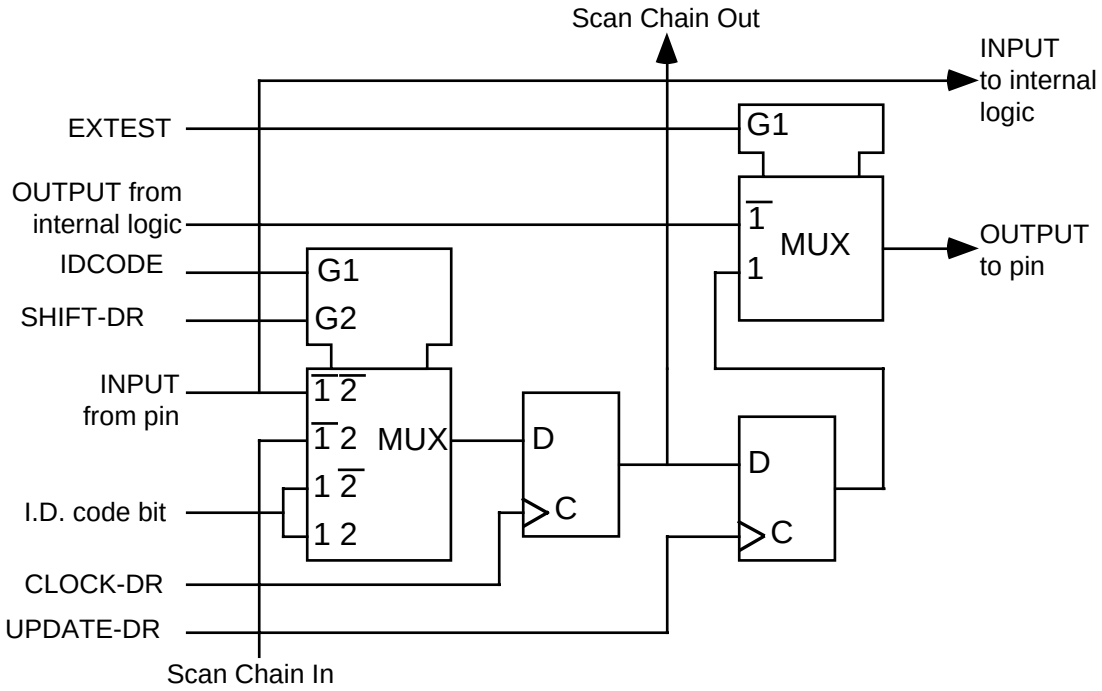
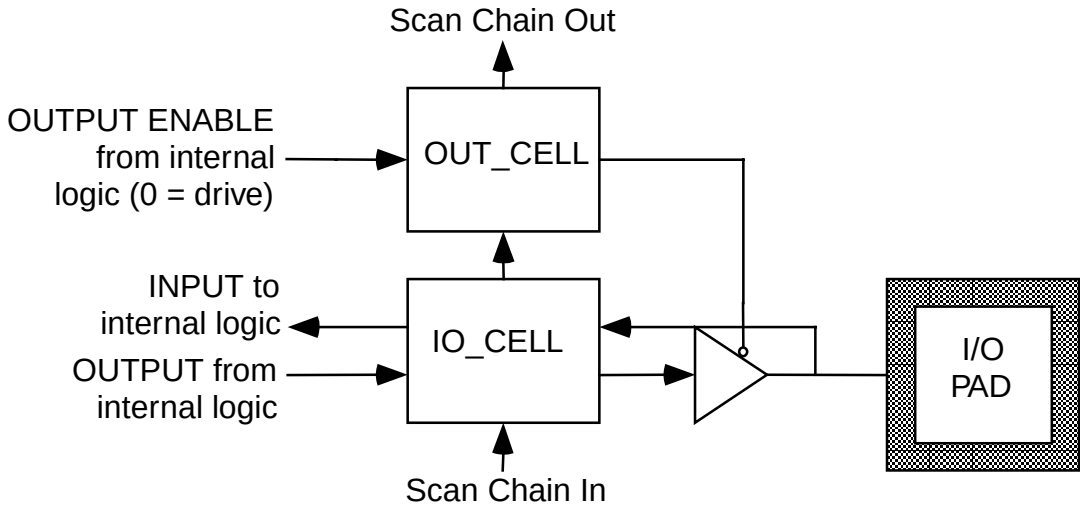


**Figure 54 - Layout of Output Enable and Bidirectional Cells**



# 15 ABSOLUTE MAXIMUM RATINGS

Maximum ratings are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

| | |
|---|---|
| Ambient Temperature under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on VDD with Respect to GND | -0.3V to 4.6V |
| Voltage on BIAS with respect to GND | VDD - 0.3V to 5.5V |
| Voltage on Any Pin | -0.3V to BIAS + 0.3V |
| Static Discharge Voltage | ±1000 V |
| Latchup current on any pin | ±100 mA |
| Maximum DC current on any pin | ±20 mA |
| Maximum Lead Temperature | +230 °C |
| Maximum Junction Temperature | +150 °C |

## 16 D.C. CHARACTERISTICS

$T_A$ = -40°C to +85°C, $V_{DD}$ = 3.3 V ± 5%, $V_{DD} \leq V_{BIAS} \leq 5.5$ V

(Typical Conditions: $T_A$ = 25°C, $V_{DD}$ = 3.3 V, $V_{BIAS}$ = 5 V)

**Table 115 - D.C. Characteristics**

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply | 3.135 | 3.3 | 3.465 | Volts | |
| BIAS | 5 V Tolerant Bias | $V_{DD}$ | 5.0 | 5.5 | Volts | |
| $I_{BIAS}$ | Current into 5 V Bias | | 6.0 | | µA | $V_{BIAS}$ = 5.5V |
| $V_{IL}$ | Input Low Voltage (TTL Only) | 0 | | 0.8 | Volts | Guaranteed Input LOW Voltage |
| $V_{IH}$ | Input High Voltage (TTL Only) | 2.0 | | BIAS | Volts | Guaranteed Input HIGH Voltage |
| $V_{OL}$ | Output or Bi-directional Low Voltage (TTL Only) | | 0.25 | 0.4 | Volts | $V_{DD}$ = min, $I_{OL}$ = -6 mA for BTCLK and BRCLK, -2 mA for all other digital outputs. Note 3 |
| $V_{OH}$ | Output or Bi-directional High Voltage (TTL Only) | 2.4 | | | Volts | $V_{DD}$ = min, $I_{OH}$ = 6 mA for BTCLK and BRCLK, 2 mA for all other digital outputs. Note 3 |
| $V_{T+}$ | Reset Input High Voltage | 2.0 | | | Volts | TTL Schmitt trigger |
| $V_{T-}$ | Reset Input Low Voltage | | | 0.8 | Volts | |
| $V_{TH}$ | Reset Input Hysteresis Voltage | | 0.5 | | Volts | |

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_{ILPU}$ | Input Low Current | 10 | 60 | 100 | µA | $V_{IL}$ = GND. Notes 1, 3 |
| $I_{IHPU}$ | Input High Current | -10 | 0 | +10 | µA | $V_{IH} = V_{DD}$. Notes 1, 3 |
| $I_{IL}$ | Input Low Current | -10 | 0 | +10 | µA | $V_{IL}$ = GND. Notes 2, 3 |
| $I_{IH}$ | Input High Current | -10 | 0 | +10 | µA | $V_{IH} = V_{DD}$. Notes 2, 3 |
| $C_{IN}$ | Input Capacitance | | 5 | | pF | Excluding Package, Package Typically 2 pF |
| $C_{OUT}$ | Output Capacitance | | 5 | | pF | Excluding Package, Package Typically 2 pF |
| $C_{IO}$ | Bi-directional Capacitance | | 5 | | pF | Excluding Package, Package Typically 2 pF |
| $I_{DDOPMAX}$ | Operating Current | | | 250 | mA | $V_{DD}$ = 3.465 V, T1 mode, 1.544 MHz backplane, transmitting all ones, short haul 550 to 660 ft. Outputs Unloaded |
| $P_{DISS}$ | Power Dissipation | | | 416 | mW | $V_{DD}$ = 3.465 V, 85° C case temperature, T1 mode, 1.544 MHz backplane, transmitting 50% ones density, short haul 0 ft. Outputs Unloaded |

**Notes on D.C. Characteristics:**

1. Input pin or bi-directional pin with internal pull-up resistor.

2. Input pin or bi-directional pin without internal pull-up resistor

3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

# 17 A.C. TIMING CHARACTERISTICS

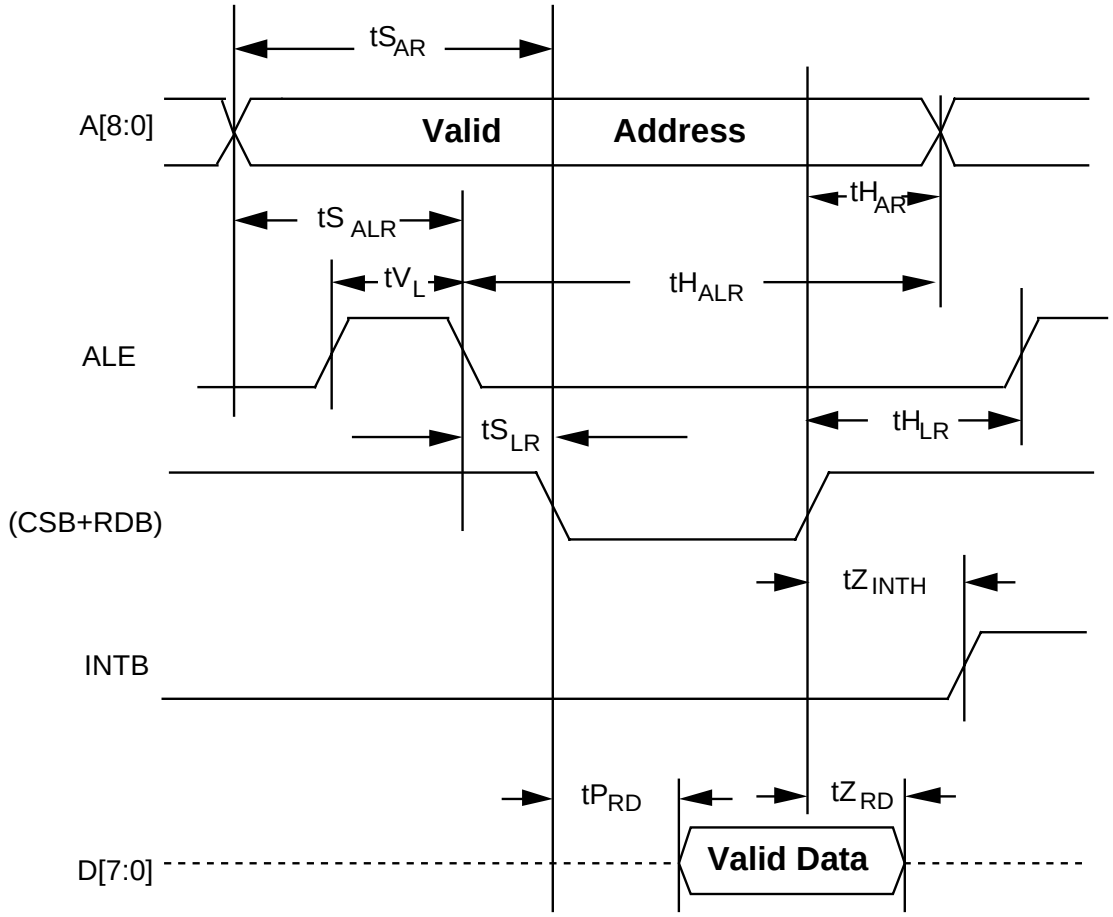
## 17.1 Microprocessor Interface Timing Characteristics

($T_A$ = -40°C to +85°C, $V_{DD}$ = 3.3 V ± 5%)

**Table 116 - Microprocessor Read Access (Figure 55)**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $tS_{AR}$ | Address to Valid Read Set-up Time | 10 | | ns |
| $tH_{AR}$ | Address to Valid Read Hold Time | 5 | | ns |
| $tS_{ALR}$ | Address to Latch Set-up Time | 10 | | ns |
| $tH_{ALR}$ | Address to Latch Hold Time | 10 | | ns |
| $tV_{L}$ | Valid Latch Pulse Width | 20 | | ns |
| $tS_{LR}$ | Latch to Read Set-up | 0 | | ns |
| $tH_{LR}$ | Latch to Read Hold | 5 | | ns |
| $tP_{RD}$ | Valid Read to Valid Data Propagation Delay | | 80 | ns |
| $tZ_{RD}$ | Valid Read Negated to Output Tri-state | | 20 | ns |
| $tZ_{INTH}$ | Valid Read Negated to INTB high | | 50 | ns |

**Figure 55 - Microprocessor Read Access Timing**




**Notes on Microprocessor Read Timing:**

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 50 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. Microprocessor Interface timing applies to normal mode register accesses only.

5. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

6. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

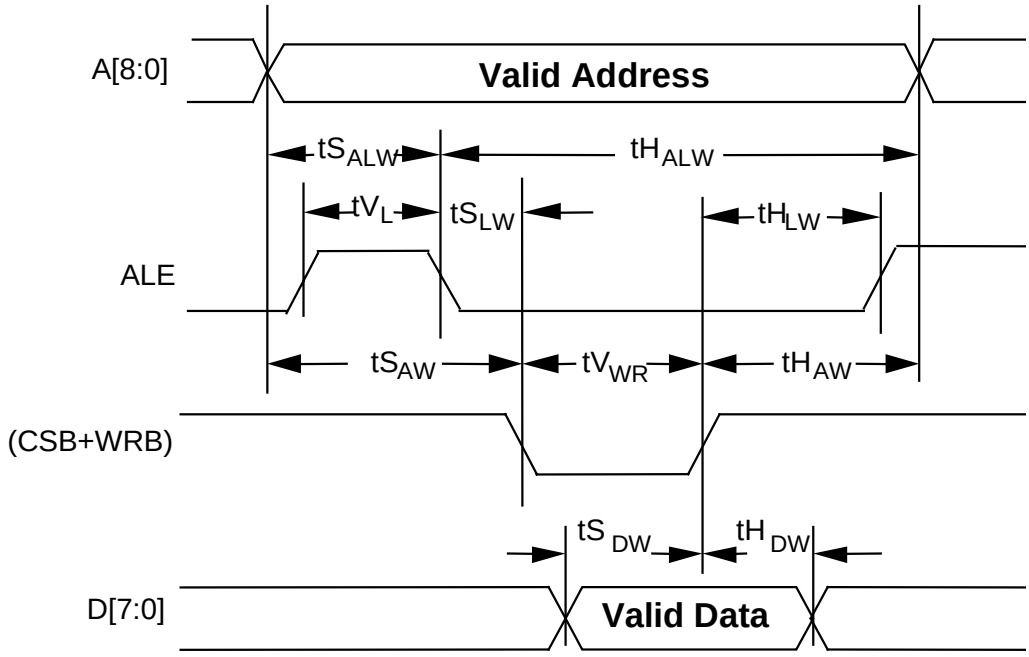
7. In non-multiplexed address/data bus architectures ALE can be held high; parameters $tS_{ALR}$, $tH_{ALR}$, $tV_L$, and $tS_{LR}$, $tH_{LR}$ are not applicable.

8. Parameter $tH_{AR}$ is not applicable when address latching is used.

**Table 117 - Microprocessor Write Access (Figure 56)**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $tS_{AW}$ | Address to Valid Write Set-up Time | 10 | | ns |
| $tS_{DW}$ | Data to Valid Write Set-up Time | 20 | | ns |
| $tS_{ALW}$ | Address to Latch Set-up Time | 10 | | ns |
| $tH_{ALW}$ | Address to Latch Hold Time | 10 | | ns |
| $tV_L$ | Valid Latch Pulse Width | 20 | | ns |
| $tS_{LW}$ | Latch to Write Set-up | 0 | | ns |
| $tH_{LW}$ | Latch to Write Hold | 5 | | ns |
| $tH_{DW}$ | Data to Valid Write Hold Time | 5 | | ns |
| $tH_{AW}$ | Address to Valid Write Hold Time | 5 | | ns |
| $tV_{WR}$ | Valid Write Pulse Width | 40 | | ns |

**Figure 56 - Microprocessor Write Access Timing**




**Notes on Microprocessor Interface Write Timing:**

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. Microprocessor Interface timing applies to normal mode register accesses only.

3. In non-multiplexed address/data bus architectures, ALE can be held high, parameters $tS_{ALW}$, $tH_{ALW}$, $tV_L$, and $tS_{LW}$, $tH_{LW}$ are not applicable.

4. Parameters $tH_{AW}$ and $tS_{AW}$ are not applicable if address latching is used.

5. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

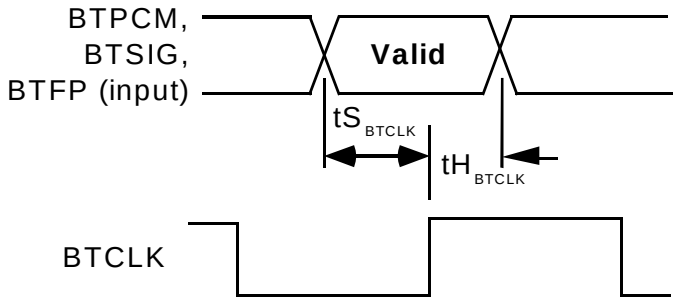
## 17.2 Transmit Backplane Interface (Figure 57, Figure 58)

($T_A$ = -40°C to +85°C, $V_{DD}$ = 3.3 V ± 5%)

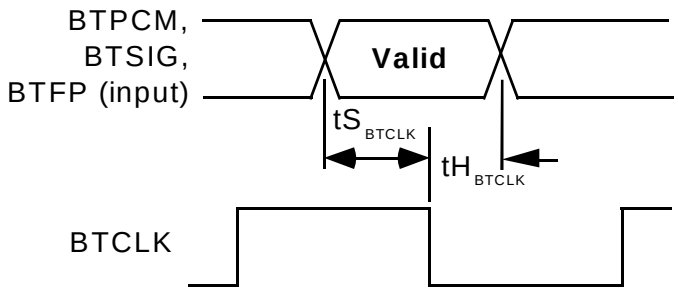
**Table 118 - Transmit Backplane Interface**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| | BTCLK Average Frequency[3] (T1 mode, CMS=0, RATE[1:0]='b00) | Typ – 200 ppm | 1.544 | Typ + 200 ppm | MHz |
| | BTCLK Average Frequency[3] (CMS=0, RATE[1:0]='b01) | Typ – 200 ppm | 2.048 | Typ + 200 ppm | MHz |
| | BTCLK Average Frequency[3] (T1 mode, CMS=1, RATE[1:0]='b00) | Typ – 200 ppm | 3.088 | Typ + 200 ppm | MHz |
| | BTCLK Average Frequency[3] (CMS=0, RATE[1:0]='b10) or (CMS=1, RATE[1:0]='b01) | Typ – 200 ppm | 4.096 | Typ + 200 ppm | MHz |
| | BTCLK Average Frequency[3] (CMS=0, RATE[1:0]='b11) or (CMS=1, RATE[1:0]='b10) | Typ – 200 ppm | 8.192 | Typ + 200 ppm | MHz |
| | BTCLK Average Frequency[3] (CMS=1, RATE[1:0]='b11) | Typ – 200 ppm | 16.384 | Typ + 200 ppm | MHz |
| | BTCLK Duty Cycle[4] | 35 | | 65 | % |
| $tS_{BTCLK}$ | BTCLK to Backplane Input Set-up Time[1] | 20 | | | ns |
| $tH_{BTCLK}$ | BTCLK to Backplane Input Hold Time[2] | 20 | | | ns |
| $tP_{BTFP}$ | BTCLK to BTFP Output Propagation Delay | -20 | | 50 | ns |

**Figure 57 - Backplane Transmit Input Timing Diagram**

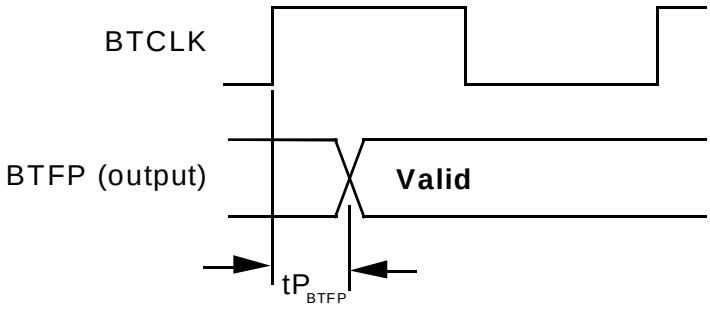



Data Sampled on Rising Edge

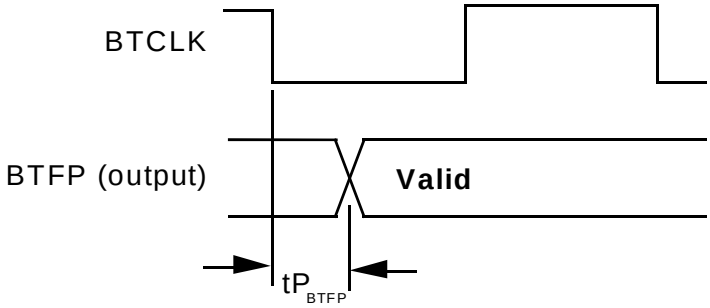



Data Sampled on Falling Edge

**Figure 58 - Backplane Transmit Output Timing Diagram**




Frame Pulse Output on Rising Edge




Frame Pulse Output on Falling Edge

## 17.3 Receive Backplane Interface (Figure 59, Figure 60)

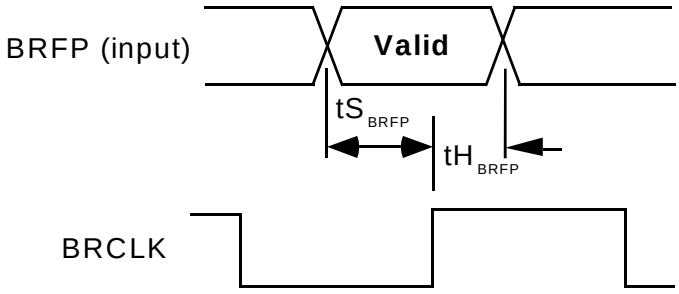
($T_A$ = -40°C to +85°C, $V_{DD}$ = 3.3 V ± 5%)

**Table 119 - Receive Backplane Interface**

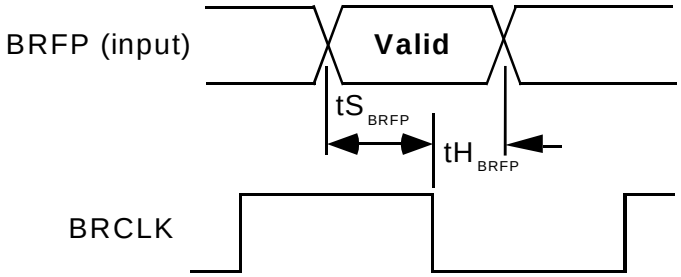
| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| | BRCLK Average Frequency[3] (T1 mode, CMS=0, RATE[1:0]='b00) | Typ – 200 ppm | 1.544 | Typ + 200 ppm | MHz |
| | BRCLK Average Frequency[3] (CMS=0, RATE[1:0]='b01) | Typ – 200 ppm | 2.048 | Typ + 200 ppm | MHz |
| | BRCLK Average Frequency[3] (T1 mode, CMS=1, RATE[1:0]='b00) | Typ – 200 ppm | 3.088 | Typ + 200 ppm | MHz |

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| | BRCLK Average Frequency[3] (CMS=0, RATE[1:0]='b10) or (CMS=1, RATE[1:0]='b01) | Typ – 200 ppm | 4.096 | Typ + 200 ppm | MHz |
| | BRCLK Average Frequency[3] (CMS=0, RATE[1:0]='b11) or (CMS=1, RATE[1:0]='b10) | Typ – 200 ppm | 8.192 | Typ + 200 ppm | MHz |
| | BRCLK Average Frequency[3] (CMS=1, RATE[1:0]='b11) | Typ – 200 ppm | 16.384 | Typ + 200 ppm | MHz |
| | BRCLK Duty Cycle[4] | 35 | | 65 | % |
| $t_{SBRFP}$ | BRFP to BRCLK Input Set-up Time[1] | 20 | | | ns |
| $t_{HBRFP}$ | BRFP to BRCLK Input Hold Time[2] | 20 | | | ns |
| $t_{PBRCLK}$ | BRCLK to Backplane Output Signals Propagation Delay[7,8] | -20 | | 50 | ns |
| $t_{ZBRCLK}$ | BRCLK to Backplane Output Signals High Impedance | -20 | | 30 | ns |

**Figure 59 - Backplane Receive Input Timing Diagram**

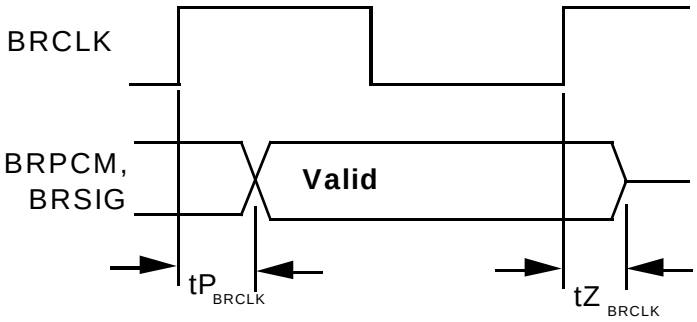



Frame Pulse Sampled on Rising Edge

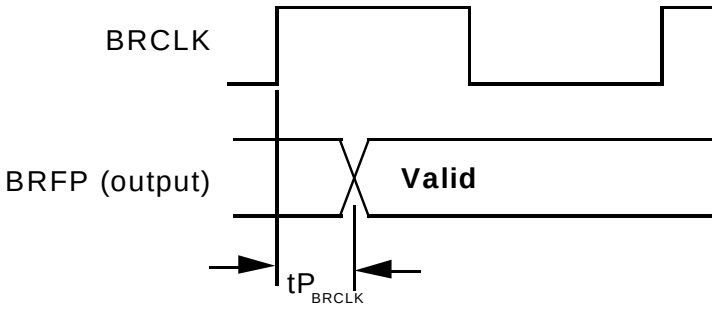



Frame Pulse Sampled on Falling Edge

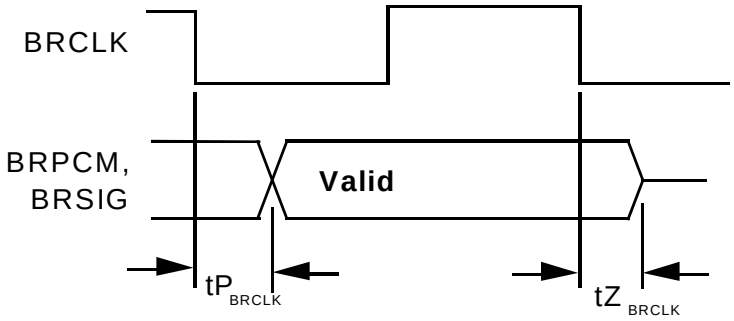
**Figure 60 - Backplane Receive Output Timing Diagram**



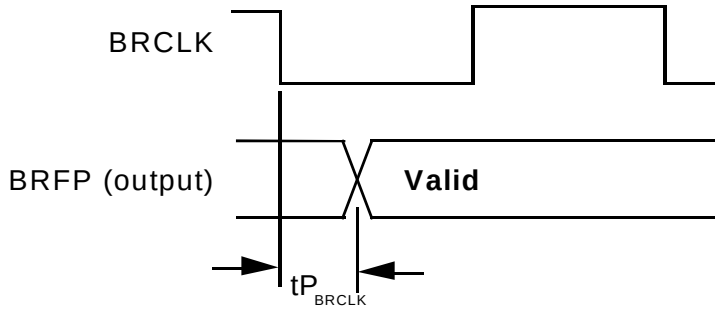

Data Output on Rising Edge




FP Output on Rising Edge




Data Output on Falling Edge




FP Output on Falling Edge

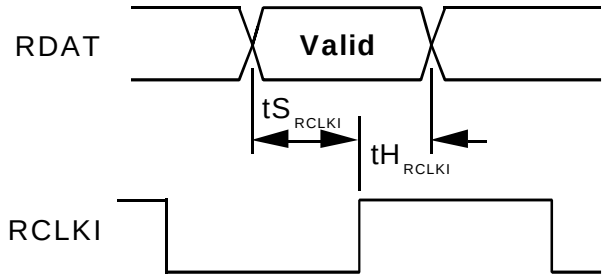
## 17.4 Receive Digital Interface (Figure 61)

($T_A$ = -40°C to +85°C, $V_{DD}$ = 3.3 V ± 5%)

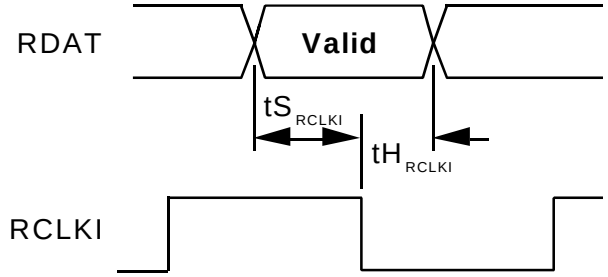
**Table 120 - Receive Digital Interface**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| | RCLKI Frequency (nominally 1.544 MHz ± 130 ppm or 2.048 MHz ± 50 ppm) | | 2.1 | MHz |
| | RCLKI Duty Cycle[4] | 30 | 70 | % |
| $tS_{RCLKI}$ | RCLKI to RDAT Setup Time[1] | 20 | | ns |
| $tH_{RCLKI}$ | RCLKI to RDAT Hold Time[2] | 20 | | ns |

**Figure 61 - Digital Receive Interface Timing Diagram**




**With RFALL bit = 0**




**With RFALL bit = 1**

## 17.5 Transmit Digital Interface (Figure 62)

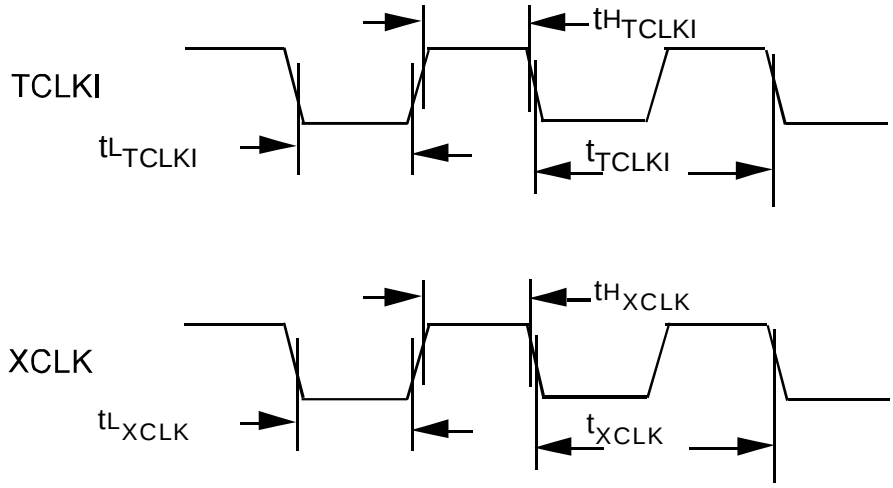
($T_A$ = -40°C to +85°C, $V_{DD}$ = 3.3 V ± 5%)

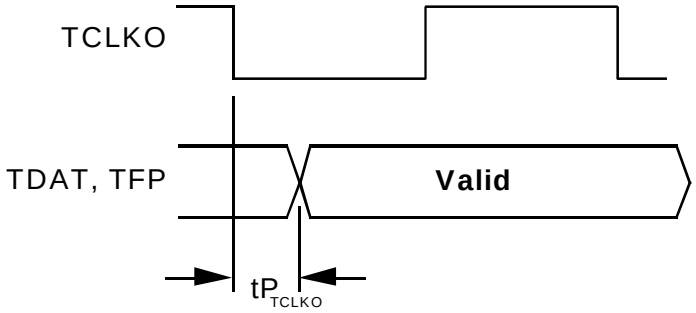
**Table 121 - Transmit Digital Interface**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $t_{TCLKI}$ | TCLKI Frequency, typically<br>1.544 MHz ± 130 ppm in T1 mode or<br>2.048 MHz ± 50 ppm in E1 mode | <br>1.543<br>2.047 | <br>1.545<br>2.049 | <br>MHz<br>MHz |
| $t_{HTCLKI}$ | TCLKI High Duration[4] | 160 | | ns |
| $t_{LTCLKI}$ | TCLKI Low Duration[4] | 160 | | ns |
| $t_{XCLK}$ | XCLK Frequency, typically<br>1.544 MHz ± 100 ppm in T1 mode or<br>2.048 MHz ± 100 ppm in E1 mode | <br>1.543<br>2.047 | <br>1.545<br>2.049 | <br>MHz<br>MHz |

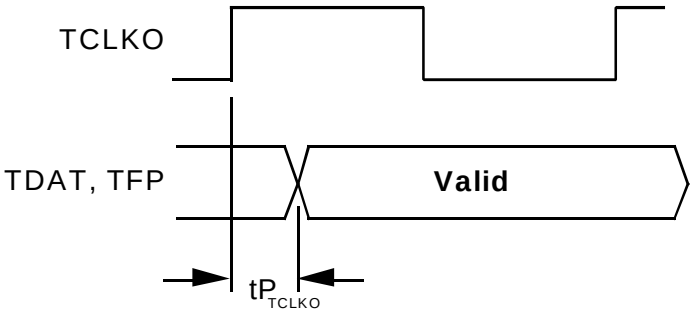
| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $t_{HXCLK}$ | XCLK High Duration[4] | 160 | | ns |
| $t_{LXCLK}$ | XCLK Low Duration[4] | 160 | | ns |
| $t_{PTCLKO}$ | TCLKO to Digital Transmit Output Signals Propagation Delay | -20 | 50 | ns |

**Figure 62 - Digital Transmit Interface Timing Diagram**






**With TRISE bit = 0**




**With TRISE bit = 1**

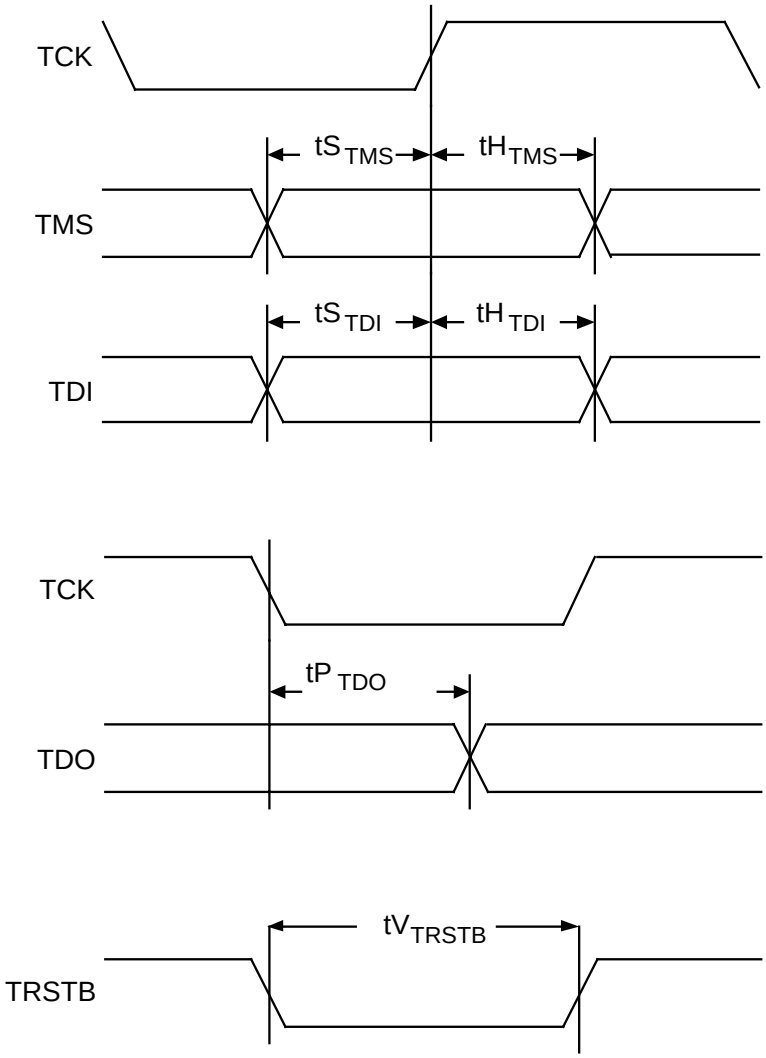
## 17.6 JTAG Port Interface (Figure 63)

($T_A$ = -40°C to +85°C, $V_{DD}$ = 3.3 V ± 5%)

**Table 122 - JTAG Port Interface**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| | TCK Frequency | | 4 | MHz |
| | TCK Duty Cycle | 40 | 60 | % |
| $tS_{TMS}$ | TMS Set-up time to TCK | 50 | | ns |
| $tH_{TMS}$ | TMS Hold time to TCK | 50 | | ns |
| $tS_{TDI}$ | TDI Set-up time to TCK | 50 | | ns |
| $tH_{TDI}$ | TDI Hold time to TCK | 50 | | ns |
| $tP_{TDO}$ | TCK Low to TDO Valid | 2 | 50 | ns |
| $tV_{TRSTB}$ | TRSTB Pulse Width | 100 | | ns |

**Figure 63 - JTAG Port Interface Timing**




**Notes on Input Timing:**

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3. BTCLK and BRCLK instantaneous period variation of +/- 8% (typical) can be tolerated by the device, as long as the frequency specification of +/- 200ppm is complied with.

4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

5. XCLK accuracy is ± 100 ppm.

6. TCLKI can be a jittered clock signal subject to the minimum high and low durations $tH_{TCLKI}$, $tL_{TCLKI}$. These durations correspond to nominal XCLK input frequencies.

**Notes on Output Timing:**

7. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

8. Maximum output propagation delays are measured with a 50 pF load on the output.

# 18 ORDERING AND THERMAL INFORMATION

**Table 123 - Ordering Information**

| Part No. | Description |
|---|---|
| PM4351-RI | 80-Pin Metric Plastic Quad Flat Pack (MQFP) |
| PM4351-NI | 81-Ball Chip Array Ball Grid Array (CABGA) |

**Table 124 - Thermal Information**

| | | | | Forced Air (Linear Feet per Minute) | | | | |
|---|---|---|---|---|---|---|---|---|
| **Part No.** | **Case Temperature** | **Theta J-A** | **Conv** | **100** | **200** | **300** | **400** | **500** |
| PM4351-RI | -40°C to 85°C | Dense Board[1] | 62.1 | 54.8 | 49.1 | 45.0 | 42.4 | 41.1 |
| | | JEDEC Board[2] | 43.2 | 40.7 | 39.2 | 38.5 | 38.2 | 38.0 |
| PM4351-NI | -40°C to 85°C | Dense Board[3] | 99.5 | 92.9 | 87.8 | 84.0 | 81.0 | 78.5 |
| | | JEDEC Board[4] | 47.8 | 45.8 | 44.4 | 43.5 | 43.0 | 42.7 |

1. - Dense Board is defined as a 3S3P board and consists of a 3x3 array of PM4351-RI devices located as close to each other as board design rules allow. All PM4351-RI devices are assumed to be dissipating 0.416 Watts. Theta J-A listed is for the device in the middle of the array.

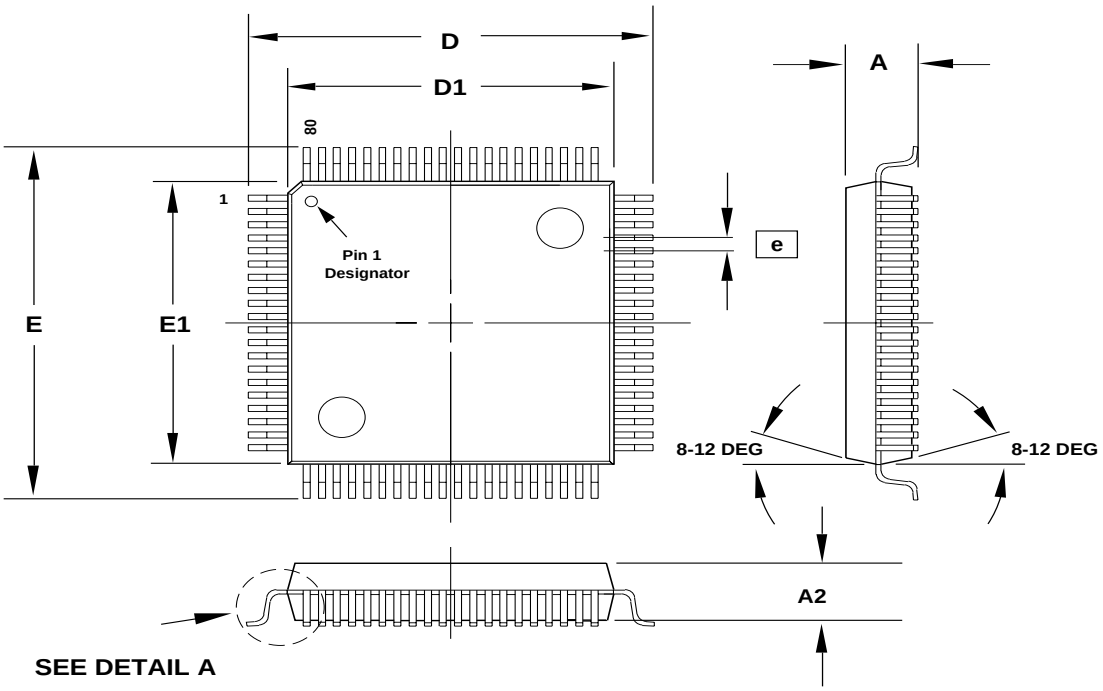
2. - JEDEC Board Theta J-A is the measured value for a single thermal device in the same package on a 2S2P board following EIA/JESD 51-3.

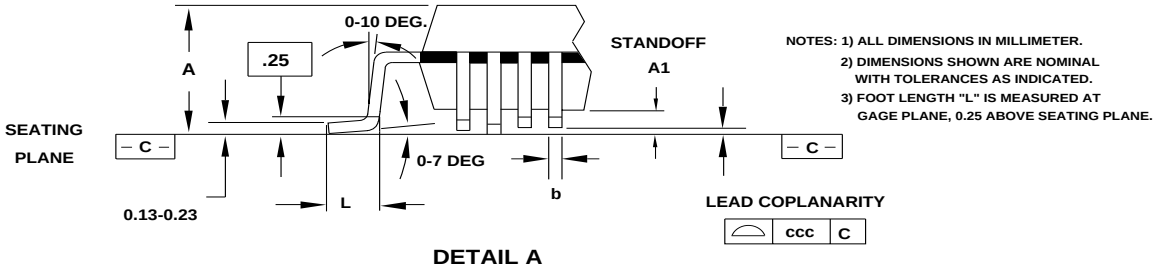
3. - Dense Board is defined as a 3S3P board and consists of a 3x3 array of PM4351-NI devices located as close to each other as board design rules allow. All PM4351-NI devices are assumed to be dissipating 0.416 Watts. Theta J-A listed is for the device in the middle of the array.

4. - JEDEC Board Theta J-A is the measured value for a single thermal device in the same package on a 2S2P board following EIA/JESD 51-3.

# 19 MECHANICAL INFORMATION

## PM4351-RI Package

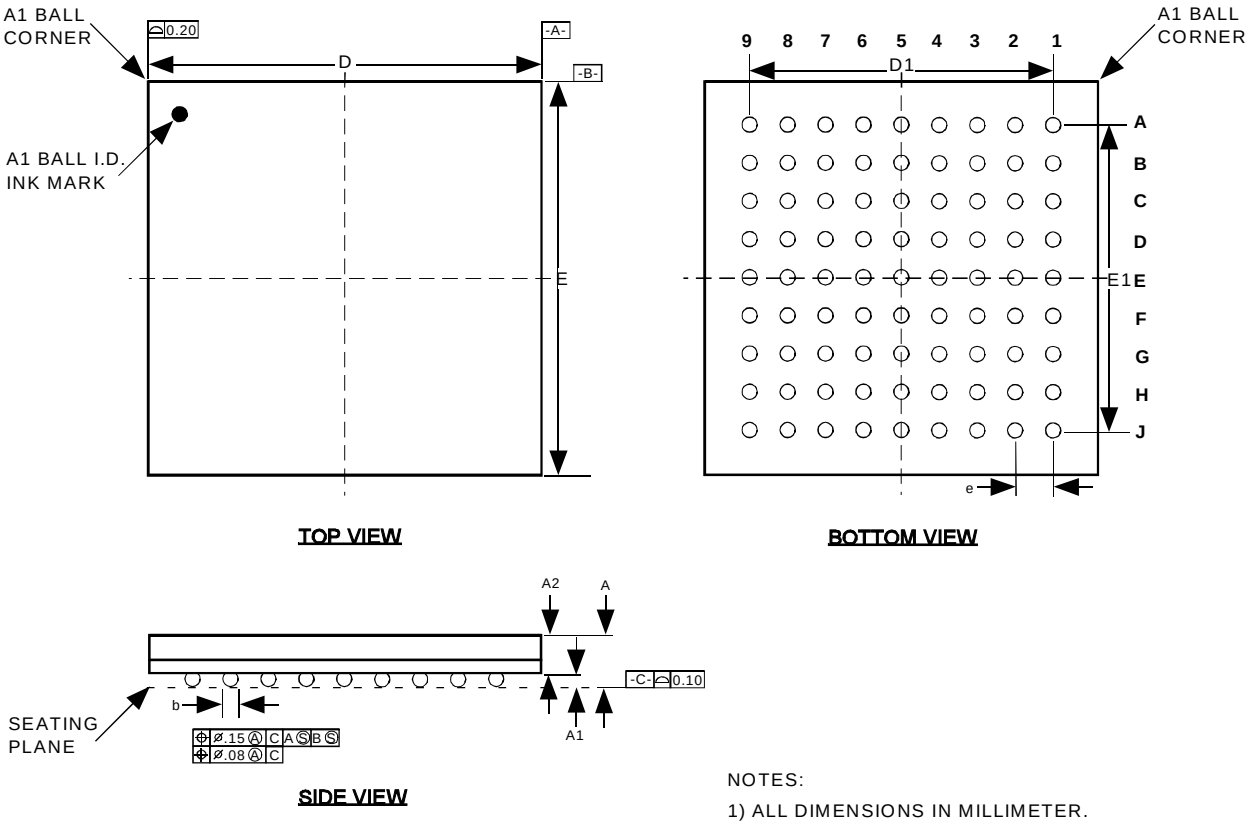



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSIONS SHOWN ARE NOMINAL WITH TOLERANCES AS INDICATED.
3) FOOT LENGTH "L" IS MEASURED AT GAGE PLANE, 0.25 ABOVE SEATING PLANE.

| PACKAGE TYPE: 80 PIN METRIC PLASTIC QUAD FLATPACK-MQFP | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| BODY SIZE: 14 x 14 x 2.0 MM | | | | | | | | | | | |
| Dim. | A | A1 | A2 | D | D1 | E | E1 | L | e | b | ccc |
| Min. | 2.00 | 0.05 | 1.95 | 16.95 | 13.90 | 16.95 | 13.90 | 0.73 | | 0.22 | |
| Nom. | 2.15 | 0.15 | 2.00 | 17.20 | 14.00 | 17.20 | 14.00 | 0.88 | 0.65 | | |
| Max. | 2.35 | 0.25 | 2.10 | 17.45 | 14.10 | 17.45 | 14.10 | 1.03 | | 0.38 | 0.10 |

## PM4351-NI Package




NOTES:

1) ALL DIMENSIONS IN MILLIMETER.

| PACKAGE TYPE : 81 CHIP ARRAY BALL GRID ARRAY - CABGA | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| BODY SIZE : 9 X 9 x 1.4 MM | | | | | | | | | | |
| Dim. | A | A1 | A2 | D | D1 | E | E1 | b | e | |
| Min. | 1.30 | 0.31 | 0.99 | | | | | | | |
| Nom. | 1.40 | 0.36 | 1.04 | 9.00 | 6.40 | 9.00 | 6.40 | 0.46 | 0.80 | |
| Max. | 1.50 | 0.41 | 1.09 | | | | | | | |

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