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LCD Driver IC with Key Input Function **PT6553**

DESCRIPTION

PT6553 is an LCD Driver IC providing key scan circuitry which can accept up to a maximum of 30 keys, thereby, reducing printed circuit board wiring. It can drive up to 126 segments and is capable of controlling up to 4 general purpose output ports. The reset circuit provides on-chip voltage detection making it possible to prevent incorrect displays. Pin assignments and application circuit are optimized for easy PCB layout and cost saving advantages.

FEATURES

- Up to 126 segments outputs
- Up to 4 general purpose output ports
- Key input function (up to 30 Keys)
- 1/3 duty - 1/2 bias and 1/3 duty - 1/3 bias drive techniques
- Sleep mode and all segments off function
- Direct display of display data without using a decoder
- On-chip voltage-detection type reset circuit
- RC oscillation circuit

APPLICATIONS

- Cellular phone
- Data bank, Organizer
- Electronic dictionary/Translator
- P.D.A.
- P.O.S.
- Information appliance
- Caller ID
- Pager
- Electronic equipment with LCD display

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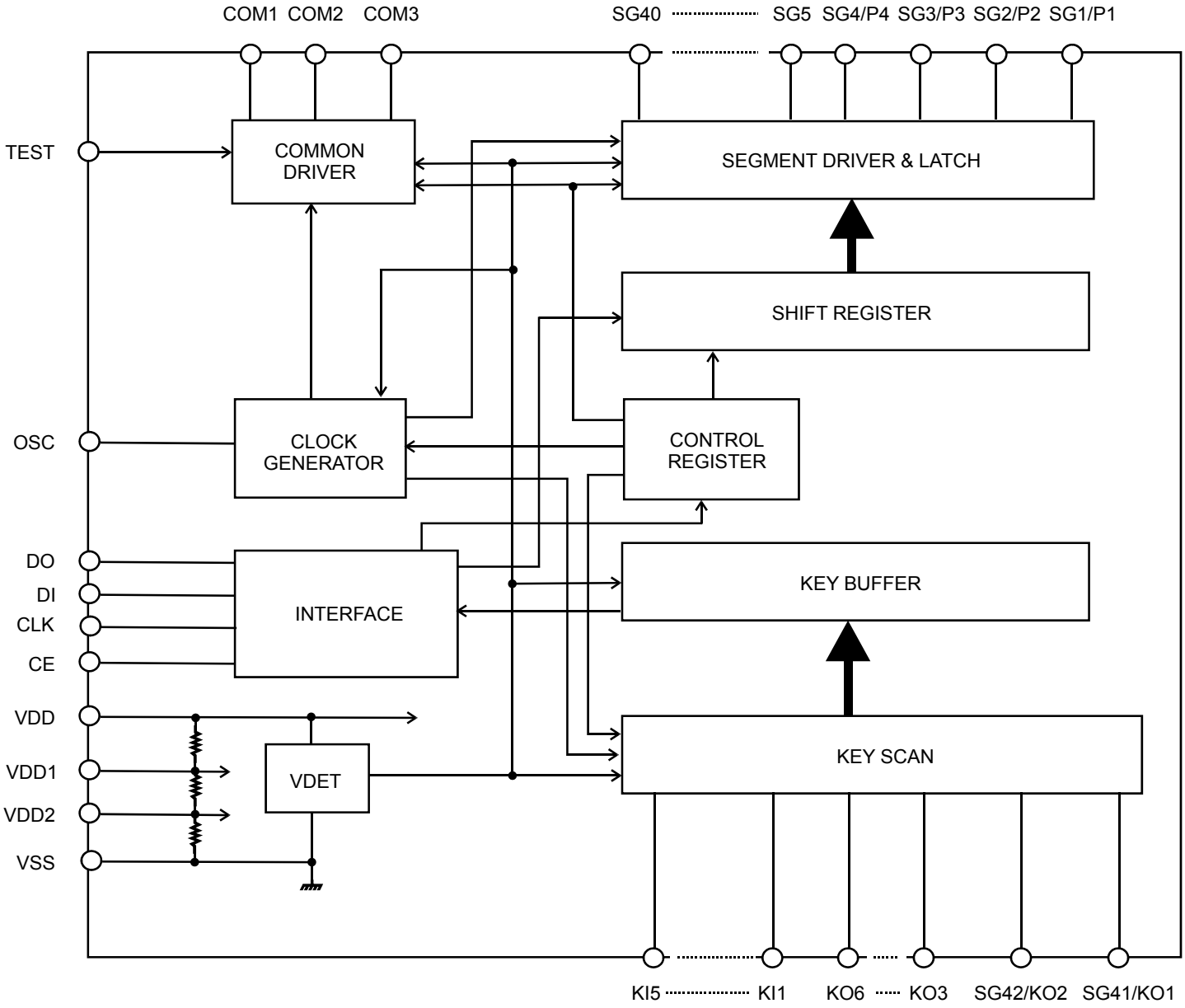
BLOCK DIAGRAM



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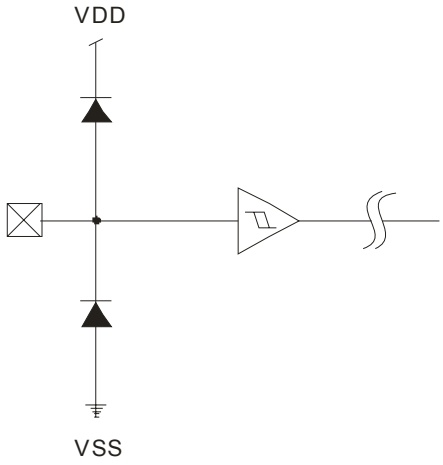
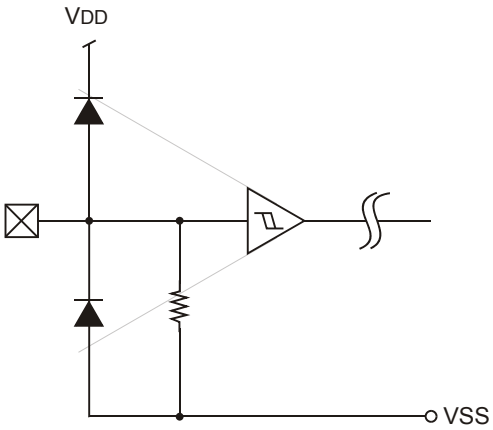
INPUT/OUTPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below:

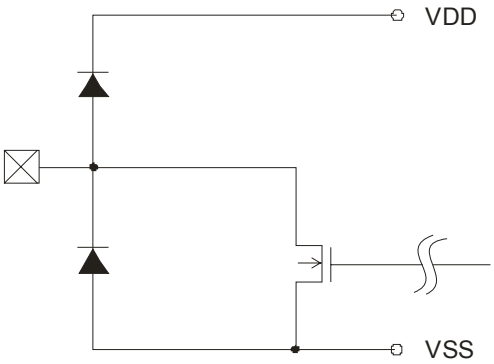
INPUT PIN: CLK, CE, DI



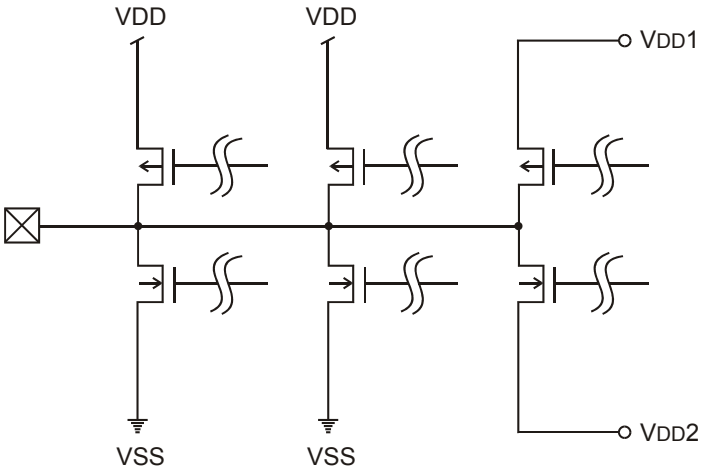
INPUT PIN: KI1 TO KI5



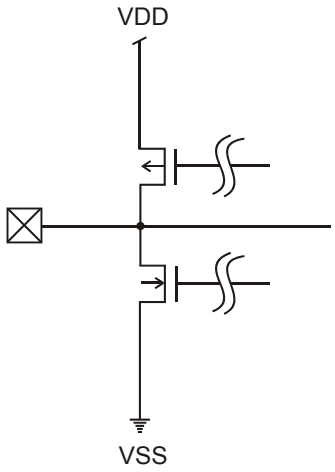
OUTPUT PIN: DO



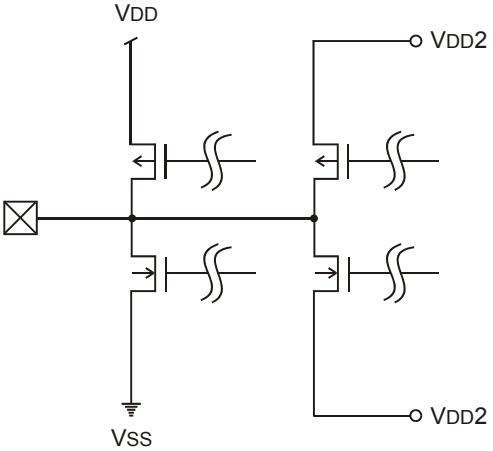
OUTPUT PIN: SG1/P1 TO SG4/P4, SG5 TO SG40, SG41/KO1, SG42/KO2



OUTPUT PIN: KO3 TO KO6



OUTPUT PIN: COM1 TO COM3



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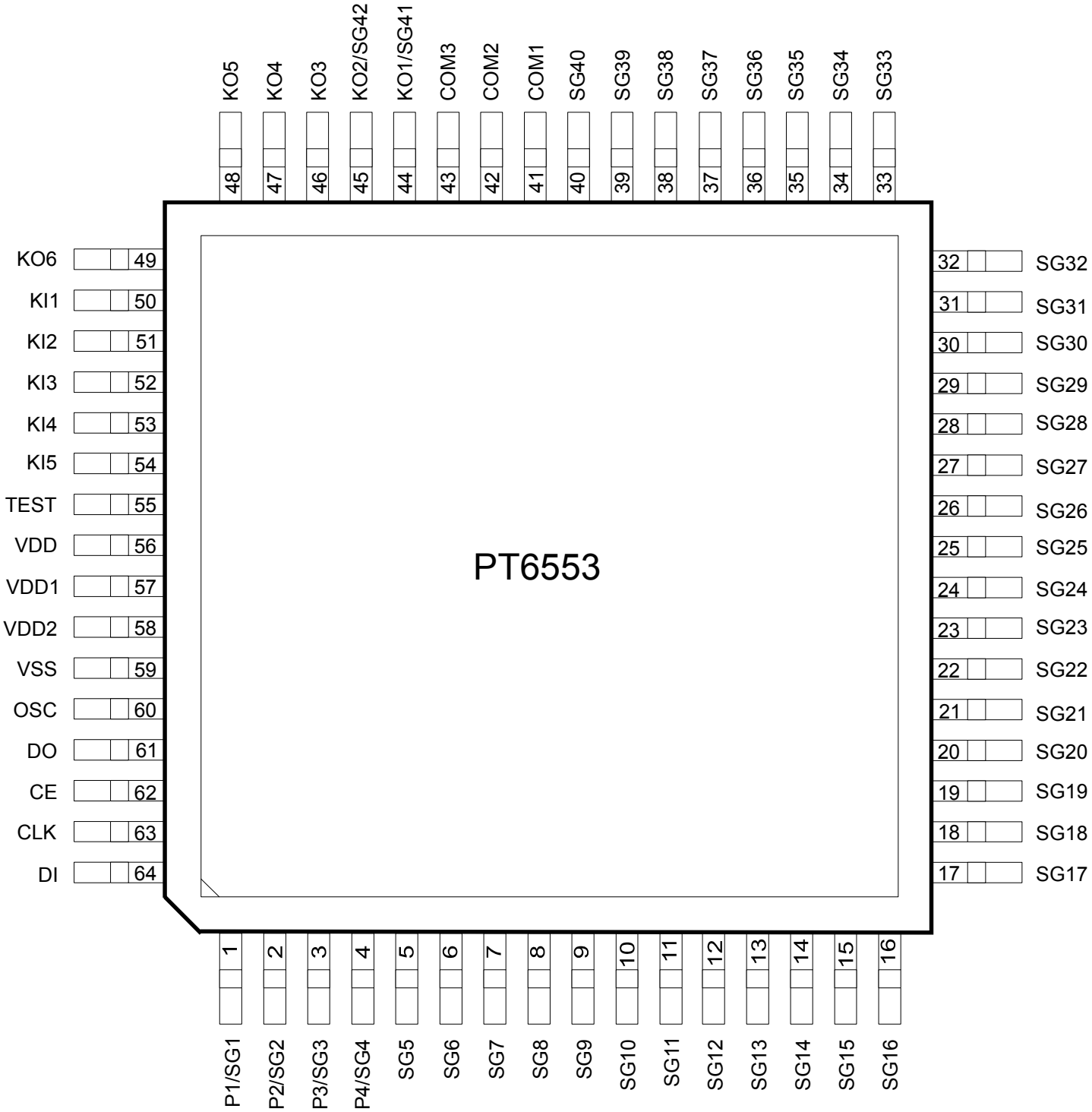
PIN CONFIGURATION



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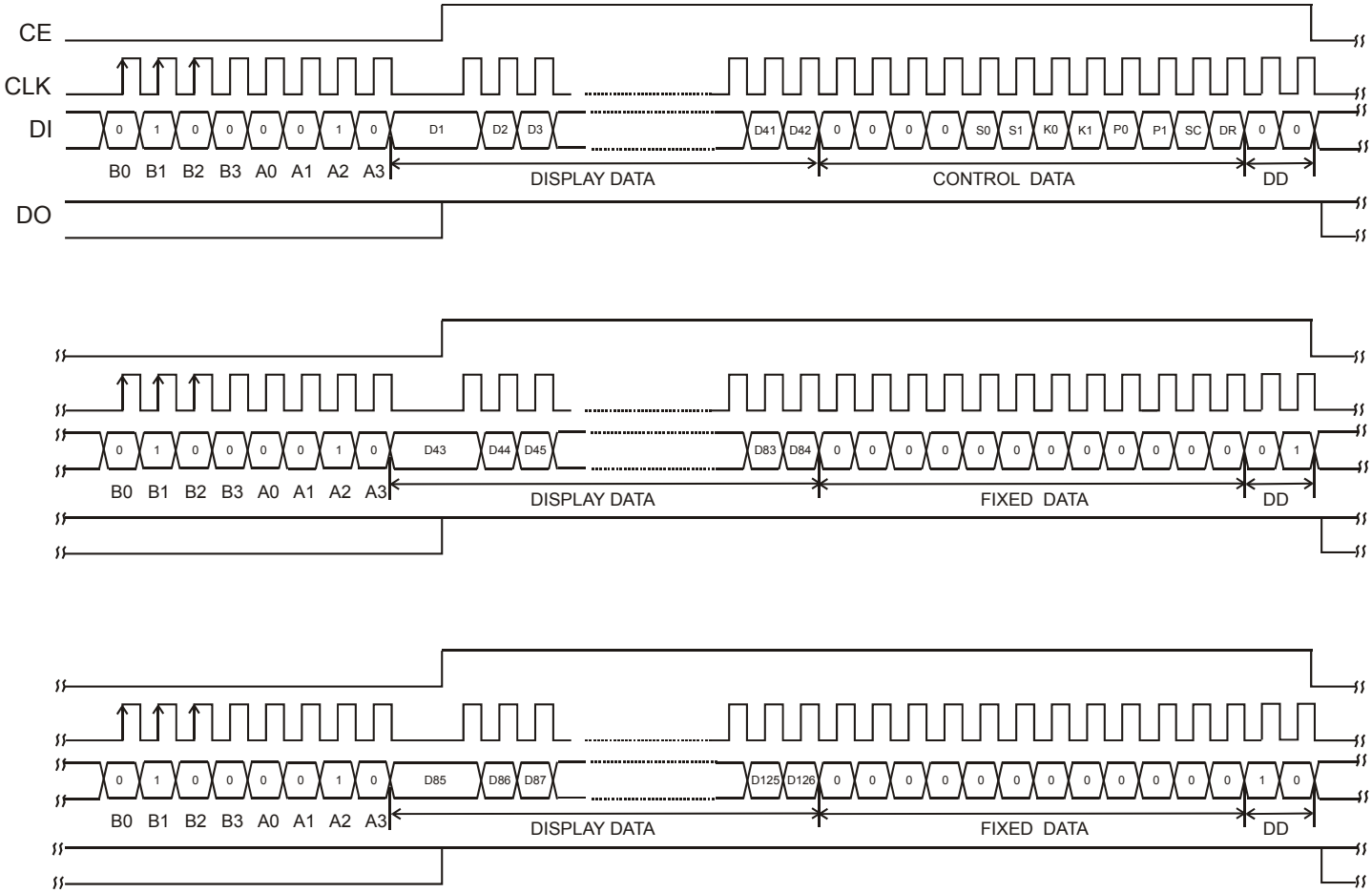
PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
SG1/P1 ~ SG4/P4	O	Segment Output/General Purpose Output Pins Under serial data control, these pins may be used a General Purpose Output Ports.	1 ~ 4
SG5 ~ SG40	O	Segment Output	5 ~ 40
COM1, COM2, COM3	O	Common Driver Output Pins	41, 42, 43
KO1/SG41	O	Key Scan Output/Segment Output Pin	44
KO2/SG42	O	Key Scan Output/Segment Output Pin	45
KO3 ~ KO6	O	Key Scan Output Pins	46 ~ 49
KI1 ~ KI5	I	Key Scan Input Pins	50 ~ 54
TEST	I	Test Pin	55
VDD	-	Power Supply	56
VDD1	-	Power Supply This power supply pin is used for applying the LCD Drive 2/3 bias voltage externally and must be connected to VDD2 when using 1/2 bias drive.	57
VDD2	-	Power Supply This power supply pin is used for applying the LCD Drive 1/3 bias voltage externally and must be connected to VDD1 when using 1/2 bias drive.	58
VSS	-	Ground	59
OSC	I/O	Oscillator Pin	60
DO	O	Data Output Pin	61
CE	I	Chip Enable Pin	62
CLK	I	Synchronization Clock Input Pin	63
DI	I	Data Transfer Input Pin	64

FUNCTION DESCRIPTION

SERIAL DATA INPUT

CONDITION 1: CLK IS TERMINATED AT THE "LOW" LEVEL



Where: DD= Direction Data

- Address: 42H
- D1 to D126: Display Data
- S0, S1: Sleep Control Data
- K0, K1: Key Scan Output/Segment Output Selection Data
- P0, P1: Segment Output Port/General Purpose Output Port Selection Data
- SC: Segment ON/OFF Control Data
- DR: 1/2 Bias or 1/3 Bias Drive Selection Data

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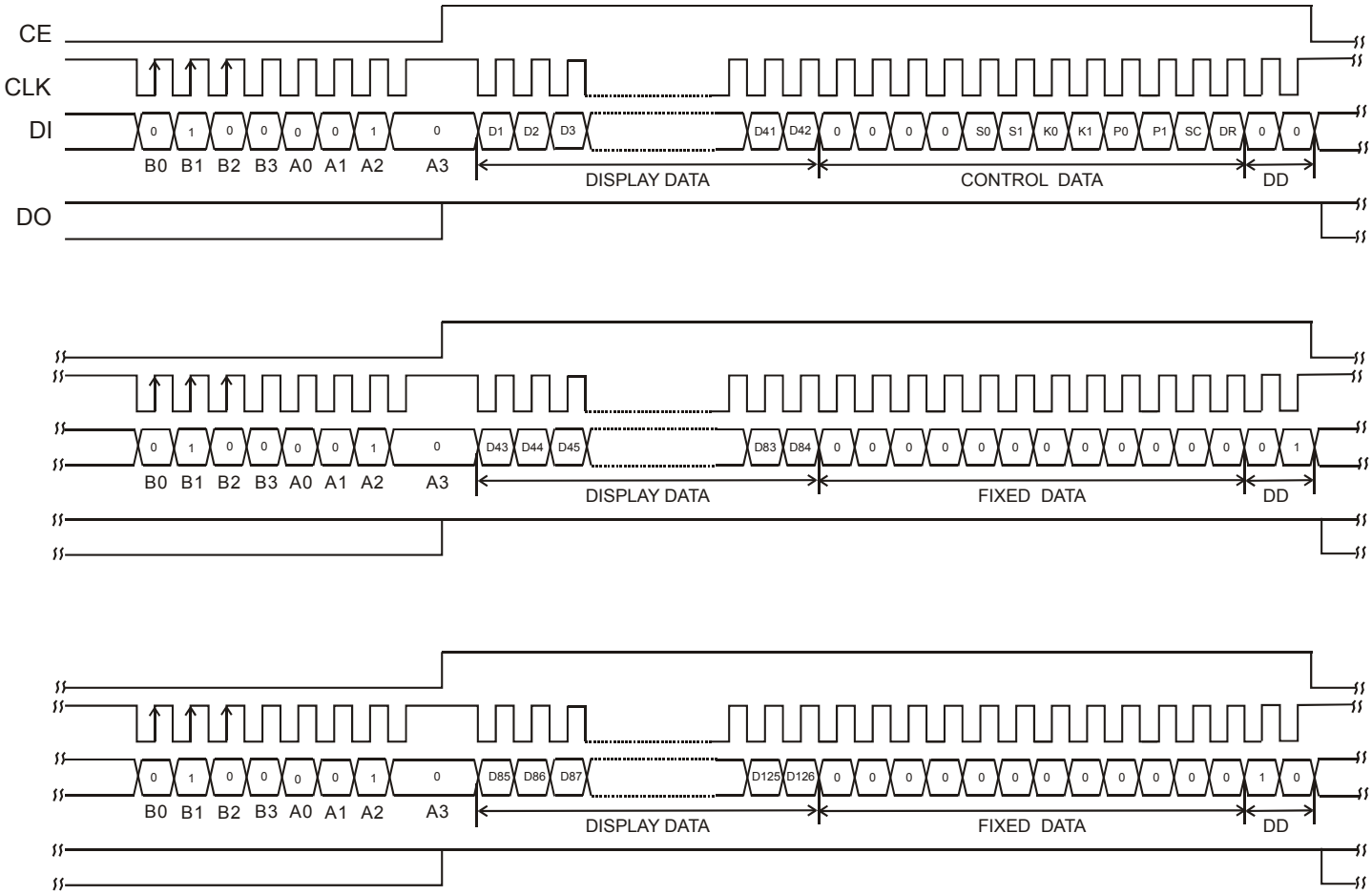
CONDITION 2: CLK IS TERMINATED AT THE "HIGH" LEVEL



Where: DD= Direction Data

- Address: 42H
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- DR: 1/2 Bias or 1/3 Bias Drive Selection Data

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CONTROL DATA FUNCTIONS

SLEEP CONTROL DATA BITS: S0, S1

S0 and S1 are sleep control data bits which can be switched between the normal and the sleep modes. They are used to set the states of the KO1 to KO6 Key Scan Outputs when the key scan is in a standby mode.

Control Data		Mode	OSC	Segment Outputs Common Outputs	State of Output Pin during Key Scan Standby Condition					
S0	S1				KO1	KO2	KO3	KO4	KO5	KO6
0	0	Normal	Operating	Operating	H	H	H	H	H	H
0	1	Sleep	Stopped	L	L	L	L	L	L	H
1	0	Sleep	Stopped	L	L	L	L	L	H	H
1	1	Sleep	Stopped	L	H	H	H	H	H	H

Note: This is under the assumption that the KO1/SG41 and KO2/SG42 Pins are selected for Key Scan Output.

KEY SCAN OUTPUT/SEGMENT OUTPUT SELECTION CONTROL DATA BITS: K0, K1

K0 and K1 are control data bits which may be used for key scan output or segment output.

Control Data		State of Output Pins		Maximum Number of Input Keys
K0	K1	KO1/SG41	KO2/SG42	
0	0	KO1	KO2	30
0	1	SG41	KO2	25
1	x	SG41	SG42	20

Note: x = Irrelevant

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SEGMENT OUTPUT/GENERAL PURPOSE OUTPUT PORTS SELECTION DATA BITS: P0, P1

P1 and P0 are control data bits which may be used for segment output port or general purpose output port.

Control Data		State of Output Pin			
P0	P1	SG1/P1	SG2/P2	SG3/P3	SG4/P4
0	0	SG1	SG2	SG3	SG4
0	1	P1	P2	SG3	SG4
1	0	P1	P2	P3	SG4
1	1	P1	P2	P3	P4

Condition 1: P0 and P1 are selected as General Purpose Output Port

When the control data bits, P0 and P1 are selected as General Purpose Output Port, the corresponding display data and output pins are listed below.

Output Pin	Corresponding Display Data
SG1/P1	D1
SG2/P2	D4
SG3/P3	D7
SG4/P4	D10

This means that, if for example the output pin -- SG4/P4 is used as a General Purpose Output Port, SG4/P4 Pin will output a high level when the display data , D10 is given a value of "1".

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SEGMENT ON/OFF CONTROL DATA BITS: SC

SC is used to control the ON/OFF state of segments.

SC	Display State
0	On
1	Off

When SC is set to "0", the segment display state is "ON". When SC is set to "1", the segment display is "OFF". This "OFF" state is achieved by outputting segment "OFF" waveforms from the segment output pins.

1/2 BIAS OR 1/3 BIAS DRIVE SELECTION DATA BIT: DR

DR is the control data bit used to select either an LCD 1/2 or 1/3 bias drive. When DR is set to "0", the 1/3 LCD Bias Drive is selected. On the other hand, if DR is set to "1", the 1/2 LCD Bias Drive is selected.

DR	LCD Bias Drive
0	1/3
1	1/2

DISPLAY DATA AND OUTPUT PINS

The display data and their corresponding output pins are listed in the table below.

Output Pin	COM1	COM2	COM3	Output Pin	COM1	COM2	COM3
SG1/P1	D1	D2	D3	SG22	D64	D65	D66
SG2/P2	D4	D5	D6	SG23	D67	D68	D69
SG3/P3	D7	D8	D9	SG24	D70	D71	D72
SG4/P4	D10	D11	D12	SG25	D73	D74	D75
SG5	D13	D14	D15	SG26	D76	D77	D78
SG6	D16	D17	D18	SG27	D79	D80	D81
SG7	D19	D20	D21	SG28	D82	D83	D84
SG8	D22	D23	D24	SG29	D85	D86	D87
SG9	D25	D26	D27	SG30	D88	D89	D90
SG10	D28	D29	D30	SG31	D91	D92	D93
SG11	D31	D32	D33	SG32	D94	D95	D96
SG12	D34	D35	D36	SG33	D97	D98	D99
SG13	D37	D38	D39	SG34	D100	D101	D102
SG14	D40	D41	D42	SG35	D103	D104	D105
SG15	D43	D44	D45	SG36	D106	D107	D108
SG16	D46	D47	D48	SG37	D109	D110	D111
SG17	D49	D50	D51	SG38	D112	D113	D114
SG18	D52	D53	D54	SG39	D115	D116	D117
SG19	D55	D56	D57	SG40	D118	D119	D120
SG20	D58	D59	D60	KO1/SG41	D121	D122	D123
SG21	D61	D62	D63	KO2/SG42	D124	D125	D126

Example: The segment output pin -- SG11 has the corresponding display data bits -- D31, D32, D33. The table below gives the segment output states of SG11 Pin.

Display Date			State of Output Pin
D31	D32	D33	SG11
0	0	0	LCD Segments for Com1, Com2, and Com3 are "Off"
0	0	1	LCD Segments for Com3 is "On"
0	1	0	LCD Segment for Com2 is "On"
0	1	1	LCD Segments for Com2 and Com3 are "On"
1	0	0	LCD Segments for Com1 is "On"
1	0	1	LCD Segments for Com1 and Com3 are "On"
1	1	0	LCD Segments for Com 1 and Com2 are "On"
1	1	1	LCD Segments for Com1, Com2, and Com3 are "On

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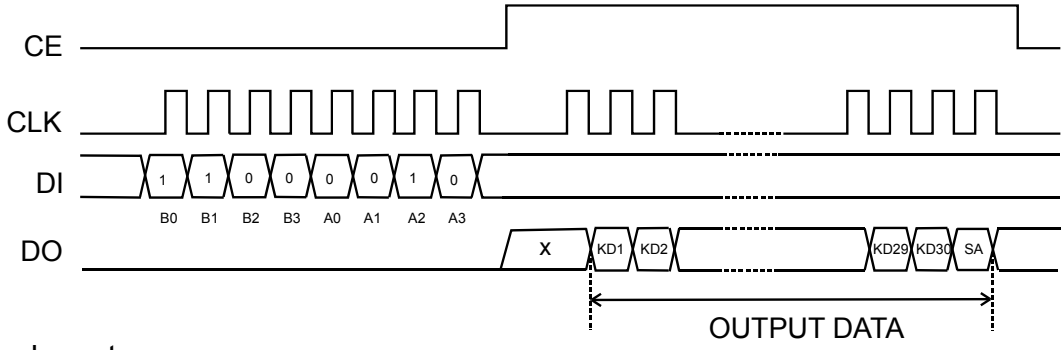
SERIAL DATA OUTPUT

CONDITION 1: CLK IS TERMINATED AT THE "LOW" LEVEL

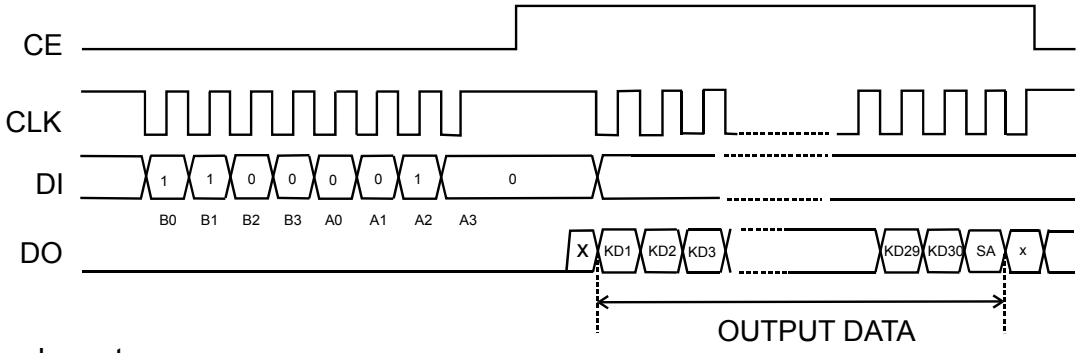


Where: x = Irrelevant

- Address: 43H
- KD1 to KD30: Key Data
- SA: Sleep Acknowledge Data

Notes:
1. The SA (Sleep Acknowledge data) will not be valid if the key data read operation is executed when the DO is in "HIGH" level.
2. To be able to read the data correctly, the data reading process must be performed in the midpoint of the rising and falling edge of the clock.

CONDITION 2: CLK IS TERMINATED AT THE "HIGH" LEVEL



Where: x = Irrelevant

- Address: 43H
- KD1 to KD30: Key Data
- SA: Sleep Acknowledge Data

Notes:
1. The SA (Sleep Acknowledge data) will not be valid if the key data read operation is executed when the DO is in "HIGH" level.
2. To be able to read the data correctly, the data reading process must be performed in the midpoint of the rising and falling edge of the clock.

OUTPUT DATA

KEY DATA: KD1 TO KD30

A key matrix having a maximum of 30 keys maybe constructed using the KO1 to KO6, and KI1 to KI5 lines. If any one of these keys are pressed, the key output data corresponding to the respective key is set to "1". Please refer to the table below.

	KI1	KI2	KI3	KI4	KI5
KO1/SG41	KD1	KD2	KD3	KD4	KD5
KO2/SG42	KD6	KD7	KD8	KD9	KD10
KO3	KD11	KD12	KD13	KD14	KD15
KO4	KD16	KD17	KD18	KD19	KD20
KO5	KD21	KD22	KD23	KD24	KD25
KO6	KD26	KD27	KD28	KD29	KD30

When a key matrix (maximum of 20 keys) are constructed using the KO3 to KO6 and KI1 to KI5 lines and the KO1/SG41 and KO2/SG42 pins are used as Segment Output Pins via the control data bits -- K0 and K1--, the KD1 to KD10 key data bits are set to "0".

SLEEP ACKNOWLEDGE DATA BIT: SA

SA is sleep acknowledge data bit. SA is set to "1" during the Sleep Mode and "0" during the Normal Mode. When the key is pressed, the sleep acknowledge data bit will be set to the state.

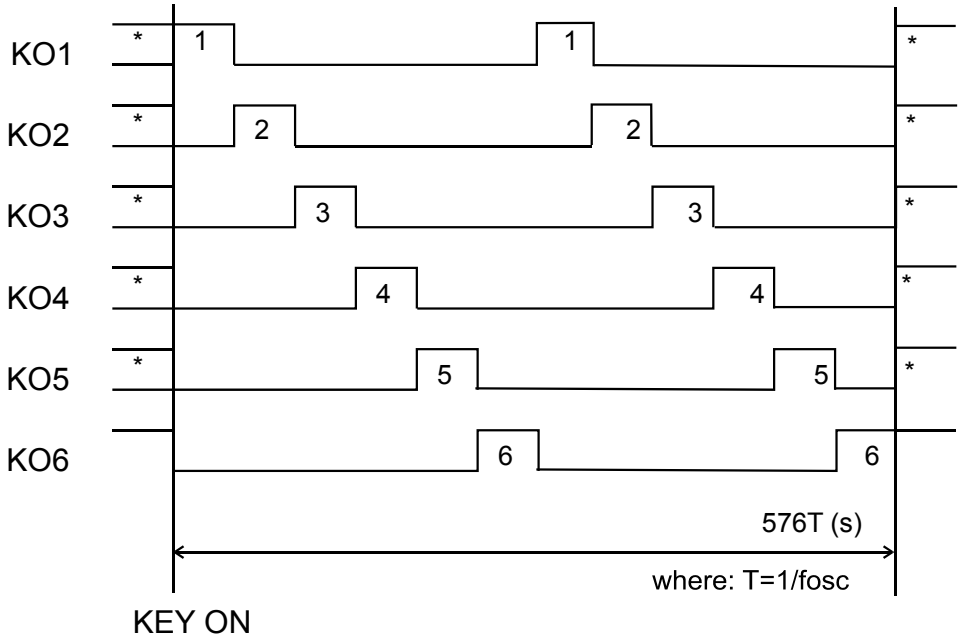
SLEEP MODE FUNCTION

The Sleep Mode is activated by setting S0 or S1 to "1". Both the segment and common outputs will be "LOW" and oscillation operation will stop reducing the power dissipation. However, oscillation operation will be activated again when a key is pressed. The Sleep Mode is deactivated when both S0 and S1 bits are set to "0". It should be noted that even in the Sleep Mode, the SG1/P1 to SG4/P4 pins can also be used as General Purpose Output Ports depending on the states of the P0 and P1 control data bits. Please refer to the control data section for details.

KEY SCAN OPERATION

KEY SCAN TIMING

The key scan period is 288T (s). The key is scanned twice and when the key data is in agreement with the key that has been pressed, then the key operation is valid. The key data read request (DO is set to "LOW") is outputted after starting a key scan operation. If the key data is not in agreement with the key that has been pressed, the PT6553 scans the key again. PT6553 can only detect a key press longer than or equal to 615T (s). Please refer to the diagram below.



Note:
* = During the Sleep Mode Condition, the States ("HIGH" or "LOW") of these pins are determined by the control data bits -- S0 and S1 bits. When these pins are set to "LOW" State the key scan output signals are not outputted.

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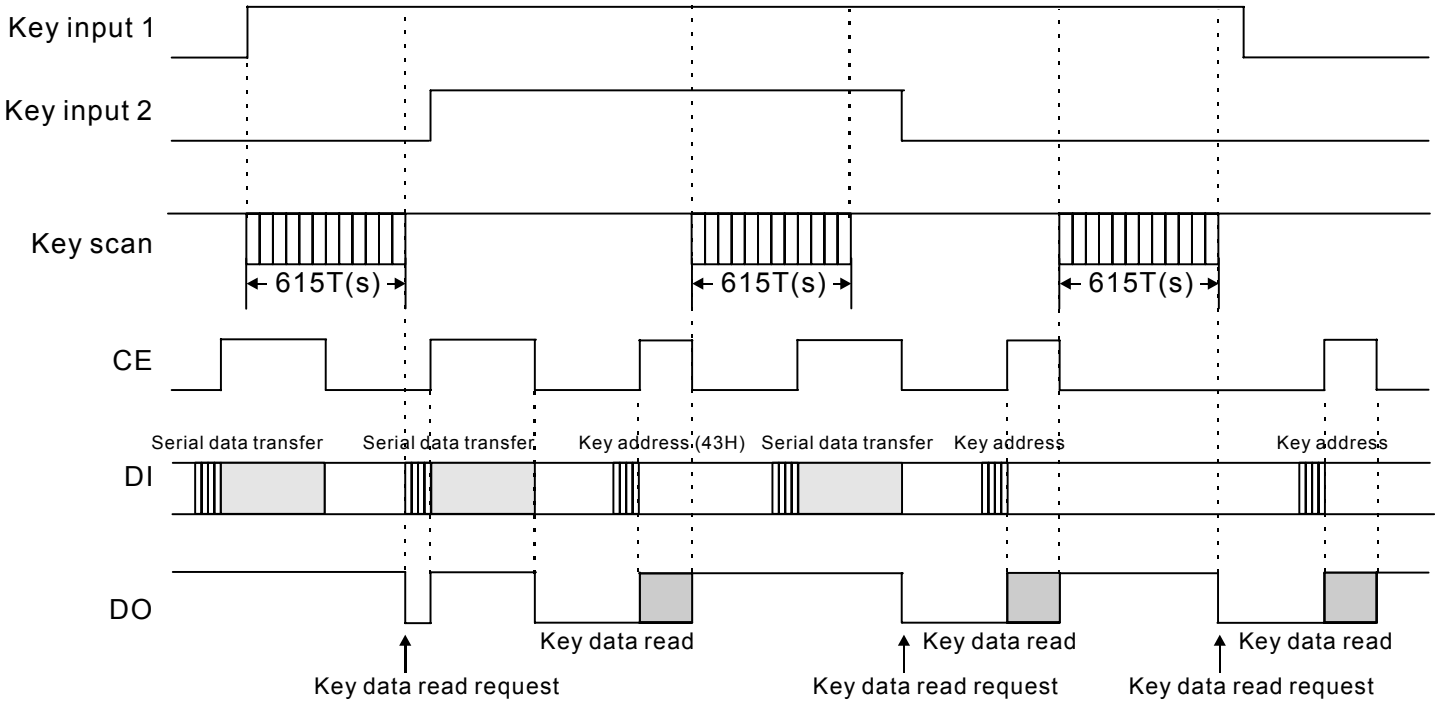
NORMAL MODE

Under the normal mode, the pins -- KO1 to KO6 -- are set to "HIGH". When a key is pressed, a key scan operation commences. The keys are scanned until all keys are released. Multiple key operation is recognized. When a key is pressed longer than 615T (s), PT6553 outputs a key data read request to the controller. Please take note that T= 1/[fosc] and during the key data read request, the DO is set to "LOW". The controller then acknowledges the key data request and reads the key data. However, if the CE is "HIGH" during the serial data transfer, DO will be set to "HIGH". After the key data reading operation is completed, the key data request is cleared (DO is set to "HIGH") and another key scan operation is performed. It must be noted that DO is an open-drain output and thus requires a 1K to 10K Ohms pull-up resistor. Please refer to the diagram below.



T = 1/fosc

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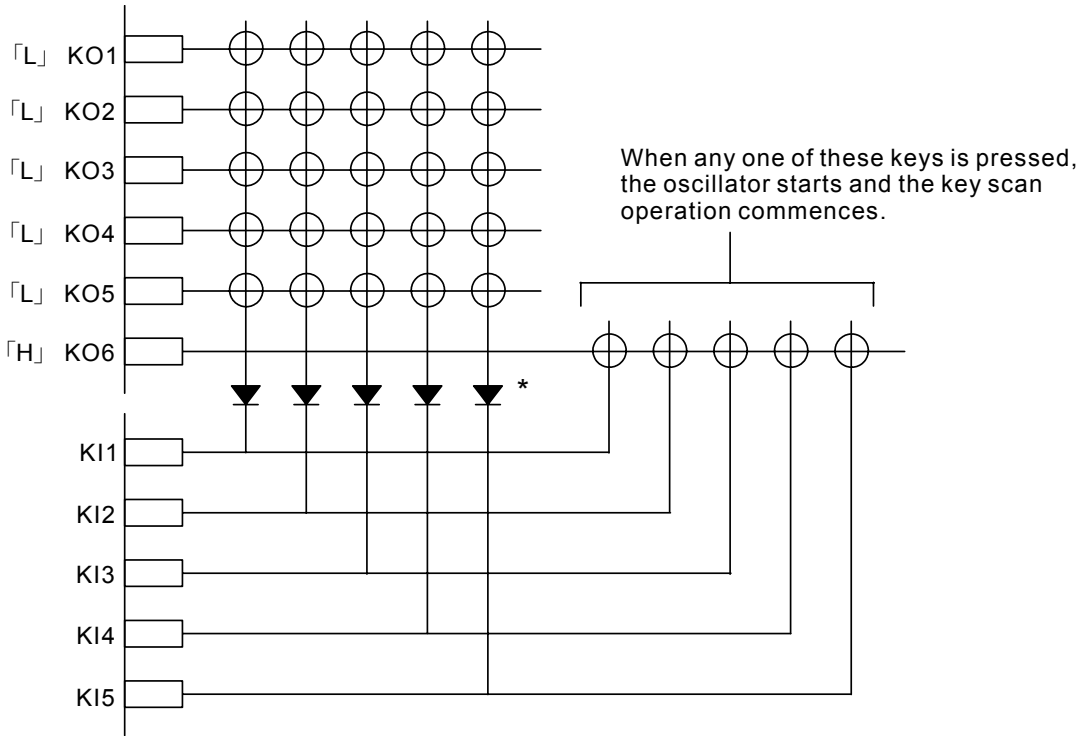
SLEEP MODE

Under the Sleep Mode, the pins -- KO1 to KO6 are set to "HIGH" or "LOW" depending on the states of the S0 and S1 control data bits. When a key located in one of the lines connected to any of the KO1 to KO6 pins which is set to "HIGH" is pressed, the oscillation starts and a key scan operation is performed. Keys are scanned until all the keys are released. Multiple key operation is valid if the multiple key data bits are set. When a key is pressed longer than 615T (s), PT6553 outputs a key data request to the controller. The controller acknowledges this request and performs the key data read operation. However, of CE is set to "HIGH" during the serial data transfer, DO will be set to "HIGH".

After completion of the key data read operation by the controller, the key data read request is cleared (DO is set to "HIGH") and another key scan operation is performed. Please note that this does not clear the Sleep Mode. Please also be aware the DO is an open-drain output and requires 1K to 10 KΩ pull-up resistor. The following is an example of a Sleep Mode Key Scan.

Example: S0="0", S1="1", Sleep Mode with KO6 = "HIGH"



Note: * = It is recommended that these diodes be connected in order to prevent incorrect operation due to sneak currents in the KO6 scan output signals when the keys on the KO1 to KO5 lines are pressed simultaneously. These diodes are needed to recognize multiple key presses on the KO6 line under the sleep mode state with only the KO6 Line is "HIGH" (i.e. the example above.)

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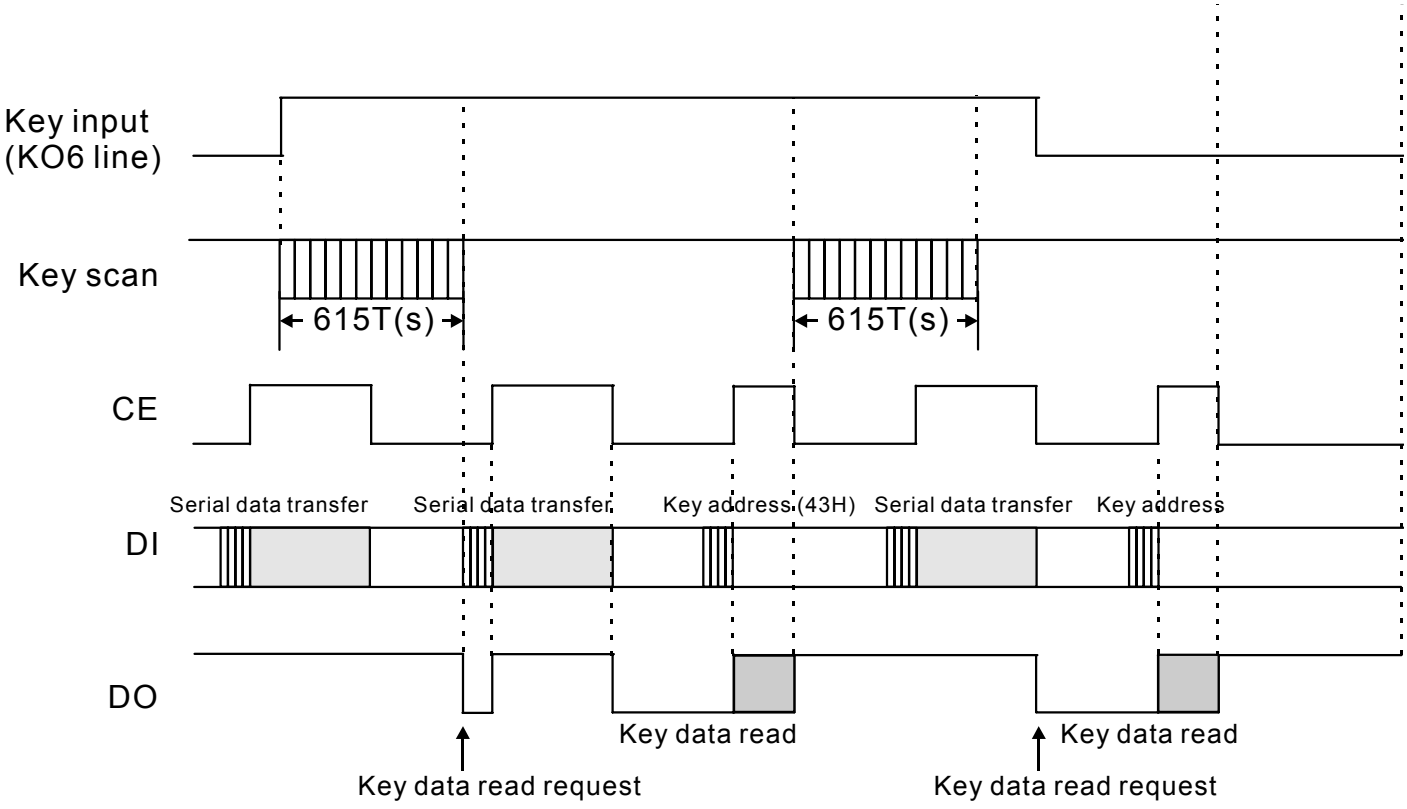

T = 1/fosc

MULTIPLE KEY OPERATION

For dual key operation, triple key operation on the KI1 to KI5 input lines, or multiple key operation on the KO1 to KO6 output lines do not to connect an external diode. Other multiple key operation other than those stated may result in erroneous key press recognition. Therefore, to avoid this from happening, a diode must be inserted in series with each key. Applications that do not recognize multiple (3 or more) key operation should check the key data for three or more bits and ignore such data.

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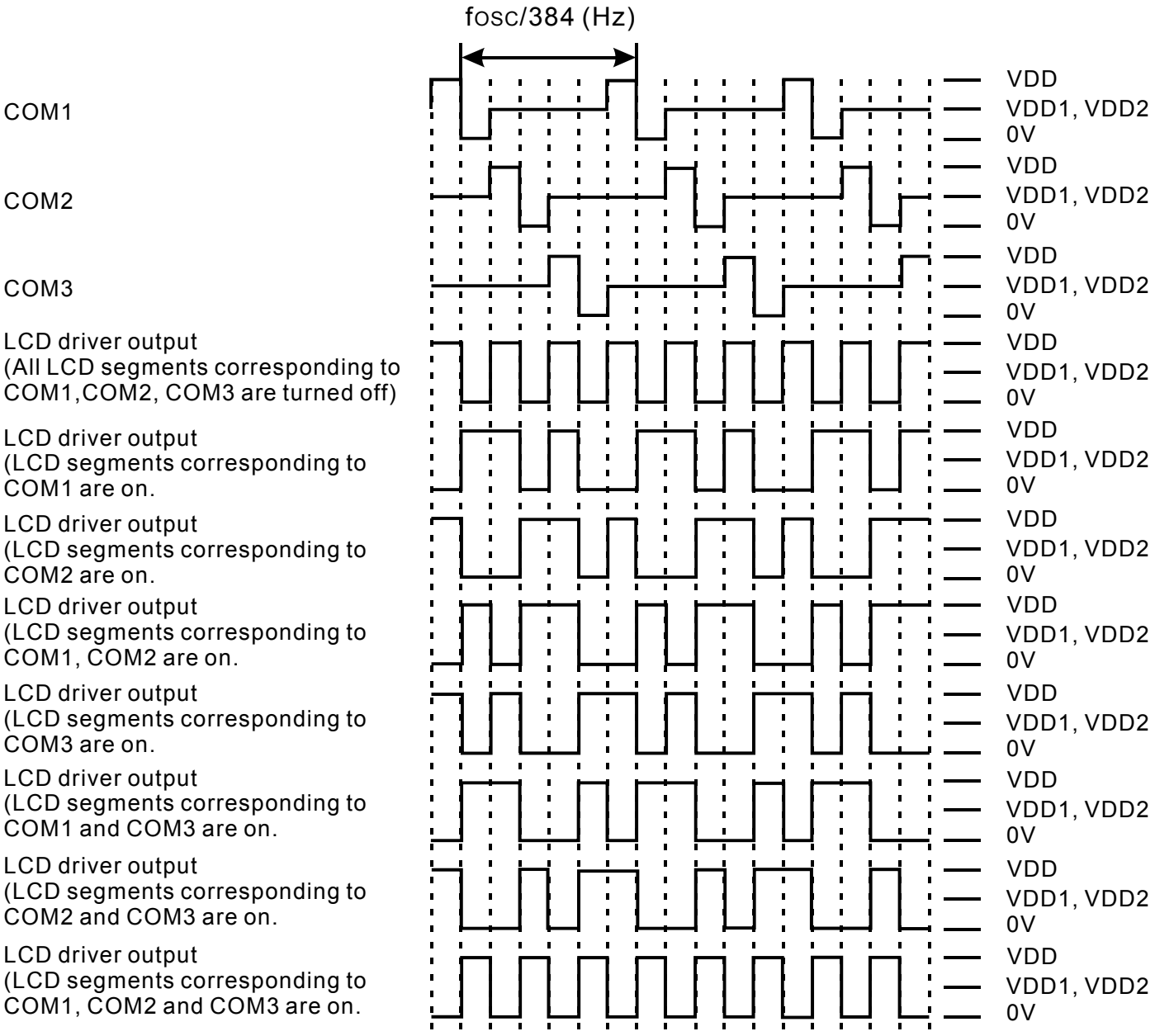
1/3 DUTY, 1/2 BIAS DRIVE WAVEFORMS



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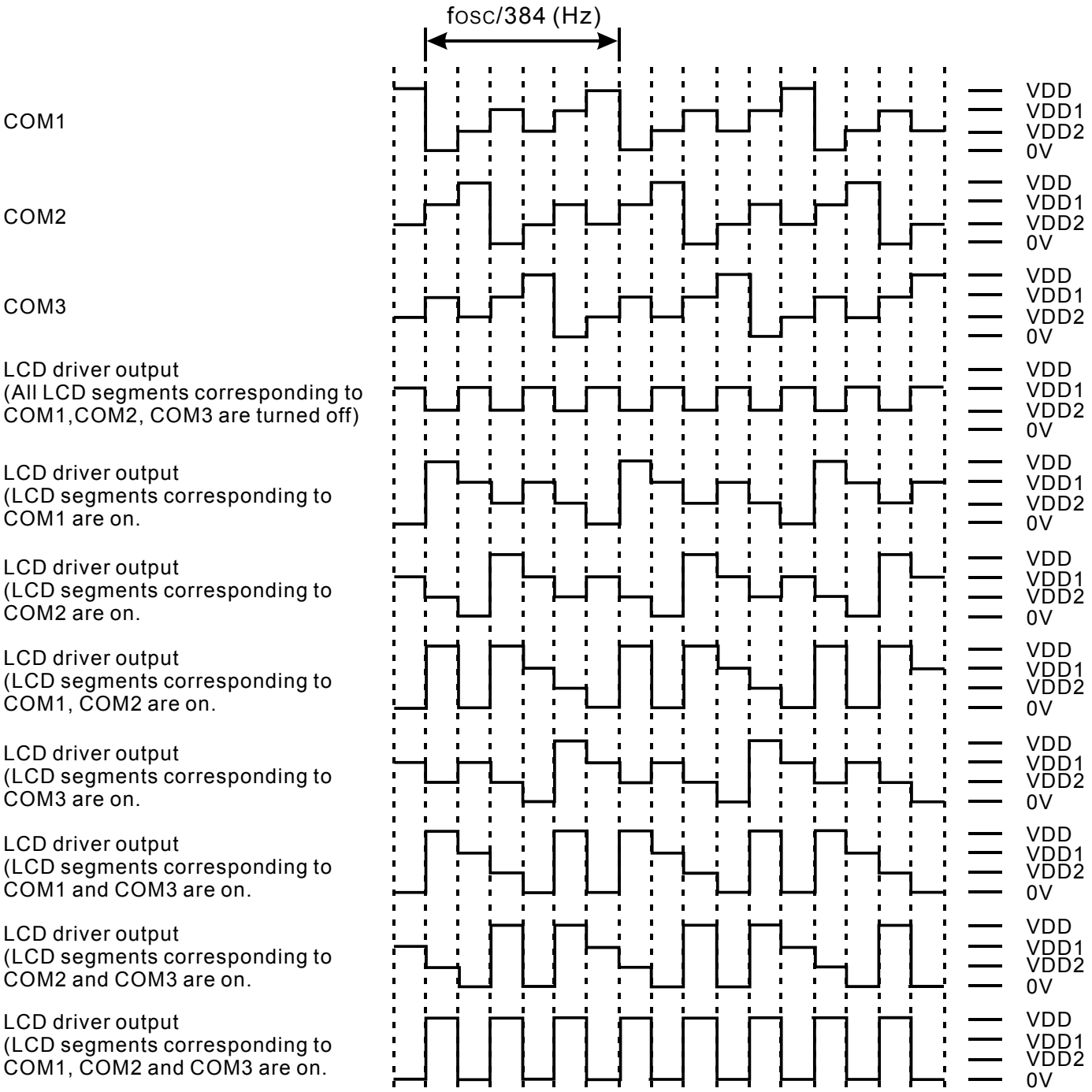
1/3 DUTY, 1/3 BIAS DRIVE WAVEFORMS



VOLTAGE DETECTION TYPE RESET CIRCUIT (VDET)

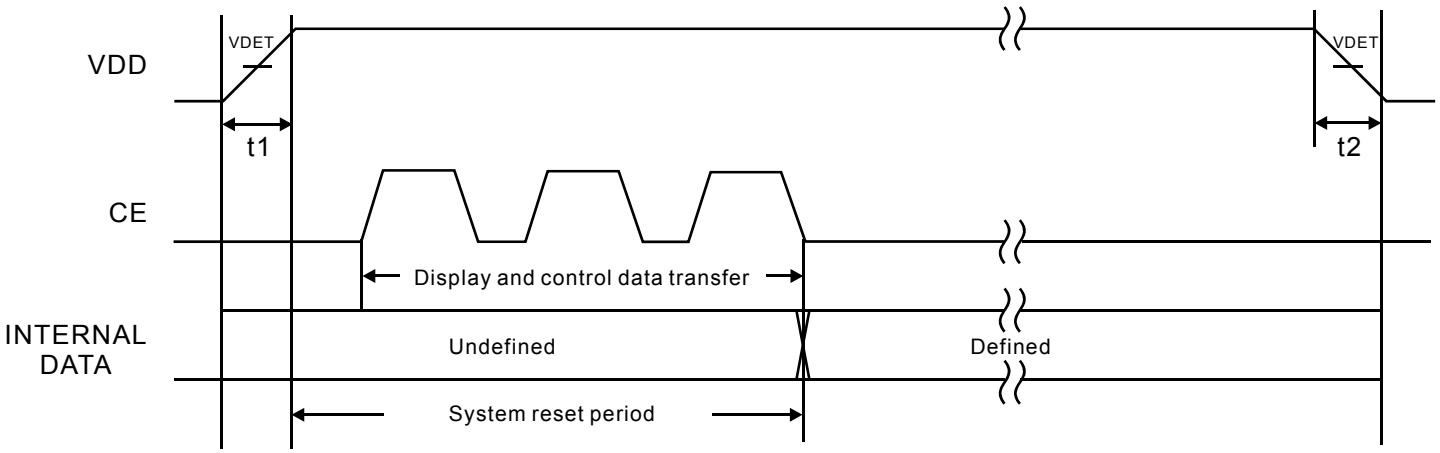
The Voltage Detection Type Reset Circuit (V_{DET}) generates an output signal and resets the system when the power is first applied as well as when the voltage drops (i.e., when the power supply voltage is less than or equal to the power down detection voltage, V_{DET} [3.0v typ.]). To insure proper operation of this function, a capacitor must be connected to the power supply line so that the power supply voltage (V_{DD}) rise time (when the power is first applied) and the power supply voltage (V_{DD}) fall time (when the voltage drops) are at least 1ms. Please refer to the diagram below.

SYSTEM RESET

RESET METHOD

If the Supply voltage V_{DD} rise time is at least 1 ms when power is applied, a system reset will be initialized by the V_{DET} output signal when the supply voltage is increased. If the supply voltage V_{DD} fall time is at least 1ms when the power drops, a system reset will be initialized by the V_{DET} output signal when the supply voltage is decreased. When all the serial data (including display data, D1 to D126 and the control data) has been transferred, reset function is cleared.

This means that if for example, on the falling edge of the last direction data transfer's CE signal, (that is after all the direction data have been transferred), the reset function is cleared. Please refer to the diagram below.



Power Supply Voltage (V_{DD}) Rise Time: t1 ≥ 1ms
Power Supply Voltage (V_{DD}) Fall Time: t2 ≥ 1ms

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STATES OF THE PT6553 INTERNAL BLOCK DURING THE RESET PERIOD

Clock Generator

When the reset function is initialized, the base clock is terminated. The OSC Pin state, however is determined after the S0 and S1 control data bits are transferred.

Common Driver, Segment Driver & Latch

When the reset function is initialized, the display is turned off. The display data, however, can be inputted to the latch circuit in this state.

Key Scan

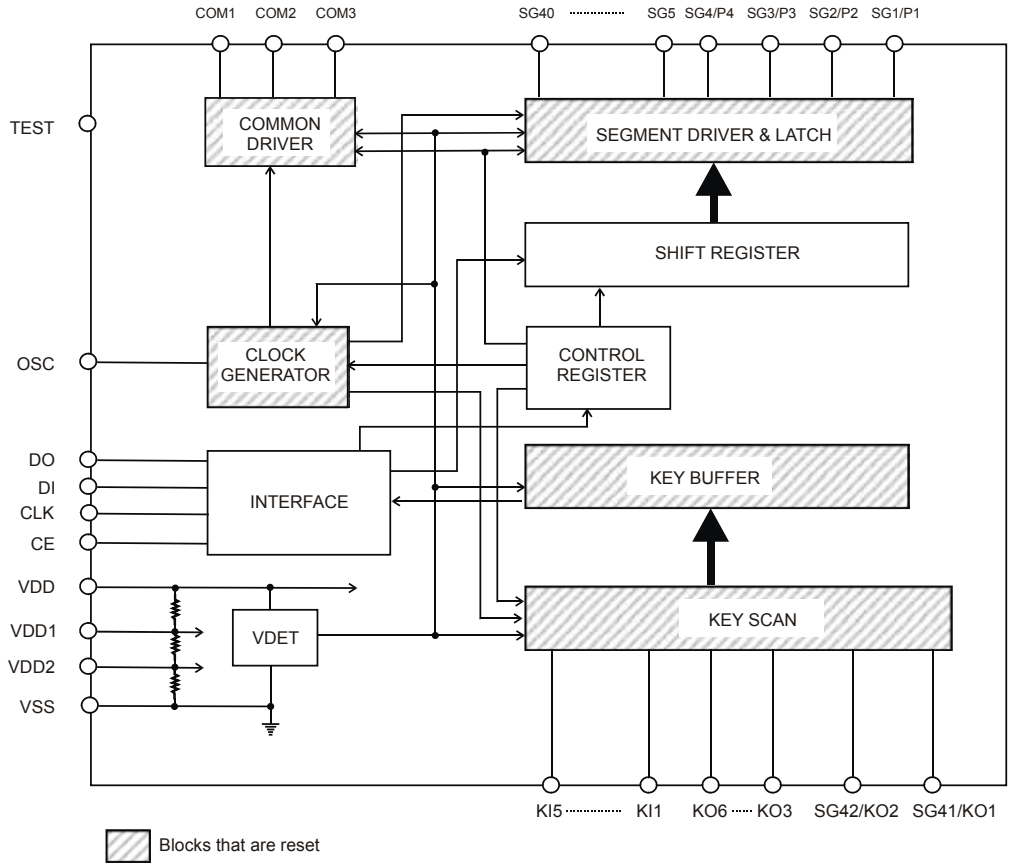
When the reset function is applied, the circuit is set to the initial state and at the same time, the key scan operation is disabled.

Key Buffer

When the reset function is initialized, all the key data are set to "LOW".

Interface, Control Register, Shift Register

These circuits are not reset since serial data transfer is possible.



STATES OF THE OUTPUT PINS DURING THE RESET PERIOD

The states of the output pins during the reset period are shown in the table below.

Output Pin	State during the Reset Period
SG1/P1 to SG4/P4	L(see Note 1)
SG5 to SG40	L
COM1 to COM3	L
KO1/SG41, KO2/SG42	L (see Note 1)
KO3 to KO5	x (see Note 2)
KO6	H
DO	H (see Note 3)

Notes:
1. These output pins are forcibly set to the "Segment Output Function" and set to "LOW".
2. When the power is first applied, these output pins are undefined until the S0 and S1 control data bits have been transferred.
3. This output pin is an open drain output, therefore, a 1K to 10 KΩ pull-up resistor is needed. This pin remains "HIGH" during the reset period even if a key data read operation is performed.
4. x = irrelevant

DISPLAY DATA TRANSFER FROM CONTROLLER

There are three operations involved in the transfer of display data (D1 to D126) to the PT6553. All display data must be transferred within 30 ms so as to insure and maintain the quality of the displayed image.

CONTROLLER KEY DATA READ TECHNIQUE

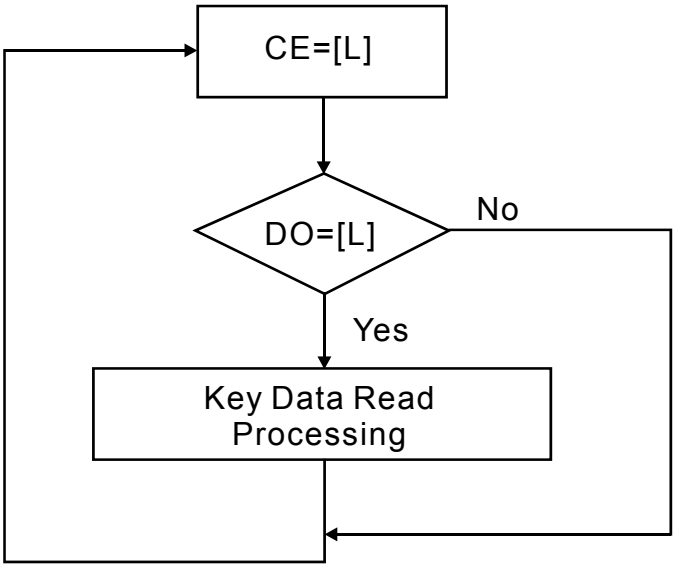
Timer - based key Data Acquisition

The controller makes use of a timer to determine the Key ON/OFF states and to read the key data. The controller must check every t7 period the DO state when the CE is in the "LOW" state. If the DO is "LOW", the controller will acknowledge the key that has been pressed and execute the key data read operation. The t7 must satisfy the following condition:

$t7 \geq (t5 + t6 + t4)$

If a key read operation is executed when the DO is in "HIGH" State, the read key data (KD1 to KD30) and the sleep acknowledge data (SA) will be invalid.

The timer based key data acquisition flowchart is given below.



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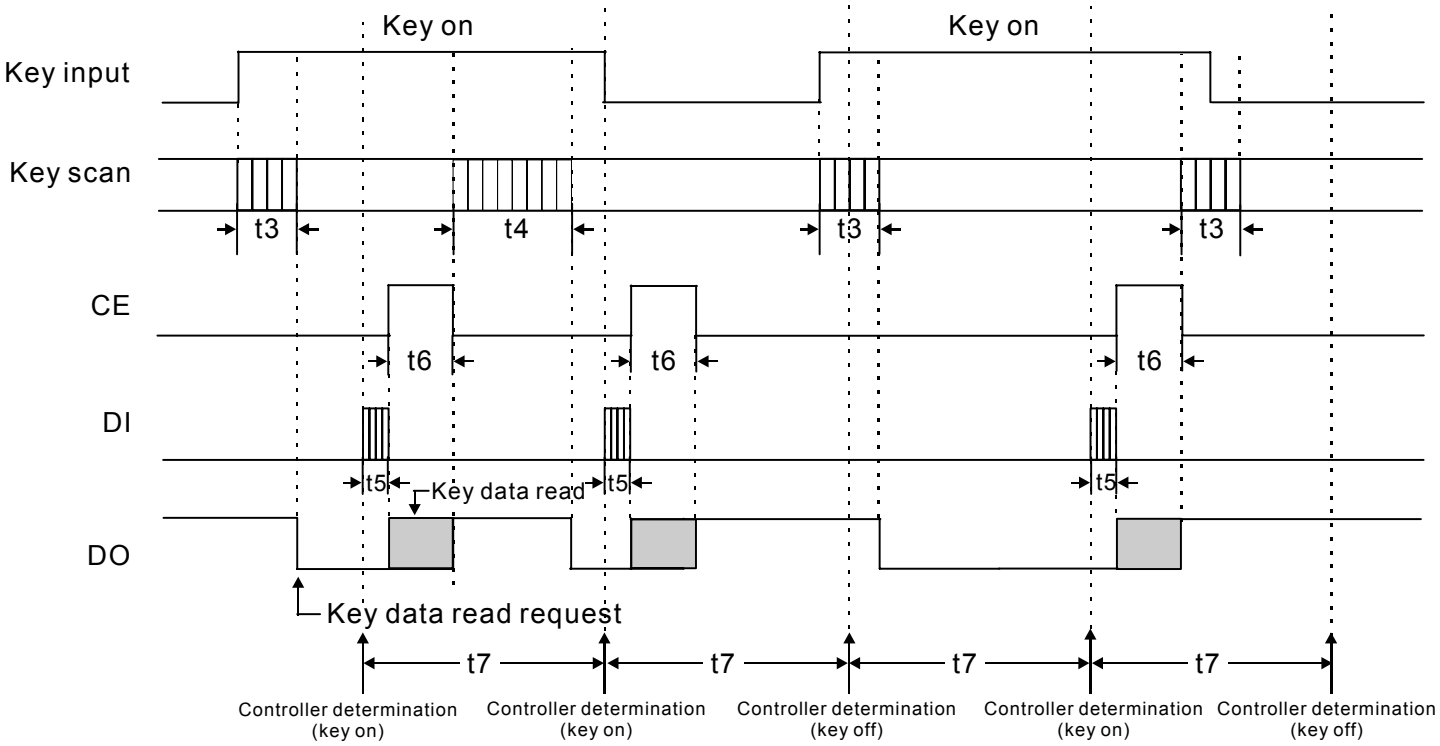
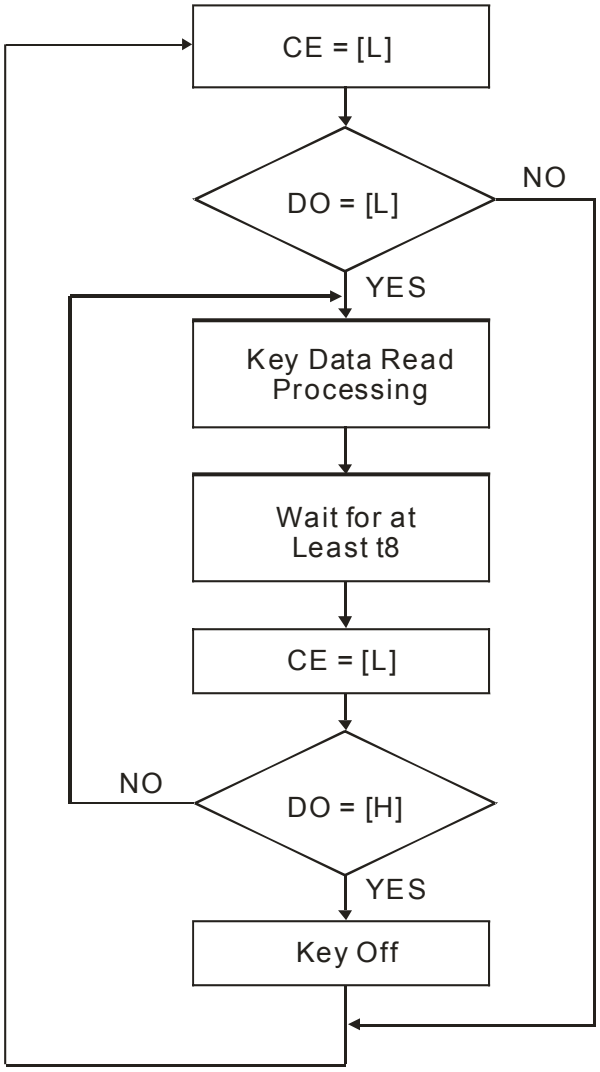
Timing Diagram



Notes:
1. t3 = Key Scan Execution Time when after two key scan operations, the key data match (615T (s))
2. t4 = Key Scan Execution Time when after two key scan operations, the key data do not match and the key scan operation was once again performed. (1230T (s)).
3. T = 1/fosc
4. t5 = Key Address (43H) Transfer Time
5. t6 = Key Data Read Time

Interrupt - Based Key Data Acquisition

The interrupt-based key data acquisition flowchart is given below.



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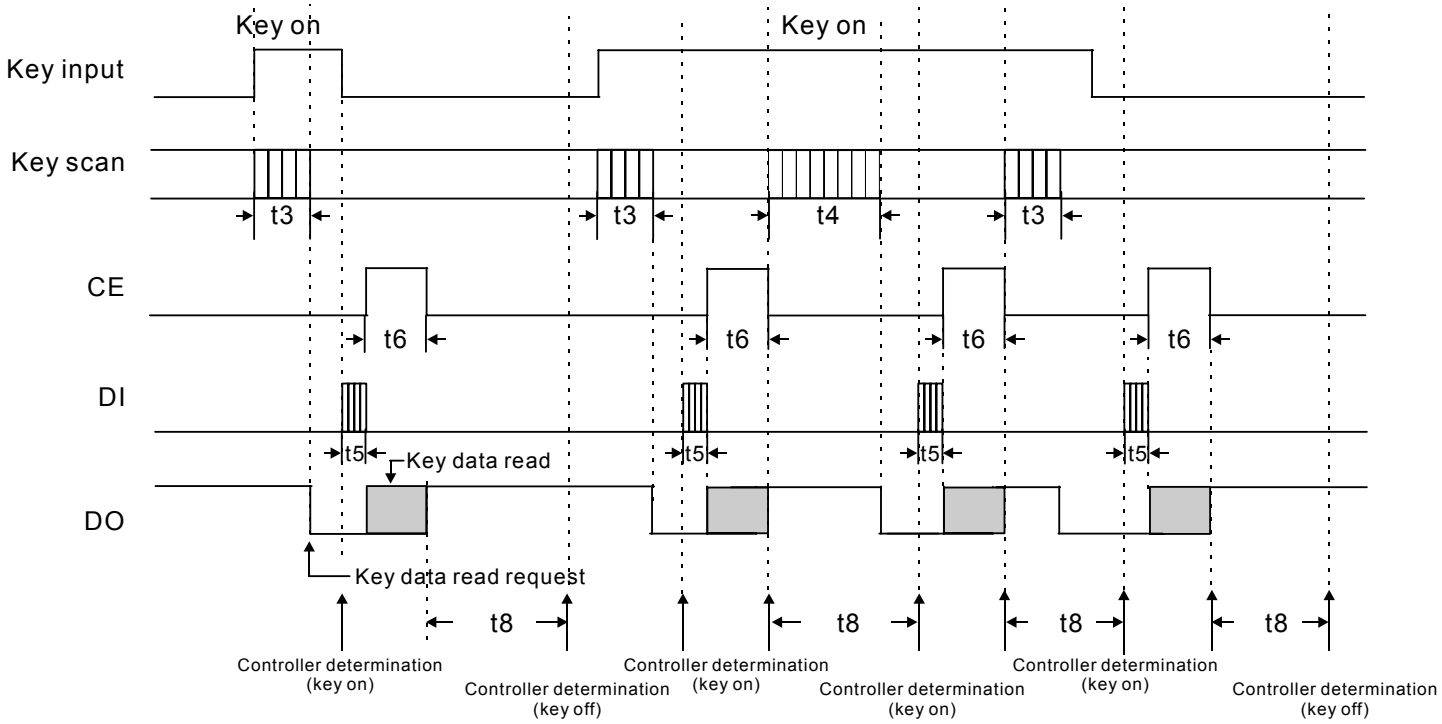
Interrupt - Based Key Data Acquisition Timing Diagram



Notes:
1. t3 = Key Scan Execution Time when after two key scan operations, the key data match (615T (s))
2. t4 = Key Scan Execution Time when after two key scan operations, the key data do not match and the key scan operation was once again performed. (1230T (s)).
3. T = 1/fosc
4. t5 = Key Address (43H) Transfer Time
5. t6 = Key Data Read Time

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ABSOLUTE MAXIMUM RATING

(Unless otherwise specified Ta=25℃, Vss=0V)

Parameter	Symbol	Conditions	Rating	Unit
Maximum supply voltage	V_{DD}max	V_{DD}	-0.3 to +7.0	V
Input voltage	V_{IN1}	CE, CLK, DI	-0.3 to V_{DD}+0.3	V
	V_{IN2}	OSC, KI1 to KI5, TEST, V_{DD1}, V_{DD2}	-0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT1}	DO	-0.3 to V_{DD}+0.3	V
	V_{OUT2}	OSC, SG1 to SG42, COM1 to COM3, KO1 to KO6, P1 to P4	-0.3 to +V_{DD}+0.3	V
Output current	I_{OUT1}	SG1 to SG42	300	μA
	I_{OUT2}	COM1 to COM3	3	mA
	I_{OUT3}	KO1 to KO6	1	mA
	I_{OUT4}	P1 to P4	5	mA
Allowable power dissipation	Pdmax	Ta=85℃	200	mW
Operating temperature	Topr	-	-40 ~ +85	℃
Storage temperature	Tstg	-	-65 ~ +150	℃

ALLOWABLE OPERATING CONDITION

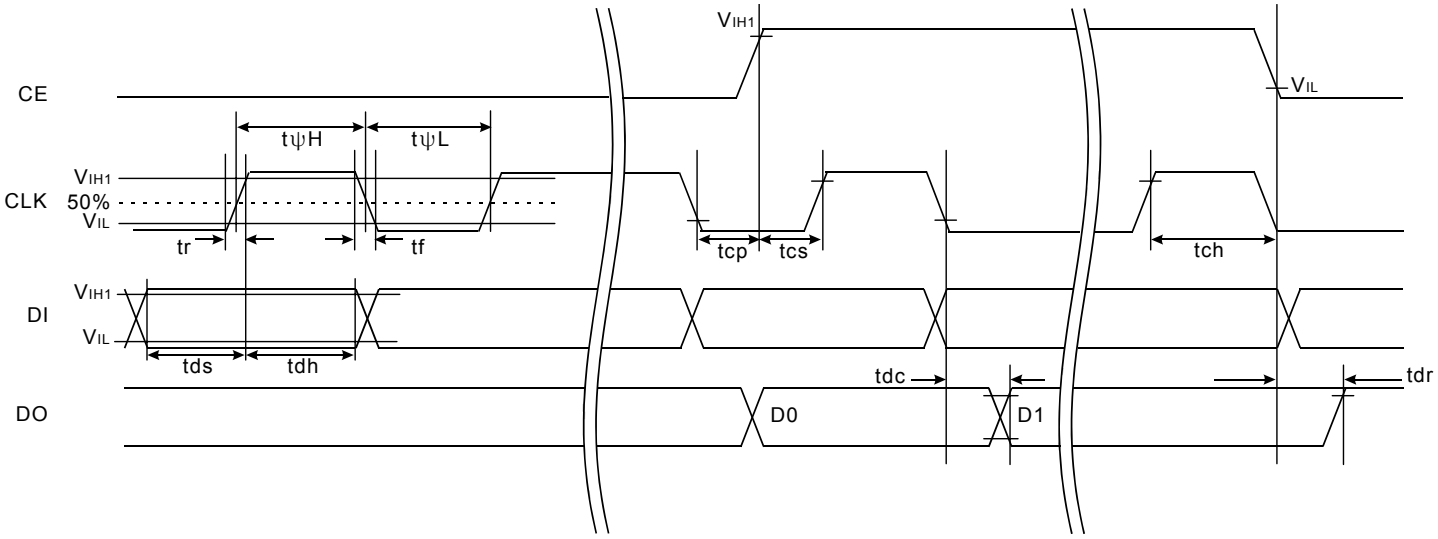
(Unless otherwise specified, Ta=25℃, Vss=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{DD}	4.5	-	6.0	V
Input voltage	V_{DD1}	V_{DD1}	-	$2/3V_{DD}$	V_{DD}	V
	V_{DD2}	V_{DD2}	-	$1/3V_{DD}$	V_{DD}	V
High level input voltage	V_{IH1}	CE, CLK, DI	$0.8V_{DD}$	-	V_{DD}	V
	V_{IH2}	KI1 to KI5	$0.6V_{DD}$	-	V_{DD}	V
Low level input voltage	V_{IL}	CE, CLK, DI, KI1 to KI5	0	-	$0.2V_{DD}$	V
Oscillation resistance	R_{OSC}	OSC	-	68	-	KΩ
Oscillation capacitor	C_{OSC}	OSC	-	820	-	pF
Oscillation range	f_{OSC}	OSC	19	38	76	KHz
Data setup time	tds	CLK, DI (see Note 2)	160	-	-	ns
Data hold time	tdh	CLK, DI (see Note 2)	160	-	-	ns
CE wait time	tcp	CE, CLK (see Note 2)	160	-	-	ns
CE setup time	tcs	CE, CLK (see Note 2)	160	-	-	ns
CE hold time	tch	CE, CLK (see Note 2)	160	-	-	ns
High level clock pulse width	$t_{øH}$	CLK (see Note 2)	160	-	-	ns
Low level clock pulse width	$t_{øL}$	CLK (see Note 2)	160	-	-	ns
Rise time	tr	CE, CLK, DI (see Note 2)	-	160	-	ns
Fall time	t_f	CE, CLK, DI (see Note 2)	-	160	-	ns
DO output delay time	tdc	DO, Rpu=4.7KΩ, CL=10pF (see Note 1 & 2)	-	-	1.5	μs
DO rise time	tdr	DO, Rpu=4.7KΩ, CL=10pF (see Note 1 & 2)	-	-	1.5	μs

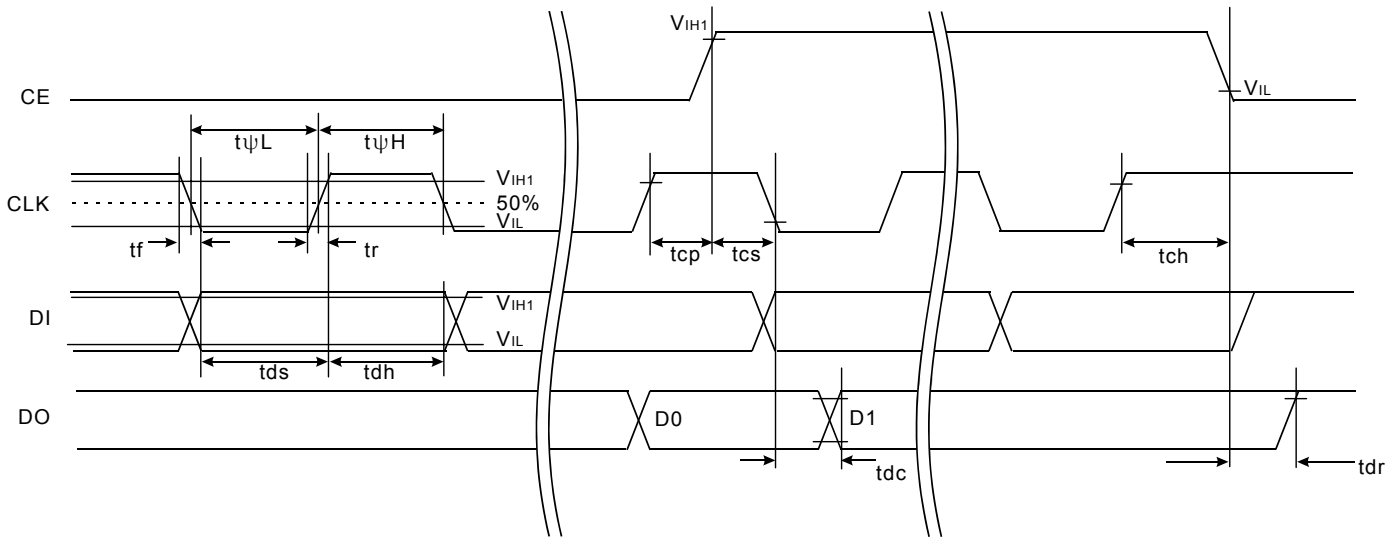
Notes:
1. DO is an open-drain output, therefore, these values depend on the resistance value of pull-up resistor Rpu and the capacitance value of the load capacitor, CL.
2. Refer to the Timing Waveforms shown on page 30.

TIMING WAVEFORMS

CONDITION 1: WHEN CLK IS TERMINATED AT "LOW" LEVEL



CONDITION 2: WHEN CLK IS TERMINATED AT "HIGH" LEVEL



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ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, Ta=25℃, V_{DD}=5V, V_{SS}=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Hysteresis	V_H	CE, CLK, DI	-	$0.1V_{DD}$	-	V
Power-down detection voltage	V_{DET}		2.7	3.0	3.3	V
High level input current	I_{IH}	CE, CLK, DI, VI=VDD	-	-	5.0	μA
Low level input current	I_{IL}	CE, CLK, DI, VI=0V	-5.0	-	-	μA
Pull-down resistance	R_{PD}	KI1 to KI5, V_{DD}=5.0V	50	100	250	KΩ
High level output voltage	V_{OH1}	KO1 to KO6, I_O=-500μA	V_{DD}-1.2	V_{DD}-0.5	V_{DD}-0.2	V
	V_{OH2}	P1 to P4, I_O=-1mA	V_{DD}-1.0	-	-	V
	V_{OH3}	SG1 to SG42, I_O=-20μA	V_{DD}-1.0	-	-	V
	V_{OH4}	COM1 to COM3, I_O=-100μA	V_{DD}-1.0	-	-	V
Low level output voltage	V_{OL1}	KO1 to KO6, I_O=35μA	0.2	0.5	1.5	V
	V_{OL2}	P1 to P4, I_O=1mA	-	-	1.0	V
	V_{OL3}	SG1 to SG42, I_O=20μA	-	-	1.0	V
	V_{OL4}	COM1 to COM3, I_O=100μA	-	-	1.0	V
	V_{OL5}	DO, I_O=1mA	-	0.1	0.5	V
Middle level output voltage*	V_{MID1}	COM1 to COM3, 1/2 Bias. I_O=±100μA	$1/2V_{DD}$-1.0	-	$1/2V_{DD}$+1.0	V
	V_{MID2}	SG1 to SG42, 1/3 Bias. I_O=±20μA	$2/3V_{DD}$-1.0	-	$2/3V_{DD}$+1.0	V
	V_{MID3}	SG1 to SG42, 1/3 Bias. I_O=±20μA	$1/3V_{DD}$-1.0	-	$1/3V_{DD}$+1.0	V
	V_{MID4}	COM1 to COM3, 1/3 Bias. I_O=±100μA	$2/3V_{DD}$-1.0	-	$2/3V_{DD}$+1.0	V
	V_{MID5}	COM1 to COM3, 1/3 Bias. I_O=±100μA	$1/3V_{DD}$-1.0	-	$1/3V_{DD}$+1.0	V
Oscillation frequency	fosc	OSC, R=68KΩ, C=820pF	30.4	38	45.6	KHz
Current drain	I_{DD1}	Sleep Mode	-	-	100	μA
	I_{DD2}	V_{DD}=6.0, Output Open 1/3 Bias fosc=38kHz	-	350	700	μA
	I_{DD3}	V_{DD}=6.0 Output Open 1/2 Bias fosc=38kHz	-	300	600	μA

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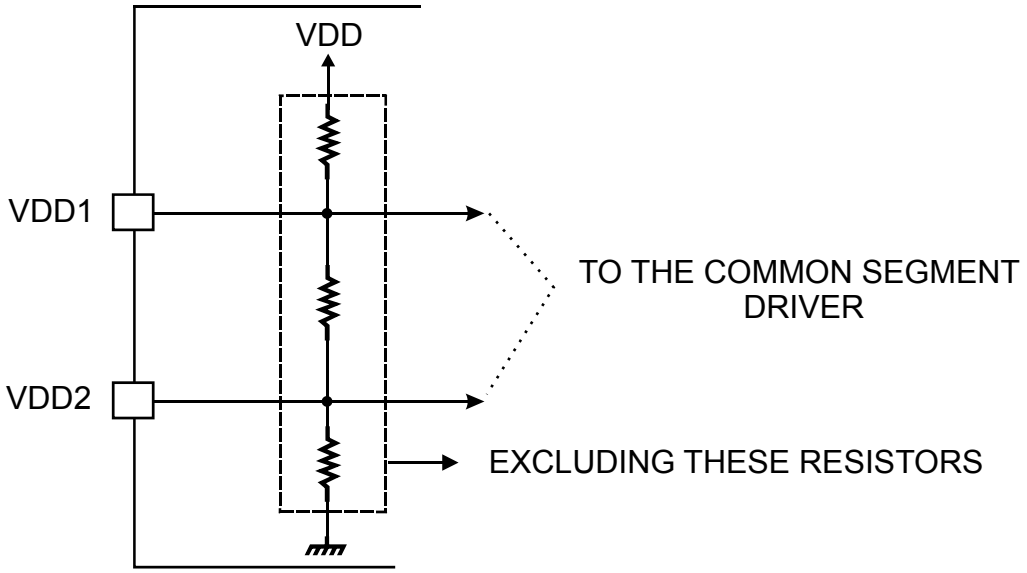
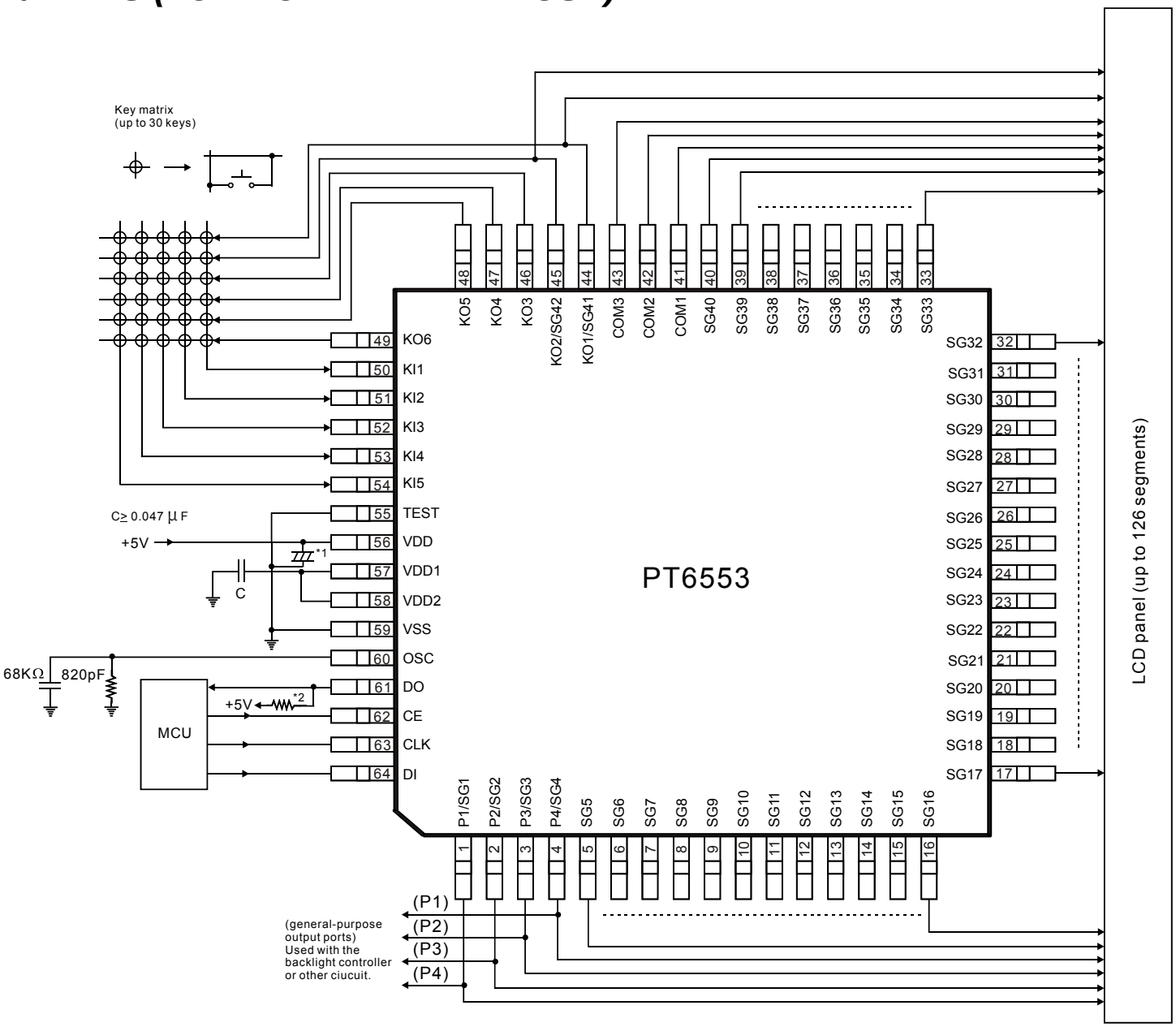
Note: * Excluding the Bias Voltage Generation Divider Resistor built into the V_{DD1} and V_{DD2}. Refer to the diagram below.



APPLICATION CIRCUIT 1

1/2 BIAS (FOR NORMAL PANEL USE)



Notes:

1. Connect a capacitor to the power supply line so that the when the PT6553 is reset by the V_{DET}, the power supply V_{DD} rise time when power is applied and the power supply voltage V_{DD} fall time when power drops are both at least 1ms.
2. Since the DO Pin is an open drain output, it needs a pull-up resistor (1K to 10KΩ) which is appropriate for the capacitance of the external wiring so that the waveforms are not degraded.

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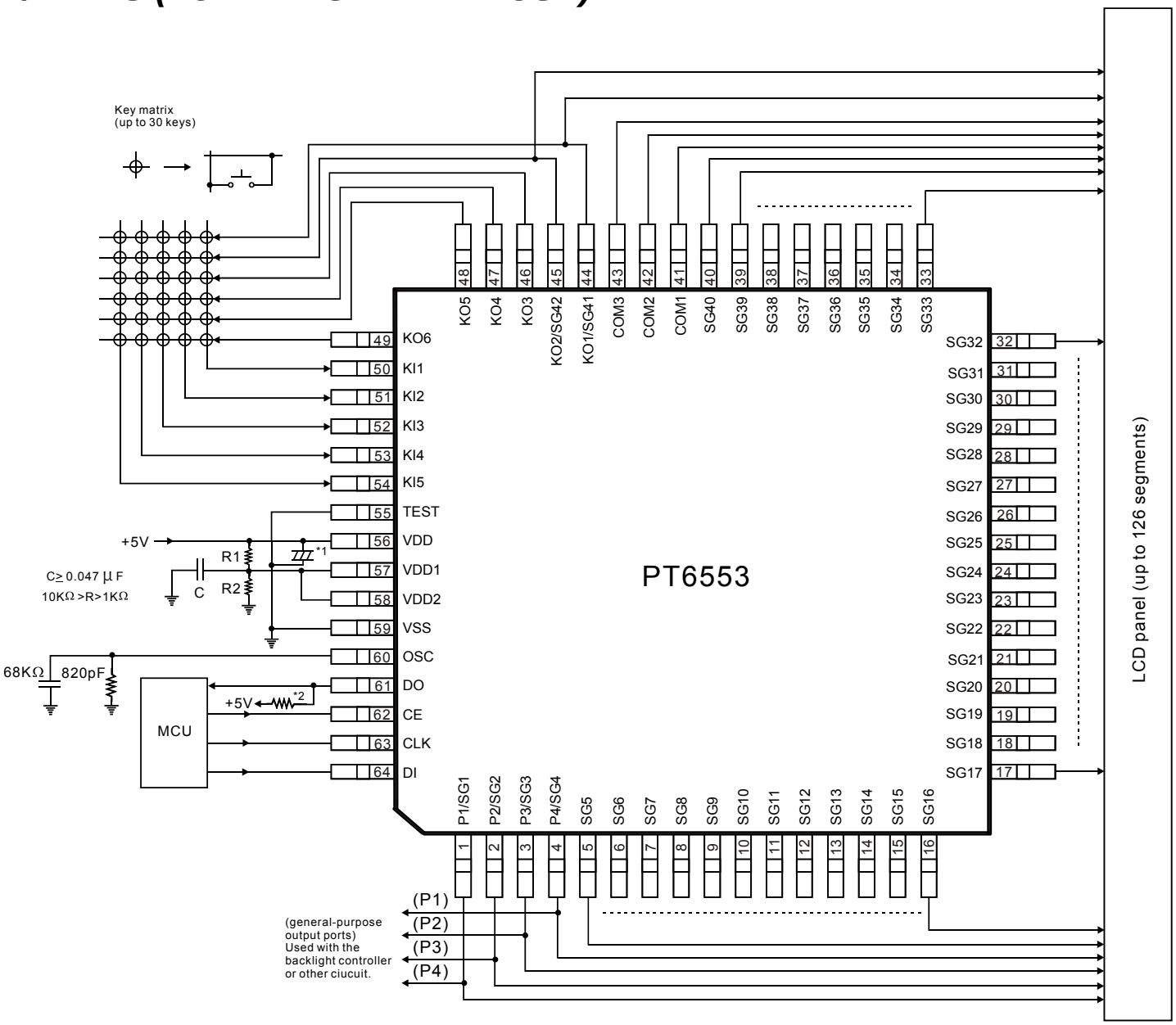
APPLICATION CIRCUIT 2

1/2 BIAS (FOR LARGE PANEL USE)



Notes:

1. Connect a capacitor to the power supply line so that the when the PT6553 is reset by the V_{DET}, the power supply V_{DD} rise time when power is applied and the power supply voltage V_{DD} fall time when power drops are both at least 1ms.
2. Since the DO Pin is an open drain output, it needs a pull-up resistor (1K to 10KΩ) which is appropriate for the capacitance of the external wiring so that the waveforms are not degraded.
3. R1=R2, the resistance value must be decide by the LCD panel size.

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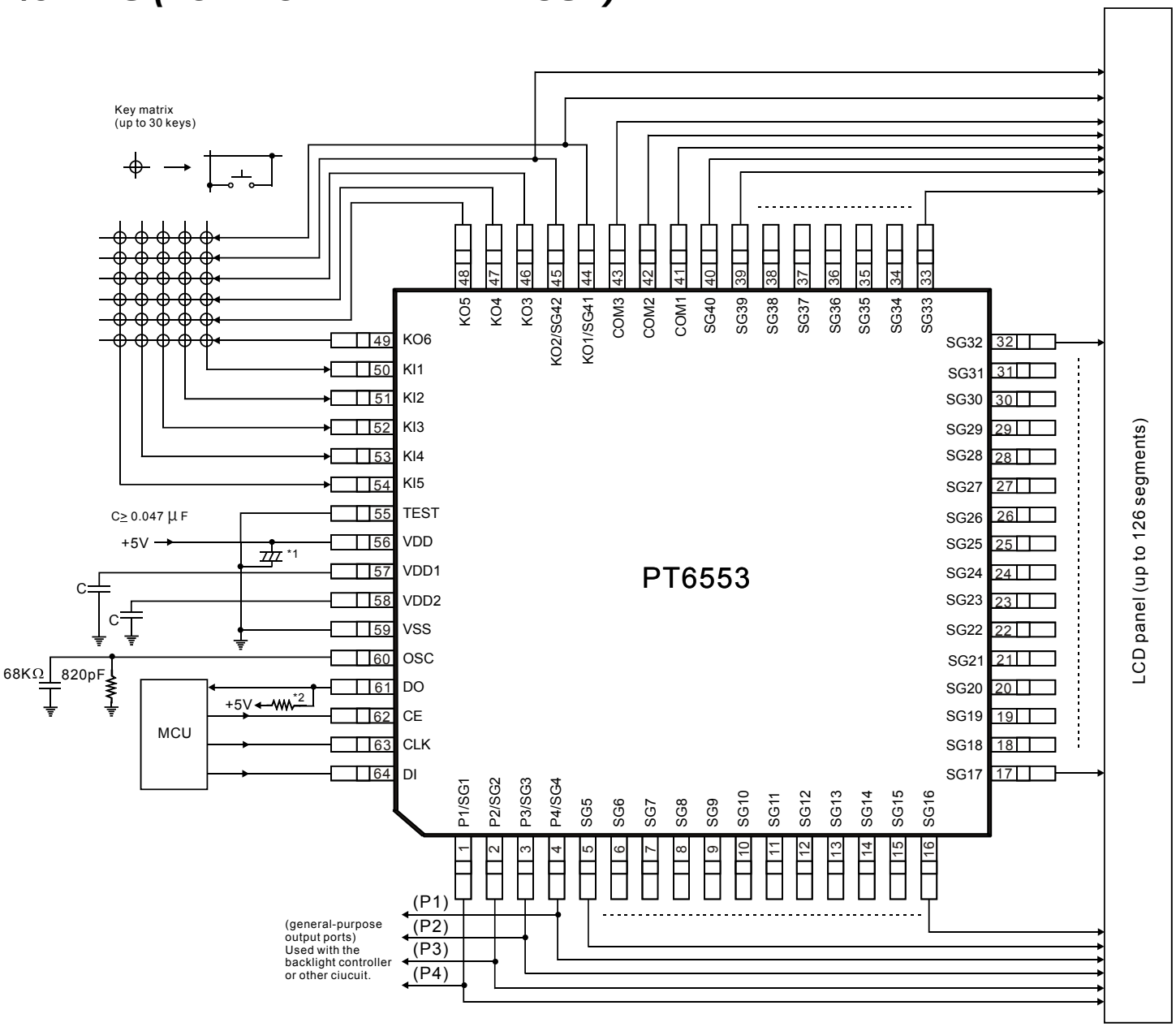
APPLICATION CIRCUIT 3

1/3 BIAS (FOR NORMAL PANEL USE)

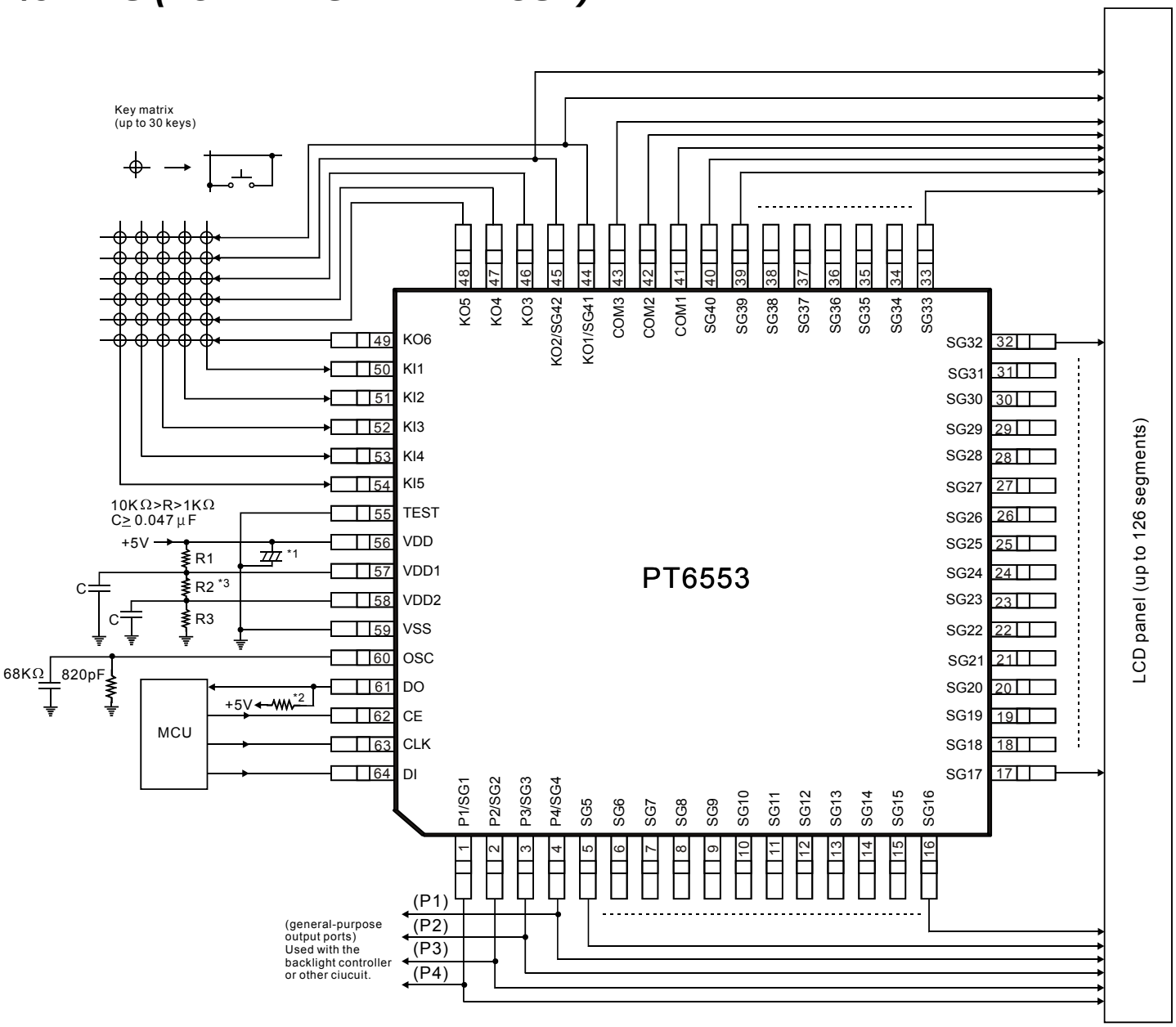


Notes:

1. Connect a capacitor to the power supply line so that the when the PT6553 is reset by the V_{DET}, the power supply V_{DD} rise time when power is applied and the power supply voltage V_{DD} fall time when power drops are both at least 1ms.
2. Since the DO Pin is an open drain output, it needs a pull-up resistor (1K to 10KΩ) which is appropriate for the capacitance of the external wiring so that the waveforms are not degraded.

APPLICATION CIRCUIT 4

1/3 BIAS (FOR LARGE PANEL USE)



Notes:

1. Connect a capacitor to the power supply line so that the when the PT6553 is reset by the V_{DET}, the power supply V_{DD} rise time when power is applied and the power supply voltage V_{DD} fall time when power drops are both at least 1ms.
2. Since the DO Pin is an open drain output, it needs a pull-up resistor (1K to 10KΩ) which is appropriate for the capacitance of the external wiring so that the waveforms are not degraded.
3. R1=R2=R3, the resistance value must be decide by the LCD panel size.

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ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6553-Q	64 Pins, QFP	PT6553-Q
PT6553-LQ	64 Pins, LQFP	PT6553-LQ

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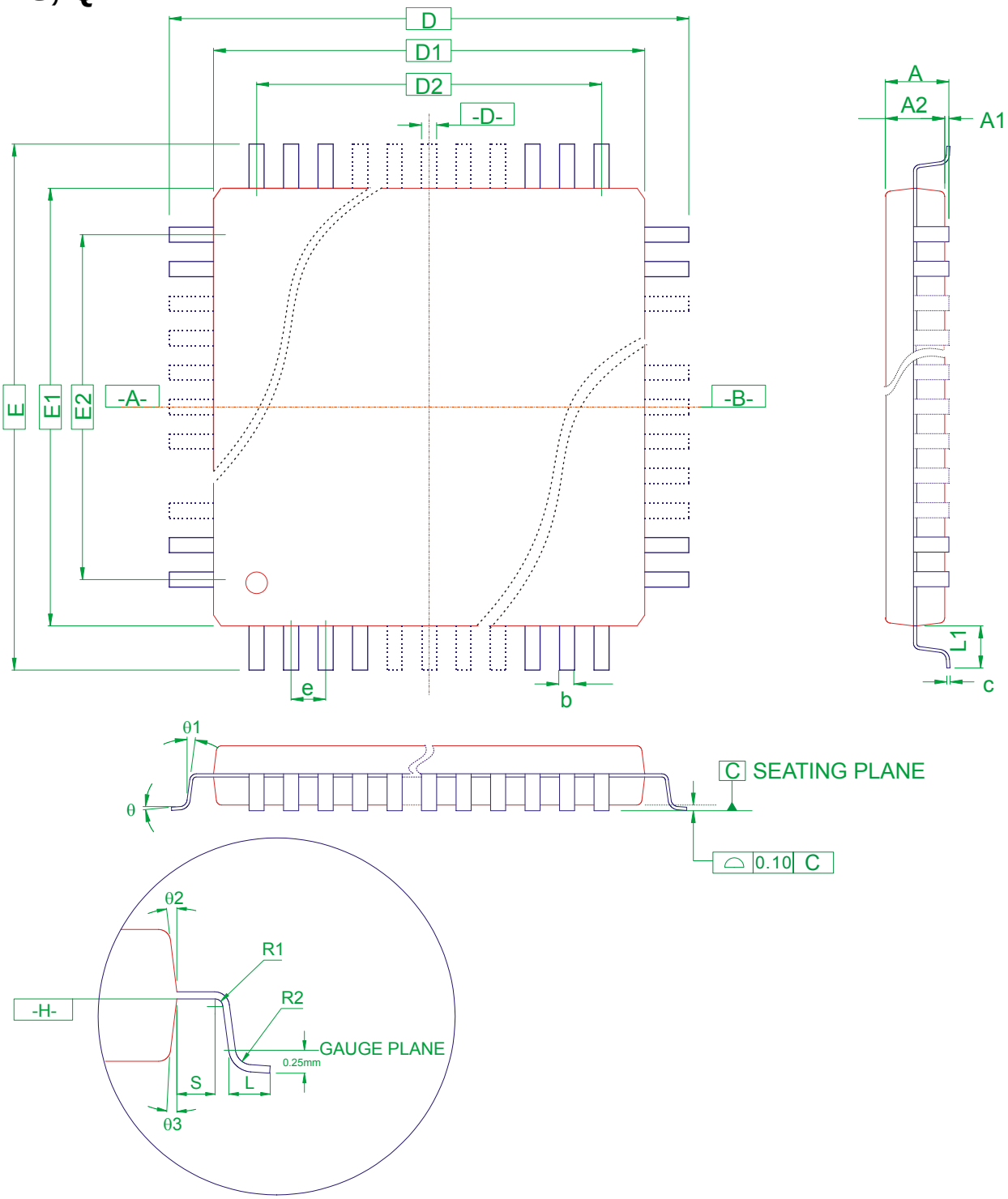
PACKAGE INFORMATION

64 PINS, QFP



Symbol	Min.	Nom.	Max.
c	0.11	-	0.23
L	0.73	0.88	1.03
L1	1.60 BASIC		
A	-	-	3.15
A1	0.00	-	0.25
A2	2.50	2.70	2.90
b	0.29	-	0.45
D	17.20 BSC.		
D1	14.00 BSC.		
D2	12.00 REF.		
E	17.20 BSC.		
E1	14.00 BSC.		
E2	12.00 REF.		
e	0.80 BSC.		
S	0.20	-	-
θ	0°	-	7°
θ1	0°	-	-
θ2	5°	-	16°
θ3	5°	-	16°
R1	0.13	-	-
R2	0.13	-	0.30

Notes:
1. All dimensioning and tolerancing conform to ASME Y14.5M - 1994.
2. Datum Plane H is located at the bottom of the mold parting line coincident with where the lead exits the body.
3. Datums A-B and D to be determined at datum plane H.
4. Dimensions D1 and E1 do not include mold prortrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 do include mold mismatch and are determined at the datum plane H.
5. Controlling Dimension: MILLIMETERS
6. Dimension b does not include dambar protrusion. The dambar protrusion (s) shall not cause the lead width to exceed b maximum by more than 0.08 mm. Dambar cannot be located on the lower radius or the lead foot.
7. A1 is defined as the distance from the seating plane to the lowest point of the package body.
8. Refer to JEDEC MS-022 Variation BE

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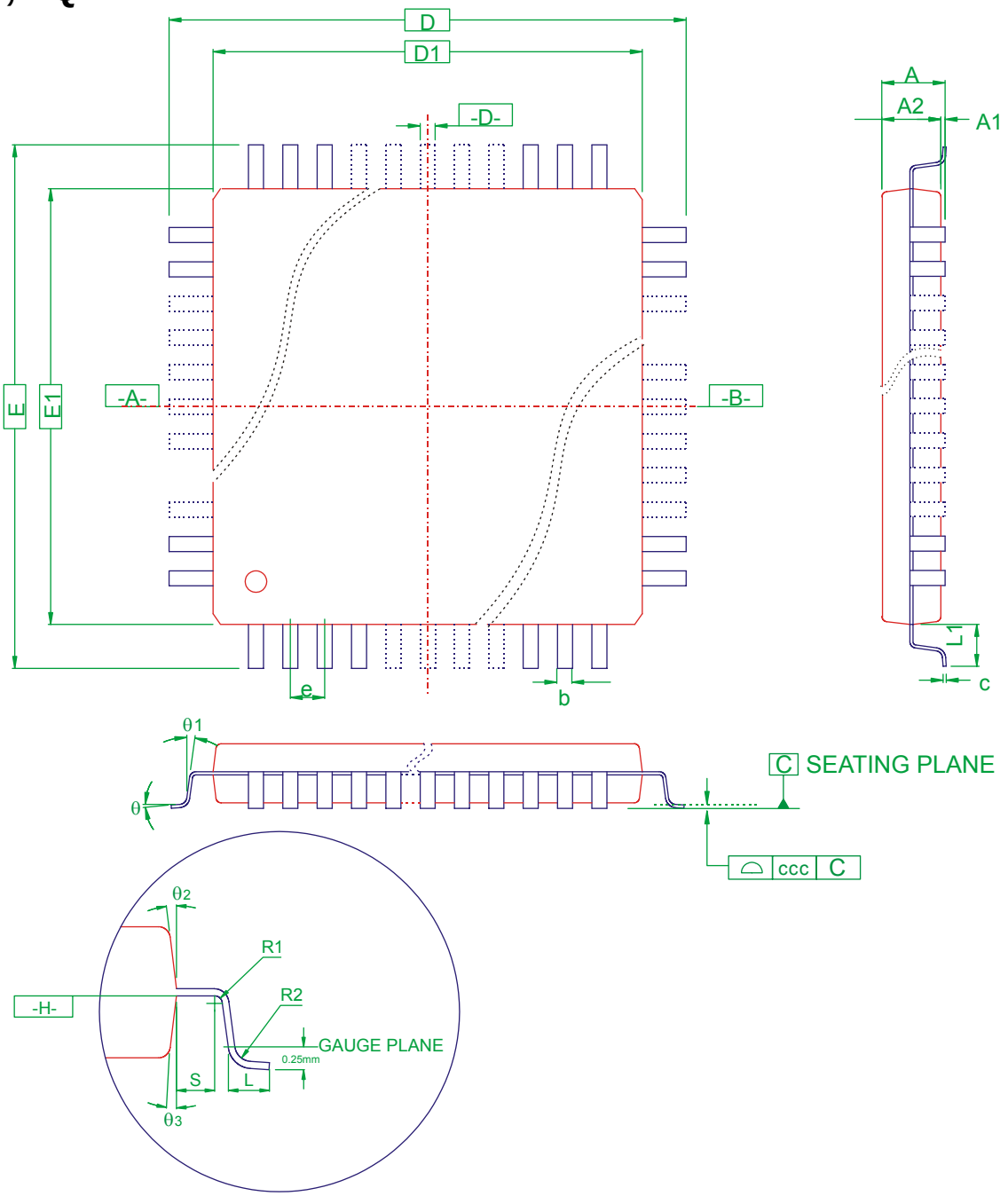
64 PINS, LQFP



Symbol	Min.	Typ.	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
D		12.00 BSC	
D1		10.00 BSC	
e		0.50 BSC	
E		12.00 BSC	
E1		10.00 BSC	
ccc		0.08	
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	-	0.20
L	0.45	0.60	0.75
L1		1.00 REF	
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994
2. The top package body size may be smaller than the bottom package size by as much as 0.15mm.
3. Datum A-B and D to be determined at the datum plane H.
4. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
5. Controlling Dimension: MILLIMETER
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located on the lower radius or the foot. Minimum space between the protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm PITCH package.
7. These dimensions apply to the flat section of the lead between 0.10mm and 0.25mm from the lead tip.
8. A1 is defined as the distance from the seating plane to the lowest point on the package body.
9. Details of pin 1 identifier are optional but must be located within the zone identified.
10. Dimension D2 and E2 show the minimum allowed for the optional exposed heat slug. The maximum allowed is equal to the package body size (D1 and E1). However, the size of the exposed heat slug is variable depending on the device function (die size). End users should verify the actual size or either top or bottom exposed thermal pad for specific device application.
11. Refer to JEDEC MS-026 Variation BCD.

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