



SINGLE CHANNEL HIGH SIDE DRIVER

Table 1. General Features

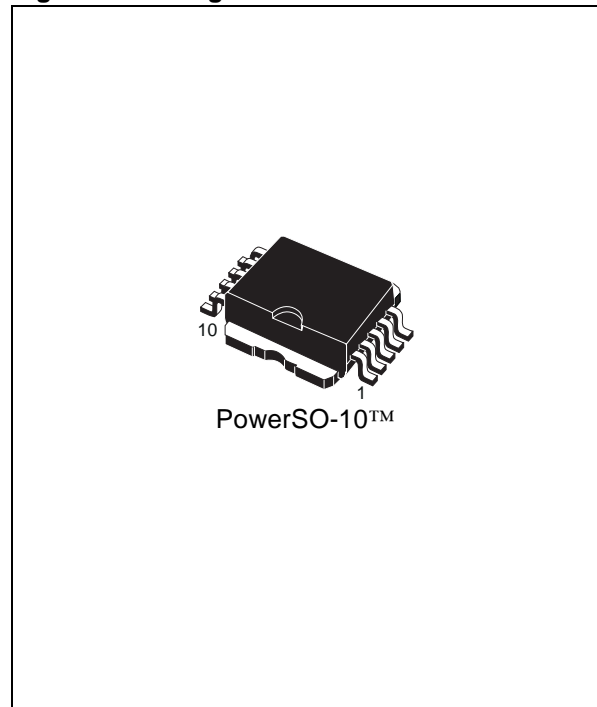
Type	R _{DS(on)}	I _{out}	V _{CC}
VN610SP-E	10 mΩ	45 A	36 V

- OUTPUT CURRENT: 45 A
- CMOS COMPATIBLE INPUT
- PROPORTIONAL LOAD CURRENT SENSE
- UNDERVOLTAGE AND OVERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT DOWN
- CURRENT LIMITATION
- VERY LOW STAND-BY POWER DISSIPATION
- PROTECTION AGAINST:
 - LOSS OF GROUND AND LOSS OF V_{CC}
- REVERSE BATTERY PROTECTION (*)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

DESCRIPTION

The VN610SP-E is a monolithic device made using STMicroelectronics VIPower M0-3 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

Figure 1. Package



This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio). Active current limitation combined with thermal shut-down and automatic restart protect the device against overload. Device automatically turns off in case of ground pin disconnection.

Table 2. Order Codes

Package	Tube	Tape and Reel
PowerSO-10™	VN610SP-E	VN610SPTR-E

Note: (*) See application schematic at page 9

Figure 2. Block Diagram

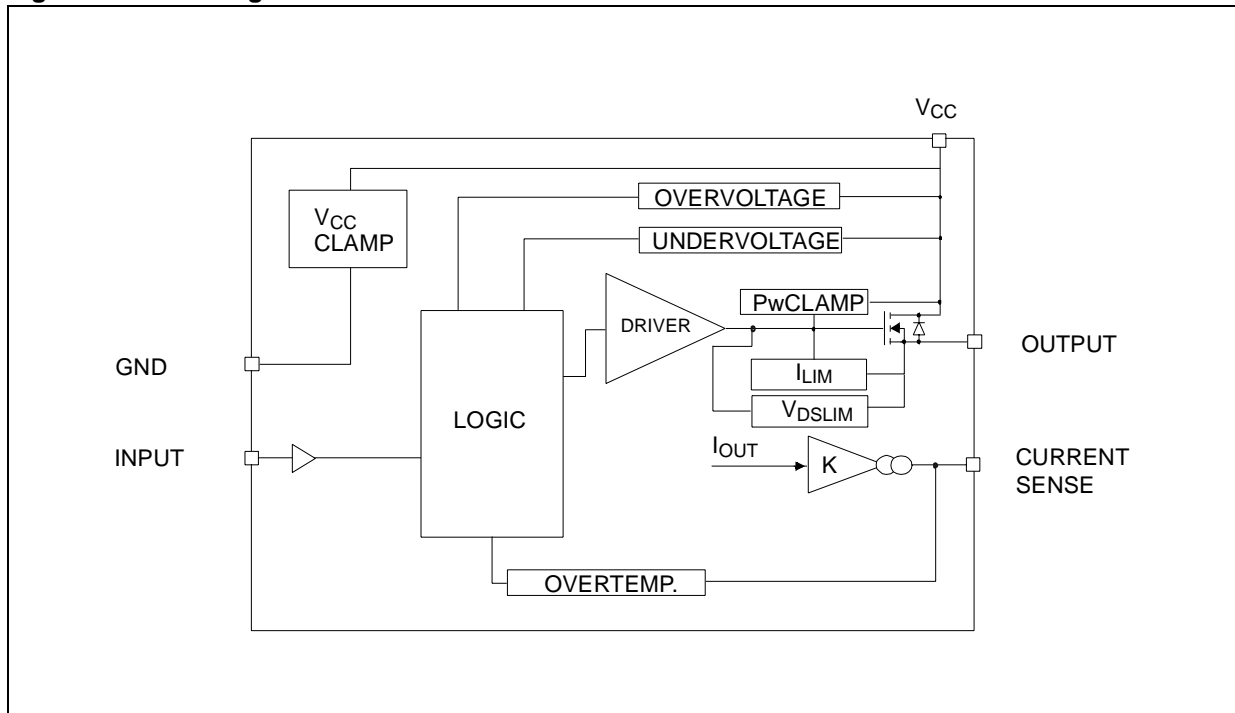


Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-50	A
I_{IN}	DC input current	+/- 10	mA
V_{CSense}	Current sense maximum voltage	-3 +15	V V
V_{ESD}	Electrostatic Discharge (Human Body Model: R=1.5K Ω ; C=100pF)		
	- INPUT	4000	V
	- CURRENT SENSE	2000	V
	- OUTPUT	5000	V
	- V_{CC}	5000	V
E_{MAX}	Maximum Switching Energy (L=0.05mH; R _L =0 Ω ; V _{bat} =13.5V; T _{jstart} =150 $^{\circ}$ C; I _L =75A)	193	mJ
P_{tot}	Power dissipation at T _C ≤25 $^{\circ}$ C	139	W
T_j	Junction operating temperature	Internally limited	$^{\circ}$ C
T_c	Case operating temperature	-40 to 150	$^{\circ}$ C
T_{STG}	Storage temperature	-55 to 150	$^{\circ}$ C

Figure 3. Configuration Diagram (Top View) & Suggested Connections for Unused and N.C. Pins

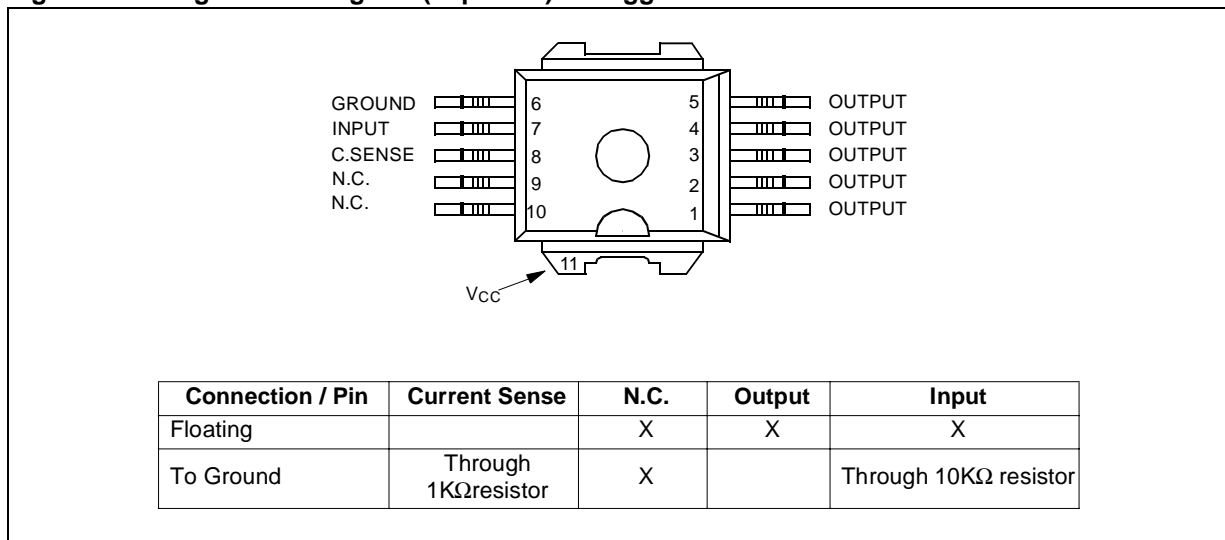


Figure 4. Current and Voltage Conventions

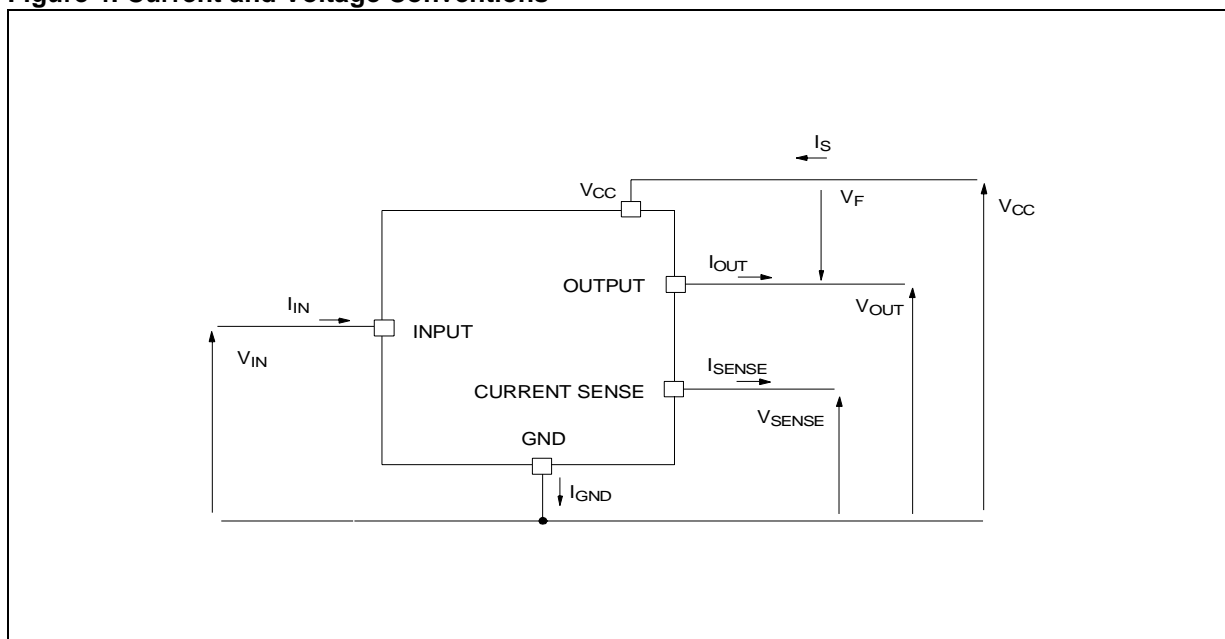


Table 4. Thermal Data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (MAX)	0.9	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (MAX)	50.9 ⁽¹⁾	°C/W
		36 ⁽²⁾	°C/W

Note: ⁽¹⁾ When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35μm thick).

Note: ⁽²⁾ When mounted on a standard single-sided FR-4 board with 6 cm² of Cu (at least 35μm thick).

ELECTRICAL CHARACTERISTICS

 (8V<V_{CC}<36V; -40°C<T_j<150°C; unless otherwise specified)

(Per each channel)

Table 5. Power

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{CC}	Operating supply voltage		5.5	13	36	V
V _{USD}	Undervoltage shutdown		3	4	5.5	V
V _{OV}	Overvoltage shutdown	(See Note 1)	36			V
R _{ON}	On state resistance	I _{OUT} =15A; T _j =25°C I _{OUT} =15A; T _j =150°C I _{OUT} =9A; V _{CC} =6V			10 20 35	mΩ mΩ mΩ
V _{clamp}	Clamp Voltage	I _{CC} =20 mA (see note 1)	41	48	55	V
I _S	Supply current	Off State; V _{CC} =13V; V _{IN} =V _{OUT} =0V Off State; V _{CC} =13V; V _{IN} =V _{OUT} =0V; T _j =25°C On State; V _{CC} =13V; V _{IN} =5V; I _{OUT} =0A R _{SENSE} =3.9K		10 10	25 20 5	μA μA mA
I _{L(off1)}	Off State Output Current	V _{IN} =V _{OUT} =0V	0		50	μA
I _{L(off2)}	Off State Output Current	V _{IN} =0V; V _{OUT} =3.5V	-75		0	μA
I _{L(off3)}	Off State Output Current	V _{IN} =V _{OUT} =0V; V _{CC} =13V; T _j =125°C			5	μA
I _{L(off4)}	Off State Output Current	V _{IN} =V _{OUT} =0V; V _{CC} =13V; T _j =25°C			3	μA

 Note: 1. V_{clamp} and V_{OV} are correlated. Typical difference is 5V.

Table 6. Protection (see note 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I _{lim}	DC Short circuit current	V _{CC} =13V 5.5V<V _{CC} <36V	45	75	120 120	A A
T _{TSD}	Thermal shutdown temperature		150	175	200	°C
T _R	Thermal reset temperature		135			°C
T _{HYST}	Thermal hysteresis		7	15		°C
V _{DEMAG}	Turn-off output voltage clamp	I _{OUT} =2A; V _{IN} =0; L=6mH	V _{CC} -41	V _{CC} -48	V _{CC} -55	V
V _{ON}	Output voltage drop limitation	I _{OUT} =1.5A; T _j = -40°C...+150°C		50		mV

Note: 2. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

Table 7. V_{CC} - Output Diode

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _F	Forward on Voltage	-I _{OUT} =8A; T _j =150°C			0.6	V

ELECTRICAL CHARACTERISTICS (continued)

Table 8. Current Sense ($9V \leq V_{CC} \leq 16V$) (See Figure 5)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} =1.5A; V _{SENSE} =0.5V; T _j = -40°C...150°C	3300	4400	6000	
dK ₁ /K ₁	Current Sense Ratio Drift	I _{OUT} =1.5A; V _{SENSE} =0.5V; T _j = -40°C...150°C	-10		+10	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} =15A; V _{SENSE} =4V; T _j =-40°C T _j =25°C...150°C	4200 4400	4900 4900	6000 5750	
dK ₂ /K ₂	Current Sense Ratio Drift	I _{OUT} =15A; V _{SENSE} =4V; T _j =-40°C T _j =25°C...150°C	-6		+6	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} =45A; V _{SENSE} =4V; T _j =-40°C T _j =25°C...150°C	4200 4400	4900 4900	5500 5250	
dK ₃ /K ₃	Current Sense Ratio Drift	I _{OUT} =45A; V _{SENSE} =4V; T _j =-40°C T _j =25°C...150°C	-6		+6	%
I _{SENSE0}	Analog sense current	V _{CC} =6...16V; I _{OUT} =0A; V _{SENSE} =0V; T _j =-40°C...150°C Off State; V _{IN} =0V On State; V _{IN} =5V	0 0		5 10	μA μA
V _{SENSE}	Max analog sense output voltage	V _{CC} =5.5V; I _{OUT} =7.5A; R _{SENSE} =10KΩ V _{CC} >8V; I _{OUT} =15A; R _{SENSE} =10KΩ	3.5 5			V V
V _{SENSEH}	Analog sense output voltage in overtemperature condition	V _{CC} =13V; R _{SENSE} =3.9KΩ		5.5		V
R _{VSENSEH}	Analog sense output impedance in overtemperature condition	V _{CC} =13V; T _j >T _{TSD} ; Output Open		400		Ω
t _{DSENSE}	Current sense delay reponse	to 90% I _{SENSE} (see note 3)			500	μs

Note: 3. Current sense signal delay after positive input slope.

Table 9. Switching (V_{CC}=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t _{d(on)}	Turn-on delay time	R _L =0.87Ω		50		μs
t _{d(off)}	Turn-off delay time	R _L =0.87Ω		50		μs
(dV _{OUT} /dt) _{on}	Turn-on voltage slope	R _L =0.87Ω		See relative diagram		V/μs
(dV _{OUT} /dt) _{off}	Turn-off voltage slope	R _L =0.87Ω		See relative diagram		V/μs

Table 10. Logic Input

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage				1.25	V
I_{IL}	Low level input current	$V_{IN}=1.25V$	1			μA
V_{IH}	Input high level voltage		3.25			V
I_{IH}	High level input current	$V_{IN}=3.25V$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	$I_{IN}=1mA$	6	6.8	8	V
		$I_{IN}=-1mA$		-0.7		V

Figure 5.

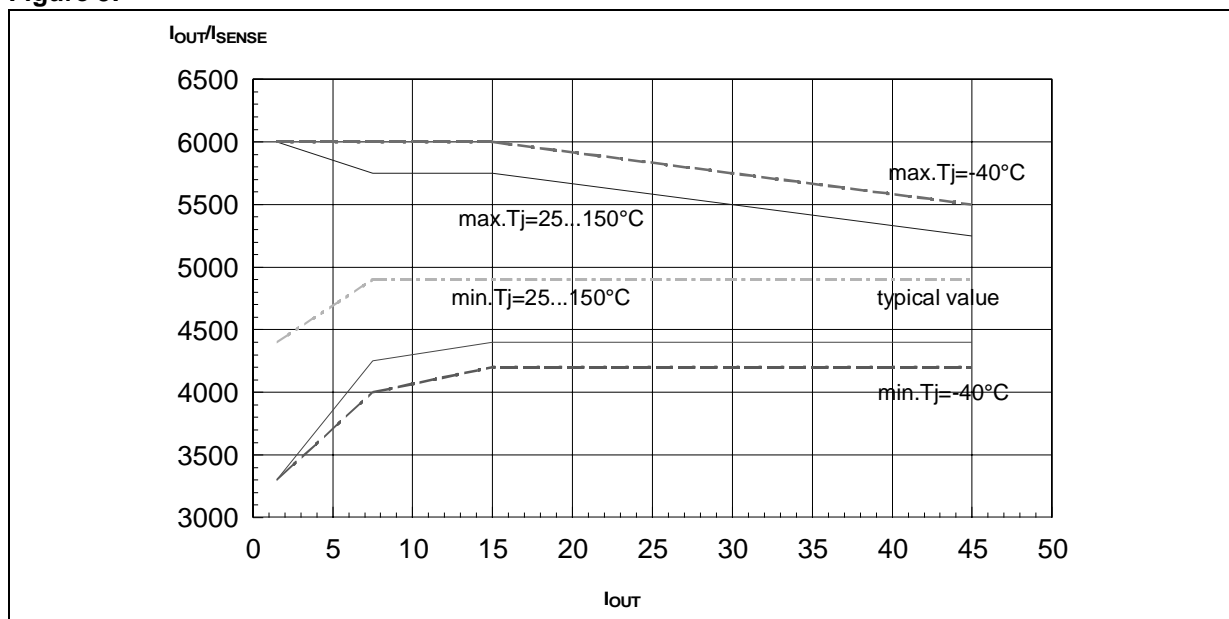
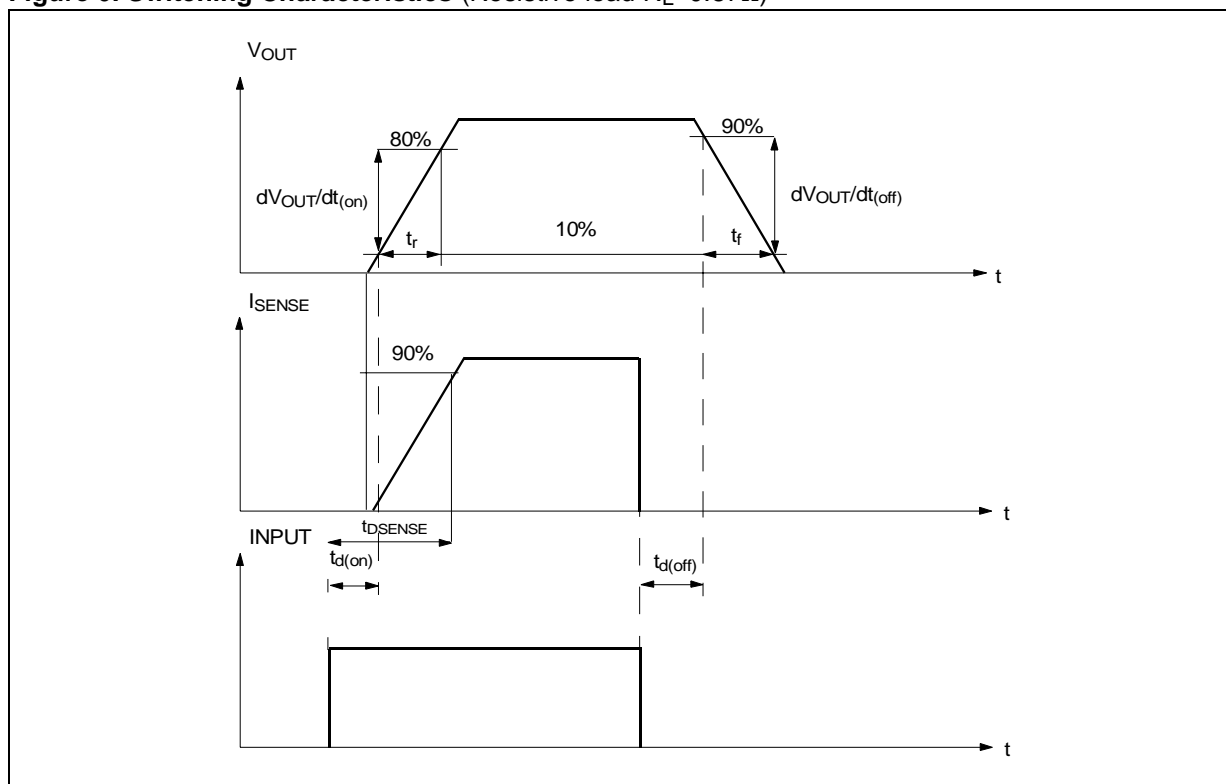


Table 11. Truth Table

CONDITIONS	INPUT	OUTPUT	SENSE
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Overvoltage	L	L	0
	H	L	0
Short circuit to GND	L	L	0
	H	L	$(T_j < T_{TSD}) 0$ $(T_j > T_{TSD}) V_{SENSEH}$
Short circuit to V_{CC}	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

Figure 6. Switching Characteristics (Resistive load $R_L=0.87\Omega$)Table 12. Electrical Transient Requirements On V_{CC} Pin

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μ s 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μ s 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 7. Waveforms

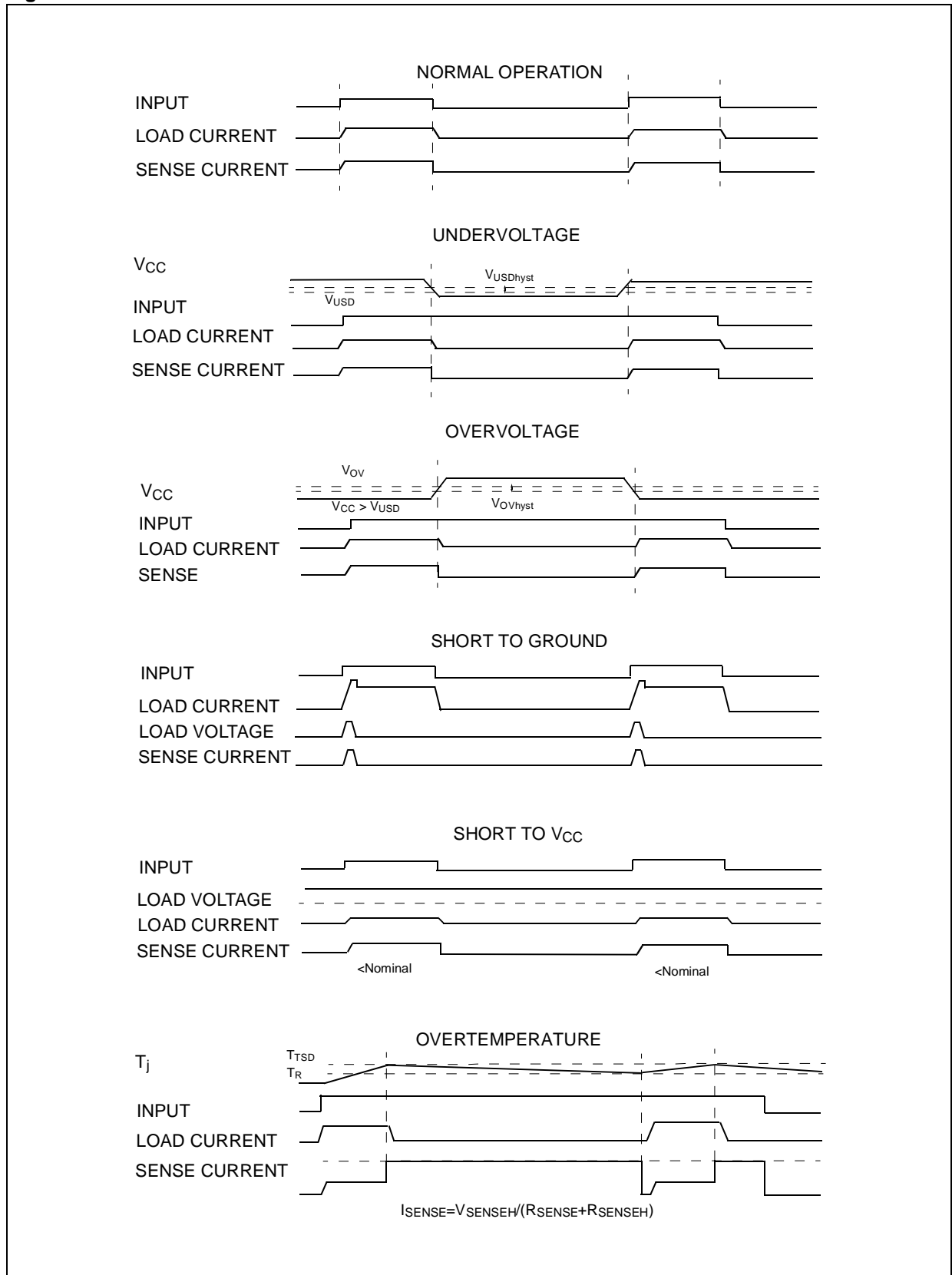
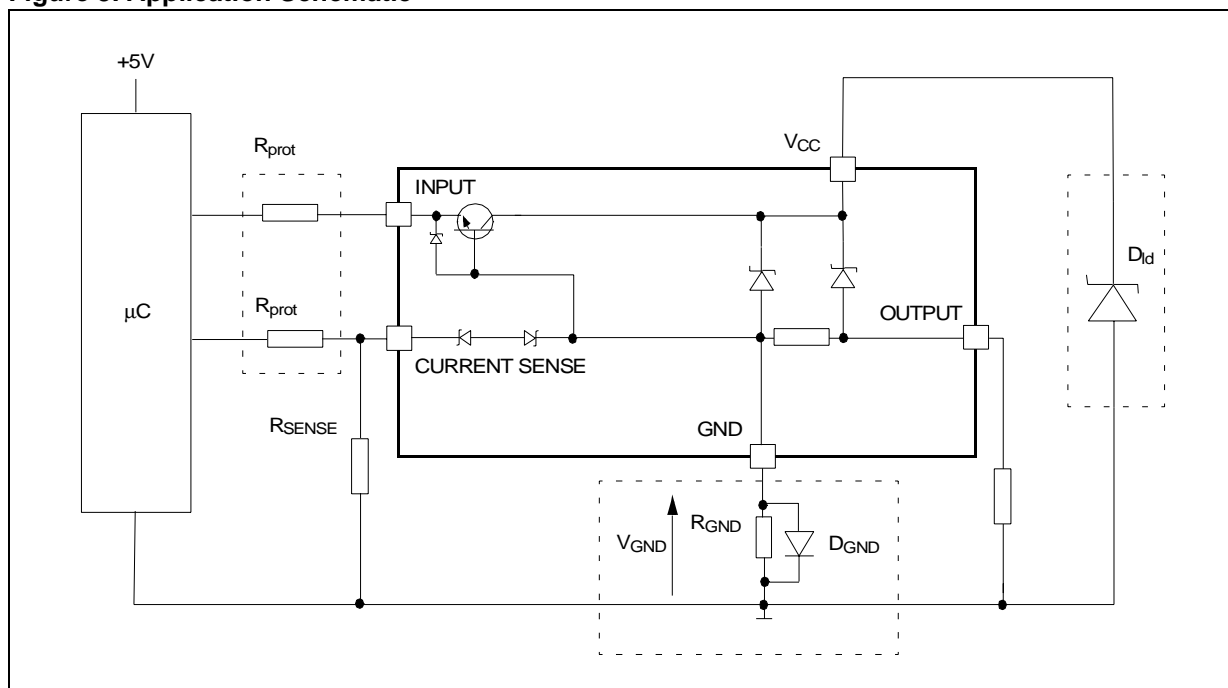


Figure 8. Application Schematic



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1) $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$.
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor ($R_{GND} = 1\text{k}\Omega$) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ($\approx 600\text{mV}$) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT line is also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT pin is to leave it unconnected, while unused SENSE pin has to be connected to Ground pin.

LOAD DUMP PROTECTION

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

μC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -100\text{V}$ and $I_{latchup} \geq 20\text{mA}$; $V_{OH\mu C} \geq 4.5\text{V}$
 $5\text{k}\Omega \leq R_{prot} \leq 65\text{k}\Omega$.

Recommended R_{prot} value is $10\text{k}\Omega$.

Figure 9. Off State Output Current

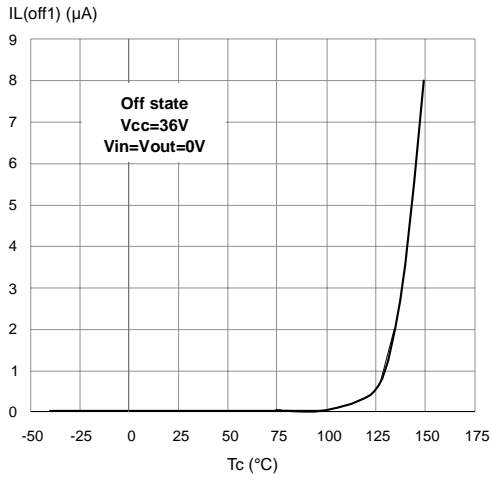


Figure 10. High Level Input Current

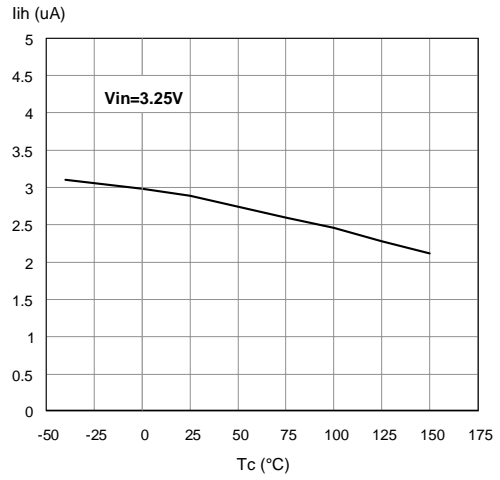


Figure 11. Input Low Level

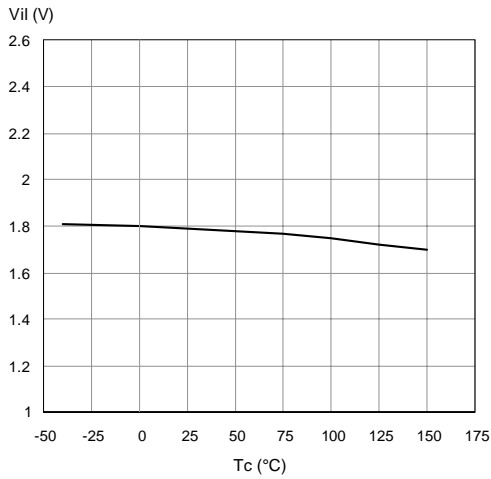


Figure 13. Input High Level

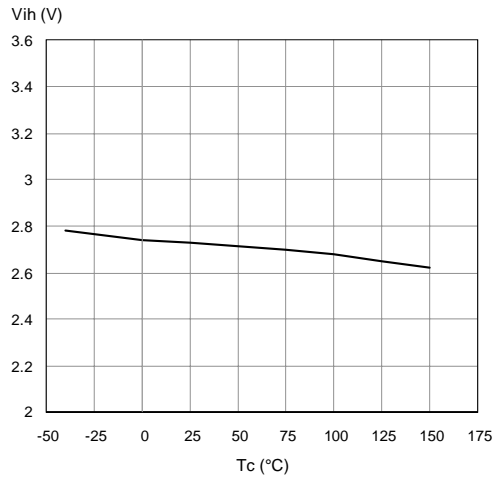


Figure 12. Input Clamp Voltage

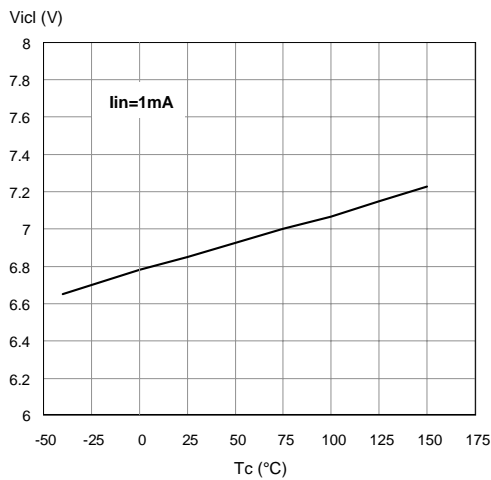


Figure 14. Input Hysteresis Voltage

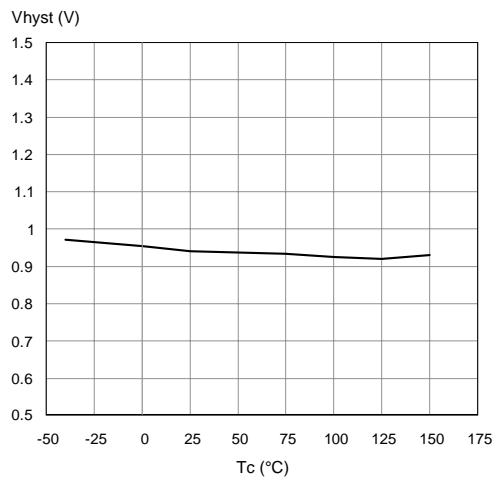


Figure 15. Overvoltage Shutdown

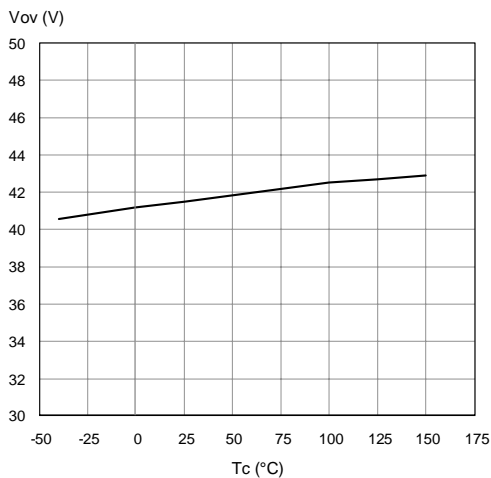


Figure 18. I_{LIM} Vs T_{case}

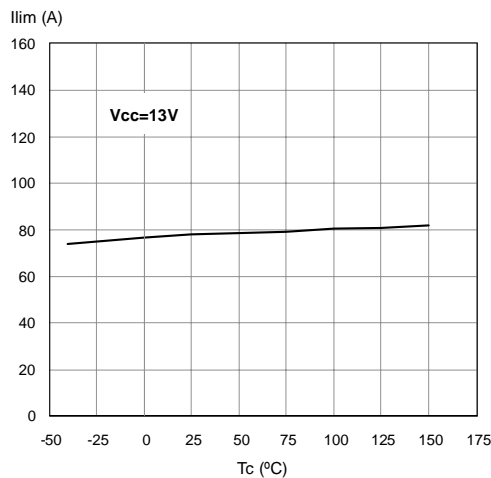


Figure 16. Turn-on Voltage Slope

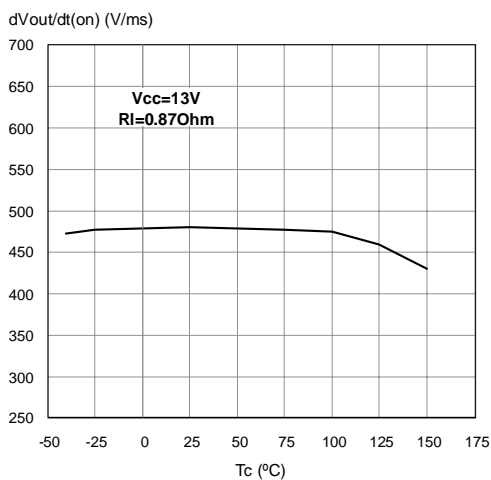


Figure 19. Turn-off Voltage Slope

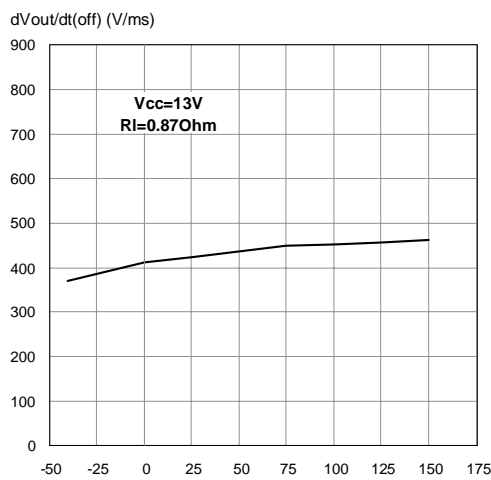


Figure 17. On State Resistance Vs T_{case}

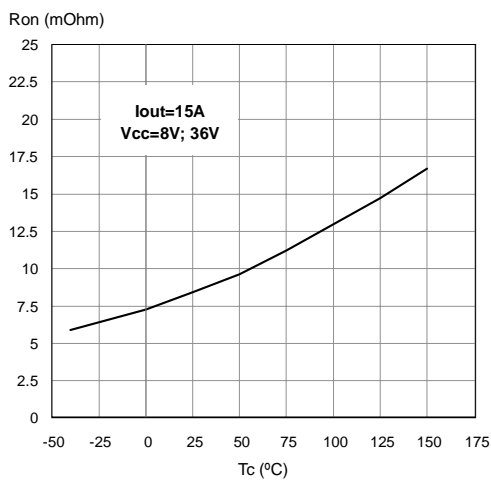


Figure 20. On State Resistance Vs V_{CC}

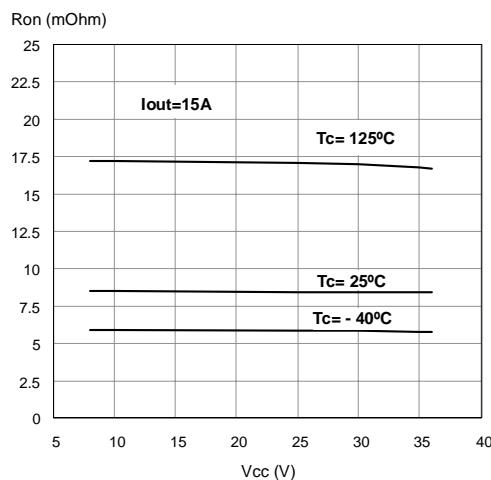
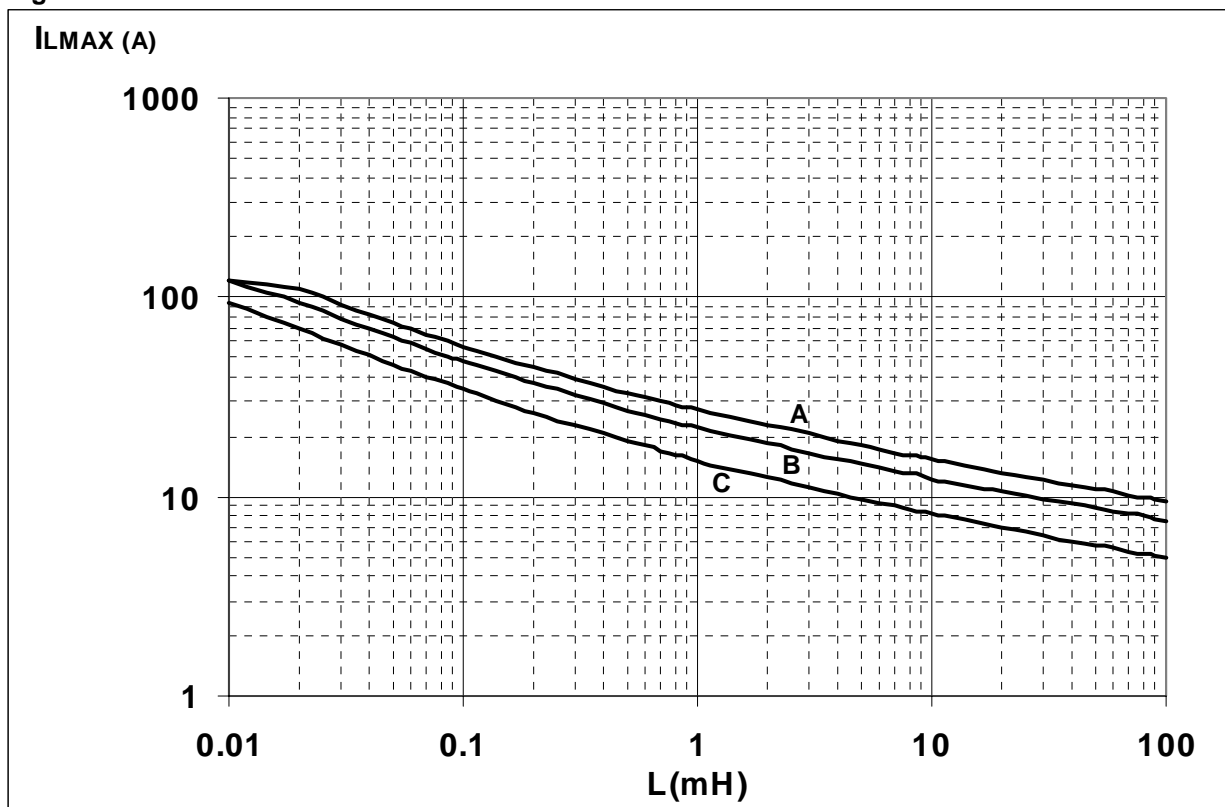


Figure 21. Maximum turn off current versus load inductance



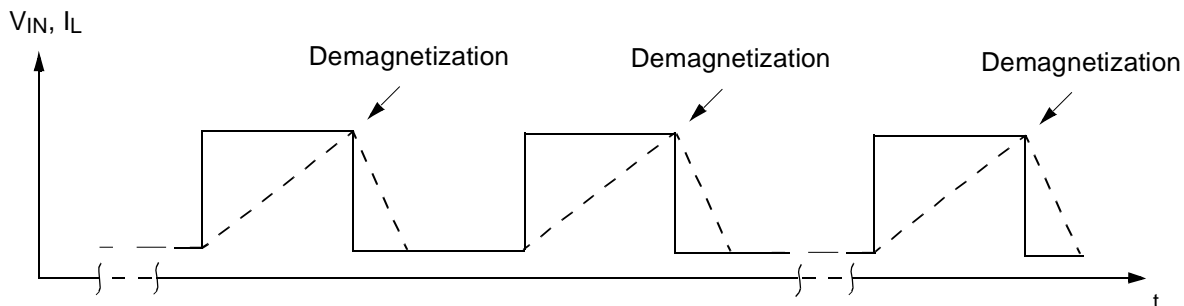
- A = Single Pulse at $T_{Jstart}=150^{\circ}C$
- B= Repetitive pulse at $T_{Jstart}=100^{\circ}C$
- C= Repetitive Pulse at $T_{Jstart}=125^{\circ}C$

Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

Conditions:

$V_{CC}=13.5V$



PowerSO-10™ Thermal Data

Figure 22. PowerSO-10™ PC Board

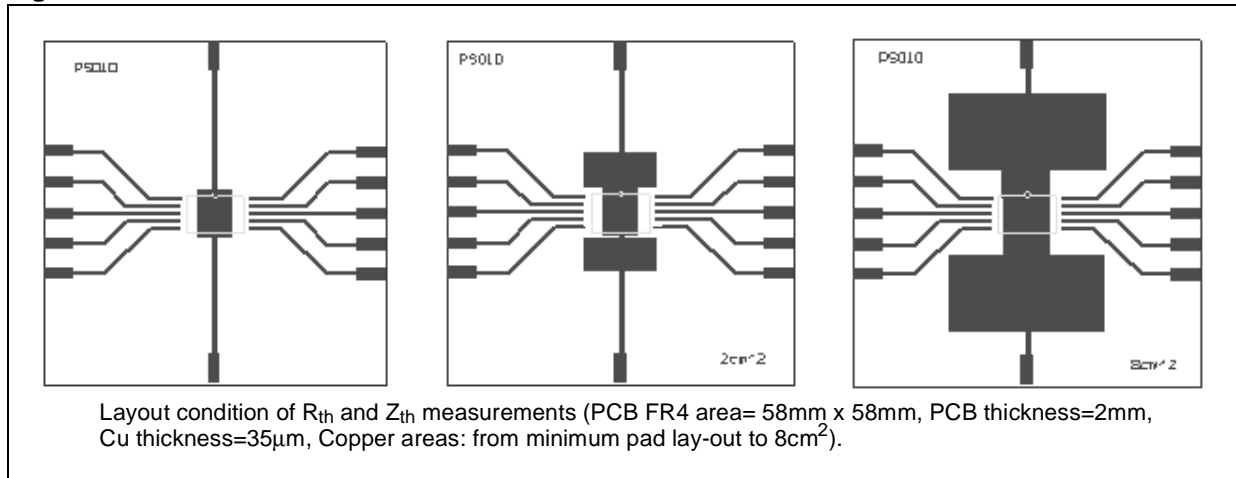


Figure 23. $R_{thj-amb}$ Vs PCB copper area in open box free air condition

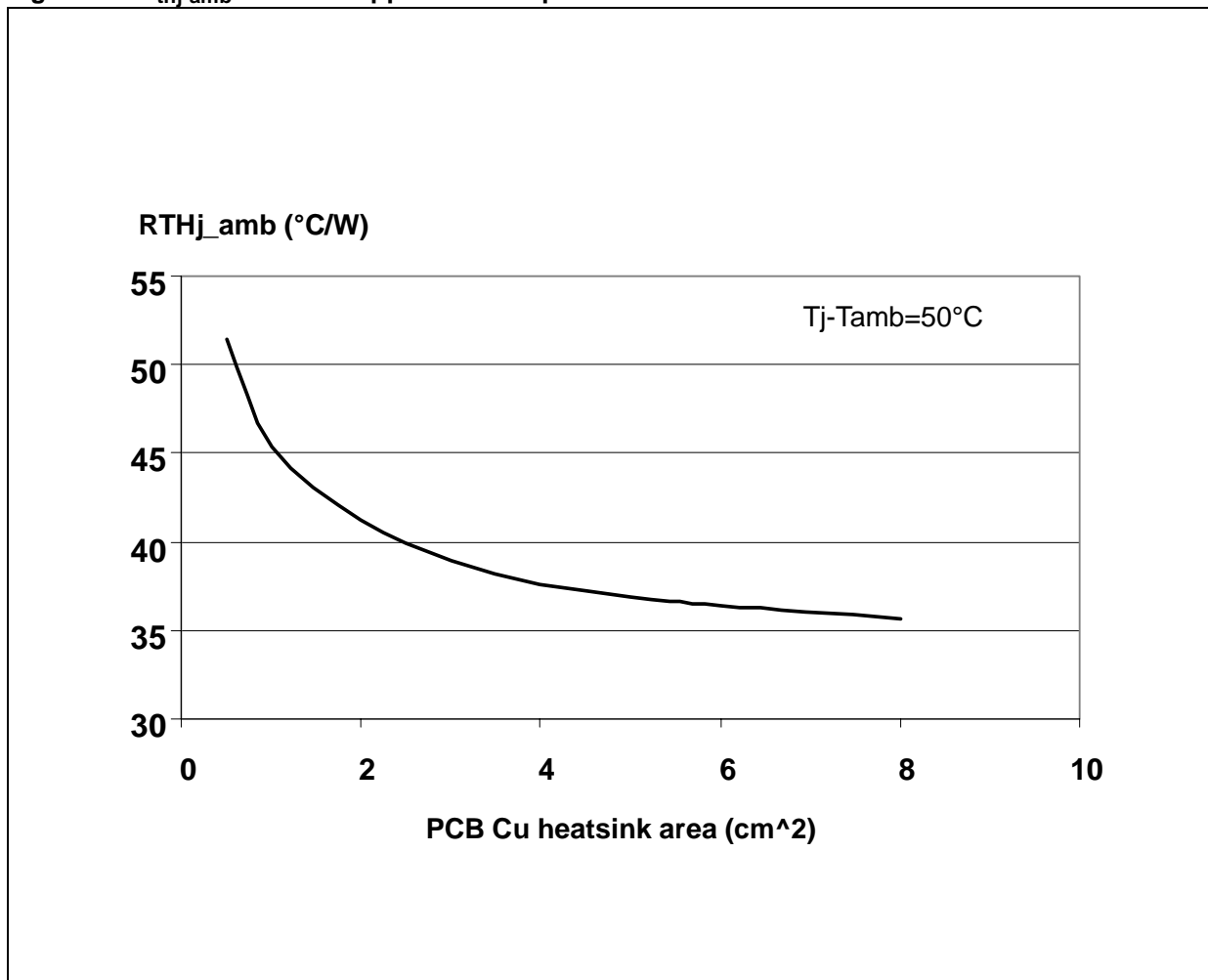


Figure 24. PowerSO-10 Thermal Impedance Junction Ambient Single Pulse

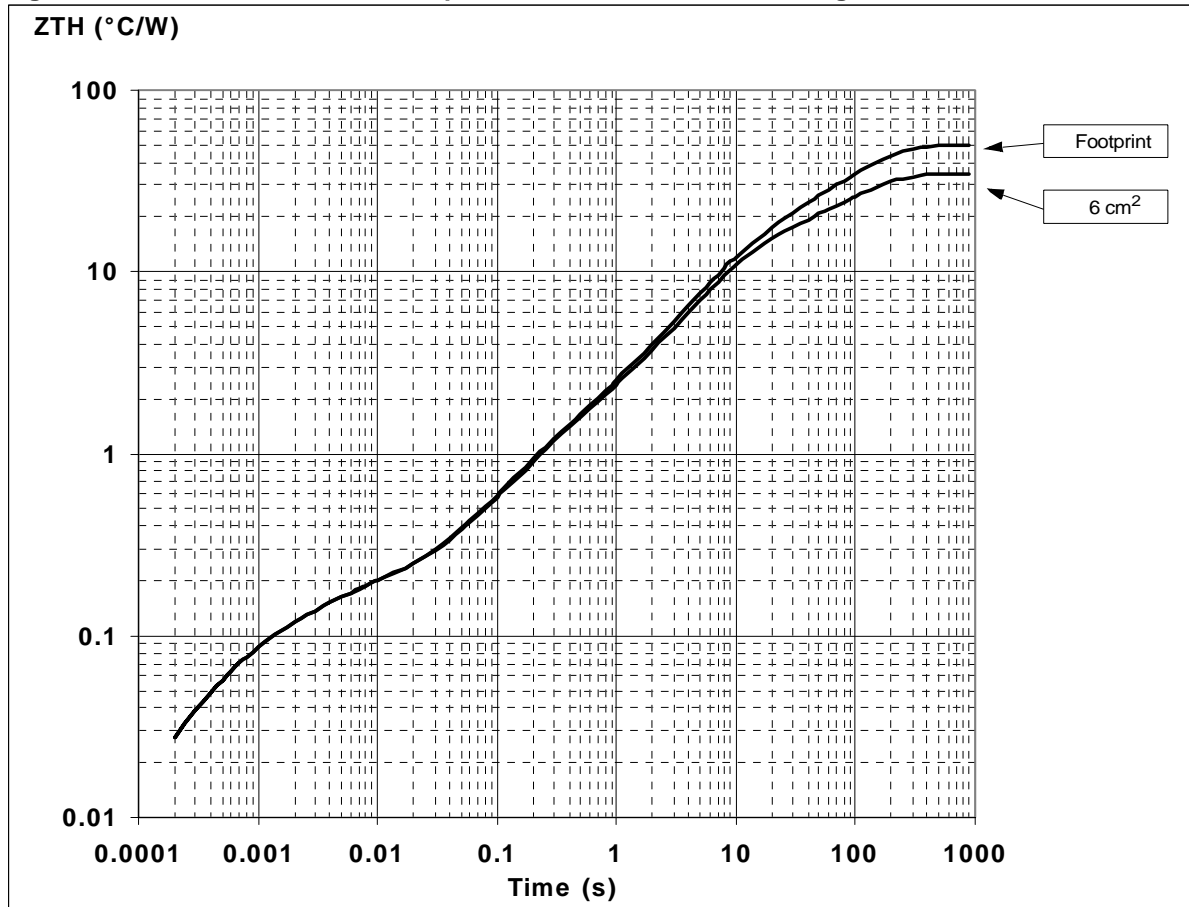
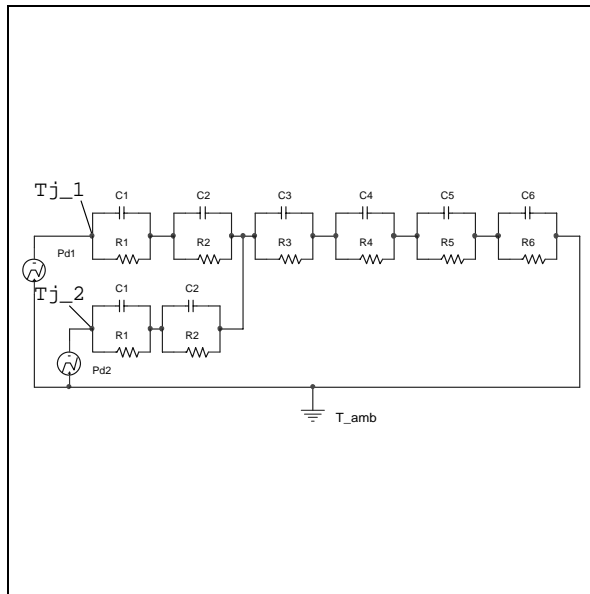


Figure 25. Thermal fitting model of a double channel HSD in PowerSO-10



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Table 13. Thermal Parameter

	Area/island (cm ²)	Footprint	6
R1 (°C/W)		0.05	
R2 (°C/W)		0.3	
R3 (°C/W)		0.3	
R4 (°C/W)		0.8	
R5 (°C/W)		12	
R6 (°C/W)		37	22
C1 (W.s/°C)		0.001	
C2 (W.s/°C)		5.00E-03	
C3 (W.s/°C)		0.02	
C4 (W.s/°C)		0.3	
C5 (W.s/°C)		0.75	
C6 (W.s/°C)		3	5

PACKAGE MECHANICAL

Table 14. PowerSO-10™ Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	3.35		3.65
A (*)	3.4		3.6
A1	0.00		0.10
B	0.40		0.60
B (*)	0.37		0.53
C	0.35		0.55
C (*)	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2 (*)	7.30		7.50
E4	5.90		6.10
E4 (*)	5.90		6.30
e		1.27	
F	1.25		1.35
F (*)	1.20		1.40
H	13.80		14.40
H (*)	13.85		14.35
h		0.50	
L	1.20		1.80
L (*)	0.80		1.10
a	0°		8°
α (*)	2°		8°

Note: (*) Muar only POA P013P

Figure 26. PowerSO-10™ Package Dimensions

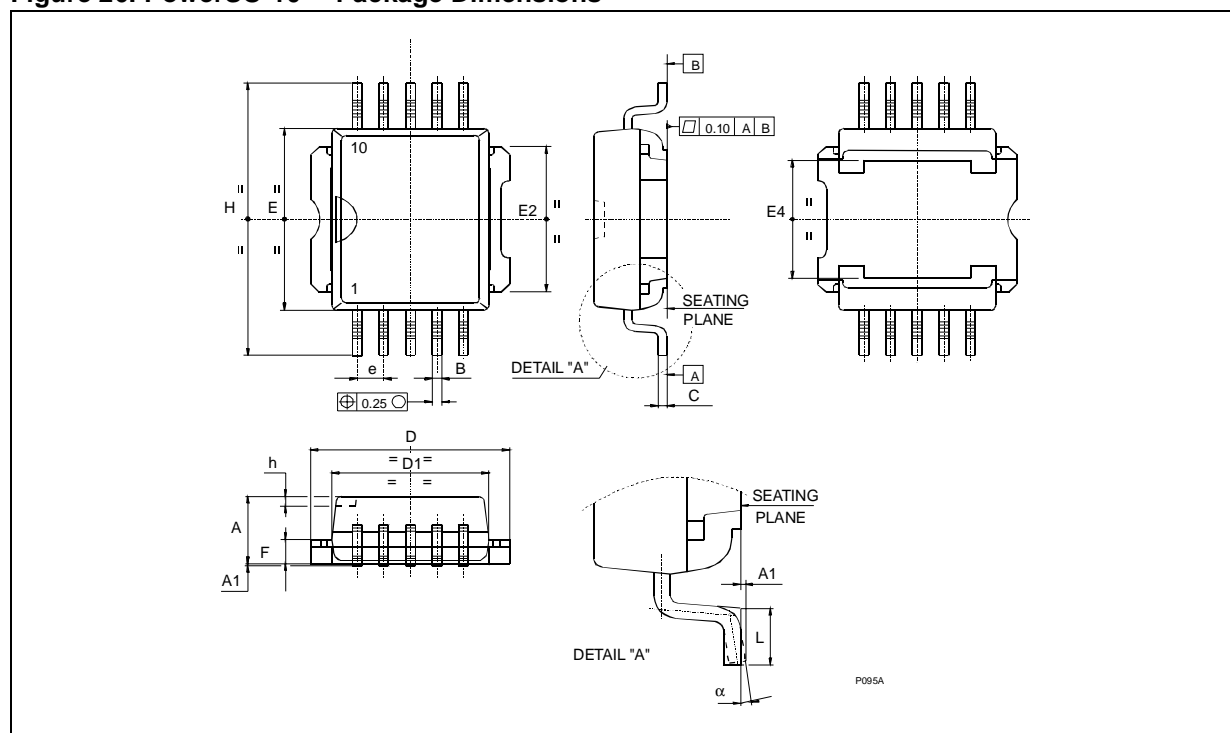


Figure 27. PowerSO-10™ Suggested Pad Layout and Tube Shipment (no suffix)

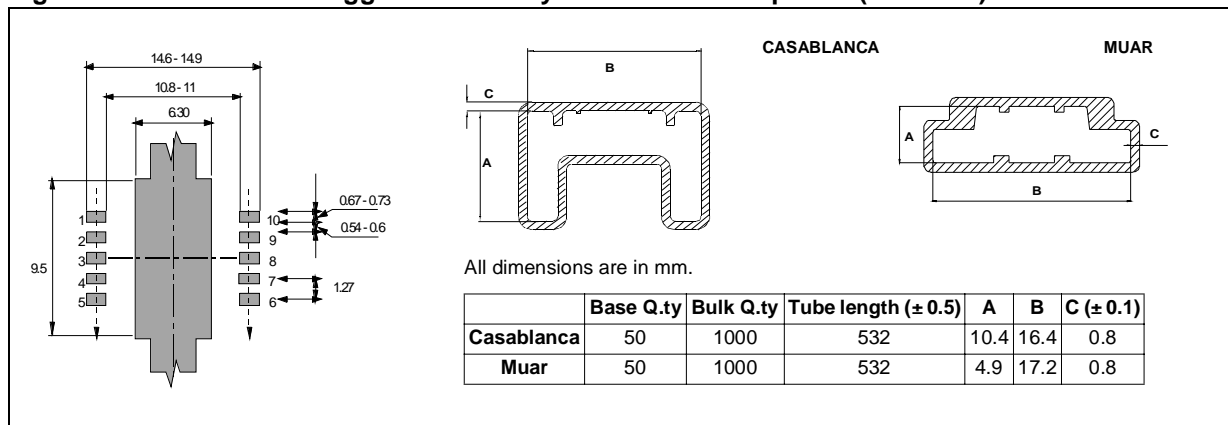
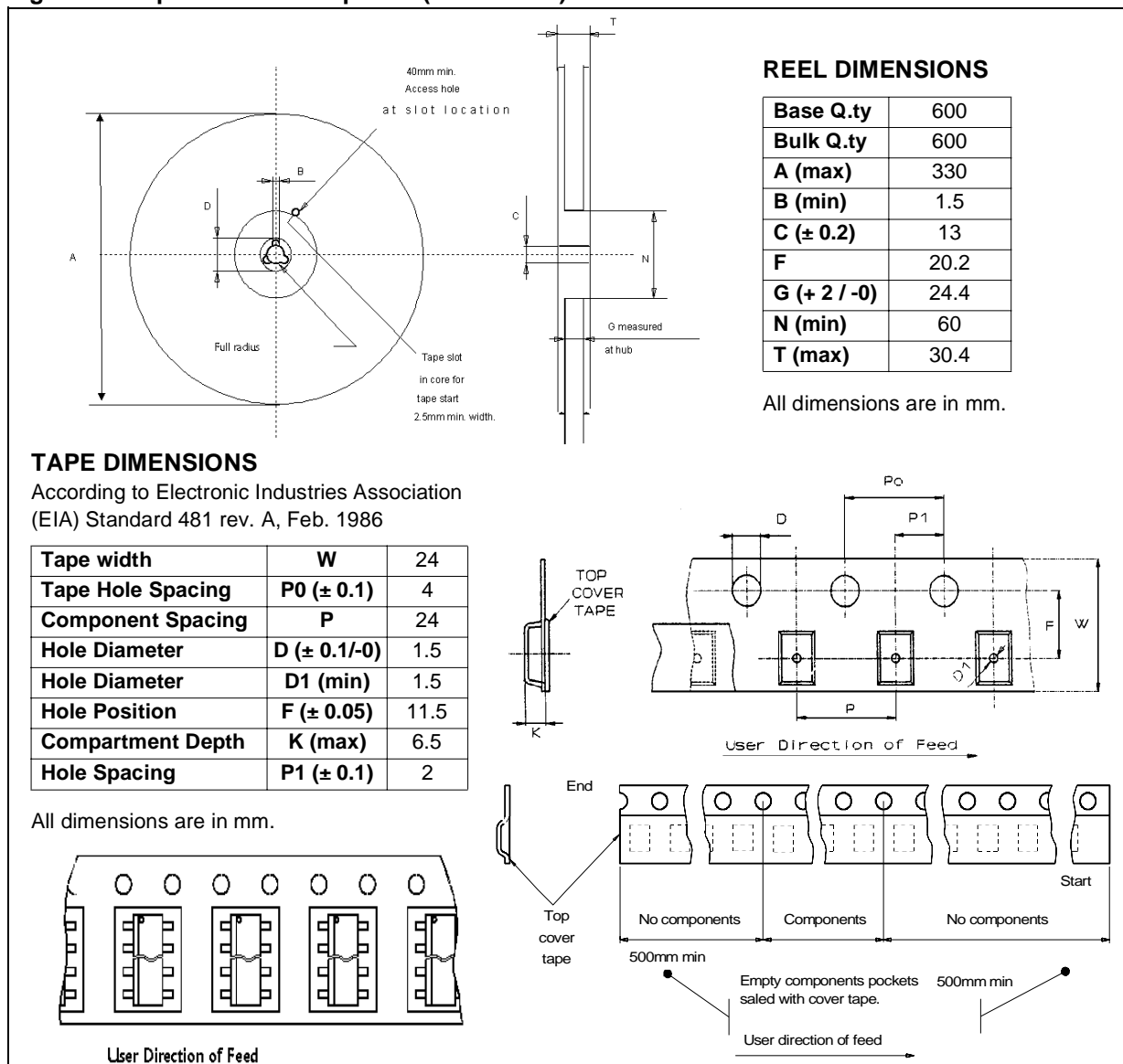


Figure 28. Tape And Reel Shipment (suffix “TR”)



REVISION HISTORY

Date	Revision	Description of Changes
Oct. 2004	1	- First Issue.

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics.
All other names are the property of their respective owners

© 2004 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -
Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com