TABLE OF CONTENTS

LCD SEGMENT / COMMON DRIVER WITH CONTROLLER 1

FEATURES 1

ORDERING INFORMATION 2

BLOCK DIAGRAM 3

DIE PAD ARRANGEMENT 4

PIN DESCRIPTION 7

FUNCTIONAL BLOCK DESCRIPTIONS 11

COMMAND TABLE 17

COMMAND TABLE 18

COMMAND DESCRIPTIONS 24

MAXIMUM RATINGS 30

DC CHARACTERISTICS 31

AC CHARACTERISTICS 33

APPLICATION EXAMPLES 36

INITIALIZATION ROUTINE 39

SSD0817

Advance Information

CMOS

LCD Segment / Common Driver with Controller

SSD0817 is a single-chip CMOS LCD driver with controllers for dot-matrix graphic liquid crystal display system. It consists of 169 high-voltage driving outputs for driving maximum 104 Segments, 64 Commons and 1 icon line.

SSD0817 consists of 104 x 65 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from common MCU through I^2C-bus Interface.
SSD0817 embeds DC-DC Converter with booster capacitors, On-Chip Oscillator and Bias Divider so as to reduce the number of external components. With the advanced design for low power consumption, stable LCD operating voltage and flexible die layout, SSD0817 is suitable for any portable battery-driven applications requiring long operation period with compact size.

FEATURES

104 x 64 + 1 Icon Line
Single Supply Operation, 2.4 V - 3.5V
Minimum -12.0V LCD Driving Output Voltage
Low Current Sleep Mode
On-Chip Voltage Generator or External LCD Driving Power Supply Selectable
2X / 3X / 4X/ 5X On-Chip DC-DC Converter
On-Chip Oscillator
On-Chip Bias Divider
Programmable bias ratio [1/4 – 1/9]
I^2C-bus Interface
On-Chip 104 X 65 Graphic Display Data RAM
Row Re-mapping and Column Re-mapping
Vertical Scrolling
Display Offset Control
64 Levels Internal Contrast Control & External Contrast Control
Programmable MUX ratio [2-64 MUX] (Partial display mode)
Programmable LCD Driving Voltage Temperature Coefficients
Available in Gold Bump Die

ORDERING INFORMATION

Table 1 - Ordering Information

Ordering Part Number	SEG	COM	Default Bias	Package Form	Reference
SSD0817Z	104	64 + 1	1/9, 1/7	Gold Bump Die	

BLOCK DIAGRAM

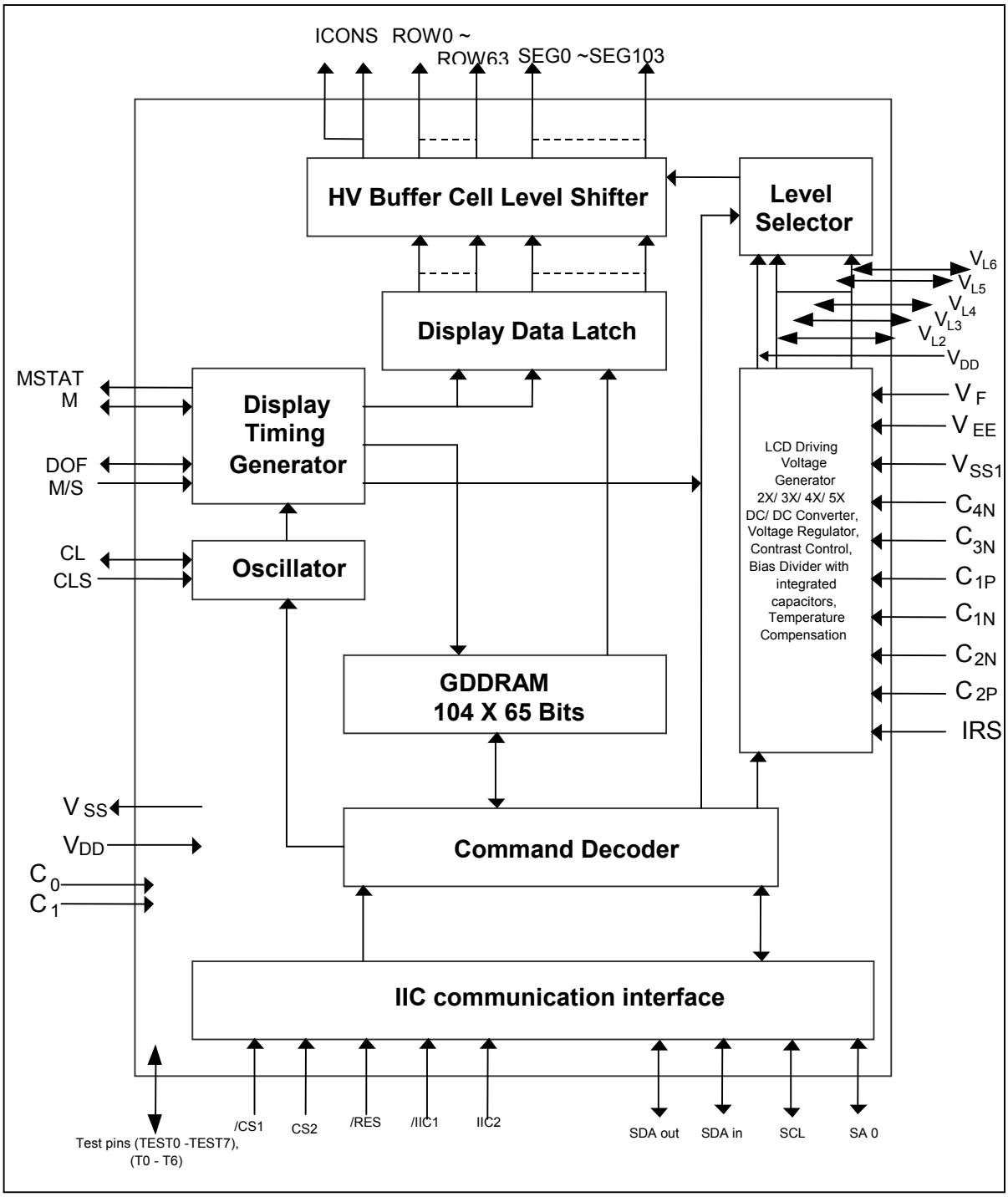
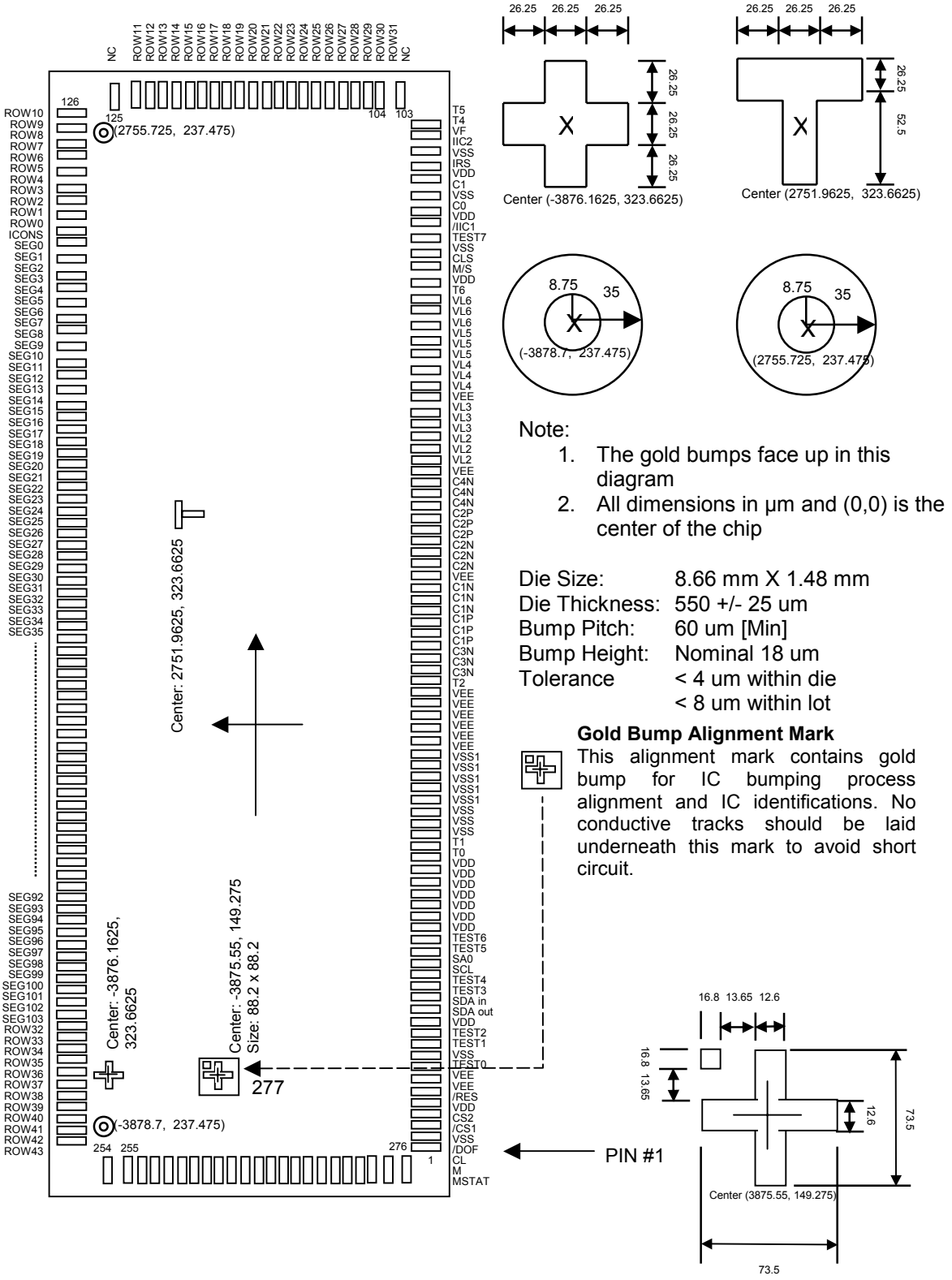


Figure 1 – SSD0817 Block Diagram

DIE PAD ARRANGEMENT



Note:

1. The gold bumps face up in this diagram
2. All dimensions in μm and (0,0) is the center of the chip

Die Size:	8.66 mm X 1.48 mm
Die Thickness:	550 +/- 25 um
Bump Pitch:	60 um [Min]
Bump Height:	Nominal 18 um
Tolerance	< 4 um within die
	< 8 um within lot

Gold Bump Alignment Mark

This alignment mark contains gold bump for IC bumping process alignment and IC identifications. No conductive tracks should be laid underneath this mark to avoid short circuit.

Figure 2 – SSD0817 Pin Assignment

Table 2 – SSD0817 Series Bump Die Pad Coordinates (Bump center)

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
1	MSTAT	-3873.80	-581.35	51	C3N	-27.48	-581.35	101	T4	3799.95	-581.35
2	M	-3797.50	-581.35	52	C1P	48.83	-581.35	102	T5	3876.25	-581.35
3	CL	-3721.20	-581.35	53	C1P	125.13	-581.35	103	NC	4178.48	-655.03
4	/DOF	-3644.90	-581.35	54	C1P	201.43	-581.35	104	ROW31	4178.48	-594.83
5	VSS	-3568.60	-581.35	55	C1N	277.73	-581.35	105	ROW30	4178.48	-534.63
6	/CS1	-3492.30	-581.35	56	C1N	354.03	-581.35	106	ROW29	4178.48	-474.43
7	CS2	-3416.00	-581.35	57	C1N	430.33	-581.35	107	ROW28	4178.48	-414.23
8	VDD	-3339.70	-581.35	58	VEE	506.63	-581.35	108	ROW27	4178.48	-354.03
9	/RES	-3263.40	-581.35	59	C2N	582.93	-581.35	109	ROW26	4178.48	-293.83
10	VEE	-3178.35	-581.35	60	C2N	659.23	-581.35	110	ROW25	4178.48	-233.63
11	VEE	-3102.05	-581.35	61	C2N	735.53	-581.35	111	ROW24	4178.48	-173.43
12	TEST0	-3017.00	-581.35	62	C2P	811.83	-581.35	112	ROW23	4178.48	-113.23
13	VSS	-2940.70	-581.35	63	C2P	888.13	-581.35	113	ROW22	4178.48	-53.03
14	TEST1	-2864.40	-581.35	64	C2P	964.43	-581.35	114	ROW21	4178.48	7.18
15	TEST2	-2788.10	-581.35	65	C4N	1040.73	-581.35	115	ROW20	4178.48	67.38
16	VDD	-2711.80	-581.35	66	C4N	1117.03	-581.35	116	ROW19	4178.48	127.58
17	SDA out	-2635.50	-581.35	67	C4N	1193.33	-581.35	117	ROW18	4178.48	187.78
18	SDA in	-2557.63	-581.35	68	VEE	1269.63	-581.35	118	ROW17	4178.48	247.98
19	TEST3	-2481.33	-581.35	69	VL2	1345.93	-581.35	119	ROW16	4178.48	308.18
20	TEST4	-2403.10	-581.35	70	VL2	1422.23	-581.35	120	ROW15	4178.48	368.38
21	SCL	-2325.23	-581.35	71	VL2	1498.53	-581.35	121	ROW14	4178.48	428.58
22	SA0	-2248.93	-581.35	72	VL3	1574.83	-581.35	122	ROW13	4178.48	488.78
23	TEST5	-2172.63	-581.35	73	VL3	1651.13	-581.35	123	ROW12	4178.48	548.98
24	TEST6	-2096.33	-581.35	74	VL3	1727.43	-581.35	124	ROW11	4178.48	609.18
25	VDD	-2020.03	-581.35	75	VEE	1803.73	-581.35	125	NC	4178.48	663.25
26	VDD	-1943.73	-581.35	76	VL4	1880.03	-581.35	126	ROW10	3834.60	587.83
27	VDD	-1867.43	-581.35	77	VL4	1956.33	-581.35	127	ROW9	3774.40	587.83
28	VDD	-1791.13	-581.35	78	VL4	2032.63	-581.35	128	ROW8	3714.20	587.83
29	VDD	-1714.83	-581.35	79	VL5	2108.93	-581.35	129	ROW7	3654.00	587.83
30	VDD	-1638.53	-581.35	80	VL5	2185.23	-581.35	130	ROW6	3593.80	587.83
31	VDD	-1562.23	-581.35	81	VL5	2261.53	-581.35	131	ROW5	3533.60	587.83
32	T0	-1485.93	-581.35	82	VL6	2337.83	-581.35	132	ROW4	3473.40	587.83
33	T1	-1409.63	-581.35	83	VL6	2414.13	-581.35	133	ROW3	3413.20	587.83
34	VSS	-1333.33	-581.35	84	VL6	2490.60	-581.35	134	ROW2	3353.00	587.83
35	VSS	-1257.03	-581.35	85	T6	2566.73	-581.35	135	ROW1	3292.80	587.83
36	VSS	-1180.73	-581.35	86	VDD	2651.78	-581.35	136	ROW0	3232.60	587.83
37	VSS1	-1095.68	-581.35	87	M/S	2728.08	-581.35	137	ICONS	3172.40	587.83
38	VSS1	-1019.38	-581.35	88	CLS	2804.38	-581.35	138	SEG0	3112.20	587.83
39	VSS1	-943.08	-581.35	89	VSS	2880.68	-581.35	139	SEG1	3052.00	587.83
40	VSS1	-866.78	-581.35	90	TEST7	2956.98	-581.35	140	SEG2	2991.80	587.83
41	VSS1	-790.48	-581.35	91	/IIC1	3033.28	-581.35	141	SEG3	2931.60	587.83
42	VEE	-714.18	-581.35	92	VDD	3109.58	-581.35	142	SEG4	2871.40	587.83
43	VEE	-637.88	-581.35	93	C0	3185.88	-581.35	143	SEG5	2811.20	587.83
44	VEE	-561.58	-581.35	94	VSS	3262.18	-581.35	144	SEG6	2751.00	587.83
45	VEE	-485.28	-581.35	95	C1	3338.48	-581.35	145	SEG7	2690.80	587.83
46	VEE	-408.98	-581.35	96	VDD	3414.78	-581.35	146	SEG8	2630.60	587.83
47	VEE	-332.68	-581.35	97	IRS	3491.08	-581.35	147	SEG9	2570.40	587.83
48	T2	-256.38	-581.35	98	VSS	3567.38	-581.35	148	SEG10	2510.20	587.83
49	C3N	-180.08	-581.35	99	IIC2	3643.68	-581.35	149	SEG11	2450.00	587.83
50	C3N	-103.78	-581.35	100	VF	3723.65	-581.35	150	SEG12	2389.80	587.83

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
151	SEG13	2329.60	587.83	201	SEG63	-680.40	587.83	251	ROW41	-3690.40	587.83
152	SEG14	2269.40	587.83	202	SEG64	-740.60	587.83	252	ROW42	-3750.60	587.83
153	SEG15	2209.20	587.83	203	SEG65	-800.80	587.83	253	ROW43	-3810.80	587.83
154	SEG16	2149.00	587.83	204	SEG66	-861.00	587.83	254	NC	-4178.48	663.25
155	SEG17	2088.80	587.83	205	SEG67	-921.20	587.83	255	ROW44	-4178.48	609.18
156	SEG18	2028.60	587.83	206	SEG68	-981.40	587.83	256	ROW45	-4178.48	548.98
157	SEG19	1968.40	587.83	207	SEG69	-1041.60	587.83	257	ROW46	-4178.48	488.78
158	SEG20	1908.20	587.83	208	SEG70	-1101.80	587.83	258	ROW47	-4178.48	428.58
159	SEG21	1848.00	587.83	209	SEG71	-1162.00	587.83	259	ROW48	-4178.48	368.38
160	SEG22	1787.80	587.83	210	SEG72	-1222.20	587.83	260	ROW49	-4178.48	308.18
161	SEG23	1727.60	587.83	211	SEG73	-1282.40	587.83	261	ROW50	-4178.48	247.98
162	SEG24	1667.40	587.83	212	SEG74	-1342.60	587.83	262	ROW51	-4178.48	187.78
163	SEG25	1607.20	587.83	213	SEG75	-1402.80	587.83	263	ROW52	-4178.48	127.58
164	SEG26	1547.00	587.83	214	SEG76	-1463.00	587.83	264	ROW53	-4178.48	67.38
165	SEG27	1486.80	587.83	215	SEG77	-1523.20	587.83	265	ROW54	-4178.48	7.18
166	SEG28	1426.60	587.83	216	SEG78	-1583.40	587.83	266	ROW55	-4178.48	-53.03
167	SEG29	1366.40	587.83	217	SEG79	-1643.60	587.83	267	ROW56	-4178.48	-113.23
168	SEG30	1306.20	587.83	218	SEG80	-1703.80	587.83	268	ROW57	-4178.48	-173.43
169	SEG31	1246.00	587.83	219	SEG81	-1764.00	587.83	269	ROW58	-4178.48	-233.63
170	SEG32	1185.80	587.83	220	SEG82	-1824.20	587.83	270	ROW59	-4178.48	-293.83
171	SEG33	1125.60	587.83	221	SEG83	-1884.40	587.83	271	ROW60	-4178.48	-354.03
172	SEG34	1065.40	587.83	222	SEG84	-1944.60	587.83	272	ROW61	-4178.48	-414.23
173	SEG35	1005.20	587.83	223	SEG85	-2004.80	587.83	273	ROW62	-4178.48	-474.43
174	SEG36	945.00	587.83	224	SEG86	-2065.00	587.83	274	ROW63	-4178.48	-534.63
175	SEG37	884.80	587.83	225	SEG87	-2125.20	587.83	275	ICONS	-4178.48	-594.83
176	SEG38	824.60	587.83	226	SEG88	-2185.40	587.83	276	NC	-4178.48	-655.03
177	SEG39	764.40	587.83	227	SEG89	-2245.60	587.83	277	NC	-3875.55	149.28
179	SEG41	644.00	587.83	229	SEG91	-2366.00	587.83				
180	SEG42	583.80	587.83	230	SEG92	-2426.20	587.83				
181	SEG43	523.60	587.83	231	SEG93	-2486.40	587.83				
182	SEG44	463.40	587.83	232	SEG94	-2546.60	587.83				
183	SEG45	403.20	587.83	233	SEG95	-2606.80	587.83				
184	SEG46	343.00	587.83	234	SEG96	-2667.00	587.83				
185	SEG47	282.80	587.83	235	SEG97	-2727.20	587.83				
186	SEG48	222.60	587.83	236	SEG98	-2787.40	587.83				
187	SEG49	162.40	587.83	237	SEG99	-2847.60	587.83				
188	SEG50	102.20	587.83	238	SEG100	-2907.80	587.83				
189	SEG51	42.00	587.83	239	SEG101	-2968.00	587.83				
190	SEG52	-18.20	587.83	240	SEG102	-3028.20	587.83				
191	SEG53	-78.40	587.83	241	SEG103	-3088.40	587.83				
192	SEG54	-138.60	587.83	242	ROW32	-3148.60	587.83				
193	SEG55	-198.80	587.83	243	ROW33	-3208.80	587.83				
195	SEG57	-319.20	587.83	245	ROW35	-3329.20	587.83				
196	SEG58	-379.40	587.83	246	ROW36	-3389.40	587.83				
197	SEG59	-439.60	587.83	247	ROW37	-3449.60	587.83				
198	SEG60	-499.80	587.83	248	ROW38	-3509.80	587.83				
199	SEG61	-560.00	587.83	249	ROW39	-3570.00	587.83				
200	SEG62	-620.20	587.83	250	ROW40	-3630.20	587.83				

Bump Size

PAD#	X [um]	Y [um]
1 – 102	50.05	50.05
103 – 124	66.675	40.95
125	66.675	28.7
126 – 253	40.95	66.675
254	66.675	28.7
255 – 276	66.675	40.95
277	88.2	88.2

PIN DESCRIPTION

MSTAT

This pin is the static indicator driving output. It is only active in master operation. The frame signal output pin, M, should be used as the back plane signal for the static indicator. The duration of overlapping can be programmable. This pin, MSTAT, becomes high impedance if the chip is operating in slave mode. Please see the Extended Command Table for reference.

M

This pin is the frame signal input/output. In master mode, this pin supplies the frame signal to slave devices. In slave mode, this pin receives the frame signal from the master device.

CL

This pin is the system clock input/output. When both the internal oscillator (CLS pin pulled high) and the master mode (M/S pin pulled high) are enabled, the CL pin will supplies system clock signal to the slave device. When both internal oscillator and the slave mode are enabled, the CL pin receives system clock signal from either the master device or the external clock source.

$\overline{\text{DOF}}$ DOF

This pin is the display blanking signal control pin. In master mode, the $\overline{\text{DOF}}$ pin supplies “display on” or “display off” signal (blanking signal) to the slave devices. In slave mode, the $\overline{\text{DOF}}$ pin receives “display on” or “display off” signal from the master device.

$\overline{\text{CS1}}$, CS2

These pins are the chip selection inputs. The chip is enabled for MCU communication only when $\overline{\text{CS1}}$ is pulled low and CS2 is pulled high.

$\overline{\text{RES}}$

This pin is the reset signal input. Initialization of the chip is started once the reset pin is pulled low. The minimum pulse width for completion of the reset procedure is 5 -10 us.

SA0, SCL, SDA_{out}, SDA_{in}

These pins are bi-directional data bus to be connected to the MCU in I^2C-bus interface. Please refer to the section: I^2C Communication interface on page 11 for detail pin descriptions.

V_{DD}

The V_{DD} is the Chip’s Power Supply pins. V_{DD} is also acted as a reference level of both the DC-DC Converter and the LCD driving output.

V_{SS}

The V_{ss} is the grounding of the chip. V_{ss} is also acted as a reference level of the logic input/output.

V_{SS1}

The V_{SS1} is the input of the internal DC-DC converter. The generated voltage from the internal DC-DC converter, V_{EE}, is equal to the multiple factors (2X, 3X, 4X, 5X) times the potential different between V_{SS1}, and V_{DD}. The multiple factors, 2X, 3X, 4X or 5X are selected by different arrangements of the external boosting capacitors.
Note: the potential at this input pin must lower than or equal to V_{SS}.

V_{EE}

This is the most negative voltage supply pin of the chip. It can be supplied externally or generated by the internal DC-DC converter. If the internal DC-DC converter generates the voltage level at V_{EE}, the

voltage level is used for internal referencing only. The voltage level at V_{EE} pins is not used for driving external circuitry.

C_{1P}, C_{1N}, C_{2N}, C_{2P} C_{3N} and C_{4N}

When internal DC-DC voltage converter is used, external capacitor(s) is/are connected between these pins. Different connections result in different DC-DC converter multiple factors, for example, 2X, 3X, 4X or 5X. Please refer to the voltage converter section in the functional block description for detail description.

V_{L2}, V_{L3}, V_{L4} and V_{L5}

These pins are outputs with voltage levels equal to the LCD driving voltage. All these voltage levels are referenced to V_{DD}. The voltage levels can be supplied externally or generated by the internal bias divider. The bias divider is turned on once the output op-amp buffers are enabled. Please refer to the Set Power Control Register command for detail description.
The voltage potential relationship is given as: $V_{DD} > V_{L2} > V_{L3} > V_{L4} > V_{L5} > V_{L6}$
In addition, assume the bias factor is known as a,
VL2 - VDD = 1/a * (VL6 - VDD)
VL3 - VDD = 2/a * (VL6 - VDD)
VL4 - VDD = (a-2)/a * (VL6 - VDD)
VL5 - VDD = (a-1)/a * (VL6 - VDD)

V_{L6}

This pin outputs the most negative LCD driving voltage level. The V_{L6} can be supplied externally or generated by the internal regulator. Please refer to the Set Power Control Register command for detail description.

M/$\overline{S}$

This pin is the master/slave mode selection input. When this pin is pulled high, master mode is selected. CL, M, MSTAT and $\overline{DOF}$ signals will become output pins of the slave devices.
When this pin is pulled low, slave mode is selected. CL, M, $\overline{DOF}$ will become input pins. The CL, M, $\overline{DOF}$ signals are received from the master device. The MSTAT pin will stay at high impedance state.

V_F

This pin is the input of the built-in voltage regulator for generating V_{L6}. When external resistor network is selected (IRS pulled low) to generate the LCD driving level, V_{L6}, two external resistors should be added. R_1 should be connected between V_{DD} and V_F. R_2 should be connected between V_F and V_{L6}.

CLS

This pin is the internal clock enable pin. When this pin is pulled high, the internal clock is enabled. The internal clock will be disabled when CLS is pulled low. Under such circumstances, an external clock source must be fed into the CL pin.

$\overline{IIC1}$, IIC2

These pins are I^2C-bus interface selection inputs. The IIC communication interface is enabled only when $\overline{IIC1}$is pulled low and IIC2 is pulled high.

C1, C0

These two pins are the Chip Mode Selection input. The chip mode is determined by multiplex ratio. Altogether there are four chip modes. Please see the following list for reference.

C1	C0	Chip Mode
0	0	48 MUX Mode
0	1	54 MUX Mode
1	0	32 MUX Mode
1	1	64 MUX Mode

ROW0 - ROW63

These pins provide the driving signals, COMMON, to the LCD panel. Please refer to the Table 3 on Page 10 for the COM signal mapping in different MUX.

SEG0 - SEG103

These pins provide the LCD driving signals, SEGMENT, to the LCD panel. The output voltage level of these pins is V_{DD} during sleep mode or standby mode.

ICONS

There are two ICONS pins (pin137 and 275) on the chip. Both pins output exactly the same signal. The duplicated ICON pins will enhance the flexibility of the LCD layout.

IRS

This is the input pin to enable the internal resistors network for the voltage regulator. When this pin is pulled high, the internal feedback resistors of the internal regulator for generating V_{L6} will be enabled. When it is pulled low, external resistors, R_1 should be connected to V_{DD} and V_F. R_2 should be connected between V_F and V_{L6}, respectively.

TEST0-TEST7

These are input pins that reserved for testing purpose. These pins should be connected to VDD.

NC/T0 – T6

These are the No Connection pins. These pins should be left open and they are prohibited to have any connections with one another.

Table 3 - Example of ROW pin assignment for different programmable MUX of SSD0817

	48 MUX Mode	54 MUX Mode	32 MUX Mode	64 MUX Mode
ROW0	COM0	COM0	COM0	COM0
ROW1	COM1	COM1	COM1	COM1
ROW2	COM2	COM2	COM2	COM2
ROW3	COM3	COM3	COM3	COM3
ROW4	COM4	COM4	COM4	COM4
ROW5	COM5	COM5	COM5	COM5
ROW6	COM6	COM6	COM6	COM6
ROW7	COM7	COM7	COM7	COM7
ROW8	COM8	COM8	COM8	COM8
ROW9	COM9	COM9	COM9	COM9
ROW10	COM10	COM10	COM10	COM10
ROW11	COM11	COM11	COM11	COM11
ROW12	COM12	COM12	COM12	COM12
ROW13	COM13	COM13	COM13	COM13
ROW14	COM14	COM14	COM14	COM14
ROW15	COM15	COM15	COM15	COM15
ROW16	COM16	COM16	NC	COM16
ROW17	COM17	COM17	NC	COM17
ROW18	COM18	COM18	NC	COM18
ROW19	COM19	COM19	NC	COM19
ROW20	COM20	COM20	NC	COM20
ROW21	COM21	COM21	NC	COM21
ROW22	COM22	COM22	NC	COM22
ROW23	COM23	COM23	NC	COM23
ROW24	NC	COM24	NC	COM24
ROW25	NC	COM25	NC	COM25
ROW26	NC	COM26	NC	COM26
ROW27	NC	NC	NC	COM27
ROW28	NC	NC	NC	COM28
ROW29	NC	NC	NC	COM29
ROW30	NC	NC	NC	COM30
ROW31	NC	NC	NC	COM31
ROW32	COM24	COM27	COM16	COM32
ROW33	COM25	COM28	COM17	COM33
ROW34	COM26	COM29	COM18	COM34
ROW35	COM27	COM30	COM19	COM35
ROW36	COM28	COM31	COM20	COM36
ROW37	COM29	COM32	COM21	COM37
ROW38	COM30	COM33	COM22	COM38
ROW39	COM31	COM34	COM23	COM39
ROW40	COM32	COM35	COM24	COM40
ROW41	COM33	COM36	COM25	COM41
ROW42	COM34	COM37	COM26	COM42
ROW43	COM35	COM38	COM27	COM43
ROW44	COM36	COM39	COM28	COM44
ROW45	COM37	COM40	COM29	COM45
ROW46	COM38	COM41	COM30	COM46
ROW47	COM39	COM42	COM31	COM47
ROW48	COM40	COM43	NC	COM48
ROW49	COM41	COM44	NC	COM49
ROW50	COM42	COM45	NC	COM50
ROW51	COM43	COM46	NC	COM51
ROW52	COM44	COM47	NC	COM52
ROW53	COM45	COM48	NC	COM53
ROW54	COM46	COM49	NC	COM54
ROW55	COM47	COM50	NC	COM55
ROW56	NC	COM51	NC	COM56
ROW57	NC	COM52	NC	COM57
ROW58	NC	COM53	NC	COM58
ROW59	NC	NC	NC	COM59
ROW60	NC	NC	NC	COM60
ROW61	NC	NC	NC	COM61
ROW62	NC	NC	NC	COM62
ROW63	NC	NC	NC	COM63

(Note: X - output non-selected COM signal)

FUNCTIONAL BLOCK DESCRIPTIONS

IIC communication Interface

The IIC communication interface consists of slave address bit (SA0), I^2C-bus data signal (SDA) and I^2C-bus clock signal (SCL). Both the SDA and the SCL must be connected to pull-up resistors. There are also five input signals including, $\overline{RES}$, $\overline{CS1}$, $\overline{IIC1}$, CS2, IIC2, which is used for the initialization of device.

a) Slave address bit (SA0)
SSD0817 have to recognize the slave address before transmitting or receiving any information by the I^2C-bus. The device will responds to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/$\overline{W}$" bit) with the following byte format,
b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0
0 1 1 1 1 0 SA0 R/$\overline{W}$
"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD0817.
"R/$\overline{W}$" bit determines the I^2C-bus interface is operating at either write mode or read status mode.

b) I^2C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA. If SDA in is connected to the "SDA out", the device becomes fully IIC bus compatible.
It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".
The "SDA out" pin may be disconnected from the "SDA in" pin. With such arrangement, the acknowledgement signal will be ignored in the I^2C-bus.

c) I^2C-bus clock signal (SCL)
The transmission of information in the I^2C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

Command Decoder

Input is directed to the command decoder based on the input of control byte which consists of a D/$\overline{C}$ bit and a R/$\overline{W}$ bit. For further information about the control byte, please refer to the section "I^2C-bus Write data and read register status" on page 21. If both the D/$\overline{C}$ bit and the R/$\overline{W}$ bit are low, the input signal is interpreted as a Command. It will be decoded and written to the corresponding command register. If the D/$\overline{C}$ bit is high and the R/$\overline{W}$ bit is low, input signal is written to Graphic Display Data RAM (GDDRAM).

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 104 x 65 = 6760 bits. Table 4 on Page 12 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.
During the vertical scrolling of the display, an internal register (display start line register) stores the address of the display start line. The re-mapping operation can be started at the address of the display start line according to the internal register. Table 4 on Page 12 shows the case in which the display start line register is set to 38h.
For those GDDRAM out of the display common range, they can be accessed for either the preparation of vertical scrolling data or the system usage.

RAM Row	RAM Column	Normal	00h	01h	02h	03h	.....	64h	65h	66h	67h	Common Pins: 48 MUX Mode Normal	48 MUX Mode Remapped	54 MUX Mode Normal	54 MUX Mode Remapped	32 MUX Mode Normal	32 MUX Mode Remapped	64 MUX Mode Normal	64 MUX Mode Remapped
		Remapped	67h	66h	65h	64h	.....	03h	02h	01h	00h								
00h	Page 0	D0 (LSB)					.....					8	39	8	45	8	23	8	55
01h		D1					.....					9	38	9	44	9	22	9	54
02h		D2					.....					10	37	10	43	10	21	10	53
03h		D3					.....					11	36	11	42	11	20	11	52
04h		D4					.....					12	35	12	41	12	19	12	51
05h		D5					.....					13	34	13	40	13	18	13	50
06h		D6					.....					14	33	14	39	14	17	14	49
07h		D7 (MSB)					.....					15	32	15	38	15	16	15	48
08h	Page 1	D0 (LSB)					.....					16	31	16	37	16	15	16	47
09h		D1					.....					17	30	17	36	17	14	17	46
0Ah		D2					.....					18	29	18	35	18	13	18	45
0Bh		D3					.....					19	28	19	34	19	12	19	44
0Ch		D4					.....					20	27	20	33	20	11	20	43
0Dh		D5					.....					21	26	21	32	21	10	21	42
0Eh		D6					.....					22	25	22	31	22	9	22	41
0Fh		D7 (MSB)					.....					23	24	23	30	23	8	23	40
10h	Page 2	D0 (LSB)					.....					24	23	24	29	24	7	24	39
11h		D1					.....					25	22	25	28	25	6	25	38
12h		D2					.....					26	21	26	27	26	5	26	37
13h		D3					.....					27	20	27	26	27	4	27	36
14h		D4					.....					28	19	28	25	28	3	28	35
15h		D5					.....					29	18	29	24	29	2	29	34
16h		D6					.....					30	17	30	23	30	1	30	33
17h		D7 (MSB)					.....					31	16	31	22	31	0	31	32
18h	Page 3	D0 (LSB)					.....					32	15	32	21	X	X	32	31
19h		D1					.....					33	14	33	20	X	X	33	30
1Ah		D2					.....					34	13	34	19	X	X	34	29
1Bh		D3					.....					35	12	35	18	X	X	35	28
1Ch		D4					.....					36	11	36	17	X	X	36	27
1Dh		D5					.....					37	10	37	16	X	X	37	26
1Eh		D6					.....					38	9	38	15	X	X	38	25
1Fh		D7 (MSB)					.....					39	8	39	14	X	X	39	24
20h	Page 4	D0 (LSB)					.....					40	7	40	13	X	X	40	23
21h		D1					.....					41	6	41	12	X	X	41	22
22h		D2					.....					42	5	42	11	X	X	42	21
23h		D3					.....					43	4	43	10	X	X	43	20
24h		D4					.....					44	3	44	9	X	X	44	19
25h		D5					.....					45	2	45	8	X	X	45	18
26h		D6					.....					46	1	46	7	X	X	46	17
27h		D7 (MSB)					.....					47	0	47	6	X	X	47	16
28h	Page 5	D0 (LSB)					.....					X	X	48	5	X	X	48	15
29h		D1					.....					X	X	49	4	X	X	49	14
2Ah		D2					.....					X	X	50	3	X	X	50	13
2Bh		D3					.....					X	X	51	2	X	X	51	12
2Ch		D4					.....					X	X	52	1	X	X	52	11
2Dh		D5					.....					X	X	53	0	X	X	53	10
2Eh		D6					.....					X	X	X	X	X	X	54	9
2Fh		D7 (MSB)					.....					X	X	X	X	X	X	55	8
30h	Page 6	D0 (LSB)					.....					X	X	X	X	X	X	56	7
31h		D1					.....					X	X	X	X	X	X	57	6
32h		D2					.....					X	X	X	X	X	X	58	5
33h		D3					.....					X	X	X	X	X	X	59	4
34h		D4					.....					X	X	X	X	X	X	60	3
35h		D5					.....					X	X	X	X	X	X	61	2
36h		D6					.....					X	X	X	X	X	X	62	1
37h		D7 (MSB)					.....					X	X	X	X	X	X	63	0
38h	Page 7	D0 (LSB)					.....					0	47	0	53	0	31	0	63
39h		D1					.....					1	46	1	52	1	30	1	62
3Ah		D2					.....					2	45	2	51	2	29	2	61
3Bh		D3					.....					3	44	3	50	3	28	3	60
3Ch		D4					.....					4	43	4	49	4	27	4	59
3Dh		D5					.....					5	42	5	48	5	26	5	58
3Eh		D6					.....					6	41	6	47	6	25	6	57
3Fh		D7 (MSB)					.....					7	40	7	46	7	24	7	56
	Page 8	D0 (LSB)					.....					ICONS	ICONS	ICONS	ICONS	ICONS	ICONS	ICONS	ICONS
		Segment Pins	0	1	2	3	.....	100	101	102	103								

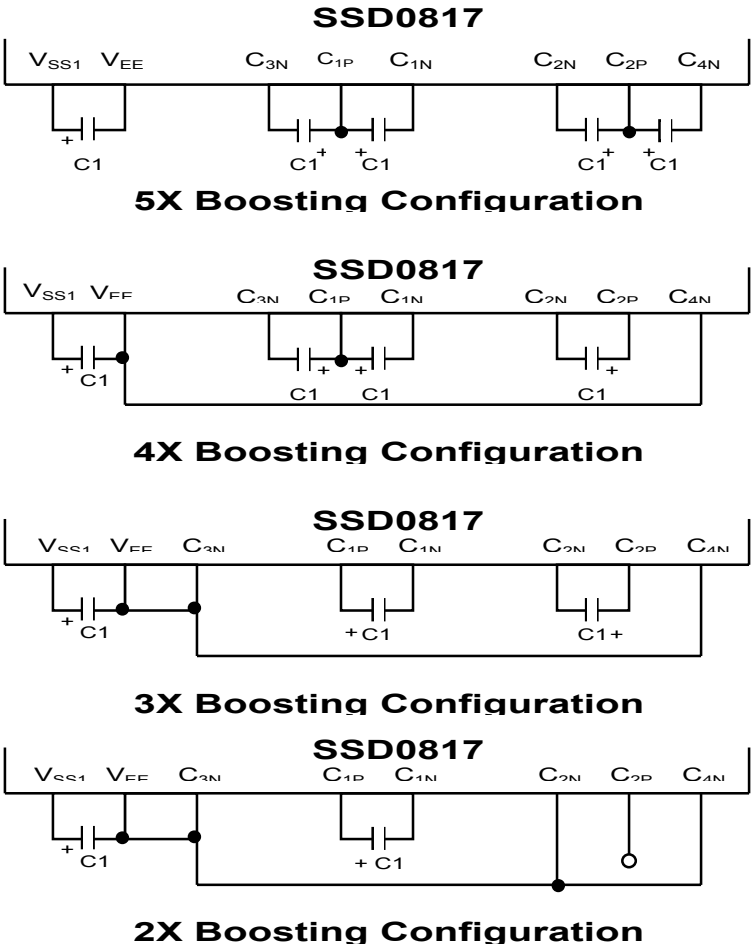
Remarks : DB0 – DB7 represent the data bit of the GDDRAM

Table 4 - Graphic Display Data RAM (GDDRAM) Address Map with Display Start Line set to 38h LCD Driving Voltage Generator and Regulator

LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage required for display driving output. With reference to V_{DD}, it takes a single supply input, V_{SS}, and generates all the necessary voltage levels. This block consists of:

1. 2X, 3X, 4X and 5X DC-DC voltage converter
The built-in DC-DC voltage converter is used to generate the negative voltage with reference to VDD from the voltage input (VSS1). For SSD0817, it is possible to produce 2X, 3X, 4X or 5X boosting from the potential different between V_{SS1} - V_{DD}. Detailed configurations of the DC-DC converter for different boosting multiples are given in Figure 3.



Remarks:
1. C1= 0.47 – 4.7uF
2. Boosting input from VSS1
3. VSS1 should be lower potential than or equal to VSS
4. All voltages are referenced to VDD

Figure 3 - DC-DC Converter Configurations

2. Voltage Regulator (Voltages referenced to V_{DD})
Internal (IRS pin = H) feedback gain can control the LCD driving contrast curves.
If internal resistor network is enabled, eight settings can be selected through software command. If external control is selected, external resistors are connected between V_{DD} and V_F (R1), and between V_F and V_{L6} (R2).
3. Contrast Control (Voltage referenced to V_{DD})
Software control of the 64-contrast voltage levels at each voltage regulator feedback gain. The equation of calculating the LCD driving voltage is given as:

$V_{L6} - V_{DD}$ = Gain * [1 + $\frac{(18 + \alpha)}{81}$] * V_{ref} α stands for the contrast set (0 to 63)

Gain = (1 + Rb/Ra), the reference value is shown in table 5.

Register ratio D2 D1 D0	Thermal Gradient = -0.07 %/°C
0 0 0	2.92
0 0 1	3.40
0 1 0	3.89
0 1 1	4.37
1 0 0	4.85
1 0 1	5.23
1 1 0	5.72
1 1 1	6.19

Table 5 Gain value at different register ratio and thermal gradient settings

V_{ref} is a fixed IC–internal voltage supply and its voltage at room temperature (25 °C) is shown in table 6 for reference.

Type	Thermal Gradient	V_{ref}
TC 0	-0.07 %/°C	-1.08V
TC 2	-0.13 %/°C	-1.12V
TC 4	-0.26 %/°C	-1.09V
TC 7	-0.29 %/°C	-1.10V
External resistor gain mode [Gain = 5.00] @ TC0	-0.07 %/°C	-1.08V

Table 6 V_{ref} values at different thermal gradient settings

The voltage regulator output for different gain/contrast settings is shown in figure 4.

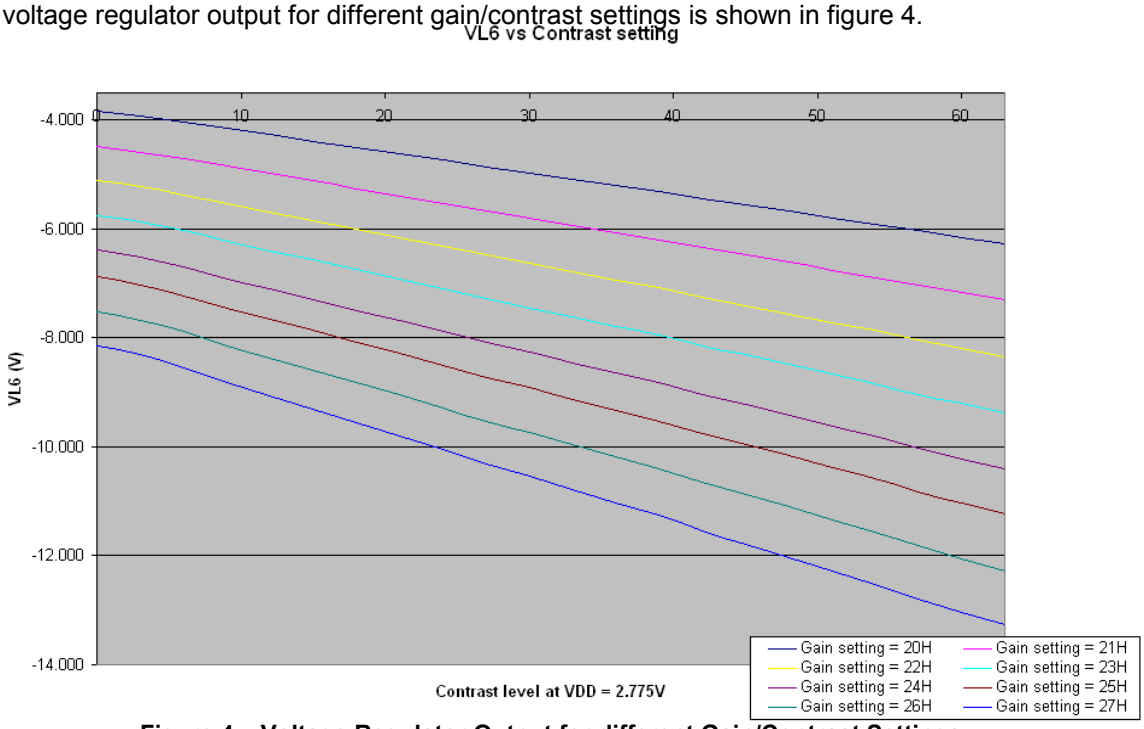


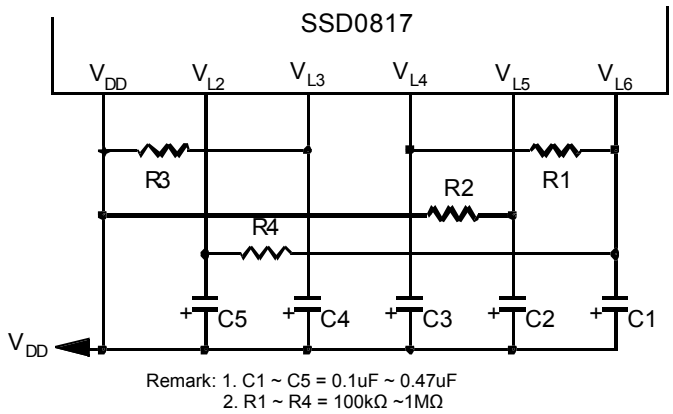
Figure 4 – Voltage Regulator Output for different Gain/Contrast Settings

4. Bias Ratio Selection circuitry

The bias ratios can be software selected from 1/4, 1/5, 1/6, 1/7, 1/8 and 1/9.

Since there will be slightly different in command pattern for different MUX, please refer to Command Descriptions section of this data sheet. If the output op-amp buffer option in Set Power Control Register command is enabled, this circuit block will divide the regulator output (V_{L6}) to give the LCD driving levels (V_{L2} ~ V_{L5}). A low power consumption circuit design in this bias divider saves most of the display current comparing to the traditional design. Stabilizing Capacitors (0.1uF ~ 0.47uF) are

required to be connected between these voltage level pins (V_{L2} ~ V_{L5}) and (V_{DD}). If the LCD panel loading is heavy, four additional resistors are suggested to add to the application circuit as follows:



5. Self adjust temperature compensation circuitry
This block provides 4 different compensation settings to satisfy various liquid crystal temperature grades by software control. The default temperature coefficient (TC) setting is TC0.

Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 5). The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

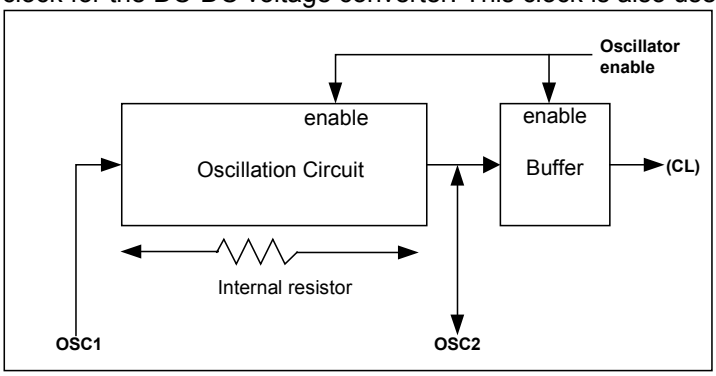


Figure 5 - On-Chip low power RC oscillator circuitry

Reset Circuit

This block includes Power On Reset (POR) circuitry and the hardware reset pin, $\overline{RES}$. The POR and Hardware reset performs the same reset function. Once $\overline{RES}$ receives a reset pulse, all internal circuitry will start to initialize. Minimum pulse width the reset sequence is 5 -10us. Status of the chip after reset is given by:
Display is turned OFF
Default Display Mode
64 MUX: 104 x 64 + 1 Icon Line
Normal segment and display data column address mapping (Seg0 mapped to Row address 00h)
Read-modify-write mode is OFF
Power control register is set to 000b
Register data clear in I^2C-bus interface
Bias ratio is set to default
64 MUX: 1/9
Static indicator is turned OFF
Display start line is set to GDDRAM column 0
Column address counter is set to 00h
Page address is set to 0
Normal scan direction of the COM outputs
Contrast control register is set to 20h
Test mode is turned OFF
Temperature Coefficient is set to TC0

Display Data Latch

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the HV Buffer Cell and Level Selector to output the required voltage level.
The numbers of latches of different members are given by:
64 MUX: 104 + 65 = 169

HV Buffer Cell (Level Shifter)

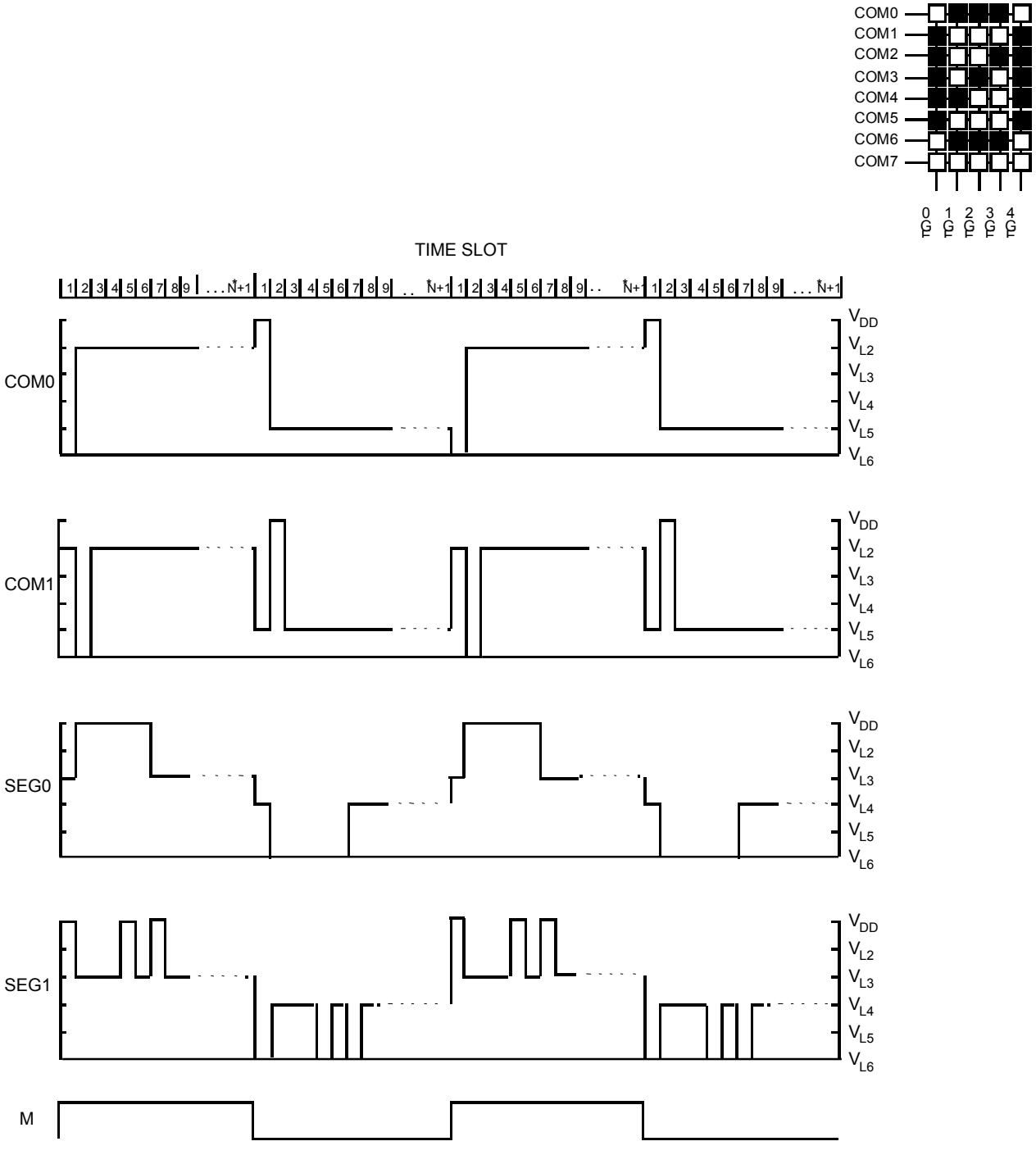
HV Buffer Cell works as a level shifter which translates the low voltage output signal to the required driving voltage. The output is shifted out with reference to the internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

Level Selector

Level Selector is a control of the display synchronization. Display voltage levels can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

LCD Panel Driving Waveform

Figure 6 is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveforms illustrate the desired multiplex scheme.



* Note 1: N+1 is the number of multiplex ratio including Icon.

Figure 6 - LCD Driving Waveform for Displaying "0"

COMMAND TABLE

Bit Pattern	Command	Description
$0000X_3X_2X_1X_0$	Set Lower Column Address	Set the lower nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The lower nibble of column address is reset to 0000b after POR
$0001X_3X_2X_1X_0$	Set Higher Column Address	Set the higher nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The higher nibble of column address is reset to 0000b after POR.
$00100X_2X_1X_0$	Set Internal Regulator Resistor Ratio	Feedback gain of the internal regulator generating VL6 increases as $X_2X_1X_0$ increased from 000b to 111b. After POR, $X_2X_1X_0$ = 100b
$00101X_2X_1X_0$	Set Power Control Register	X_0=0: turns off the output op-amp buffer (POR) X_0=1: turns on the output op-amp buffer X_1=0: turns off the internal regulator (POR) X_1=1: turns on the internal regulator X_2=0: turns off the internal voltage booster (POR) X_2=1: turns on the internal voltage booster
$01X_5X_4X_3X_2X_1X_0$	Set Display Start Line	Set GDDRAM display start line register from 0-63 using $X_5X_4X_3X_2X_1X_0$. Display start line register is reset to 000000 after POR.
10000001 ** $X_5X_4X_3X_2X_1X_0$	Set Contrast Control Register	Select contrast level from 64 contrast steps. Contrast increases (VL6 decreases) as $X_5X_4X_3X_2X_1X_0$ is increased from 000000b to 111111b. $X_5X_4X_3X_2X_1X_0$ = 100000b after POR
$1010000X_0$	Set Segment Re-map	X_0=0: column address 00h is mapped to SEG0 (POR) X_0=1: column address 67h is mapped to SEG0 Refer to Table 4 on page 12 for example.
$1010001X_0$	Set LCD Bias	X_0=0: POR default bias 48 MUX Mode: 1/8 54 MUX Mode: 1/8.4 32 MUX Mode: 1/6 64 MUX Mode: 1/9 X_0=1: alternate bias 48 MUX Mode: 1/6 54 MUX Mode: 1/6 32 MUX Mode: 1/5 64 MUX Mode: 1/7 For other bias ratio settings, see “Set 1/4 Bias Ratio” and “Set Bias Ratio” in Extended Command Set.
$1010010X_0$	Set Entire Display On/Off	X_0=0: normal display (POR) X_0=1: entire display on
$1010011X_0$	Set Normal/Inverse Display	X_0=0: normal display (POR) X_0=1: inverse display
$1010111X_0$	Set Display On/Off	X_0=0: turns off LCD panel (POR) X_0=1: turns on LCD panel
$1011X_3X_2X_1X_0$	Set Page Address	Set GDDRAM Page Address (0-8) for read/write using $X_3X_2X_1X_0$
$1100X_3$ * * *	Set COM Output Scan Direction	X_3=0: normal mode (POR) X_3=1: remapped mode, COM 0 to COM [N-1] becomes COM [N-1] to COM 0 when Multiplex ratio is equal to N. See Figure 5 on page 17 for detail mapping.
11100000	Set Read-Modify-Write Mode	Read-Modify-Write mode will be entered in which the column address will not be increased during display data read. After POR, Read-modify-write mode is turned OFF.
11100010	Software Reset	Initialize internal status registers
11101110	Set End of Read-Modify-Write Mode	Exit Read-Modify-Write mode. RAM Column address before entering the mode will be restored. After POR, Read-modify-write mode is OFF.
$1010110X_0$	Indicator Display Mode	This second byte command is required ONLY when

* * * * * * X_1X_0 Set Indicator On/Off		"Set Indicator On" command is sent. X_0 = 0: indicator off (POR, second command byte is not required) X_0 = 1: indicator on (second command byte required) X_1X_0 = 00: indicator off X_1X_0 = 01: indicator on and blinking at ~1 second interval X_1X_0 = 10: indicator on and blinking at ~1/2 second interval X_1X_0 = 11: indicator on constantly
11100011	NOP	Command result in No Operation
11110000	Test Mode Reset	Reserved for IC testing. Do NOT use
1111 * * * *	Set Test Mode	Reserved for IC testing. Do NOT use.
10101110 10100101	Set Power Save Mode	(Standby or Sleep) Standby or sleep mode will be entered using compound commands. Issue compound commands "Set Display Off" followed by "Set Entire Display On".

Table 7 - Write Command Table (D/$\overline{C}$ =0, R/$\overline{W}$ =0)

Bit Pattern	Command	Description
10101000 00$X_5X_4X_3X_2X_1X_0$	Set Multiplex Ratio	To select multiplex ratio N from 2 to the maximum multiplex ratio (POR value) for each member (including icon line). Max. MUX ratio: 64 MUX: 65 N = $X_5X_4X_3X_2X_1X_0$ + 2, e.g. N = 001111b + 2 = 17
10101001 $X_7X_6X_5X_4X_3X_2X_1X_0$	Set Bias Ratio (X_1X_0)	For 64 MUX Mode X_1X_0 = 00(POR) 01 10 11 1/9 or 1/7 1/5 1/6 1/8 For 54 MUX Mode X_1X_0 = 00(POR) 01 10 11 1/8.4 or 1/6 1/5 1/6 1/8 For 48 MUX Mode X_1X_0 = 00(POR) 01 10 11 1/8 or 1/6 1/5 1/6 1/8 For 32 MUX Mode X_1X_0 = 00(POR) 01 10 11 1/6 or 1/5 1/5 1/6 1/8
	Set TC Value ($X_4X_3X_2$)	$X_4X_3X_2$ = 000: (TC0) Typ. –0.07%/°C $X_4X_3X_2$ = 010: (TC1) Typ. –0.13%/°C $X_4X_3X_2$ = 100: (TC5) Typ. –0.26%/°C $X_4X_3X_2$ = 111: (TC7) Typ. –0.29%/°C $X_4X_3X_2$ = 001, 011, 101, 110: Reserved Increase the value of $X_7X_6X_5$ will increase the oscillator frequency and vice versa.
	Modify Osc. Freq. ($X_7X_6X_5$)	Default Mode: $X_7X_6X_5$ = 011 (POR for 48 MUX Mode, 54 MUX Mode) : Typ. 31.5kHz $X_7X_6X_5$ = 011 (POR for 32 MUX Mode, 64 MUX Mode) : Typ. 18.7Hz

		Remarks: By software program the multiplex ratio, the typical oscillator frequency is listed above.
1010101X_0	Set 1/4 Bias Ratio	X_0 = 0: use normal setting (POR) X_0 = 1: fixed at 1/4 bias regardless of other bias setting commands
11010100 00$X_5X_4$0000	Set Total Frame Phases	The On/Off of the Static Icon is given by 3 phases / 1 phase overlapping of the M and MSTAT signals. This command set total phases of the M/MSTAT signals for each frame. The more the total phases, the less the overlapping time and thus the lower the effective driving voltage. X_5X_4 = 00: 5 phases X_5X_4 = 01: 7 phases X_5X_4 = 10: 9 phases (POR) X_5X_4 = 11: 16 phases
11010011 00$X_5X_4X_3X_2X_1X_0$	Set Display Offset	After POR, $X_5X_4X_3X_2X_1X_0$ = 0 After setting MUX ratio less than default value, data will be displayed at Center of display matrix. To move display towards Row 0 by L, $X_5X_4X_3X_2X_1X_0$ = L To move display away from Row 0 by L, $X_5X_4X_3X_2X_1X_0$ = 64-L Note: max. value of L = (POR default MUX ratio – display MUX)/2
11010110 001111X_1X_0	Enable Band Gap Reference Circuit	X_1X_0 = 00 01 10 11(POR) 100 ms 200 ms 400 ms 800 ms Approx. band gap clock period This command should execute if divider is used without capacitor at VL2 to VL5. Recommendation: set the band gap clock period to approx. 200ms

Table 8 - Extended Command Table

Note: Command patterns other than that given in Command Table and Extended Command Table are prohibited. Otherwise, unexpected result will occur.

I²C-bus Write data and read register status

The I²C-bus interface gives access to write data and command into the device. Please refer to figure 7 for the write mode of I²C-bus in chronological order.

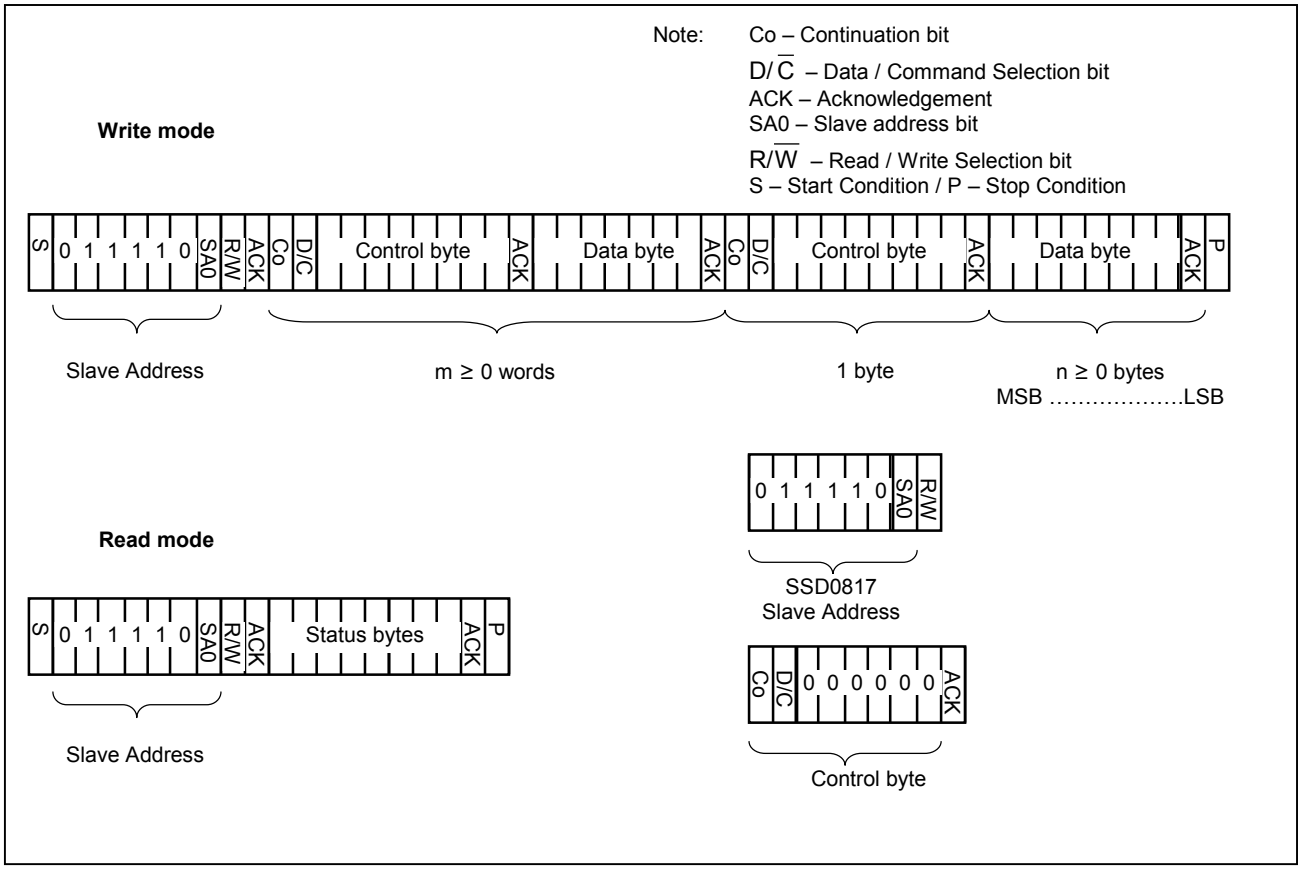


Figure 7 I²C-bus data format

Write mode

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in figure 8 on page 22. The start condition is established by pulling the SDA from high to low while the SCL stays high.
2) The slave address is following the start condition for recognition use. For the SSD0817, the slave address is either "b0111100" or "b0111101" by changing the SA0 to high or low.
3) The write mode is established by setting the R/$\overline{W}$ bit to logic "0".
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/$\overline{W}$ bit. Please refer to the figure 9 on page 22 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the high period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/$\overline{C}$ bits following by six "0" 's.
    a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.

b. The D/$\overline{C}$ bit determines the next data byte is acted as a command or a data. If the D/$\overline{C}$ bit is set to logic “0”, it defines the following data byte as a command. If the D/$\overline{C}$ bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.

6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in figure 8 on page 22. The stop condition is established by pulling the “SDA in” from low to high while the “SCL” stays high.

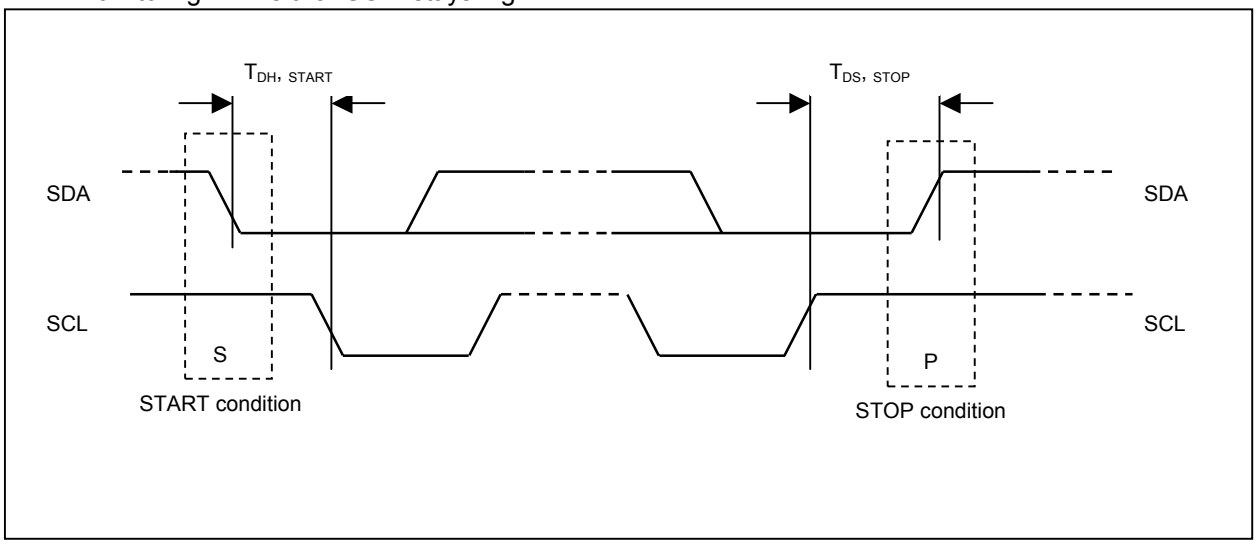


Figure 8 Definition of the start and stop condition

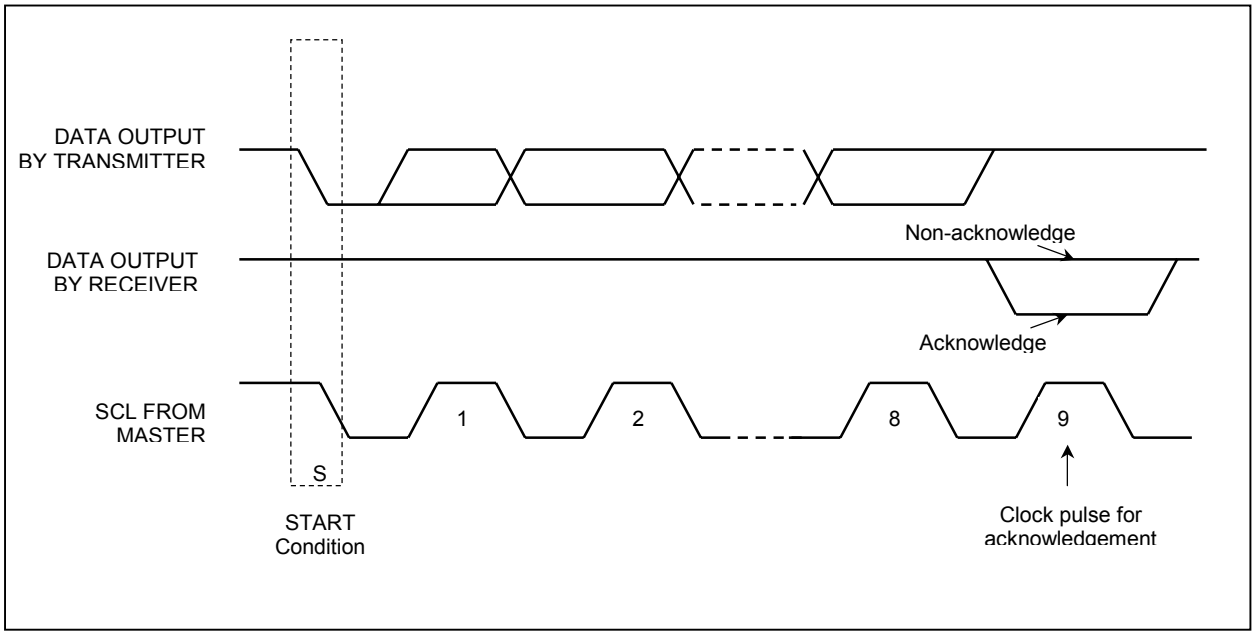


Figure 9 Definition of the acknowledgement condition

Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the “high” period of the clock pulse. Please refer to the figure 10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is low.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

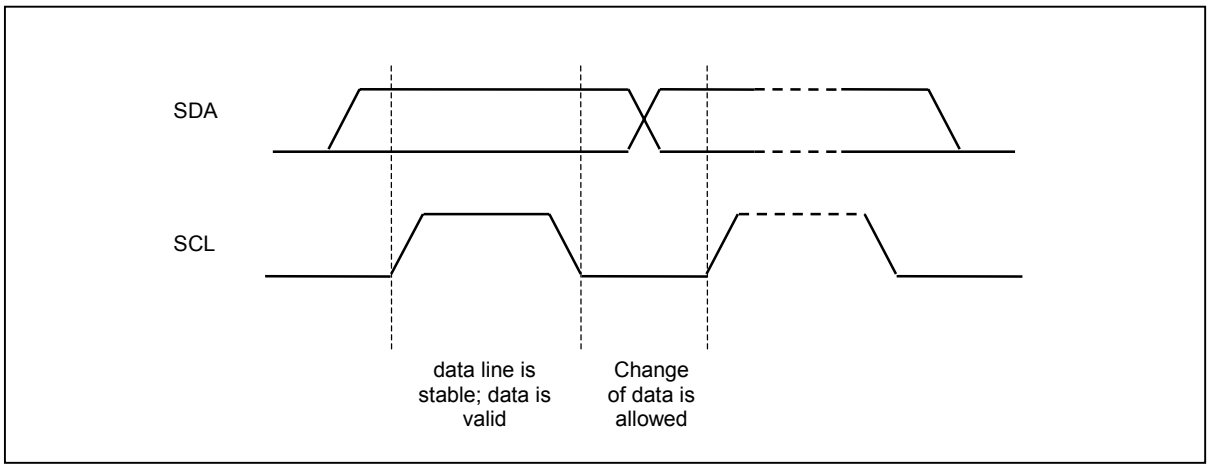


Figure 10 Definition of the data transfer condition

Read mode (Read status register)

1) The master device firstly initiates the data communication by a start condition. The definition of the start condition is shown in figure 8 on page 22.
2) The slave address is following the start condition for recognition use. For the SSD0817, the slave address is either “b0111100” or “b0111101”.
3) The read mode is established by setting R/$\overline{W}$ bit to logic “1”. The read mode allows the MCU to monitor the internal status of the chip.
4) An acknowledgement signal will be generated after sending one byte of data, including the slave address and the R/$\overline{W}$ bit. Please refer to the figure 9 on page 22 for the graphical representation of the acknowledge signal.
5) The status of the register will be read at the next status byte. Please refer to the Table 9 for the explanation of the status byte.
6) The read mode will be finished when a stop condition is applied. The stop condition is also defined in figure 8 on page 22.

$S_7S_6S_5S_4S_3S_2S_1S_0$	Status Register Read	S_7=0: indicates the driver is ready for command. S_7=1: indicates the driver is Busy. S_6=0: indicates reverse segment mapping with column address. S_6=1: indicates normal segment mapping with column address. S_5=0: indicates the display is ON. S_5=1: indicates the display is OFF. S_4=0: initialization is completed. S_4=1: initialization process is in progress after RES or software reset. $S_3S_2S_1S_0$ = 1001, the 4-bit is fixed to 1001 which could be used to identify as Solomon-Systech Device.

Table 9 - Read Command Table (R/$\overline{W}$ bit =1)

COMMAND DESCRIPTIONS

Set Lower Column Address

This command specifies the lower nibble of the 8-bit column address of the display data RAM. The column address will be increased by each data access after it is pre-set by the MCU.

Set Higher Column Address

This command specifies the higher nibble of the 8-bit column address of the display data RAM. The column address will be increased by each data access after it is pre-set by the MCU.

Set Internal Regulator Resistors Ratio

This command is to enable any one of the eight internal resistor sets for different regulator gain when using internal regulator resistor network (IRS pin pulled high). In other words, this command is used to select which contrast curve from the eight possible selections. Please refer to Functional Block Descriptions section for detail calculation of the LCD driving voltage.

Set Power Control Register

This command turns on/off the various power circuits associated with the chip. There are three related power sub-circuits could be turned on/off by this command.
Internal voltage booster is used to generate the negative voltage supply (V_{EE}) from the voltage input (V_{SS1} - V_{DD}). An external negative power supply is required if this option is turned off.
Internal regulator is used to generate the LCD driving voltage, V_{L6}, from the negative power supply, V_{EE}.
Output op-amp buffer is the internal divider for dividing the different voltage levels (V_{L2}, V_{L3}, V_{L4}, V_{L5}) from the internal regulator output, V_{L6}. External voltage sources should be fed into this driver if this circuit is turned off.

Set Display Start Line

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 63. With value equals to 0, D0 of Page 0 is mapped to COM0. With value equals to 1, D1 of Page0 is mapped to COM0 and so on. Display start line values of 0 to 63 are assigned to Page 0 to 7.
Please refer to Table 4 on Page 12 as an example for display start line set to 56 (38h).

Set Contrast Control Register

This command adjusts the contrast of the LCD panel by changing the LCD driving voltage, V_{L6}, provided by the On-Chip power circuits. V_{L6} is set with 64 steps (6-bit) in the contrast control register by a set of compound commands. See Figure 11 for the contrast control flow.

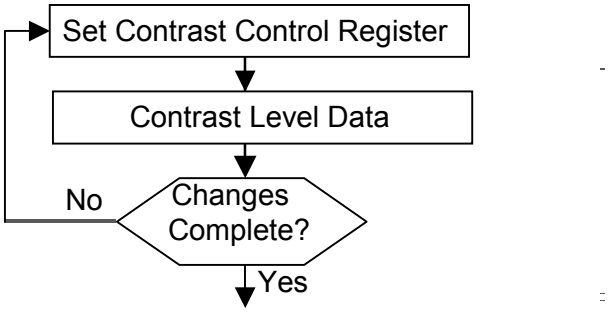


Figure 11 - Contrast Control Flow

Set Segment Re-map

This command changes the mapping between the display data column addresses and segment drivers. It allows flexibility in mechanical layout of LCD glass design. Please refer to Table 4 on Page 12 for example.

Set LCD Bias

This command is used to select a suitable bias ratio required for driving the particular LCD panel in use.
The selectable values of this command for 64 MUX are 1/9 or 1/7.
For other bias ratio settings, extended commands should be used.

Set Entire Display On/Off

This command forces the entire display, including the icon row, to be illuminated regardless of the contents of the GDDRAM. In addition, this command has higher priority than the normal/inverse display.
This command is used together with “Set Display ON/OFF” command to form a compound command for entering power save mode. See “Set Power Save Mode” later in this section.

Set Normal/Inverse Display

This command turns the display to be either normal or inverse. In normal display mode, a RAM data of 1 indicates an illumination on the corresponding pixel. In inverse display mode, a RAM data of 0 will turn on the pixel. It should be noted that the icon line is not affect. The icon line is not inversed by this command.

Set Display On/Off

This command is used to turn the display on or off. When display off is issued with entire display is on, power save mode will be entered. See “Set Power Save Mode” later in this section for details.

Set Page Address

This command enters the page address from 0 to 8 to the RAM page register for read/write operations. Please refer to Table 4 on Page 12 for detail mapping.

Set COM Output Scan Direction

This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly. See Table 4 on Page 12 for the relationship between turning on or off of this feature.
In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will have vertical flipping effect.

Set Read-Modify-Write Mode

This command puts the chip in read-modify-write mode in which:

1. The column address is saved before entering the mode
2. The column address is increased only after display data write but not after display data read.

This Read-Modify-Write mode is used to save the MCU ’s loading when a very portion of display area is being updated frequently.
As reading the data will not change the column address, it could be get back from the chip and do some operation in the MCU. Then the updated data could be written back to the GDDRAM with automatic address increment.
After updating the area, “Set End of Read-Modify-Write Mode” is sent to restore the column address and ready for next update sequence.

Software Reset

Issuing this command causes some of the chip's internal status registers to be initialized:
Read-Modify-Write mode is off
Static indicator is turned OFF
Display start line register is cleared to 0
Column address counter is cleared to 0
Page address is cleared to 0
Normal scanning direction of the COM outputs
Internal regulator resistors Ratio is set to 4
Contrast control register is set to 20h

Set End of Read-Modify-Write Mode

This command relieves the chip from read-modify-write mode. The column address before entering read-modify-write mode will be restored no matter how much modification during the read-modify-write mode.

Set Indicator On/Off

This command turns on or off the static indicator driven by the M and MSTAT pins.
When the "Set Indicator On" command is sent, the second command byte "Indicator Display Mode" must be followed. However, the "Set Indicator Off" command is a single byte command and no second byte command is required.
The status of static indicator also controls whether standby mode or sleep mode will be entered, after issuing the power save compound command. See "Set Power Save Mode" later in this section.

NOP

A command causing the chip takes No Operation.

Set Test Mode

This command forces the driver chip into its test mode for internal testing of the chip. Under normal operation, users should NOT use this command.

Set Power Save Mode

The Standby or Sleep Mode operation should be executed by a compound command. The compound command is composed of "Set Display ON/OFF" and "Set Entire Display ON/OFF" commands. When the "Set Entire Display" is ON and the "Set display" is OFF, either Standby Mode or Sleep Mode will be entered. The status of the Static Indicator will determine which power save mode is entered. If static indicator is off, the Sleep Mode will be entered:
Internal oscillator and LCD power supply circuits are stopped
Segment and Common drivers output V_{DD} level
The display data and operation mode before sleep are held
Internal display RAM can still be accessed
If the static indicator is on, the chip enters Standby Mode, which is similar to sleep mode except addition with:
Internal oscillator is on
Static drive system is on
Please also be noted that during Standby Mode, if the "software reset" command is issued, Sleep Mode will be entered. Both power save modes can be exited by the issue of a new software command or by pulling Low at hardware pin $\overline{RES}$.

EXTENDED COMMANDS

These commands are used, in addition to basic commands, to trigger the enhanced features designed for the chip.

Set Multiplex Ratio

This command switches default multiplex ratio to any multiplex mode from 2 to the maximum multiplex ratio (POR value), including the icon line. Max. MUX ratio: 65
The chip pins ROW0-ROW63 will be switched to corresponding COM signal output, see Table 10 on Page 29 for examples of 18 multiplex (including icon line) settings with and without 7 lines display offset for different MUX.
Remarks: After changing the display multiplex ratio, the bias ratio may be adjusted in order to make display contrast consistent.

Set Bias Ratio

Except the 1/4 bias, all other available bias ratios could be selected using this command plus the “Set LCD Bias” command.
For detail setting values and POR default, please refer to the extended command table, Table 8 on Page 19.

Set Temperature Coefficient (TC) Value

One out of four different temperature coefficient settings is selected by this command in order to match various liquid crystal temperature grades. Please refer to the extended command table, Table 8 on Page 19, for detailed TC values.

Modify Oscillator Frequency

The oscillator frequency can be fine tuned by applying this command. Since the oscillator frequency will be affected by some other factors, this command is not recommended for general usage. Please contact SOLOMON-Systech Limited application engineers for more detail explanation on this command.

Set 1/4 Bias Ratio

This command sets the bias ratio directly to 1/4. This bias ratio is especially designed for use in under 12 MUX display.
In order to restore to other bias ratio, this command must be executed, with LSB=0, before the “Set Multiplex ratio” or “Set LCD Bias” command is sent.

Set Total Frame Phases

The total number of phases for one display frame is set by this command.
The Static Icon is generated by overlapping the M and the MSTAT signals. These two pins output either V_{SS} or V_{DD} at same frequency but with phase different.
To turn on the Static Icon, 3 phases overlapping is applied to these signals, while 1 phase overlapping is given to the “Off “status.
With the increase in the total number of phases in a single frame, the overlapping time decreases. Thus the lower the effective driving voltage at the Static Icon on the LCD panel.

Set Display Offset

This command should be sent ONLY when the multiplex ratio is set less than the default value.
When a lesser multiplex ratio is set, the display will be mapped in the middle (y-direction) of the LCD, see the no offset columns on Table 10 on Page 29. Use this command could move the display vertically within the 64 commons.
To make the Reduced-MUX Com 0 (Com 0 after reducing the multiplex ratio) towards the Row 0 direction for L lines, the 6-bit data in second command should be given by L. An example for 7 lines moving towards to Com0 direction is given on Table 10 on Page 29.
To move in the other direction by L lines, the 6-bit data should be given by 64-L.
Please note that the display is confined within the default multiplex value. That is the maximum value of L is given by the half of the default value minus the reduced-multiplex ratio. For an odd display MUX after reduction, moving away from Row 0 direction will has 1 more step.

Enable Band Gap Reference Circuit

This command enables or disables the band gap reference circuit. It should be noticed that this command should be executed if divider is used without capacitor at VL2 to VL5. There are four selections on the band gap clock period. We recommended to set the band gap clock period to 200ms in normal operation.

	48 MUX Mode		54 MUX Mode		32 MUX Mode		64 MUX Mode	
	No Offset	7 lines Offset	No Offset	7 lines Offset	No Offset	7 lines Offset	No Offset	7 lines Offset
ROW0	X	X	X	X	X	COM0	X	X
ROW1	X	X	X	X	X	COM1	X	X
ROW2	X	X	X	X	X	COM2	X	X
ROW3	X	X	X	X	X	COM3	X	X
ROW4	X	X	X	X	X	COM4	X	X
ROW5	X	X	X	X	X	COM5	X	X
ROW6	X	X	X	X	X	COM6	X	X
ROW7	X	X	X	X	COM0	COM7	X	X
ROW8	X	COM0	X	X	COM1	COM8	X	X
ROW9	X	COM1	X	X	COM2	COM9	X	X
ROW10	X	COM2	X	X	COM3	COM10	X	X
ROW11	X	COM3	X	COM0	COM4	COM11	X	X
ROW12	X	COM4	X	COM1	COM5	COM12	X	X
ROW13	X	COM5	X	COM2	COM6	COM13	X	X
ROW14	X	COM6	X	COM3	COM7	COM14	X	X
ROW15	COM0	COM7	X	COM4	COM8	COM15	X	X
ROW16	COM1	COM8	X	COM5	NC	NC	X	COM0
ROW17	COM2	COM9	X	COM6	NC	NC	X	COM1
ROW18	COM3	COM10	COM0	COM7	NC	NC	X	COM2
ROW19	COM4	COM11	COM1	COM8	NC	NC	X	COM3
ROW20	COM5	COM12	COM2	COM9	NC	NC	X	COM4
ROW21	COM6	COM13	COM3	COM10	NC	NC	X	COM5
ROW22	COM7	COM14	COM4	COM11	NC	NC	X	COM6
ROW23	COM8	COM15	COM5	COM12	NC	NC	COM0	COM7
ROW24	NC	NC	COM6	COM13	NC	NC	COM1	COM8
ROW25	NC	NC	COM7	COM14	NC	NC	COM2	COM9
ROW26	NC	NC	COM8	COM15	NC	NC	COM3	COM10
ROW27	NC	NC	NC	NC	NC	NC	COM4	COM11
ROW28	NC	NC	NC	NC	NC	NC	COM5	COM12
ROW29	NC	NC	NC	NC	NC	NC	COM6	COM13
ROW30	NC	NC	NC	NC	NC	NC	COM7	COM14
ROW31	NC	NC	NC	NC	NC	NC	COM8	COM15
ROW32	COM9	COM16	COM9	COM16	COM9	COM16	COM9	COM16
ROW33	COM10	X	COM10	X	COM10	X	COM10	X
ROW34	COM11	X	COM11	X	COM11	X	COM11	X
ROW35	COM12	X	COM12	X	COM12	X	COM12	X
ROW36	COM13	X	COM13	X	COM13	X	COM13	X
ROW37	COM14	X	COM14	X	COM14	X	COM14	X
ROW38	COM15	X	COM15	X	COM15	X	COM15	X
ROW39	COM16	X	COM16	X	COM16	X	COM16	X
ROW40	X	X	X	X	X	X	X	X
ROW41	X	X	X	X	X	X	X	X
ROW42	X	X	X	X	X	X	X	X
ROW43	X	X	X	X	X	X	X	X
ROW44	X	X	X	X	X	X	X	X
ROW45	X	X	X	X	X	X	X	X
ROW46	X	X	X	X	X	X	X	X
ROW47	X	X	X	X	X	X	X	X
ROW48	X	X	X	X	NC	NC	X	X
ROW49	X	X	X	X	NC	NC	X	X
ROW50	X	X	X	X	NC	NC	X	X
ROW51	X	X	X	X	NC	NC	X	X
ROW52	X	X	X	X	NC	NC	X	X
ROW53	X	X	X	X	NC	NC	X	X
ROW54	X	X	X	X	NC	NC	X	X
ROW55	X	X	X	X	NC	NC	X	X
ROW56	NC	NC	X	X	NC	NC	X	X
ROW57	NC	NC	X	X	NC	NC	X	X
ROW58	NC	NC	X	X	NC	NC	X	X
ROW59	NC	NC	NC	NC	NC	NC	X	X
ROW60	NC	NC	NC	NC	NC	NC	X	X
ROW61	NC	NC	NC	NC	NC	NC	X	X
ROW62	NC	NC	NC	NC	NC	NC	X	X
ROW63	NC	NC	NC	NC	NC	NC	X	X

Table 10 - ROW pin assignment for COM signals for SSD0817 in an 18 MUX display (including icon line) without/with 7 lines display offset towards ROW0

Note: X-Row pin will output non-selected COM signal

MAXIMUM RATINGS

Table 11 - Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{EE}		0 to –12.0	V
Vin	Input Voltage	VSS-0.3 to VDD+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-30 to +85	^oC
T_{stg}	Storage Temperature	-65 to +150	^oC

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and VEE be constrained to the range VSS < or = (Vin or Vout) < or = VDD. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

DC CHARACTERISTICS

Table 12 - DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = -30 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	Logic Circuit Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	2.4	2.7	3.5	V V
I_{AC}	Access Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, Voltage Generator On, 4X DC-DC Converter Enabled, Write accessing, Tcyc =3.3MHz, Typ. Osc. Freq., Display On, no panel attached.	-	480	600	µA
I_{DP1}	Display Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, V_{EE} = -8.1V, Voltage Generator Disabled, R/$\overline{W}$ ($\overline{WR}$) Halt, Typ. Osc. Freq., Display On, V_{L6} - V_{DD} = -9V, no panel attached.	-	50	100	µA
I_{DP2}	Display Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, V_{EE} = -8.1V, Voltage Generator On, 4x DC-DC Converter Enabled, R/$\overline{W}$ ($\overline{WR}$) Halt, Typ. Osc. Freq., Display On, V_{L6} - V_{DD} = -9V, no panel attached.	-	120	200	µA
I_{SB}	Standby Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, LCD Driving Waveform Off, Typ. Osc. Freq., R/$\overline{W}$ ($\overline{WR}$) halt.	-	5	10	µA
I_{SLEEP}	Sleep Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, LCD Driving Waveform Off, Oscillator Off, R/$\overline{W}$ ($\overline{WR}$) halt.	-	1	5	µA
V_{EE}	LCD Driving Voltage Generator Output (V_{EE} Pin)	Display On, Voltage Generator Enabled, DC-DC Converter Enabled, Typ. Osc. Freq., Regulator Enabled, Divider Enabled.	-12.0	-	-2.4	V
V_{LCD}	LCD Driving Voltage Input (V_{EE} Pin)	Voltage Generator Disabled.	-12.0	-	-2.4	V
V_{OH1}	Logic High Output Voltage	Iout=-100mA	0.9*V_{DD}	-	V_{DD}	V
V_{OL1}	Logic Low Output Voltage	Iout=100mA	0	-	0.1*V_{DD}	V
V_{L6}	LCD Driving Voltage Source (V_{L6} Pin)	Regulator Enabled (V_{L6} voltage depends on Int/Ext Contrast Control)	V_{EE}-0.5	-	V_{DD}	V
V_{L6}	LCD Driving Voltage Source (V_{L6} Pin)	Regulator Disable	-	floating	-	V
V_{IH1}	Logic High Input voltage		0.8*V_{DD}	-	V_{DD}	V
V_{IL1}	Logic Low Input voltage		0	-	0.2*V_{DD}	V

V_{L2} V_{L3} V_{L4} V_{L5} V_{L6}	LCD Display Voltage Output (V_{L2}, V_{L3}, V_{L4}, V_{L5}, V_{L6} Pins)	Voltage reference to V_{DD}, Bias Divider Enabled, 1:a bias ratio	-	$1/a*V_{L6}$	-	V
			-	$2/a*V_{L6}$	-	V
			-	$(a-2)/a*V_{L6}$	-	V
			-	$(a-1)/a*V_{L6}$	-	V
			-	V_{L6}	-	V
V_{L2} V_{L3} V_{L4} V_{L5} V_{L6}	LCD Display Voltage Input (V_{L2}, V_{L3},V_{L4}, V_{L5}, V_{L6} Pins)	Voltage reference to V_{DD}, External Voltage Generator, Bias Divider Disabled	V_{L3}	-	V_{DD}	V
			V_{L4}	-	V_{L2}	V
			V_{L5}	-	V_{L3}	V
			V_{L6}	-	V_{L4}	V
			-12V	-	V_{L5}	V
I_{OH}	Logic High Output Current Source	Vout = V_{DD}-0.4V	50	-	-	µA
I_{OL}	Logic Low Output Current Drain	Vout = 0.4V	-	-	-50	µA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	µA
I_{IL}/I_{IH}	Logic Input Current		-1	-	1	µA
C_{IN}	Logic Pins Input Capacitance		-	5	7.5	pF
ΔV_{L6}	Variation of V_{L6} Output (V_{DD} is fixed)	Regulator Enabled, Internal Contrast Control Enabled, Set Contrast Control Register = 0	-3	0	3	%
TC0	Temperature Coefficient Compensation Flat Temperature Coefficient (POR)	Voltage Regulator Enabled	0	-0.07	-0.11	%/°C
TC2	Temperature Coefficient 2*		-0.11	-0.13	-0.15	%/°C
TC4	Temperature Coefficient 4*		-0.15	-0.26	-0.28	%/°C
TC7	Temperature Coefficient 7*		-0.28	-0.29	-0.30	%/°C

The formula for the temperature coefficient is:

$$TC(\%) = \frac{V_{ref} \text{ at } 50^{o}C - V_{ref} \text{ at } 0\ ^{o}C}{50\ ^{o}C - 0\ ^{o}C} \times \frac{1}{V_{ref} \text{ at } 25\ ^{o}C} \times 100\ \%$$

AC CHARACTERISTICS

Table 13 - AC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = -30 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Fosc	Oscillation Frequency of Display Timing Generator	Internal Oscillator Enabled (default), VDD = 2.7V Remark: Oscillator Frequency vs. Temperature change (-20°C to 70°C): -0.5%/°C *				
	64 Mux Mode		15.9	18.7	25.7	kHz
	54 Mux Mode		26.4	31.5	42.72	kHz
F_{FRM}	Frame Frequency					
	64 Mux Mode	104 x 64 Graphic Display Mode, Display ON, Internal Oscillator Enabled		Fosc / 4x65		Hz
		104 x 64 Graphic Display Mode, Display ON, Internal Oscillator Disabled, External clock with freq., Fext, feeding to CL pin.		Fext / 4x65		Hz
	54 Mux Mode	104 x 54 Graphic Display Mode, Display ON, Internal Oscillator Enabled		Fosc / 8x54		Hz
		104 x 54 Graphic Display Mode, Display ON, Internal Oscillator Disabled, External clock with freq., Fext, feeding to CL pin.		Fext / 8x54		Hz
	48 Mux Mode	104 x 48 Graphic Display Mode, Display ON, Internal Oscillator Enabled		Fosc / 8x49		Hz
		104 x 48 Graphic Display Mode, Display ON, Internal Oscillator Disabled, External clock with freq., Fext, feeding to CL pin.		Fext / 4x49		Hz
	32 Mux Mode	104 x 32 Graphic Display Mode, Display ON, Internal Oscillator Enabled		Fosc / 8x33		Hz
		104 x 32 Graphic Display Mode, Display ON, Internal Oscillator Disabled, External clock with freq., Fext, feeding to CL pin.		Fext / 4x33		Hz

Remarks: Fext stands for the frequency value of external clock feeding to the CL pin
Fosc stands for the frequency value of internal oscillator
Frequency limits are based on the software command: set multiplex ratio to 32/48/54/64

Table 14 - I^2C-bus timing Characteristics
(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCL}	I^2C-bus Clock frequency, SCL	0	-	500	kHz
T_{CLKL}	I^2C-bus Clock Low period, SCL	960	-	-	ns
T_{CLKH}	I^2C-bus Clock high period, SCL	960	-	-	ns
T_{DSW}	I^2C-bus Data Setup time, SDA	120	-	-	ns
T_{DHW}	I^2C-bus Data Hold time, SDA	0	-	0.98	us
T_R	Rise time between SDA & SCL	32	-	350	ns
T_F	Fall time between SDA & SCL	32	-	350	ns
C_{BUS}	Capacitive loadings at each I^2C-bus channel	-	-	400	pF
$T_{DH, START}$	I^2C-bus Setup time, START condition	180	-	-	ns
$T_{DS, STOP}$	I^2C-bus Hold time, STOP condition	180	-	-	ns

Symbol	Parameter	Min	Typ	Max	Unit
T_{cycle}	Clock Cycle Time	2.0	-	-	us
T_{DSW}	Write Data Setup Time	120	-	-	ns
T_{DHW}	Write Data Hold Time	0	-	0.98	us
T_{CLKL}	Clock Low Time	960	-	-	ns
T_{CLKH}	Clock High Time	960	-	-	ns
T_R	Rise Time	-	200	350	ns
T_F	Fall Time	-	200	350	ns
$T_{DH, START}$	Hold time, start condition	0.18	2.5	-	us
$T_{DS, STOP}$	Setup time, stop condition	0.18	2.5	-	us

Table 15 - Interface Timing Characteristics (VDD - VSS = 2.4 to 3.5V, TA = 25°C)

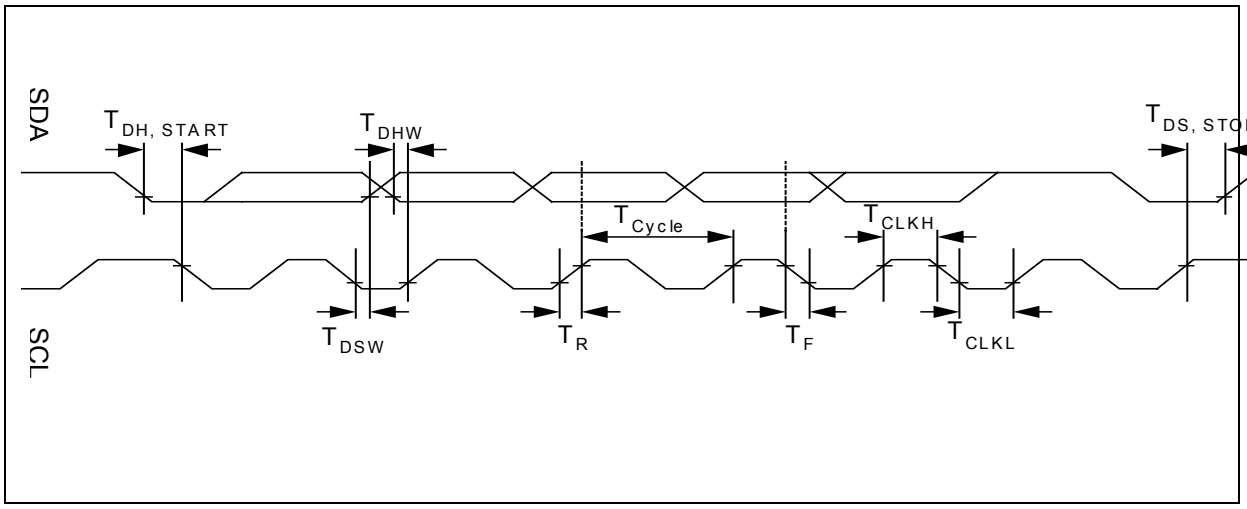
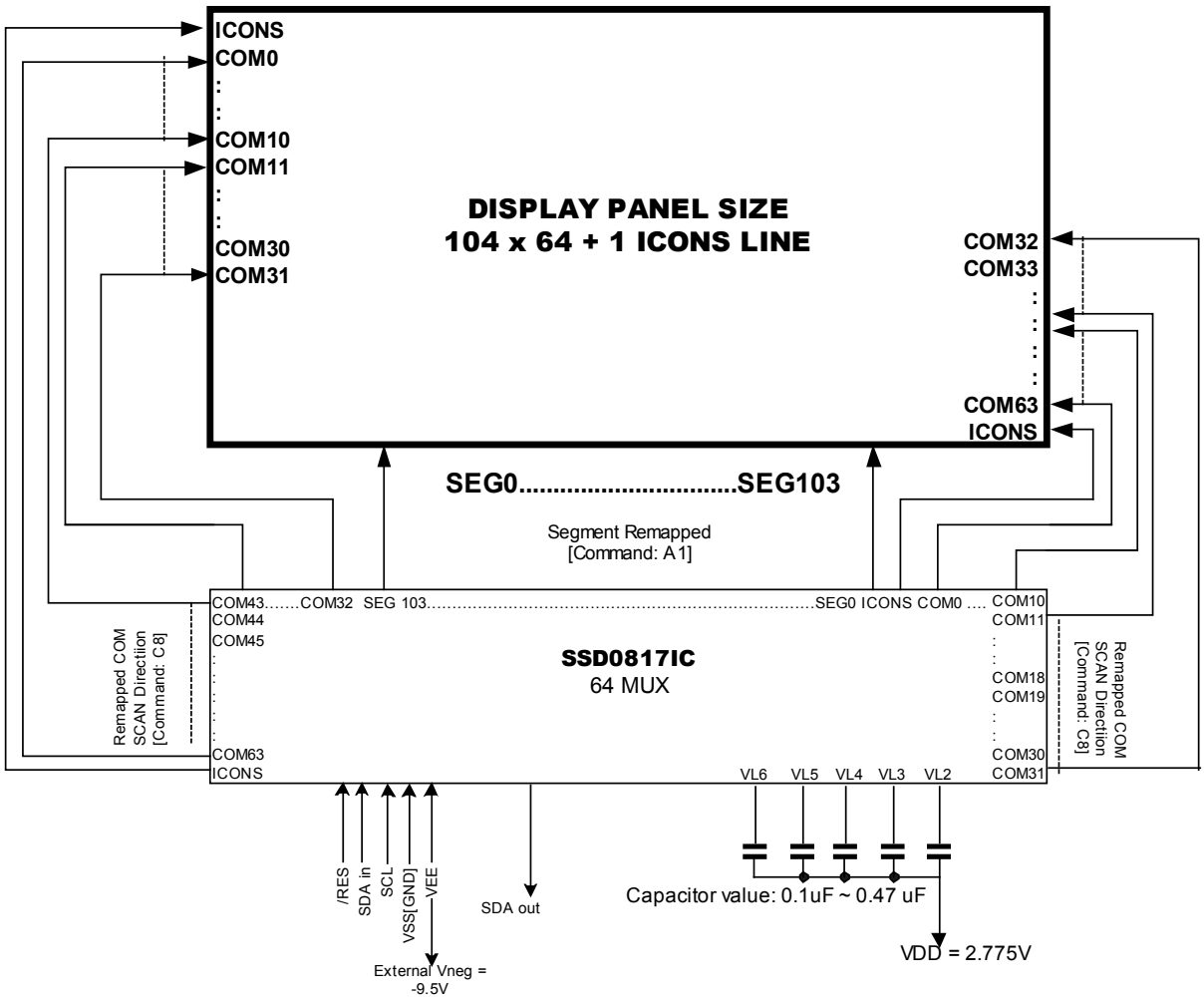


Figure 12 – IIC data bus Interface driving waveform

APPLICATION EXAMPLES



Logic pin connections not specified above:

Pins connected to VDD: IRS, CS2, M/$\overline{S}$, CLS, IIC2, TEST0 - TEST7

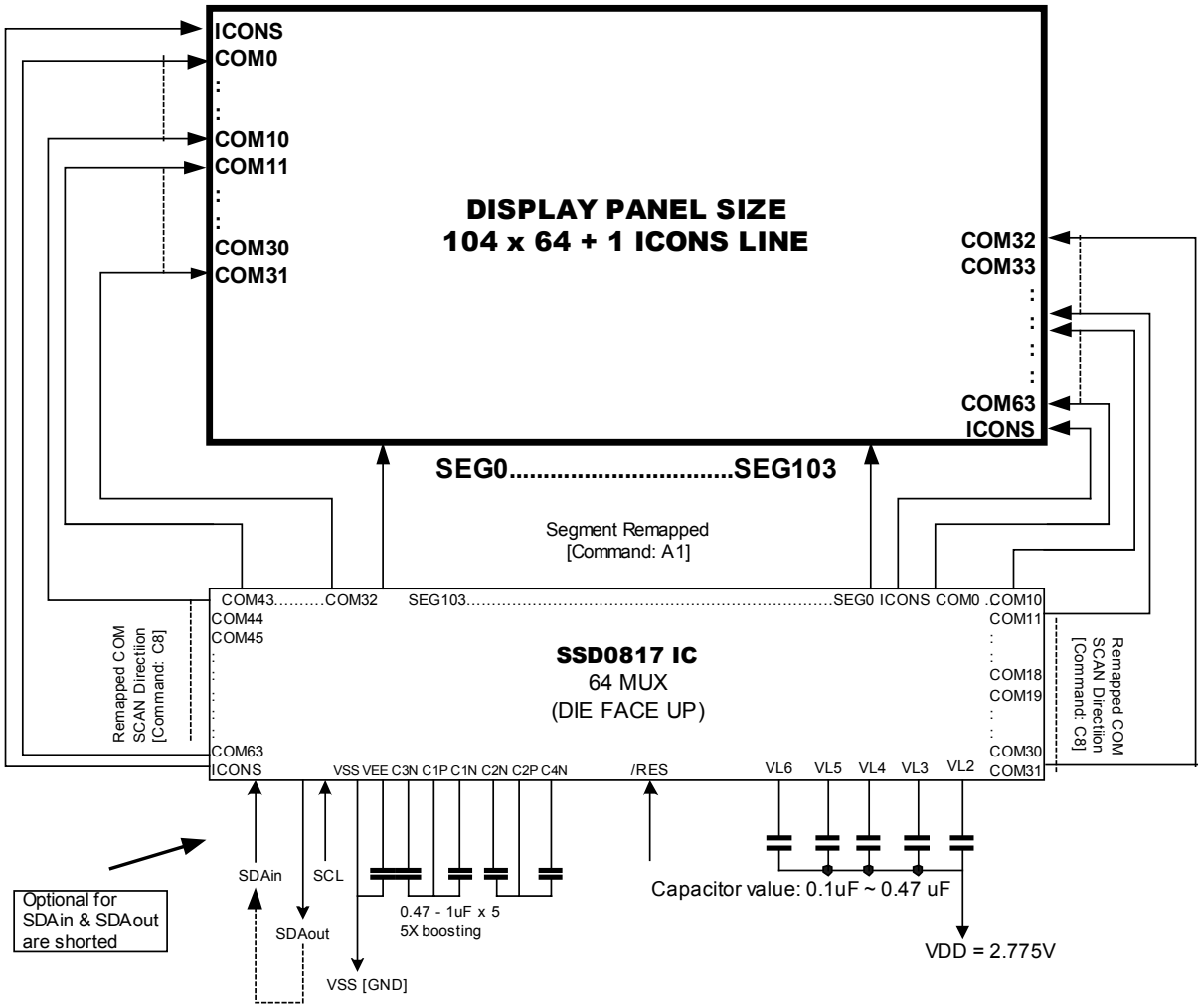
Pins connected to VSS: VSS1, $\overline{CS1}$, $\overline{IIC1}$

Pins floating: $\overline{DOF}$, CL, T0-T6

Pin connected to either VDD or VSS by user defined: C0, C1 and SA0

SDA in & SCL should be pulled high by a pair of resistors: 100k ohm

Figure 13 - Application Circuit of 104 x 64plus an icon line using SSD0817, configured with: external VEE, internal regulator, divider mode enabled (Command: 2B), IIC data bus interface, internal oscillator and master mode



Logic pin connections not specified above:

Pins connected to V_{DD}:, M/$\overline{S}$, CS2, CLS, IIC2, IRS, TEST0-TEST7

Pins connected to V_{SS}: V_{SS1}, $\overline{IIC1}$, $\overline{CSI}$

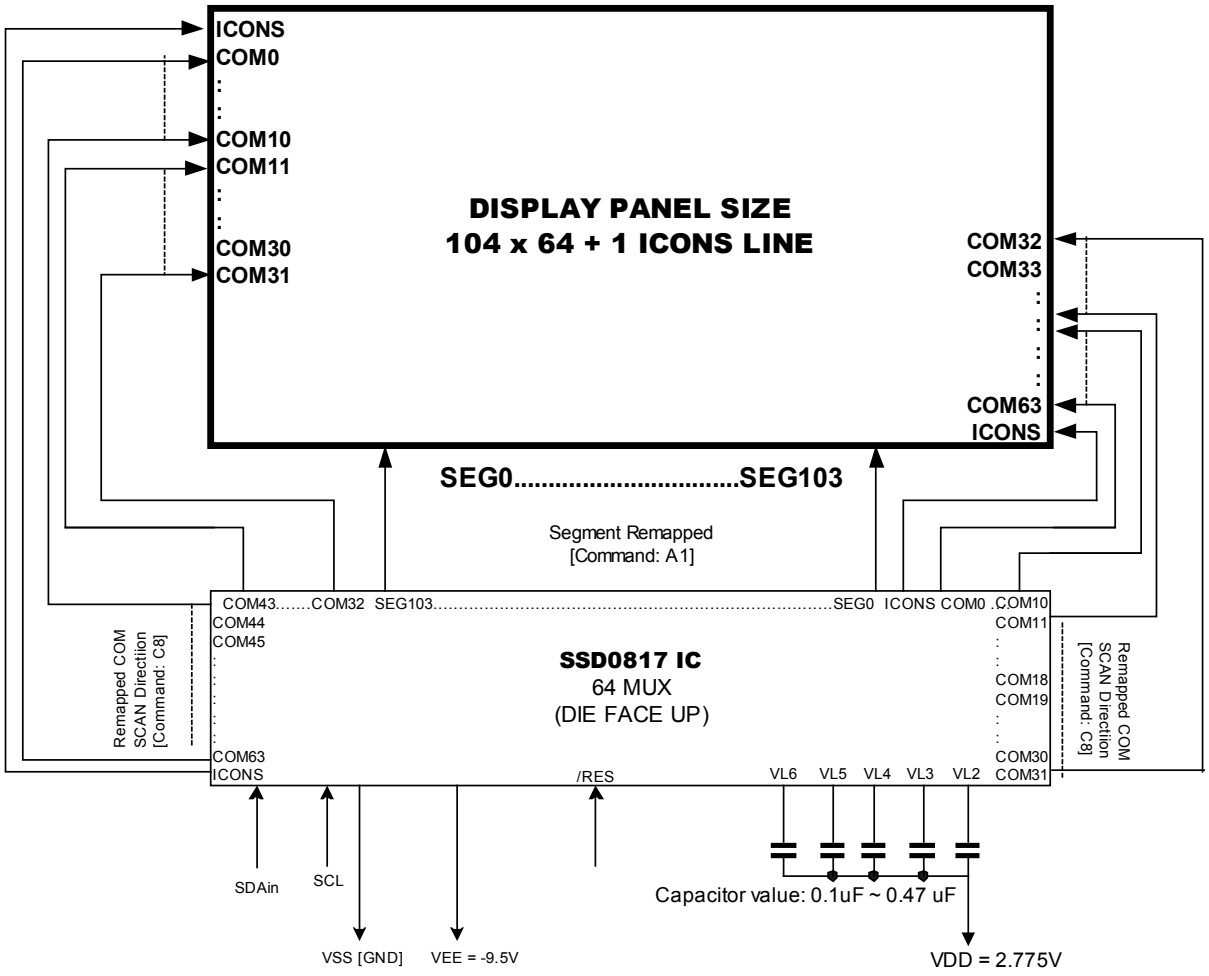
Pins floating: $\overline{DOF}$, CL, T0 - T6

Pin connected to either VDD or VSS by user defined :SA0

Pin connected together: SDA_{in} & SDA_{out}

SDA in and SCl should be pulled high by a pair of resistors: value = 100 k ohm

Figure 14 - Application Circuit of 104 x 64plus an icon line using SSD0817, configured with all internal power control circuit enabled, fully IIC data bus interface, internal oscillator and master mode.



Logic pin connections not specified above:

Pins connected to V_{DD}: CS2, M/$\overline{S}$, CLS, IIC2, D2, D3, D6, D7, IRS

Pins connected to V_{SS}: V_{SS1}, $\overline{IIC1}$, TEST0 - TEST7, $\overline{CSI}$

Pins floating: $\overline{DOF}$, CL, T0 - T6

Pin connected to either VDD or VSS by user defined :SA0

Pin connected together: SDAin & SDAout

SDA in and SCl should be pulled high by a pair of resistors: value = 100 k ohm

Figure 15 - Application Circuit of 104 x 64plus an icon line using SSD0817, configured with all external power control circuit enabled, fully IIC data bus interface, internal oscillator, internal contrast gain and master mode. (Minimum pin outlets)

Initialization Routine

	Command (Hex) (Refer to Figure 11: All internal power control circuit enable)	**Command (Hex)** (Refer to Figure 12: External V_{EE}, Internal regulator and divider enable)	**Description**
1	E2	E2	Software Reset
2	2F	2B	Set power control register
3	24	24	Set internal resistor gain = 24h
4	81 20	81 20	Set contrast level = 20h
5	D6 2D	D6 2D	Enable band gap reference circuit Set band gap clock period = 200ms
6	A0	A0	Set Column address is map to SEG0
7	C0	C0	Set Row address is map to COM0
8	A4	A4	Set entire display on/off = Normal display
9	A6	A6	Set normal / reverse display = Normal display
10	AF	AF	Set Display On
Example	Internal booster, regulator and divider are enabled. V_{OP} = approx. -8.735V with reference to V_{DD}	External booster, Internal regulator and divider are enabled. V_{OP} = approx. -8.593V with reference to V_{DD}	

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