UTRON

UT61L5128

Rev. 1.0

512K X 8 BIT HIGH SPEED CMOS SRAM

FEATURES

- Single 3.3V power supply
- Fast access time : 10/12/15 ns
- CMOS Low operating power
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options.
- Package : 44-pin 400mil TSOP-Ⅱ

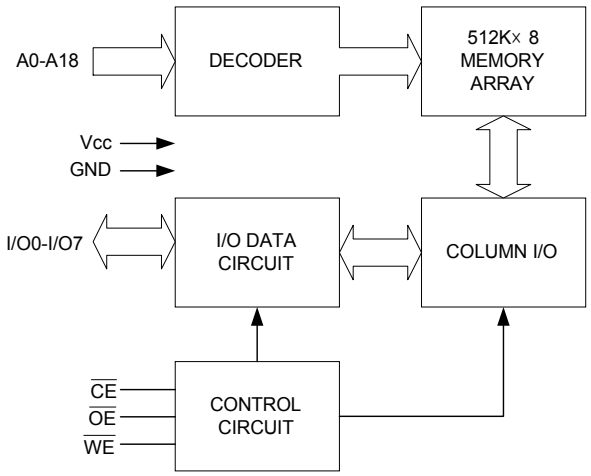
GENERAL DESCRIPTION

The UT61L5128 is a 4,194,304-bit high speed CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

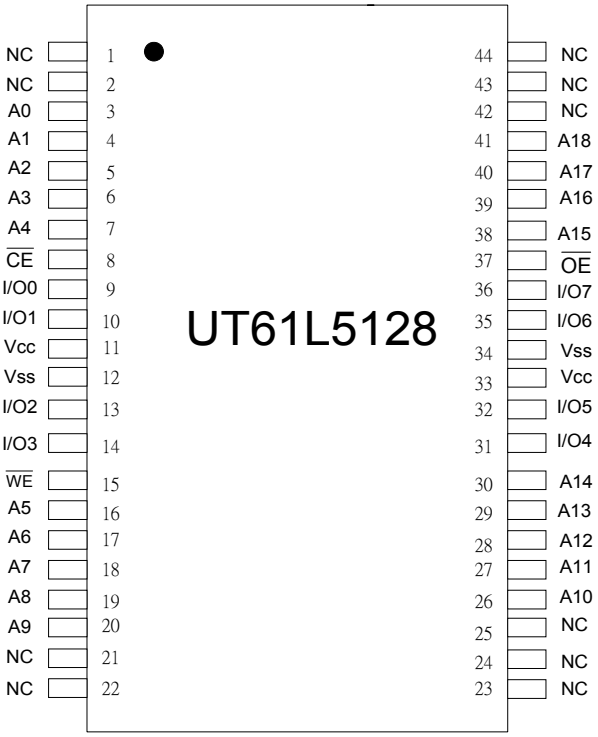
The UT61L5128 is designed for high speed system applications. It is particularly suited for use in high-density high-speed system applications.

The UT61L5128 operates from a single 3.3V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSOP-II

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
NC	No Connection
Vcc	Power supply
Vss	Ground

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ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}	V_{TERM}	-0.5 to V_{CC}+0.5	V
Operating Temperature	T_A	0 to +70	℃
Storage Temperature	T_{STG}	-65 to +150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 sec0	Tsolder	260	℃

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O OPERATION	SUPPLY CURRENT
Standby	X	H	X	High – Z	I_{SB}, I_{SB1}
Output Disable	H	L	H	High – Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.3V±10%, TA = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT
Input High Voltage	V_{IH}			2.2	V_{CC}+0.5	V
Input Low Voltage	V_{IL}			- 0.5	0.8	V
Input Leakage Current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		- 1	1	μA
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_{I/O} \leqq V_{CC}$ Output Disabled		- 1	1	μA
Output High Voltage	V_{OH}	I_{OH}= - 4mA		2.4	-	V
Output Low Voltage	V_{OL}	I_{OL}= 8mA		-	0.4	V
Operating Power Supply Current	I_{CC}	Cycle time=Min.	-10	-	170	mA
		$\overline{CE}$ = V_{IL} ,	-12	-	150	mA
		$I_{I/O}$ = 0mA ,	-15	-	130	mA
Standby Power Supply Current	I_{SB}	$\overline{CE}$ =V_{IH}	-10	-	70	mA
		other pins are at V_{IH} or V_{IL}	-12	-	60	mA
			-15	-	50	mA
	I_{SB1}	$\overline{CE}$ =V_{IH}	-10	-	20	mA
		other pins are at Vcc-0.2V	-12	-	20	mA
		or 0.2V	-15	-	20	mA

CAPACITANCE (TA=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF, I_{OH}/I_{OL} = -1mA/4mA

AC ELECTRICAL CHARACTERISTICS (VCC = 3.3V±10% , TA = 0℃ to 70℃)

(1) READ CYCLE

PARAMETER	SYMBOL	UT61L5128-10*		UT61L5128-12		UT61L5128-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	10	-	12	-	15	ns
Chip Enable Access Time	t_{ACE}	-	10	-	12	-	15	ns
Output Enable Access Time	t_{OE}	-	4.5	-	5	-	7	ns
Chip Enable to Output in Low Z	t_{CLZ*}	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	t_{OLZ*}	0	-	0	-	0	-	ns
Chip Disable to Output in High Z	t_{CHZ*}	-	4	-	5	-	6	ns
Output Disable to Output in High Z	t_{OHZ*}	-	4	-	5	-	6	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

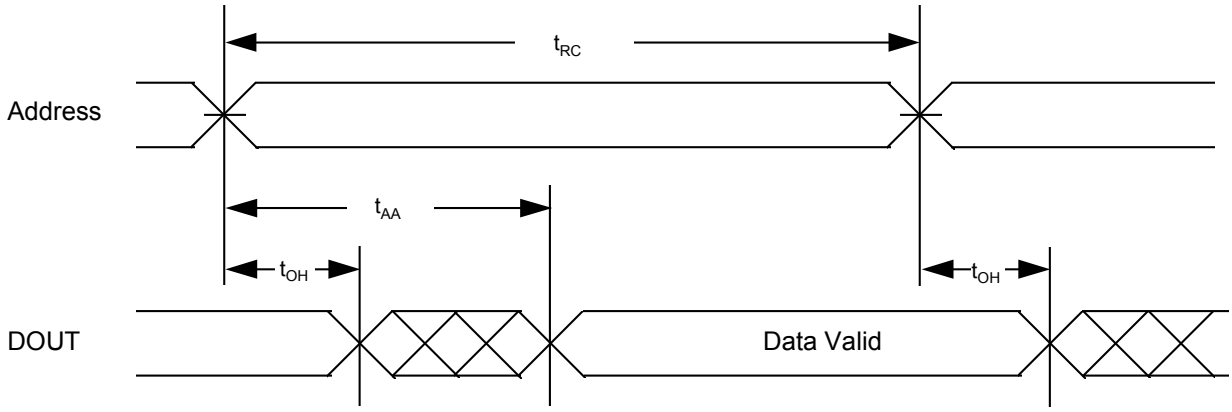
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT61L5128-10*		UT61L5128-12		UT61L5128-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	10	-	12	-	15	-	ns
Address Valid to End of Write	t_{AW}	8	-	8	-	10	-	ns
Chip Enable to End of Write	t_{CW}	8	-	8	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	8	-	8	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	6	-	6	-	7	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW*}	2	-	2	-	2	-	ns
Write to Output in High Z	t_{WHZ*}	-	5	-	6	-	7	ns

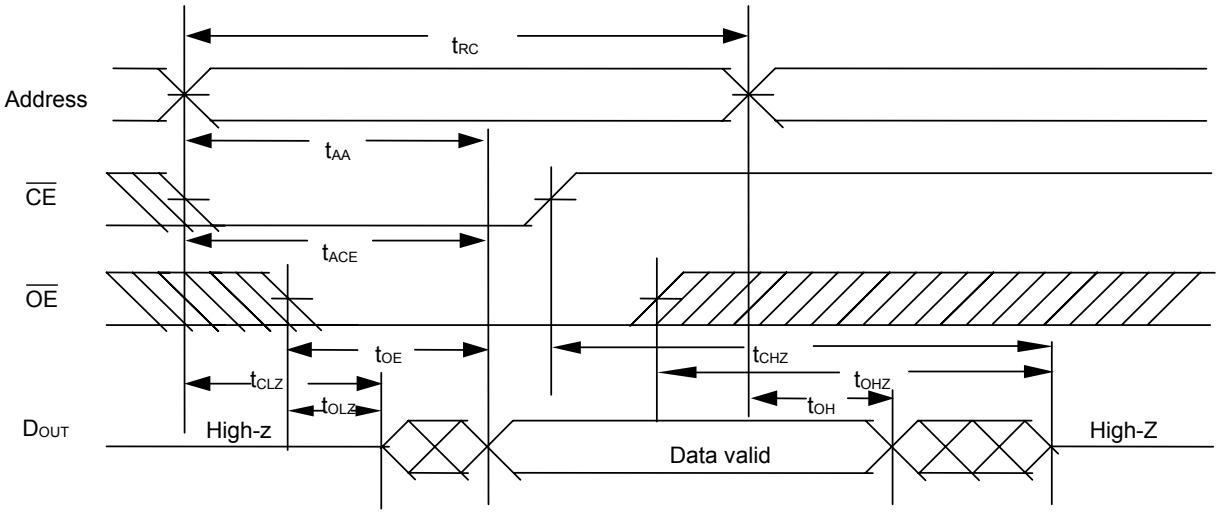
*These parameters are guaranteed by device characterization, but not production tested.
* Vcc = 3.15V to 3.6V

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



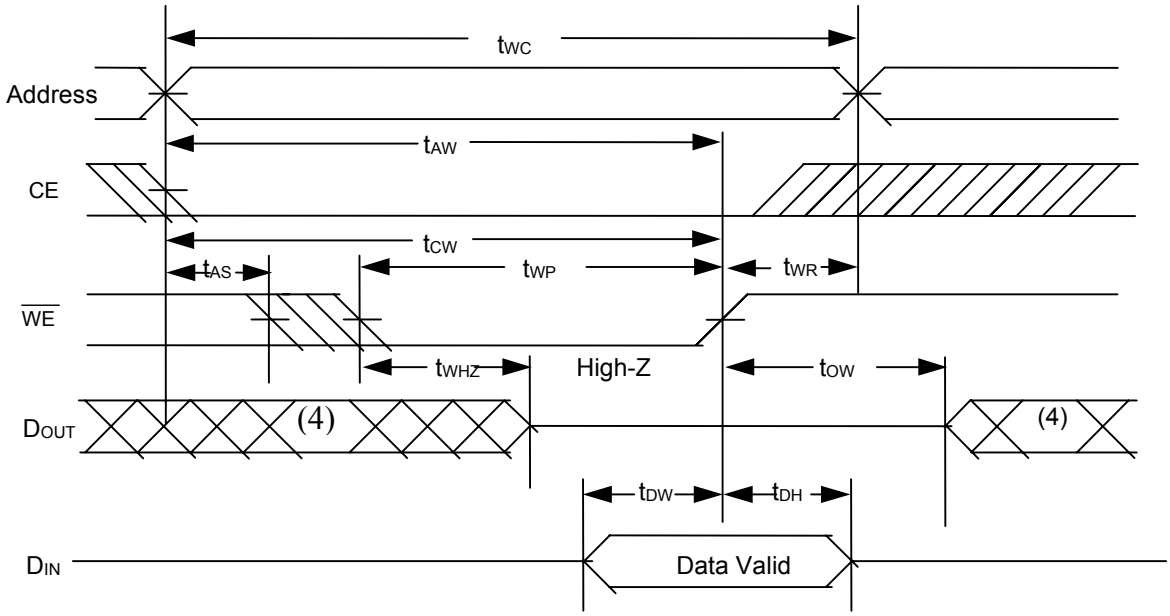
READ CYCLE 2 ($\overline{CE}$ and $\overline{OE}$ Controlled) (1,3,5,6)



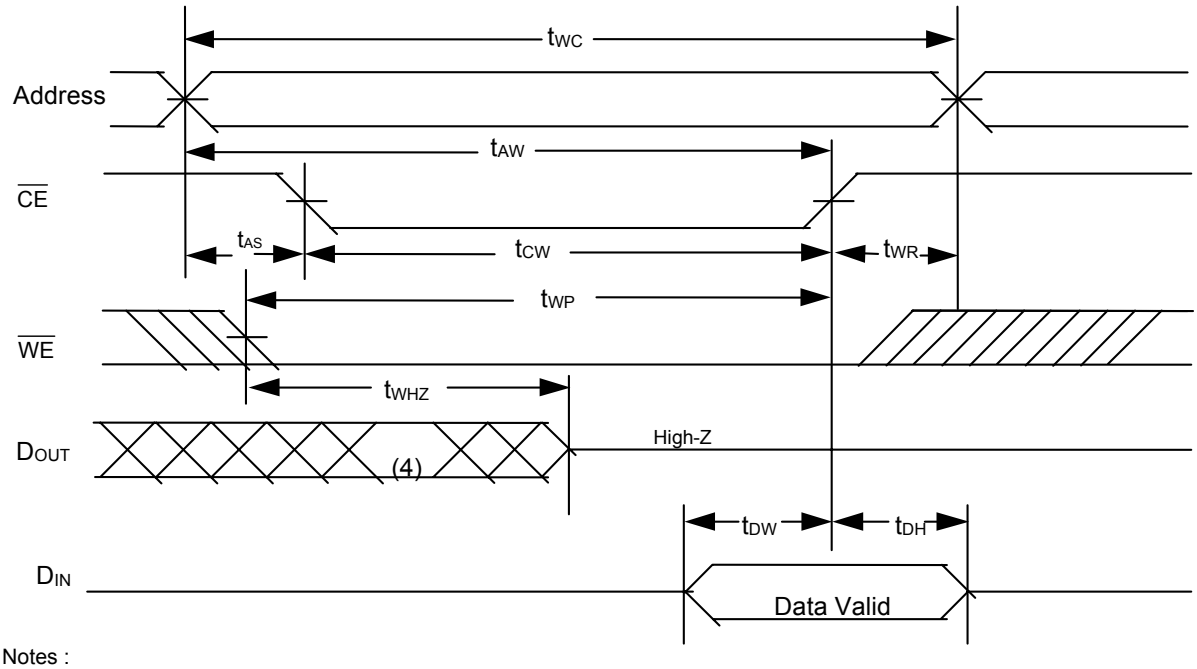
Notes :

1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected $\overline{CE}$ =V_{IL}.
3. Address must be valid prior to or coincident with $\overline{CE}$ transition; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
6. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ}, t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5)



WRITE CYCLE 2 ($\overline{CE}$ Controlled) (1,2,5)

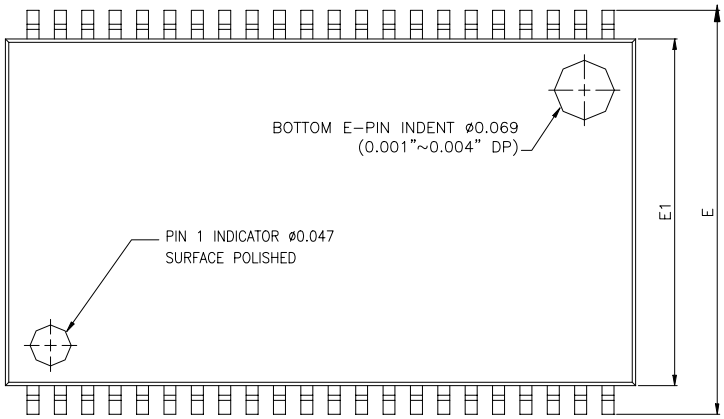


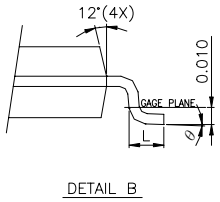
Notes :

1. $\overline{WE}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$.
3. During a $\overline{WE}$ controlled with write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input singals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after $\overline{WE}$ LOW transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

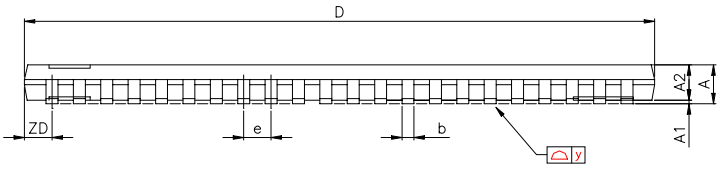
PACKAGE OUTLINE DIMENSION

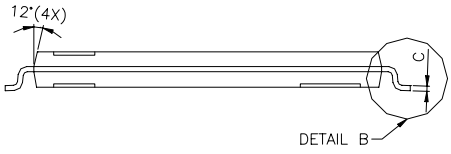
44pin 400mil TSOP-Ⅱ Package Outline Dimension





DETAIL B





1. CONTROLLING DIMENSION: INCH
2. LEAD FRAME MATERIAL: ALLOY 42
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, THE BAR BURRS AND GATE BURRS.MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH, INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALLBE 0.003"[0.008mm] TOTAL IN EXCEED OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE: ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT: JEDEC SPEC. MS-024

SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX.	MIN.	NOM.	MAX.
A	1.00	-	1.20	0.039	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	0.35	0.45	0.012	0.014	0.018
c	0.12	-	0.21	0.0047	-	0.083
D	18.313	18.415	18.517	0.721	0.725	0.728
E	11.854	11.836	11.838	0.460	0.466	0.470
E1	10.058	10.180	10.282	0.398	0.400	0.404
e	-	0.800	-	-	0.0315	-
L	0.40	0.50	0.60	0.0157	0.020	0.0236
2D	-	0.805	-	-	0.0317	-
y	0.00	-	0.076	0.000	-	0.003
ϴ	0^o	-	5^o	0^o	-	5^o

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	PACKAGE
UT61L5128MC-10	10	44 PIN TSOP-Ⅱ
UT61L5128MC-12	12	44 PIN TSOP-Ⅱ
UT61L5128MC-15	15	44 PIN TSOP-Ⅱ

REVISION HISTORY

REVISION	DESCRIPTION	DATE
Preliminary Rev. 0.1	Original.	Jun 5, 2001
Rev.1.0	1. Add test condition for $I_{SB.}$ 2. Add note to Vcc for access time=10ns.	Jun 23,2001