



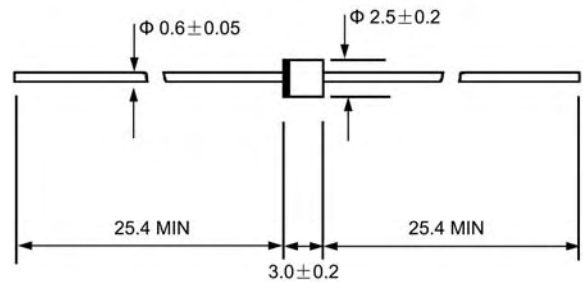
## Features

- ◇ Low cost
- ◇ Glass passivated junction
- ◇ Low leakage
- ◇ Low forward voltage drop
- ◇ High current capability
- ◇ Easily cleaned with Freon, Alcohol, Isopropanol and similar solvents
- ◇ The plastic material carries U/L recognition 94V-0

## Mechanical Data

- ◇ Case: JEDEC R--1, molded plastic
- ◇ Polarity: Color band denotes cathode
- ◇ Weight: 0.007 ounces, 0.20 grams
- ◇ Mounting position: Any

R - 1



Dimensions in millimeters

## MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Ratings at 25°C ambient temperature unless otherwise specified.

Single phase, half wave, 60 Hz, resistive or inductive load. For capacitive load, derate by 20%.

		1F1G	1F2G	1F3G	1F4G	1F5G	1F6G	1F7G	UNITS
Maximum recurrent peak reverse voltage	$V_{RRM}$	50	100	200	400	600	800	1000	V
Maximum RMS voltage	$V_{RMS}$	35	70	140	280	420	560	700	V
Maximum DC blocking voltage	$V_{DC}$	50	100	200	400	600	800	1000	V
Maximum average forward rectified current 9.5mm lead length, @ $T_A=75^\circ\text{C}$	$I_{F(AV)}$	1.0							A
Peak forward surge current 8.3ms single half-sine-wave superimposed on rated load @ $T_J=125^\circ\text{C}$	$I_{FSM}$	25.0							A
Maximum instantaneous forward voltage @1.0 A	$V_F$	1.3							V
Maximum reverse current @ $T_A=25^\circ\text{C}$ at rated DC blocking voltage @ $T_A=100^\circ\text{C}$	$I_R$	5.0 100.0							$\mu\text{A}$
Maximum reverse recovery time (Note1)	$t_{rr}$	150			250	500			ns
Typical junction capacitance (Note2)	$C_J$	12							pF
Typical thermal resistance (Note3)	$R_{\theta JA}$	55							$^\circ\text{C/W}$
Operating junction temperature range	$T_J$	- 55---- +150							$^\circ\text{C}$
Storage temperature range	$T_{STG}$	- 55---- + 150							$^\circ\text{C}$

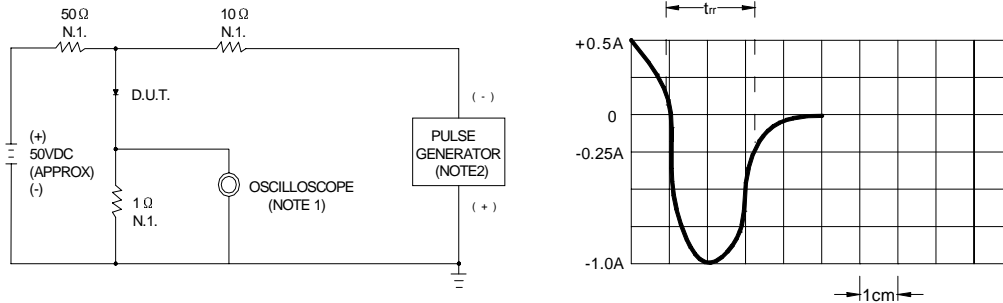
NOTE:1. Measured with  $I_F=0.5\text{A}$ ,  $I_R=1\text{A}$ ,  $I_{rr}=0.25\text{A}$ .

2. Measured at 1.0MHz and applied reverse voltage of 4.0V DC.

3. Thermal resistance from junction to ambient.

## Ratings AND Characteristic Curves

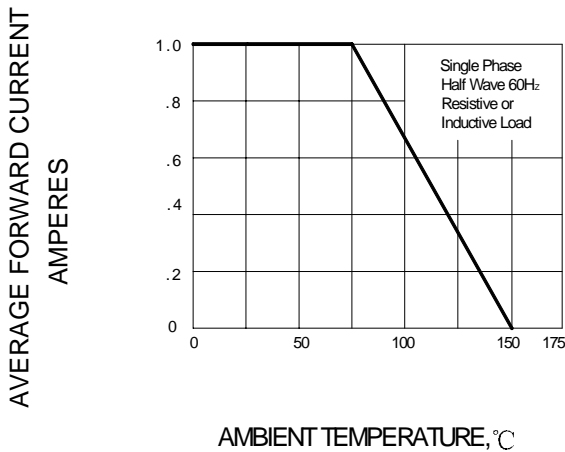
**FIG.1 – REVERSE RECOVERY TIME CHARACTERISTIC AND TEST CIRCUIT DIAGRAM**



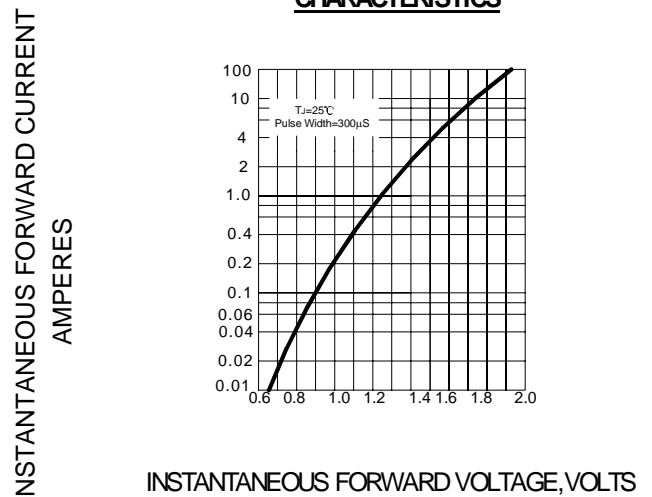
NOTES: 1. RISE TIME = 7ns MAX. INPUT IMPEDANCE =  $1M\Omega, 22pF$   
 2. RISE TIME = 10ns MAX. SOURCE IMPEDANCE =  $50\Omega$

SET TIME BASE FOR 50/100 ns/cm

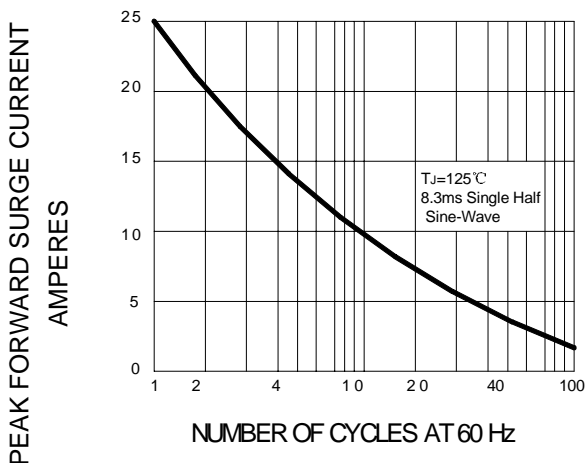
**FIG.2 – TYPICAL FORWARD CURRENT DERATING CURVE**



**FIG.3 – TYPICAL FORWARD CHARACTERISTICS**



**FIG.4 – PEAK FORWARD SURGE CURRENT**



**FIG.5 – TYPICAL JUNCTION CAPACITANCE**

