2ED2304S06F

650 V Half Bridge Gate Driver with Integrated Bootstrap Diode (BSD)

Features

- Infineon thin-film-SOI-technology
- Fully operational to +650 V
- Floating channel designed for bootstrap operation
- Output source/sink current capability +0.36 A/-0.7 A
- Integrated Ultra-fast, low $R_{DS(ON)}$ Bootstrap Diode
- Tolerant to negative transient voltage up to -100 V (Pulse width is up 300 ns) given by SOI-technology
- 10 ns typ., 60 ns max. propagation delay matching
- dV/dt immune ±50 V
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- Integrated dead-time with interlocking function
- 3.3 V, 5 V and 15 V input logic compatible
- RoHS compliant

Product summary

V_{OFFSET}	= 670 V max.
$I_{O+/-}$ (typ.)	= 0.36 A/0.7 A
V_{OUT}	= 10 V – 17.5 V
Delay Matching	= 60 ns max.
Internal deadtime	= 75 ns
$t_{on/off}$ (typ.)	= 310 ns/300 ns

Package

DSO-8

Potential applications

- Motor drives, General purpose inverters
- Refrigeration compressors
- Half-bridge and full-bridge converters in offline AC-DC power supplies for telecom and lighting

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The 2ED2304S06F is a 650-V half-bridge gate driver. Its Infineon thin-film-SOI technology provides excellent ruggedness and noise immunity. The Schmitt trigger logic inputs are compatible with standard CMOS or LSTTL logic down to 3.3 V. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction with built in interlock lock logic to prevent shoot-through. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 650 V.

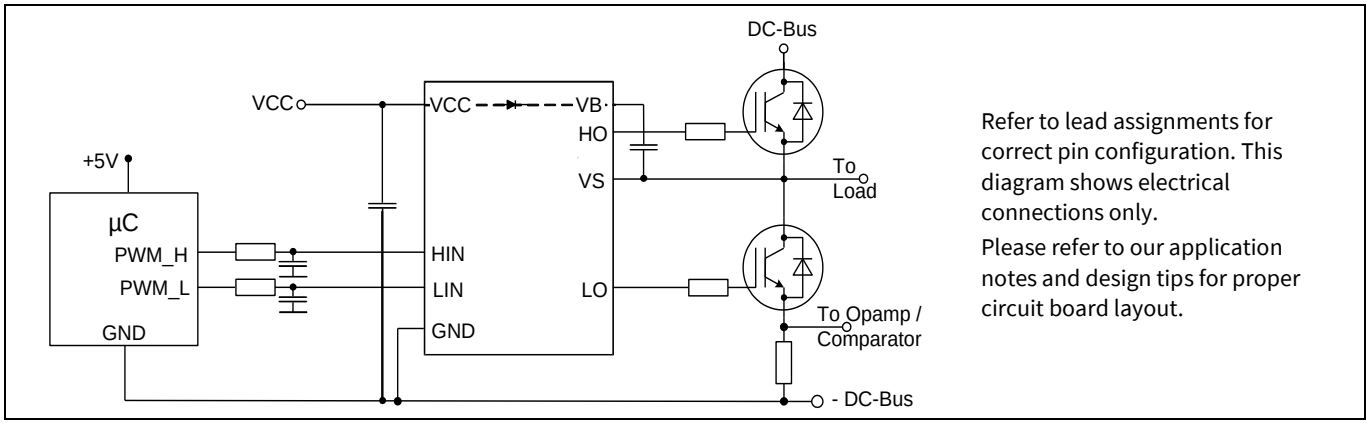


Figure 1 Typical application diagram

Ordering information

Base Part Number	Package	Standard Pack		Orderable Part Number
		Form	Quantity	
2ED2304S06F	PG-DSO-8	Tape and Reel	2500	2ED2304S06FXUMA1

Table of contents

1 Block diagram

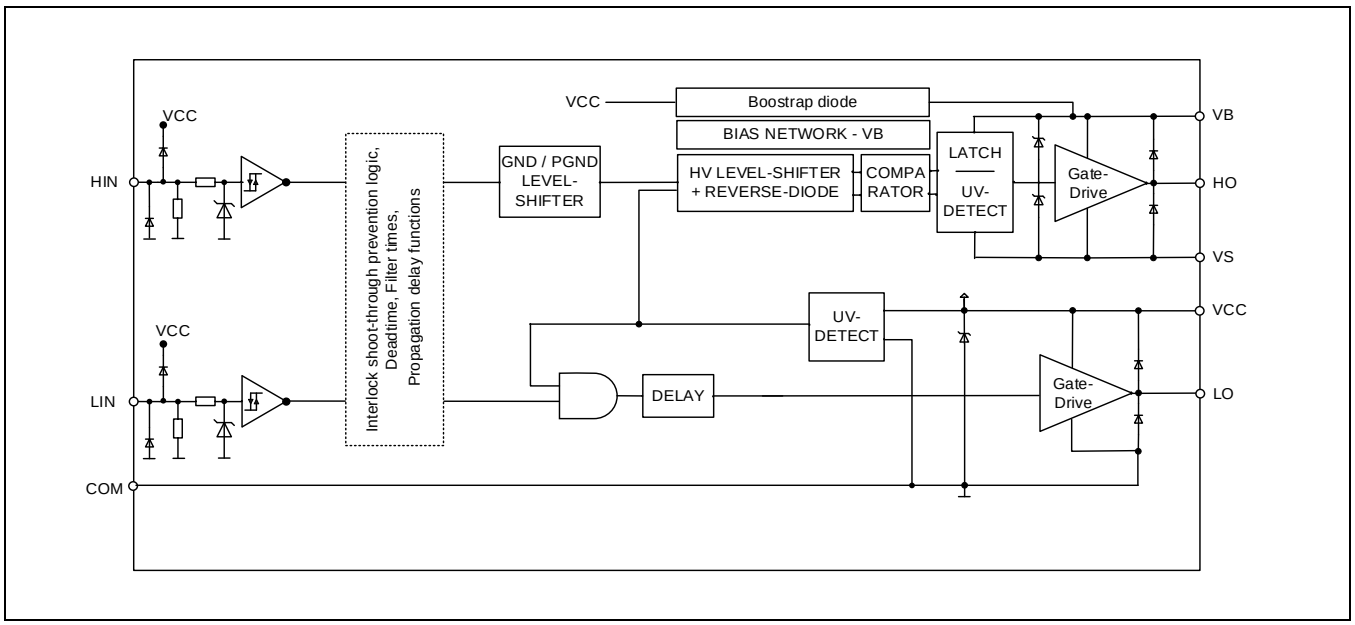


Figure 2 Functional block diagram

2 Lead definitions

Table 1 2ED2304S06F lead definitions

Pin no.	Name	Function
1	LIN	Logic input for low-side gate driver output (LO), in phase. Schmitt trigger inputs with hysteresis and pull down
2	HIN	Logic input for high-side gate driver output (HO), in phase. Schmitt trigger inputs with hysteresis and pull down
3	VCC	Low-side and logic supply voltage
4	COM	Low-side gate drive return
5	LO	Low-side driver output
6	VS	High voltage floating supply return
7	HO	High-side driver output
8	VB	High-side gate drive floating supply

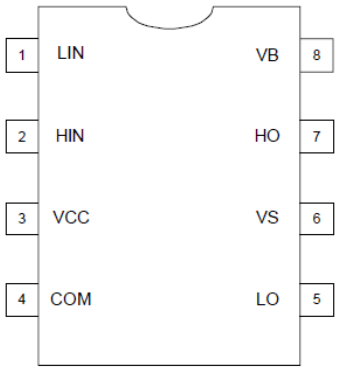


Figure 3 2ED2304S06F lead assignments PG-DSO-8 (top view)

3 Electrical parameters

3.1 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Table 2 Absolute maximum ratings

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating well supply voltage[1]	V_{CC} – 6	670	V
	High-side floating well supply voltage (tp < 300 ns)[1]	V_{CC} – 100	—	
V_S	High-side floating well supply return voltage	V_{CC} –V_{BS} – 6	650	
	High-side floating well supply return voltage (tp < 300 ns)[1]	V_{CC} –V_{BS} – 100	—	
V_{HO}	Floating gate drive output voltage	V_S – 0.5	V_B + 0.5	
V_{BS}	Floating gate drive voltage supply voltage	-1	20	
V_{CC}	Low side supply voltage	-1	20	
V_{LO}	Low-side output voltage	-0.5	V_{CC} + 0.5	
V_{IN}	Logic input voltage	-0.5	V_{CC} + 0.5	
dV_S/dt	Allowable V_S offset supply transient relative to GND[2]	—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25$ °C	—	0.6	W
Rth_{JA}	Thermal resistance, junction to ambient	—	195	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-40	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

3.2 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The offset rating is tested with supplies of (V_{CC} – COM) = (V_B – V_S) = 15 V.

Table 3 Recommended operating conditions

Symbol	Definition	Min	Max	Units
V_B	High-side floating well supply voltage	V_S + 10	V_S + 17.5	V
V_S	High-side floating well supply offset voltage[3]	V_{CC} – V_{BS} -1	650	
V_{HO}	Floating gate drive output voltage	10	V_{BS}	
V_{BS}	High-side supply voltage	10	17.5	
V_{CC}	Low-side supply voltage	10	17.5	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage[4]	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C
t_{IN}	Pulse width for ON and OFF[5]	0.3	—	µs

[1] In case $V_{CC} > V_B$ there is an additional power dissipation in the internal bootstrap diode between pins V_{CC} and V_B in case of activated bootstrap diode. Insensivity to negative transient not subject to production test. Verified by design/characterization.

[2] Not subject to production test, verified by characterization.

[3] Logic operation for V_S of -8 V to +600 V.

[4] All input pins (HIN, LIN) are internally clamped

[5] Input pulses may not be transmitted properly in case of LIN/HIN below 0.3 µs

3.3 Static electrical characteristics

(V_{CC} – COM) = (V_B – V_S) = 15 V, and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to GND and are applicable to the respective input leads: HIN and LIN. The V_O and I_O parameters are referenced to COM/VS and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

Table 4 Static electrical characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	8.3	9.1	9.9	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.5	8.3	9.0		
V_{BSUVHY}	V_{BS} supply undervoltage hysteresis	0.5	0.9	—		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8.3	9.1	9.9		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.5	8.3	9.0		
V_{CCUVHY}	V_{CC} supply undervoltage hysteresis	0.5	0.9	—		
I_{LK}	High-side floating well offset supply leakage	—	1	12.5	µA	V_B = V_S = 600 V
I_{LK}	High-side floating well offset supply leakage[1]	—	10	—		T_J = 125 °C, V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	—	170	300		
I_{QCC}	Quiescent V_{CC} supply current	—	300	600		
V_{OH}	High level output voltage drop, V_{BIAS}-V_O	—	0.45	1	V	I_O = 20 mA
V_{OL}	Low level output voltage drop, V_O	—	0.13	0.3		
I_{o+}	Peak output current turn-on[1]	—	360	—	mA	V_O = 0 V PW = 10 µs
I_{o+mean}	Mean output current from 3 V (20%) to 6 V (40%)	180	230	—		C_L = 22 nF
I_{o-}	Peak output current turn-off[1]	—	700	—		V_O = 15 V PW = 10 µs
I_{o-mean}	Mean output current from 12 V (80%) to 9 V (60%)	390	480	—		C_L = 22 nF
V_{IH}	Logic “1” input voltage	1.7	2.1	2.4	V	
V_{IL}	Logic “0” input voltage	0.7	0.9	1.1		
I_{IN+}	Input bias current (HO = High)	15	35	60	µA	V_{IN} = 3.3 V
I_{IN-}	Input bias current (HO = Low)	—	0	—		V_{IN} = 0 V
V_{FBSD}	Bootstrap diode forward voltage between Vcc and V_B	—	1	1.2	V	IF=0.3 mA
I_{FBSD}	Bootstrap diode forward current between Vcc and V_B	30	55	—	mA	V_{CC}-V_B=4 V
R_{BSD}	Bootstrap diode resistance	20	36	55	Ω	V_{F1}=4 V, V_{F2}=5 V

[1] Not subjected to production test, verified by characterization.

3.4 Dynamic electrical characteristics

V_{CC} = V_{BS}= 15 V, V_{SS} = COM, T_A = 25°C and C_L = 1000 pF unless otherwise specified.

Table 5 Dynamic electrical characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{ON}	Turn-on propagation delay	210	310	460	ns	$V_{LIN/HIN}$ = 0 or 3.3 V
t_{OFF}	Turn-off propagation delay	200	300	440		
t_R	Turn-on rise time	—	48	80		$V_{LIN/HIN}$ = 0 or 3.3 V C_L = 1 nF
t_F	Turn-off fall time	—	24	40		
t_{FILIN}	Input filter time	100	150	250		$V_{LIN/HIN}$ = 0 & 3.3 V
MT	Delay matching time (HS & LS turn-on/off)	—	10	60		external dead time > 500 ns
DT	Dead time	30	75	140		$V_{LIN/HIN}$ = 0 & 3.3 V
MDT	Dead time matching time	—	10	50		ext. dead time 0 ns

4 Input/output logic diagram

The relationships between the input and output signals of the 2ED2304S06F is illustrated below in Figure 4. Note that the input stage has integrated interlock logic to prevent shoot-through operation of the outputs.

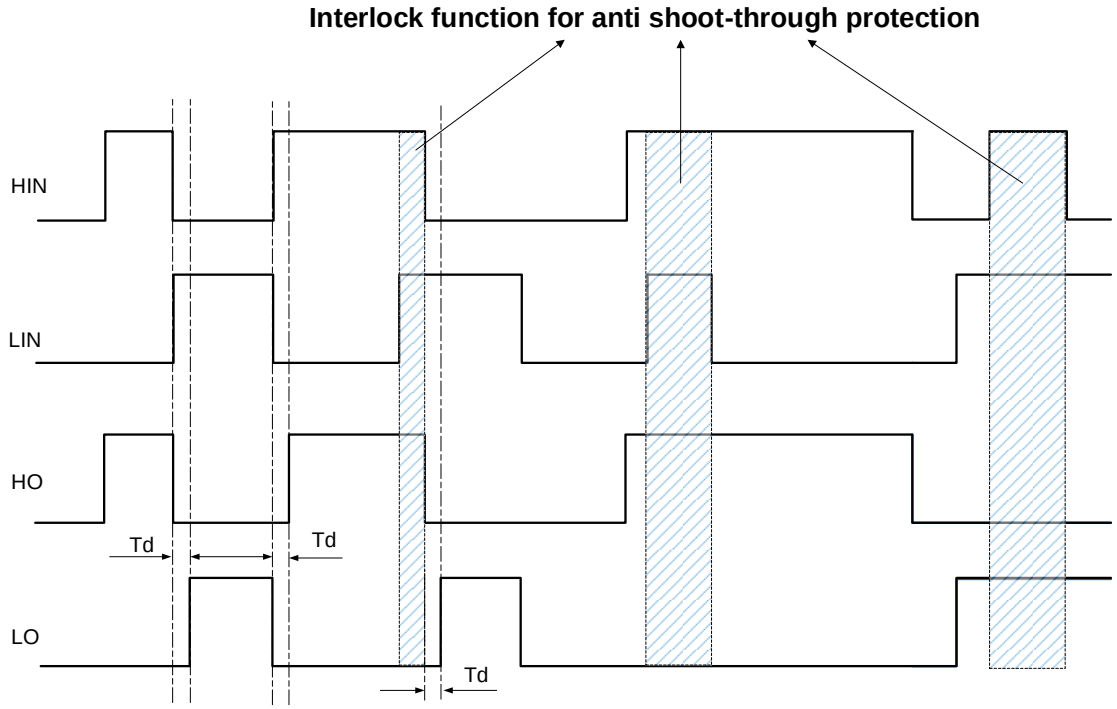


Figure 4 Input/output logic diagram

5 Tolerant to negative transient voltage on VS pin (-VS)

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical three phase inverter circuit is shown in Figure 5; here we define the power switches and diodes of the inverter.

If the high-side switch (e.g., the IGBT Q1 in Figure 6 and Figure 7) switches off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1}, swings from the positive DC bus voltage to the negative DC bus voltage.

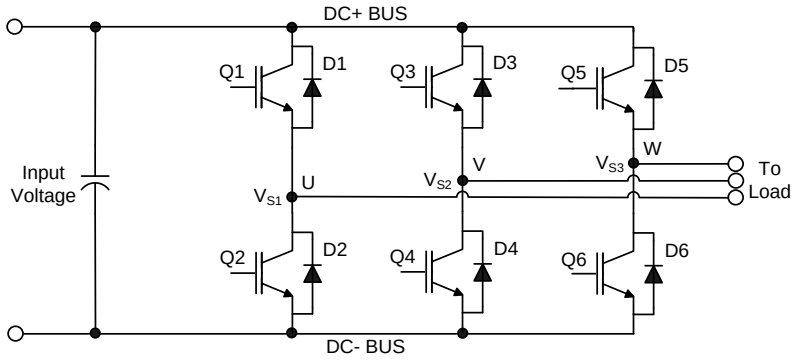


Figure 5 Three phase inverter

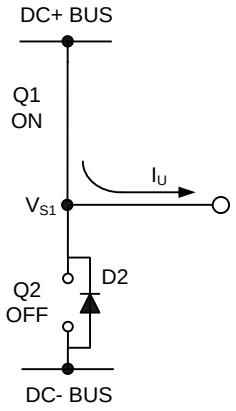


Figure 6 Q1 conducting

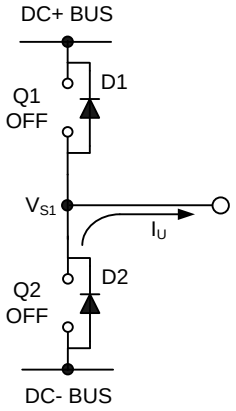


Figure 7 D2 conducting

Also when the V phase current flows from the inductive load back to the inverter (see Figure 8 and Figure 9), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2}, swings from the positive DC bus voltage to the negative DC bus voltage.

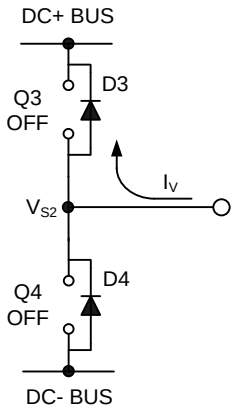


Figure 8 D3 conducting

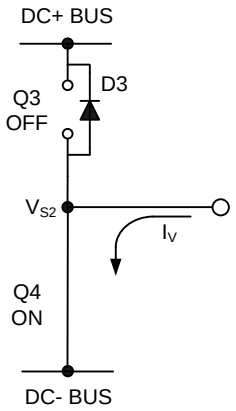


Figure 9 Q4 conducting

However, in a real inverter circuit the V_S voltage swing does not stop at the level of the negative DC bus but instead swings below the level of the negative DC bus. This undershoot voltage is called “negative transient voltage”.

The circuit shown in Figure 10 depicts one leg of the three phase inverter; Figure 11 and Figure 12 show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the VS pin).

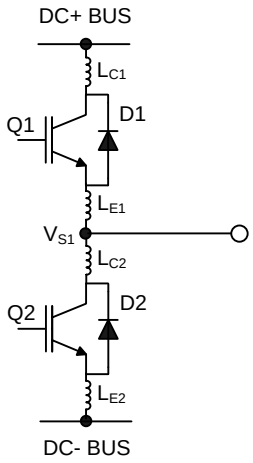


Figure 10 Parasitic Elements

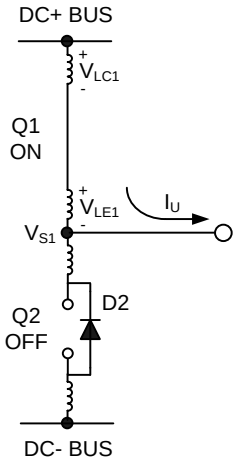


Figure 11 VS positive

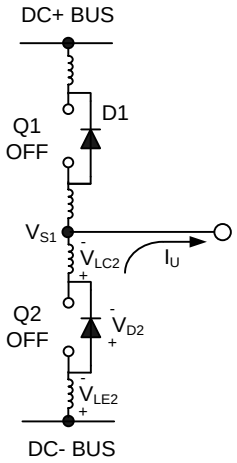


Figure 12 VS negative

In a typical motor drive system, dV/dt is typically designed to be in the range of 3-5 V/ns. The negative transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

Infineon's HVICs have been designed for the robustness required in many of today's demanding applications. An indication of the 2ED2304S06F's robustness can be seen in Figure 13, where the 2ED2304S06F Safe Operating Area is shown at V_{BS}=15 V based on repetitive negative transient voltage spikes. A negative transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; viceversa unwanted functional anomalies or permanent damage to the IC do not appear if negative VS transients fall inside the SOA.

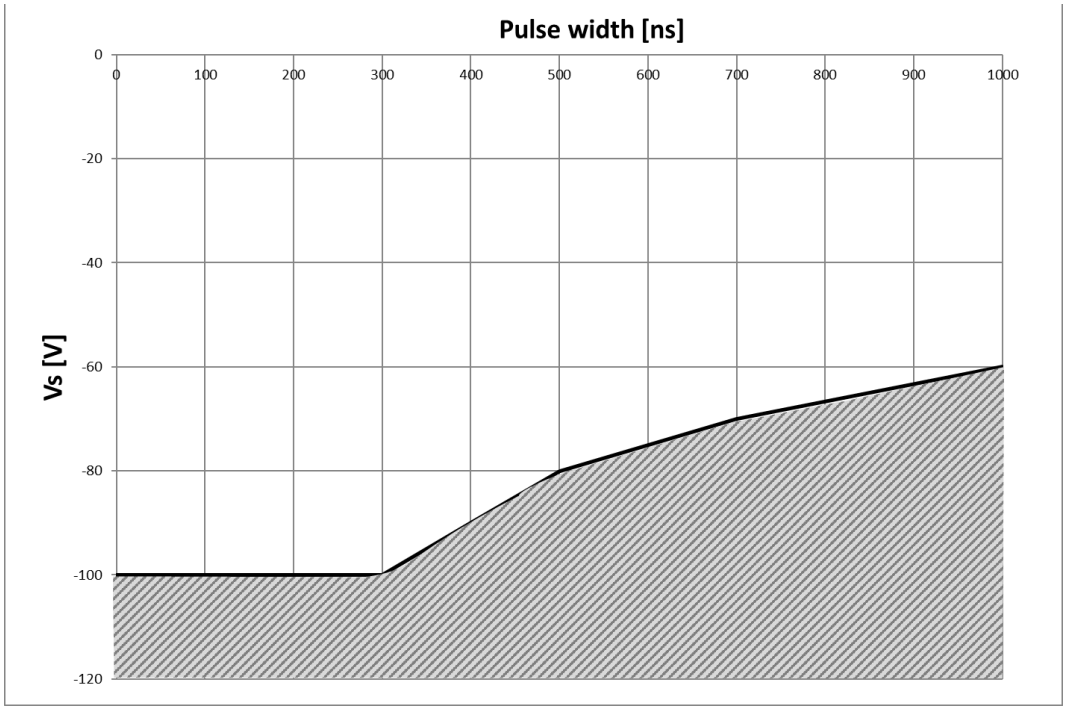
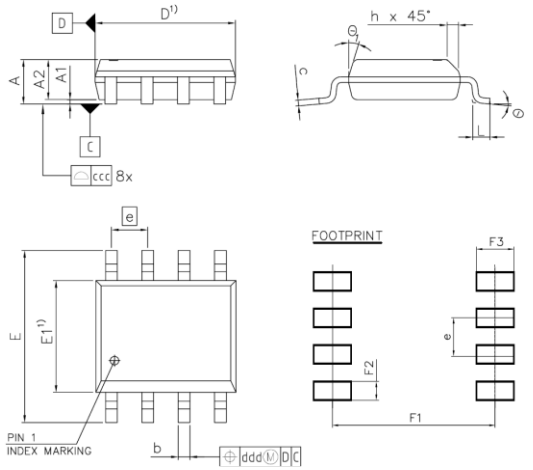


Figure 13 Negative transient voltage SOA on VS pin for 2ED2304S06F @ VBS=15 V

Even though the 2ED2304S06F has been shown to be able to handle these large negative transient voltage conditions, it is highly recommended that the circuit designer always limit the negative transient voltage on VS pin as much as possible by careful PCB layout and component use.

6 Package information DSO-8



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	0°	8°	0°	8°
Θ_1	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

Max. reflow solder temperature: 265°C acc. JEDEC
Max. wave solder temperature: 245°C acc. JEDEC

Figure 14 Package outline PG-DSO-8

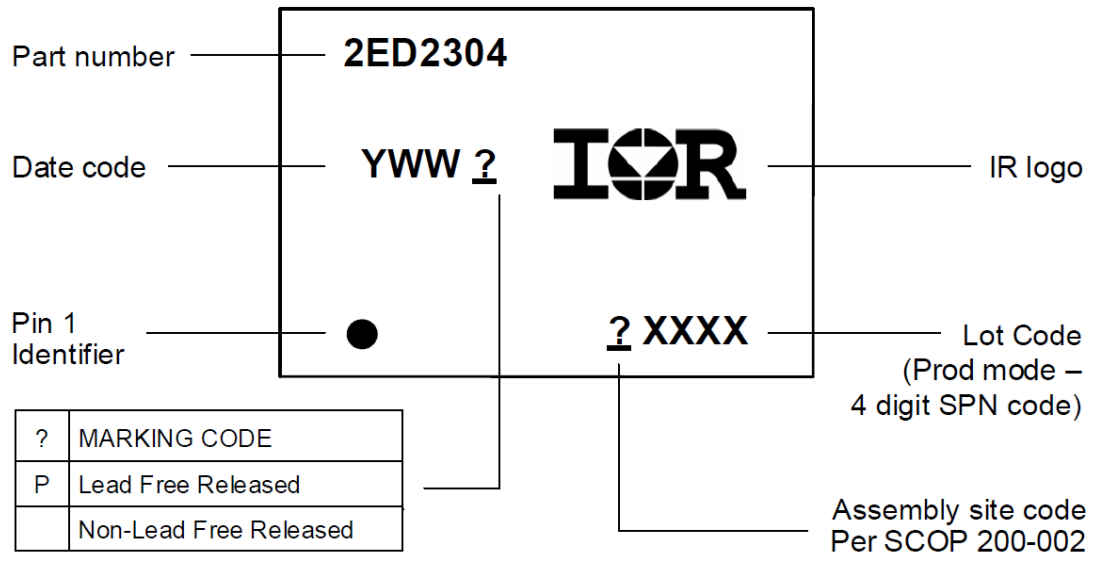
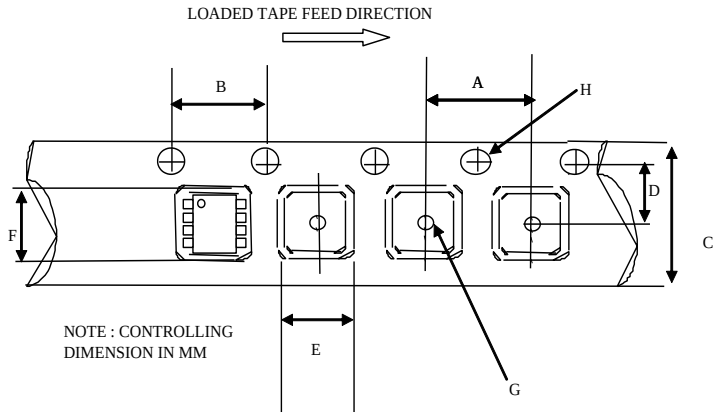
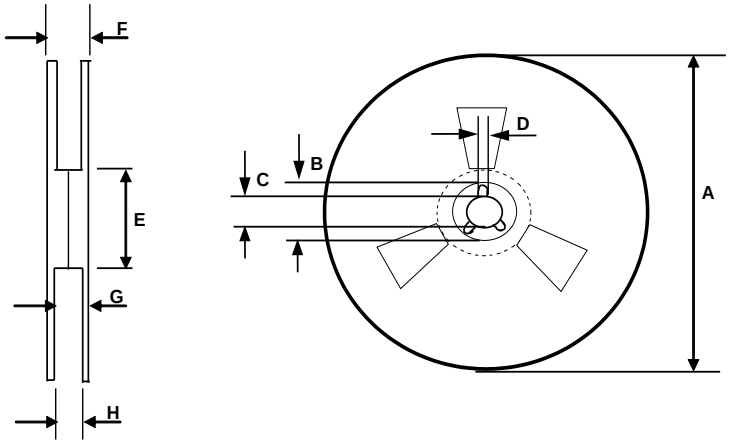


Figure 15 Marking information PG-DSO-8 (2ED2304S06F)



CARRIER TAPE DIMENSION FOR 8SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Figure 16 Tape and reel details PG-DSO-8

7 Qualification information[1]

Table 6 Qualification information

Qualification level		Industrial[2] Note: This family of Ics has passed JEDEC's Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture sensitivity level		DSO-8	MSL3[3], 260°C (per IPC/JEDEC J-STD-020)
ESD	Charged device model	Class C3 (> 1.0 kV) (per JESD22-C101)	
	Human body model	Class 2 (per JEDEC standard JESD22-A114)	
IC latch-up test		Class II Level A (per JESD78)	
RoHS compliant		Yes	

8 Related products

Table 7

Product	Description
Gate Driver Ics	
6EDL04I06 / 6EDL04N06	600 V, 3 phase level shift thin-film SOI gate driver with integrated high speed, low $R_{DS(ON)}$ bootstrap diodes with over-current protection (OCP), 240/420 mA source/sink current drive, Fault reporting, and Enable for MOSFET or IGBT switches.
2EDL23I06 / 2EDL23N06	600 V, Half-bridge thin-film SOI level shift gate driver with integrated high speed, low $R_{DS(ON)}$ bootstrap diode, with over-current protection (OCP), 2.3/2.8 A source/sink current driver, and one pin Enable/Fault function for MOSFET or IGBT switches.
Power Switches	
IKD04N60R / RF	600 V TRENCHSTOP™ IGBT with integrated diode in PG-TO252-3 package
IKD06N65ET6	650 V TRENCHSTOP™ IGBT with integrated diode in DPAK
IPD65R950CFD	650 V CoolMOS CFD2 with integrated fast body diode in DPAK
IPN50R950CE	500 V CoolMOS CE Superjunction MOSFET in PG-SOT223 package
iMOTION™ Controllers	
IRMCK099	iMOTION™ Motor control IC for variable speed drives utilizing sensor-less Field Oriented Control (FOC) for Permanent Magnet Synchronous Motors (PMSM).
IMC101T	High performance Motor Control IC for variable speed drives based on field oriented control (FOC) of permanent magnet synchronous motors (PMSM).

[1] Qualification standards can be found at Infineon's web site www.infineon.com
[2] Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.
[3] Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon sales representative for further information.

Revision history

Document version	Date of release	Description of changes
1.0	2016-07-12	Preliminary datasheet
2.0	2018-02-07	First Release Version
2.1	2018-07-13	Updated the marking information
2.11	2018-09-12	Deleting typo
2.2	2018-10-26	Adding negative VS information
2.3	2018-11-19	Updated ESD HBM information
2.4	2019-01-24	Updated Chapter 4 Tolerant to negative transient voltage on VS pin
2.5	2019-11-06	Add input/output logic diagram
2.6	2020-07-07	IC latch-up test per JESD78
2.7	2021-05-24	Updated ordering information
2.8	2021-10-04	Updated the block diagram and text with interlock logic comment
2.9	2022-05-12	Remove I_{FBSD} maximum spec

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2021-10-04

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie") .

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

Please note that this product is not qualified according to the AEC Q100 or AEC Q101 documents of the Automotive Electronics Council.

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.