MOTOROLA Semiconductors

2N6576
2N6577
2N6578

NPN SILICON POWER DARLINGTON TRANSISTORS

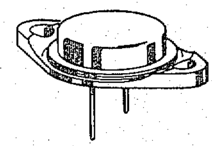
General-purpose EpiBase power darlington transistors, suitable for linear and switching applications.

- Replacement for 2N3055 and Driver
- High Gain Darlington Performance
- Built-In Diode Protection for Reverse Polarity Protection
- Can Be Driven from Low-Level Logic
- Popular Voltage Range
- Operating Range — –65 to +200°C

15 AMPERE POWER TRANSISTORS

NPN SILICON DARLINGTON

60, 90, 120 VOLTS
120 WATTS



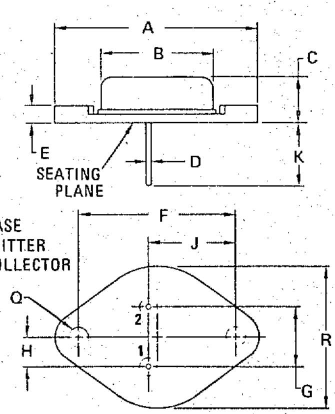
*MAXIMUM RATINGS

Rating	Symbol	2N6576	2N6577	2N6578	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	60	90	120	Vdc
Collector-Base Voltage	V_{CB}	60	90	120	Vdc
Emitter-Base Voltage	V_{EB}	← 7.0 →			Vdc
Collector Current — Continuous — Peak	I_C	← 15 → ← 30 →			Adc
Base Current — Continuous — Peak	I_B	← 0.25 → ← 0.50 →			Adc
Emitter Current — Continuous — Peak	I_E	← 15.25 → ← 30.5 →			Adc
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	← 120 → ← 0.685 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.46	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/16" from Case for 10s.	T_L	265	°C

*Indicates JEDEC Registered Data

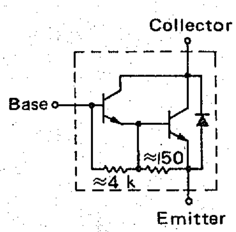


STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-03
TO-3

DARLINGTON SCHEMATIC



DS 3355
(Replaces ADI 327)

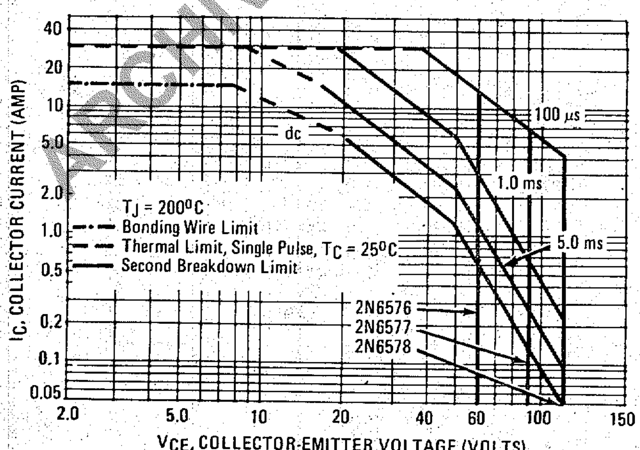
*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage(1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$			Vdc
2N6576		60	–	
2N6577		90	–	
2N6578		120	–	
Collector Cutoff Current (V_{CE} = Rated Value)	I_{CEO}	–	1.0	mAdc
Collector Cutoff Current (V_{CER} = Rated $V_{CEO(sus)}$ Value, R_{BE} = 10 kΩ, T_C = 150°C)	I_{CER}	–	5.0	mAdc
Collector Cutoff Current V_{CEX} = Rated $V_{CEO(sus)}$ Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	5.0	mAdc
Collector Cutoff Current (V_{CB} = Rated Value)	I_{CBO}	–	0.5	mAdc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			–
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)		100	–	
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)		500	5,000	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)		2000	20,000	
(I_C = 0.4 Adc, V_{CE} = 3.0 Vdc)		200	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 15 Adc, I_B = 0.15 Adc)		–	4.0	
(I_C = 10 Adc, I_B = 0.1 Adc)		–	2.8	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 15 Adc, I_B = 0.15 Adc)		–	4.5	
(I_C = 10 Adc, I_B = 0.1 Adc)		–	3.5	
Collector-Emitter Diode Voltage Drop (I_{EC} = 15 Adc)	V_F	–	4.5	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common-Emitter Small-Signal Short-Circuit Current Transfer Ratio (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)	$\|h_{fe}\|$	10	200	–
SWITCHING CHARACTERISTICS				
RESISTIVE LOAD (Figure 2)				
Delay Time (V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = 0.1 Adc, t_p = 300 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.15	μs
Rise Time (V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = 0.1 Adc, t_p = 300 μs, Duty Cycle ≤ 2.0%)	t_r	–	1.0	μs
Storage Time (V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 0.1 Adc, t_p = 300 μs, Duty Cycle ≤ 2.0%)	t_s	–	2.0	μs
Fall Time (V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 0.1 Adc, t_p = 300 μs, Duty Cycle ≤ 2.0%)	t_f	–	7.0	μs

*Indicates JEDEC Registered Data

(1) Pulse test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 – RATED FORWARD BIASED SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10%.

$T_{J(pk)}$ may be calculated from the data in Figure 7. At high case temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 — DC CURRENT GAIN

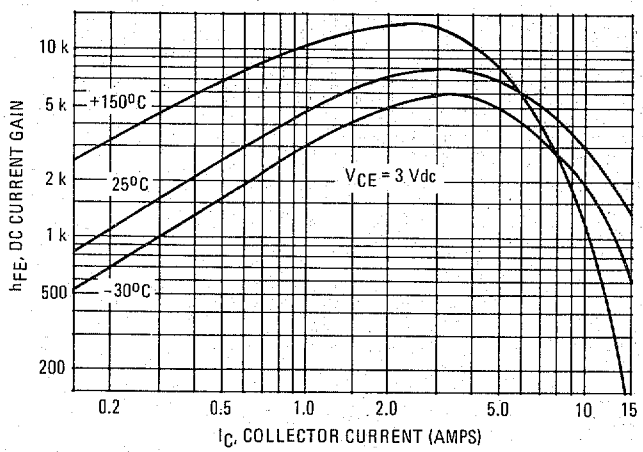


FIGURE 3 — COLLECTOR-SATURATION REGION

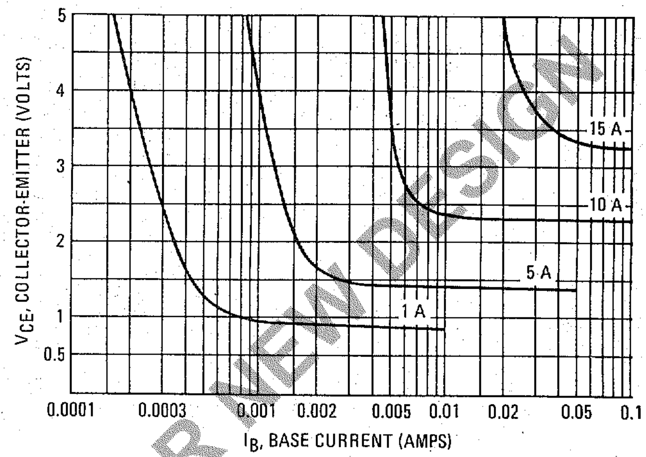


FIGURE 4 — COLLECTOR SATURATION VOLTAGE

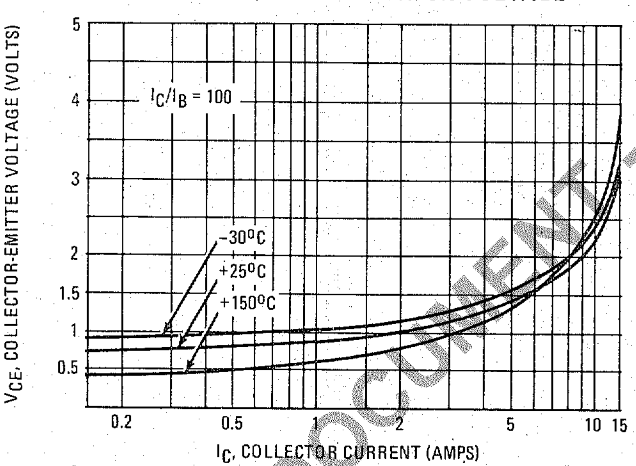


FIGURE 5 — BASE-EMITTER VOLTAGE

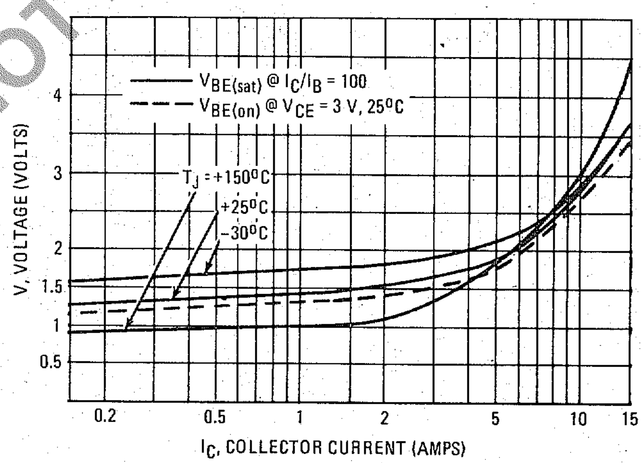


FIGURE 6 — THERMAL RESPONSE

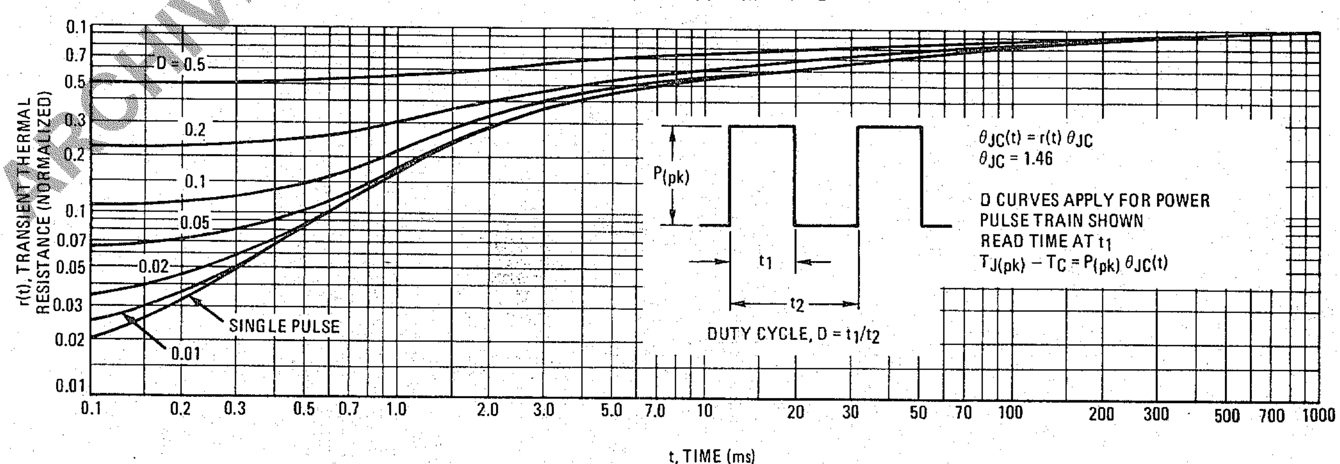
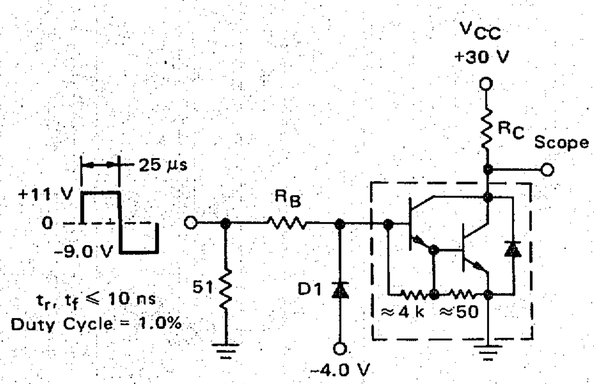


FIGURE 7 – SWITCHING TIMES TEST CIRCUIT



RB and RC Varied to Obtain Desired Current Levels
D1 Must be Fast Recovery Type, eg:

FIGURE 8 – SWITCHING TIMES

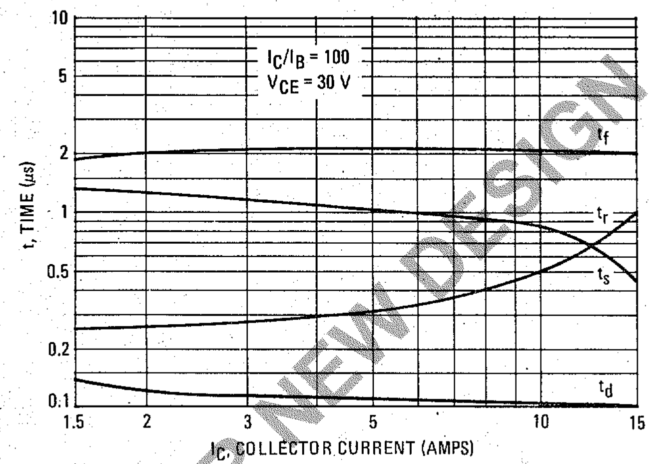


FIGURE 9 – COLLECTOR CUT-OFF REGION

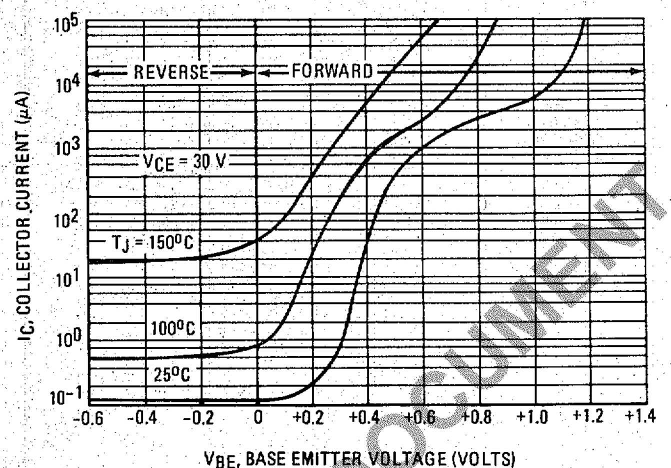


FIGURE 10 – CAPACITANCE

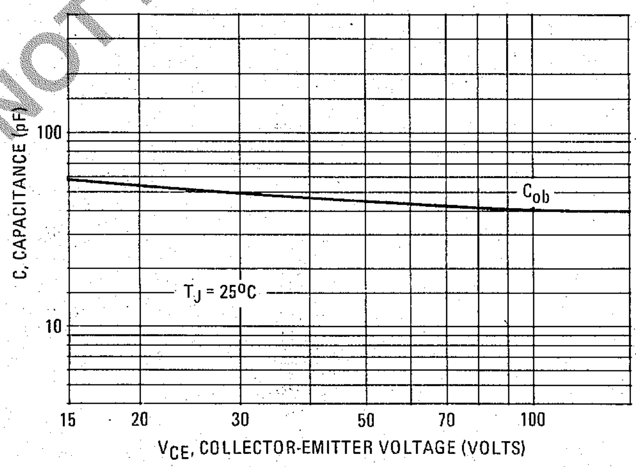


FIGURE 11 – COLLECTOR-EMITTER VOLTAGE