

## PNP SILICON POWER TRANSISTORS

...designed for the output stage of 25W to 35W AF power amplifier

### FEATURES:

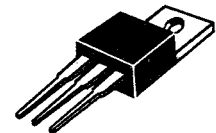
- \* Low Collector-Emitter Saturation Voltage  
 $V_{CE(sat)} = 2.0V(\text{Max}) @ I_C = 4.0A, I_B = 0.4A$
- \* DC Current Gain  
 $hFE = 40-320 @ I_C = 1.0A$
- \* Complementary to NPN 2SD613

**PNP  
2SB633**

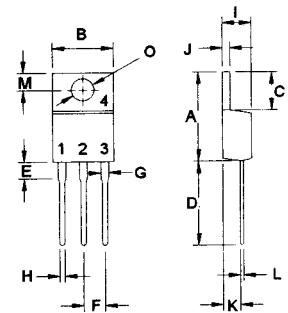
**6.0 AMPERE  
POWER  
TRANSISTORS  
85 VOLTS  
40 WATTS**

### MAXIMUM RATINGS

Characteristic	Symbol	2SB633	Unit
Collector-Emitter Voltage	$V_{CEO}$	85	V
Collector-Base Voltage	$V_{CBO}$	100	V
Emitter-Base Voltage	$V_{EBO}$	6.0	V
Collector Current - Continuous - Peak	$I_C$ $I_{CM}$	6.0 10	A
Base current	$I_B$	3.0	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40 0.32	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$



**TO-220**



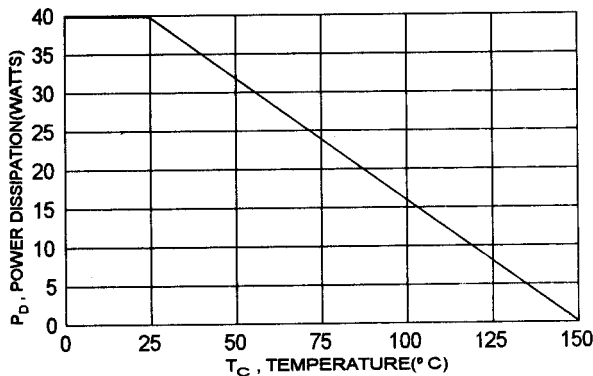
PIN 1.BASE  
2.COLLECTOR  
3.EMITTER  
4.COLLECTOR(CASE)

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case	$R_{\theta jc}$	3.125	$^\circ\text{C/W}$

DIM	MILLIMETERS	
	MIN	MAX
A	14.68	15.31
B	9.78	10.42
C	5.01	6.52
D	13.06	14.62
E	3.57	4.07
F	2.42	3.66
G	1.12	1.36
H	0.72	0.96
I	4.22	4.98
J	1.14	1.38
K	2.20	2.97
L	0.33	0.55
M	2.48	2.98
O	3.70	3.90

FIGURE -1 POWER DERATING



**ELECTRICAL CHARACTERISTICS (  $T_c = 25^\circ\text{C}$  unless otherwise noted )**

Characteristic	Symbol	Min	Max	Unit
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**OFF CHARACTERISTICS**

Collector-Emitter Breakdown Voltage ( $I_C = 50 \text{ mA}, I_B = 0$ )	$V_{(br)CEO}$	85		V
Collector-Base Breakdown Voltage ( $I_C = 5.0 \text{ mA}, I_E = 0$ )	$V_{(br)CBO}$	100		V
Emitter-Base Breakdown Voltage ( $I_E = 5.0 \text{ mA}, I_C = 0$ )	$V_{(br)EBO}$	6.0		V
Collector Cutoff Current ( $V_{CB} = 40 \text{ V}, I_E = 0$ )	$I_{CBO}$		100	$\mu\text{A}$
Emitter Cutoff Current ( $V_{EB} = 4.0 \text{ V}, I_B = 0$ )	$I_{EBO}$		100	$\mu\text{A}$

**ON CHARACTERISTICS (1)**

DC Current Gain ( $I_C = 1.0 \text{ A}, V_{CE} = 5.0 \text{ V}$ ) * ( $I_C = 3.0 \text{ A}, V_{CE} = 5.0 \text{ V}$ )	$h_{FE(2)}$ $h_{FE}$	40 20	320	
Collector-Emitter Saturation Voltage ( $I_C = 4.0 \text{ A}, I_B = 400 \text{ mA}$ )	$V_{CE(sat)}$		2.0	V
Base-Emitter On Voltage ( $I_C = 1.0 \text{ A}, V_{CE} = 5.0 \text{ V}$ )	$V_{BE(on)}$		1.5	V

**DYNAMIC CHARACTERISTICS**

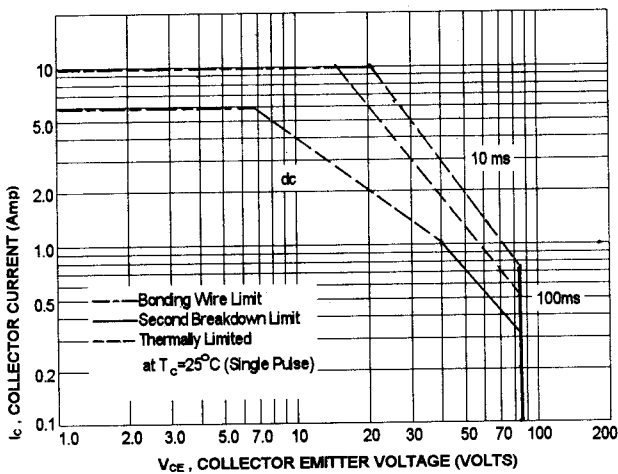
Current-Gain-Bandwidth Product ( $I_C = 1.0 \text{ A}, V_{CE} = 5.0 \text{ V}, f = 1.0 \text{ MHz}$ )	$f_T$	5.0		MHz
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(1) Pulse Test: Pulse Width = 300 $\mu$ s, Duty Cycle  $\leq$  2.0%

\*  $h_{FE(2)}$  Classification :

40	C	80	60	D	120	100	E	200	160	F	320
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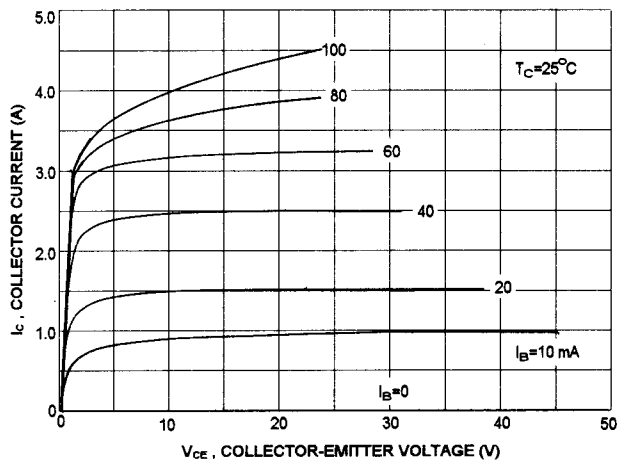
**ACTIVE-REGION SAFE OPERATING AREA (SOA)**



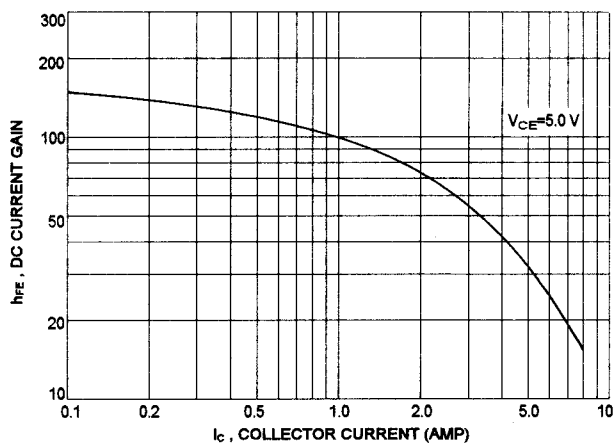
There are two limitation on the power handling ability of a transistor: average junction temperature and second breakdown safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate.

The data of SOA curve is base on  $T_{J(PK)} = 150^\circ\text{C}$ ;  $T_c$  is variable depending on conditions. second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(PK)} \leq 150^\circ\text{C}$ . At high case temperatures, thermal limitation will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

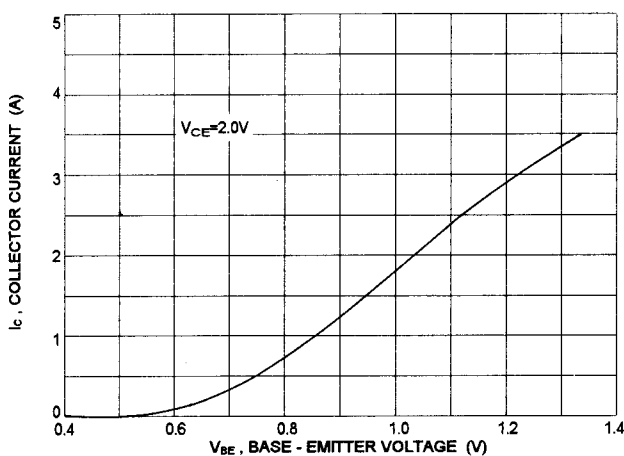
$I_c - V_{ce}$



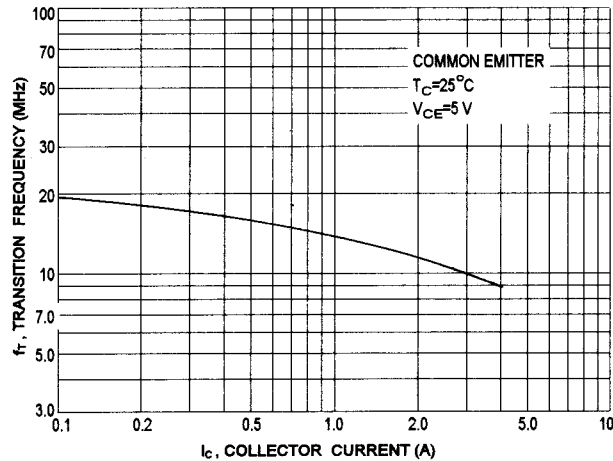
DC CURRENT GAIN



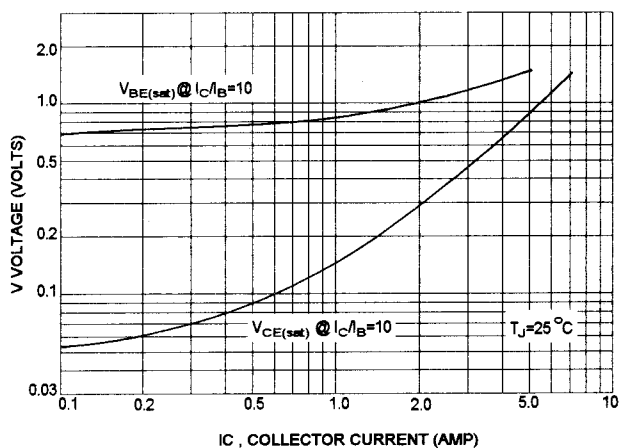
$I_c - V_{be}$



$f_T - I_c$



"ON" VOLTAGES



CAPACITANCES

