

# DATA SHEET

**74ABTL3205**

10-bit BTL transceiver with registers

Product specification

1995 Jun 16

# 10-bit BTL transceiver with registers

# 74ABTL3205

## FEATURES

- 10-bit BTL transceiver
- Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Controlled output ramp and multiple GND pins minimize ground bounce
- Tight output skew (0.5nsec typical)
- Glitch-free power up/down operation
- Low  $I_{CC}$  current
- Supports live insertion
- High density packaging
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

## DESCRIPTION

This transceiver is a 10 bit bidirectional transceiver and is intended to provide the electrical interface to a high performance wired-OR bus.

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good margins by limiting the switching threshold to a narrow region centered at 1.55V.

The B-port interfaces to "Backplane Transceiver Logic" (See the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1V p-p, between 1V and 2V) and reduced capacitive loading (<6pF) by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

To support live insertion, OEB is held Low during power on/off cycles to insure glitch free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 5V level while  $V_{CC}$  is Low. The BIAS V pin is a low current input which will reverse bias the BTL driver series Schottky diode, and also bias the B port output pins to a voltage between 1.62V and 2.1V. This bias function is in accordance with IEEE BTL standard 1194.1. If live insertion is not a requirement, the BIAS V pin should be tied to a  $V_{CC}$  pin.

The LOGIC GND and BUS GND pins are isolated inside the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package. The LOGIC  $V_{CC}$  and BUS  $V_{CC}$  pins are also isolated internally to minimize noise and may be externally decoupled separately or simply tied together.

This transceiver function is intended to operate in a half-duplex mode. Low current in standby mode is obtained by powering down unused circuitry. Likewise, transmit circuitry is powered down when in receive mode and receive circuitry is powered down while in transmit mode.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay An to $\overline{Bn}$	3.3 3.7	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay $\overline{Bn}$ to An	3.6 3.5	ns
$C_{OB}$	Output capacitance ( $\overline{B0}$ - $\overline{B8}$ ) only)	6	pF
$I_{OL}$	Output current ( $\overline{B0}$ - $\overline{B8}$ ) only)	100	mA
$I_{CC}$	Supply current	Standby	1
		An to $\overline{Bn}$	7
		$\overline{Bn}$ to An	18

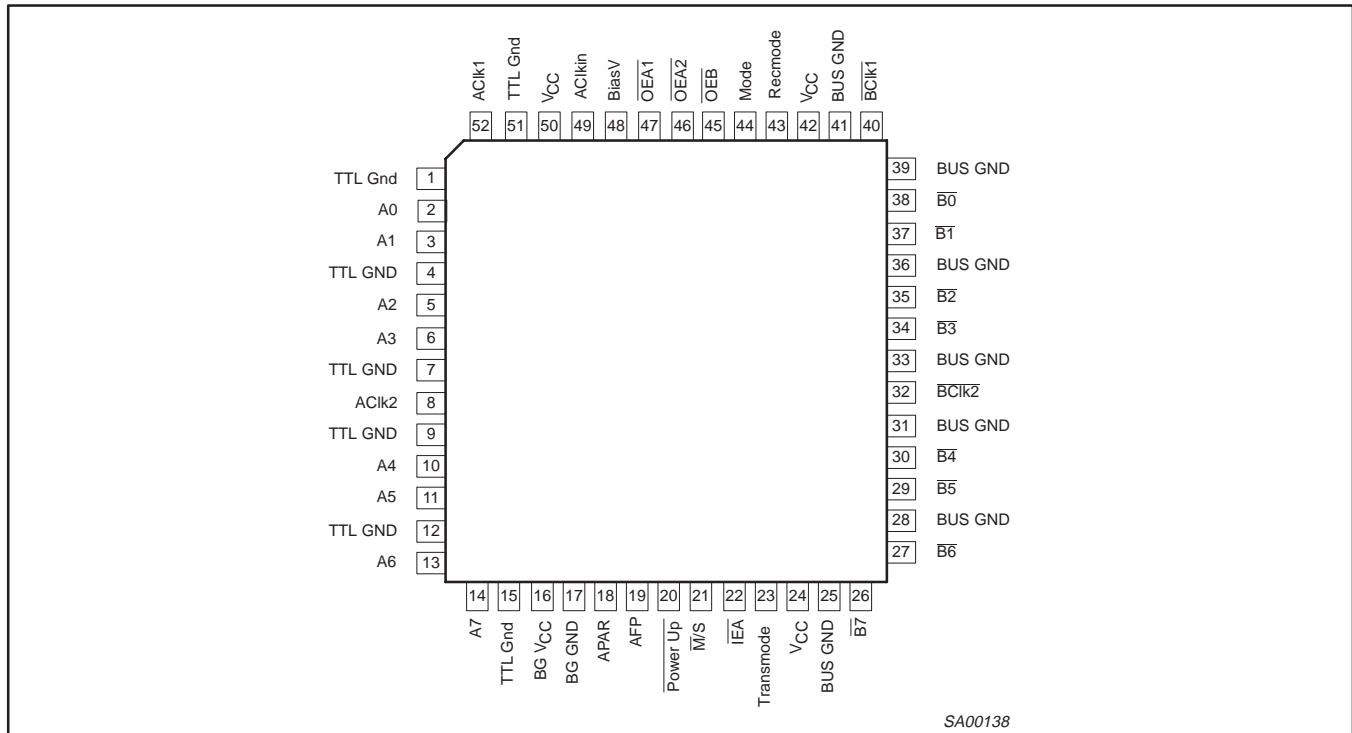
## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52-PIN PQFP	-40°C to +85°C	74ABTL3205 BB	74ABTL3205 BB	SOT379-1

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## PIN CONFIGURATION



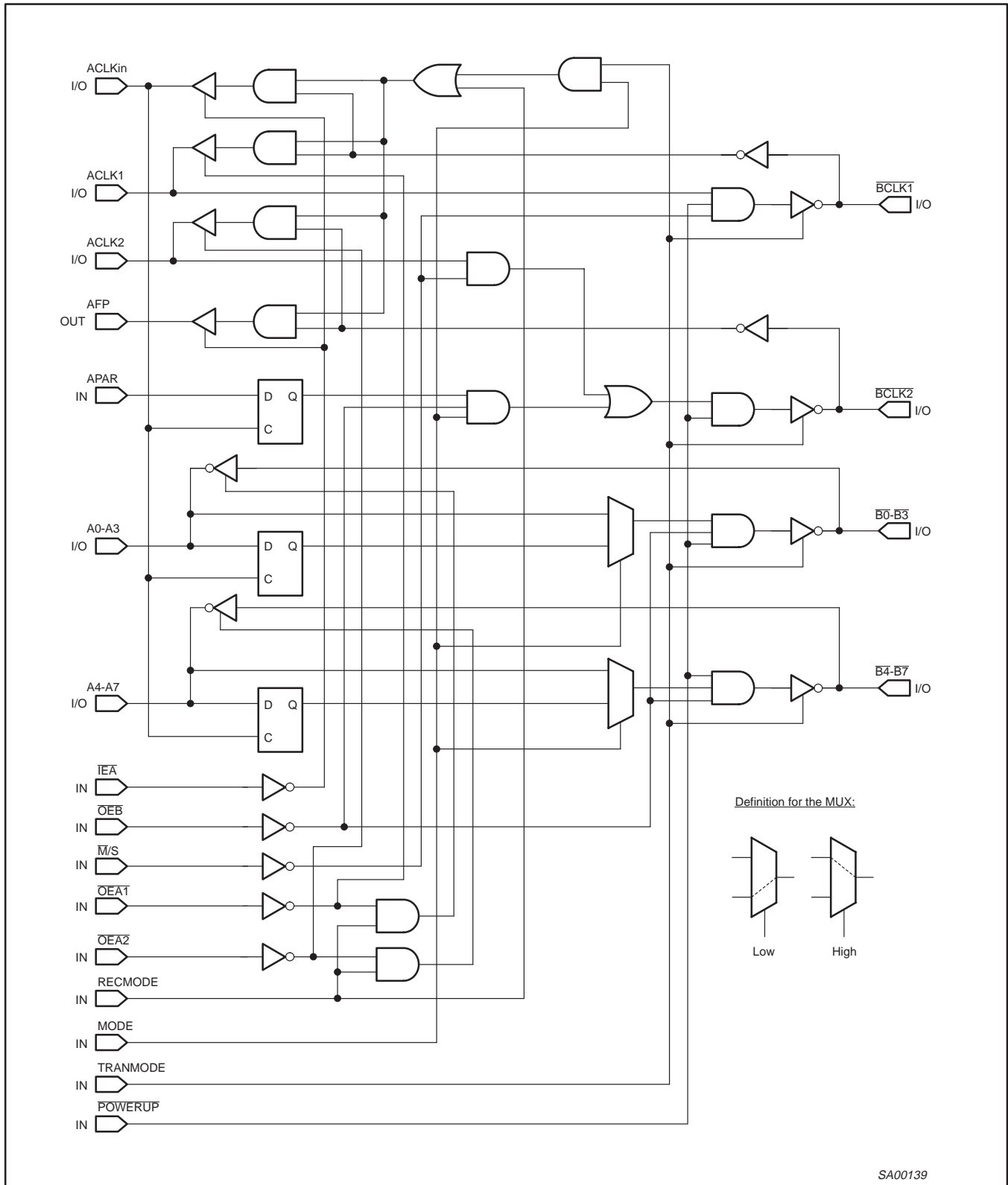
## PIN DESCRIPTION

SYMBOL	FUNCTION	ASSERTION	I/O	LOGIC
OEA1	Output enable data receiver group 1	Low	Input	TTL
OEA2	Output enable data receiver group 2	Low	Input	TTL
OEB	Output enable data transmitter	Low	Input	TTL
IEA	Output enable clock and framepulse receiver	Low	Input	TTL
M/S	Master/Slave select: L: Master, enable clock transmitter H: Slave, disable clock transmitter		Input	TTL
Mode	Low: Data through mode High: Registered data mode		Input	TTL
Power Up	Power up mode, held low during power up to disable clock and data transmitters	Low	Input	TTL
Recmode	Enables receiver	High	Input	TTL
Tranmode	Enables transmitter	High	Input	TTL
ACIk1	Clock or data path		I/O	TTL
ACIkIn	IEA = H → Input for busclock IEA = L → Output for busclock		I/O	TTL
A0..A3	data group 1		I/O	TTL
ACIk2	Clock or data path		I/O	TTL
AFPIn	Alternate data path		Output	TTL
APAR	Alternate data path		Input	TTL
A4..A7	data group 2		I/O	TTL
BCIk1	Clock or data path		I/O	BTL
B0..B3	data group 1		I/O	BTL
BCIk2	Clock or data path		I/O	BTL
B4..B7	data group 2		I/O	BTL

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## LOGIC DIAGRAM



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## FUNCTION TABLE

MODE	INPUTS																
	An	$\overline{Bn}$	ACLK <sub>in</sub>	ACLK <sub>1</sub>	ACLK <sub>2</sub>	$\overline{BCLK1}$	$\overline{BCLK2}$	OEAT	OEAT2	OE <sub>B</sub>	APAR	IEA	M/S	MODE	REC MODE	TRAN MODE	POWER UP
An to Bn (REGISTERED)	l	O	↑	X	X	X	X	H	H	L	X	H	X	H	L	H	H
	h	O	↑	X	X	X	X	H	H	L	X	H	X	H	L	H	H
AN to Bn (THROUGH)	L	O	X	X	X	X	X	H	H	L	X	X	X	L	L	H	H
	H	O	X	X	X	X	X	H	H	L	X	X	X	L	L	H	H
B0-B3 to A0-A3 (THROUGH)	O	L	X	X	X	X	X	L	X	H	X	X	X	X	H	L	L
	O	H	X	X	X	X	X	L	X	H	X	X	X	X	H	L	L
B4-B7 to A4-A7 (THROUGH)	O	L	X	X	X	X	X	X	L	H	X	X	X	X	H	L	L
	O	H	X	X	X	X	X	X	L	H	X	X	X	X	H	L	L
ACLK1 to BCLK1	X	X	X	L	X	O	X	H	X	X	X	X	L	X	X	H	H
	X	X	X	H	X	O	X	H	X	X	X	X	L	X	X	H	H
ACLK2 to BCLK2	X	X	X	X	L	X	O	X	H	H	X	X	L	L	X	H	H
	X	X	X	X	H	X	O	X	H	H	X	X	L	L	X	H	H
BCLK1 to ACLK1	X	X	X	O	X	L	X	L	X	X	X	X	X	X	H	L	X
	X	X	X	O	X	H	X	L	X	X	X	X	X	X	H	L	X
BCLK2 to ACLK2	X	X	X	X	O	X	L	X	L	X	X	X	X	X	H	L	X
	X	X	X	X	O	X	H	X	L	X	X	X	X	X	H	L	X
APAR to BCLK2	X	X	↑	X	X	X	X	X	X	L	l	X	H	H	X	H	H
	X	X	↑	X	X	X	X	X	X	L	h	X	H	H	X	H	H
BCLK2 to AFPIn	X	X	X	X	X	X	L	X	X	X	X	L	X	X	H	L	X
	X	X	X	X	X	X	H	X	X	X	X	L	X	X	H	L	X
BCLK1 to ACLKin	X	X	O	X	X	L	X	H	H	L	O	L	H	H	L	H	H
	X	X	O	X	X	H	X	H	H	L	O	L	H	H	L	H	H

MODE	OUTPUTS								
	An	$\overline{Bn}$	ACLK <sub>in</sub>	ACLK <sub>1</sub>	ACLK <sub>2</sub>	$\overline{BCLK1}$	$\overline{BCLK2}$	AF Pin	
An to Bn (REGISTERED)	Input	H*	X	X	X	X	X	X	
	Input	L	X	X	X	X	X	X	
AN to Bn (THROUGH)	Input	H*	X	X	X	X	X	X	
	Input	L	X	X	X	X	X	X	
B0-B3 to A0-A3 (THROUGH)	H	Input	Input	X	X	X	X	X	
	L	Input	Input	X	X	X	X	X	
B4-B7 to A4-A7 (THROUGH)	H	Input	Input	X	X	X	X	X	
	L	Input	Input	X	X	X	X	X	
ACLK1 to BCLK1	X	X	X	Input	X	H*	X	X	
	X	X	X	Input	X	L	X	X	
ACLK2 to BCLK2	X	X	X	X	Input	X	H*	X	
	X	X	X	X	Input	X	L	X	
BCLK1 to ACLK1	X	X	X	H	X	Input	X	X	
	X	X	X	L	X	Input	X	X	
BCLK2 to ACLK2	X	X	X	X	H	X	Input	X	
	X	X	X	X	L	X	Input	X	
APAR to BCLK2	X	X	Input	X	X	X	H*	X	
	X	X	Input	X	X	X	L	X	
BCLK2 to AFPIn	X	X	X	X	X	X	Input	H*	
	X	X	X	X	X	X	Input	L	
BCLK1 to ACLKin	X	X	H	X	X	Input	X	X	
	X	X	L	X	X	Input	X	X	

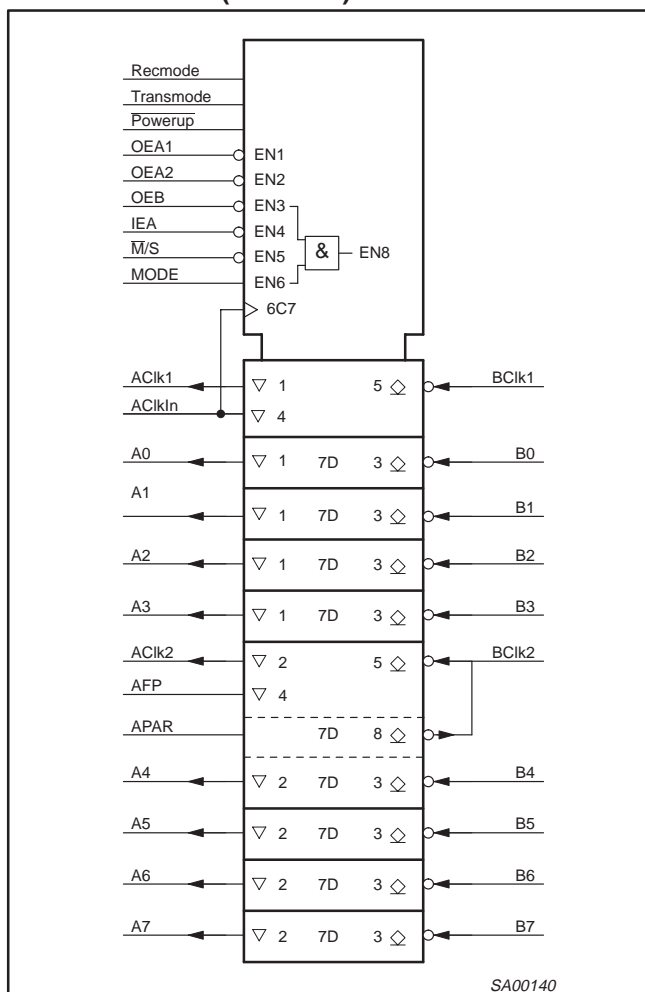
**NOTES:**

- H = High voltage level
- L = Low voltage level
- h = High voltage level one set-up time prior to Low to High ACLK<sub>in</sub> transition
- l = Low voltage level one set-up time prior to Low to High ACLK<sub>in</sub> transition
- ↑ = Low to High transition
- Z = High impedance (off) state
- H\* = Goes to level of pull-up voltage
- X = Don't care
- O = Output

# 10-bit BTL transceiver with registers

## 74ABTL3205

### LOGIC SYMBOL (IEEE/IEC)



### ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V <sub>CC</sub>	Supply voltage		-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	TTL Signals	-1.2 to +7.0	V
		BTL Signals	-1.2 to +5.5	V
I <sub>IN</sub>	Input current		-18 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state		-0.5 to +V <sub>CC</sub>	/v
I <sub>OUT</sub>	Current applied to output in Low output state	A0 - A8	48	mA
		$\overline{B0}$ - $\overline{B8}$	200	mA
T <sub>amb</sub>	Operating free-air temperature range		-40 to +85	°C
T <sub>STG</sub>	Storage temperature		-65 to +150	°C

## 10-bit BTL transceiver with registers

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**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT
				MIN	TYP <sup>2</sup>	MAX	
I <sub>OH</sub>	High level output current	BTL	V <sub>CC</sub> = MAX, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, V <sub>OH</sub> = 1.9V		0.5	100	μA
I <sub>OFF</sub>	Power-off output current	BTL	V <sub>CC</sub> = 0.0V, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, V <sub>OH</sub> = 1.9V		10	100	μA
V <sub>OH</sub>	High-level output voltage	TTL	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, <sup>4</sup> V <sub>IH</sub> = MIN, I <sub>OH</sub> = -3mA	2.5	2.85	3.4	V
			V <sub>CC</sub> = MIN to MAX, <sup>4</sup> V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OH</sub> = -10μA			V <sub>CC</sub> - 1.1	V
V <sub>OL</sub>	Low-level output voltage	TTL	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OL</sub> = 24mA		0.35	0.5	V
		BTL	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OL</sub> = 100mA	0.75	1.0	1.10	V
			V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OL</sub> = 4mA	0.5	0.7		V
V <sub>IK</sub>	Input clamp voltage	TTL	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>		0.8	-1.2	V
		BTL	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18mA		0.8	-1.2	V
I <sub>I</sub>	Input current at maximum input voltage	TTL	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V or 5.5V		0.1	±50	μA
I <sub>IH</sub>	High-level input current	TTL	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V, B <sub>n</sub> = A <sub>n</sub> = 0V		0.1	20	μA
		BTL	V <sub>CC</sub> = MAX, V <sub>I</sub> = 1.9V		0.1	100	μA
			V <sub>CC</sub> = MAX, V <sub>I</sub> = 3.5V <sup>5</sup>	100			mA
I <sub>IL</sub>	Low-level input current	TTL	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V		0.1	-20	μA
		BTL	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.75V		0.1	-100	μA
I <sub>OZH</sub>	Off-state output current	TTL	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7V		0.1	50	μA
I <sub>OZL</sub>	Off-state output current	TTL	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5V		20	-50	μA
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	TTL	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.0V	-60	130	-150	mA
I <sub>CC</sub>	Supply current (total)	Recmode Low Tranmode Low	V <sub>CC</sub> = MAX		1	3	mA
		Recmode Low Tranmode High	V <sub>CC</sub> = MAX Mode = Low		7	12	mA
		Recmode Low Tranmode High	V <sub>CC</sub> = MAX Mode = High		13	21	mA
		Recmode High Tranmode Low	V <sub>CC</sub> = MAX		18	25	mA
		Recmode High Tranmode High	V <sub>CC</sub> = MAX		29	43	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
- Due to test equipment limitations, actual test conditions are V<sub>IH</sub> = 1.8V and V<sub>IL</sub> = 1.3V for the B side.
- For B port input voltage between 3 and 5 volts I<sub>IH</sub> will be greater than 100μA, but the parts will continue to function normally.

TTL signals CLK<sub>in</sub>, CLK-1/CLK-OUT, CLK-2/FP-OUT, /FP-IN, /PARITY t<sub>A0..A7</sub>, OEB, MASTER/SLAVE, MODE, OEA1, OEA2

BTL signals CLK1BTL, CLK2BTL, B0..B7

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## LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
$V_{BIASV}$	Bias pin DC current	$V_{CC} = 0$ to 5.25V, $\overline{Bn} = 0$ to 2.0 V	4.5		5.5	V
$I_{BIASV}$	Bias pin DC current	$V_{CC} = 0$ to 4.75 V, $\overline{Bn} = 0$ to 2.0V, Bias V = 4.5 to 5.5V			1	mA
		$V_{CC} = 4.5$ to 5.5V, $\overline{Bn} = 0$ to 2.0 V, Bias V = 4.5 to 5.5V			10	$\mu$ A
$\sqrt{Bn}$	Bus voltage during prebias	$B0 - \overline{B8} = 0V$ , Bias V = 5.0V	1.62		2.1	V

## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			$T_{amb} = +25^{\circ}C$ $V_{CC} = 5V$ $C_L = 50pF, C_L = 500\Omega$			$T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF, C_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	
$t_{PLH}$ $t_{PHL}$	Propagation delay $\overline{Bn}$ to An	Waveform 2	2.0 1.8	3.6 3.5	6.5 6.1	2.0 1.8	7.3 6.7	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay, BCLK1 to ACLK1	Waveform 2	2.0 1.8	3.8 3.6	6.5 6.1	2.0 1.8	7.3 6.7	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay BCLK1 to ACLKin	Waveform 2	2.0 1.8	3.7 3.7	6.5 6.1	2.0 1.8	7.3 6.7	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay BCLK2 to ACLK2	Waveform 2	2.0 1.8	3.7 3.9	6.5 6.1	2.0 1.8	7.3 6.7	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay BCLK2 to AFP	Waveform 2	2.0 1.8	3.8 3.9	6.5 6.1	2.0 1.8	7.3 6.7	ns
$t_{PZH}$ $t_{PLZ}$	Output Enable time OEA1, OEA2, IEA to An	Waveform 1, 2	2.0 1.8	3.8 2.5	6.5 6.1	2.0 1.8	7.3 6.7	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable time OEA1, OEA2, IEA to An	Waveform 4, 5	1.6 2.0	2.5 3.3	5.6 7.8	1.4 1.8	5.7 8.2	ns
$t_{TLH}$ $t_{THL}$	Output transition time, An Port 10% to 90%, 90% to 10%	Test Circuit and Waveforms				3.0 1.7	7.0 4.0	ns
$t_{SK(p)}$	Pulse skew <sup>2</sup> $ t_{PHL} - t_{PLH} _{MAX}$	Waveform 3		2.0				ns

## NOTES:

- $|t_{PN actual} - t_{PM actual}|$  for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature,  $V_{CC}$ , loading, etc.).
- $t_{SK(p)}$  is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle. (50MHz input frequency and 50% duty cycle, tested on data paths only).



## 10-bit BTL transceiver with registers

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = 5V C <sub>D</sub> = 30pF, R <sub>U</sub> = 18.5Ω			T <sub>amb</sub> = -40°C to +85°C V <sub>CC</sub> = 5V ± 10% C <sub>L</sub> = 30pF, R <sub>U</sub> = 18.5Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay An to $\overline{Bn}$	Waveform 2	1.0 1.0	3.3 2.7	4.7 4.5	1.0 1.0	5.7	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay, ACLKin to $\overline{Bn}$	Waveform 1, 2	2.0 2.0	4.6 4.5	5.9 5.9	2.0 2.0	6.3 6.3	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay ACLKin to BCLK2	Waveform 1, 2	2.0 2.0	4.6 4.5	7.3 7.3	2.0 2.0	7.6 7.6	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay ACLK1 to BCLK1	Waveform 2	1.0 1.0	3.2 2.9	4.7 4.5	1.0 1.0	5.1 4.7	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay ACLK2 to BCLK2	Waveform 2	1.0 1.0	3.1 3.1	5.7 5.5	1.0 1.0	6.0 5.6	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Enable/disable time OEB to $\overline{Bn}$ or BCLK2	Waveform 1, 2	1.0 1.0	3.8 3.4	6.8 6.4	1.0 1.0	7.6 6.9	ns
t <sub>TLH</sub> t <sub>THL</sub>	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.0 0.6		2.5 2.0	1.0 0.6	3.0 2.5	ns
t <sub>SK(p)</sub>	Pulse skew2  t <sub>PHL</sub> - t <sub>PLH</sub>   MAX	Waveform 3		2.0				ns

## NOTES:

1. |t<sub>PN</sub> actual - t<sub>PM</sub> actual| for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V<sub>CC</sub>, loading, etc.).
2. t<sub>SK(p)</sub> is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle. (50MHz input frequency and 50% duty cycle, tested on data paths only).

## AC SETUP REQUIREMENTS

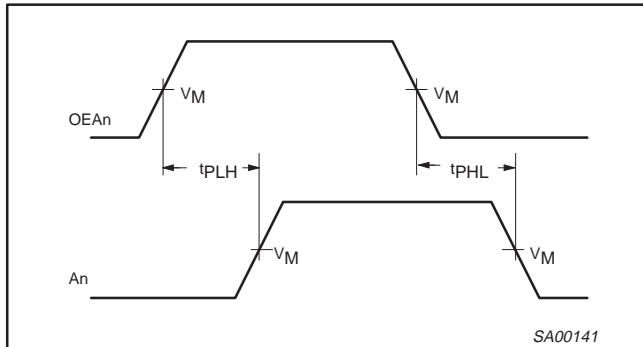
SYMBOL	PARAMETER	TEST CONDITION	LIMITS				UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = 5V		T <sub>amb</sub> = -40°C to +85°C V <sub>CC</sub> = 5V ± 10%		
			C <sub>L</sub> = 50pF (A side) / C <sub>D</sub> = 30pF (B side) R <sub>L</sub> = 500Ω (A side) / R <sub>U</sub> = 18.5Ω (B side)				
			MIN	TYP	MIN	MAX	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time An to ACLKin	Waveform 6	1.9 1.3		2.0 1.5		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time An to ACLKin	Waveform 6	1.8 2.0		2.3 2.0		ns

# 10-bit BTL transceiver with registers

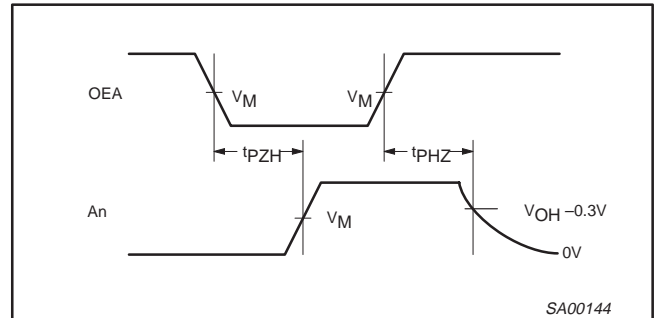
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## AC WAVEFORMS

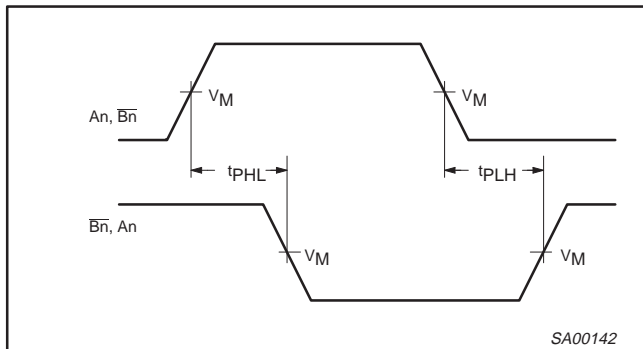
$V_M = 1.55V$  for  $\overline{Bn}$ ,  $V_M = 1.5V$  for all others



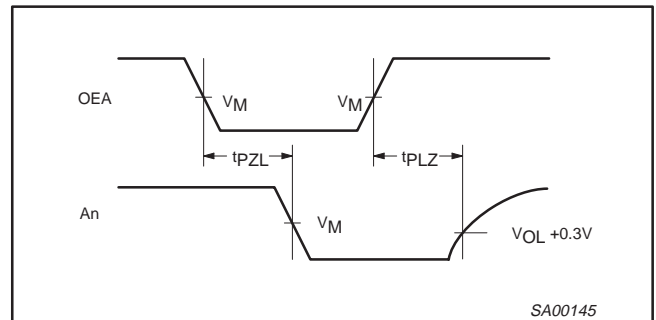
**Waveform 1. Propagation Delay for Data or Output Enable to Output**



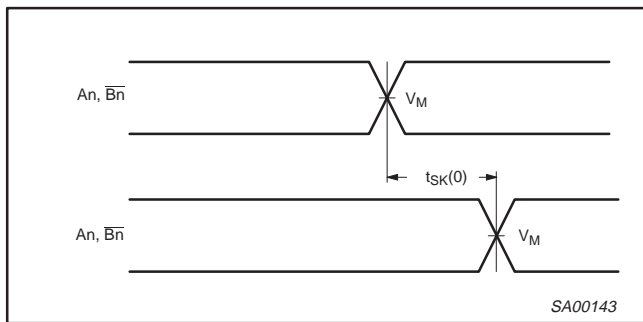
**Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level**



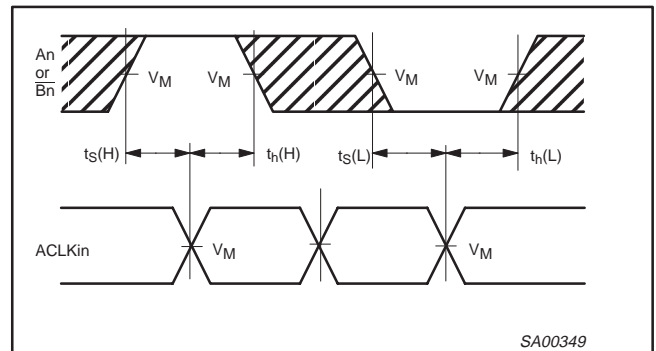
**Waveform 2. Propagation Delay for Data to Output**



**Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**



**Waveform 3. Output Skews**

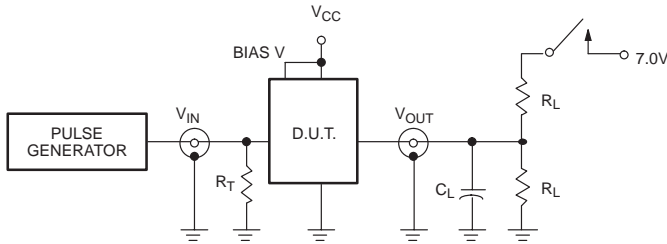


**Waveform 6. Data Setup and Hold Times**

# 10-bit BTL transceiver with registers

# 74ABTL3205

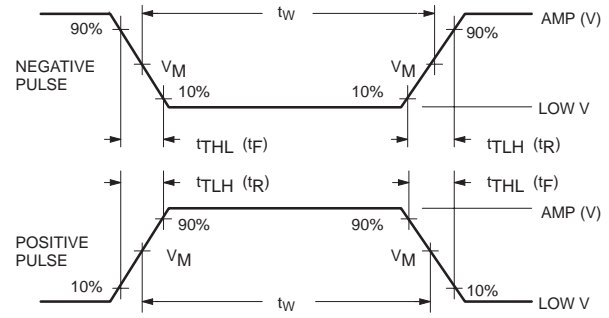
## TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs on A Port

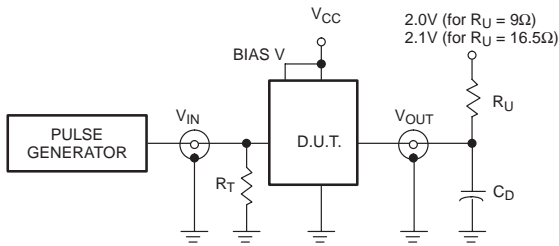
**SWITCH POSITION**

TEST	SWITCH
$t_{PLZ}$ , $t_{PZL}$	closed
All other	open



$V_M = 1.55V$  for  $B_n$  or  $\overline{B_n}$ ,  $V_M = 1.5V$  for all others

**Input Pulse Definition**



Test Circuit for Outputs on B Port

ABTL	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	$t_w$	$t_{TLH}$	$t_{THL}$
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.5ns	2.5ns

**DEFINITIONS**

- $R_L$  = Load resistor; see AC CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.
- $C_D$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- $R_U$  = Pull up resistor; see AC CHARACTERISTICS for value.

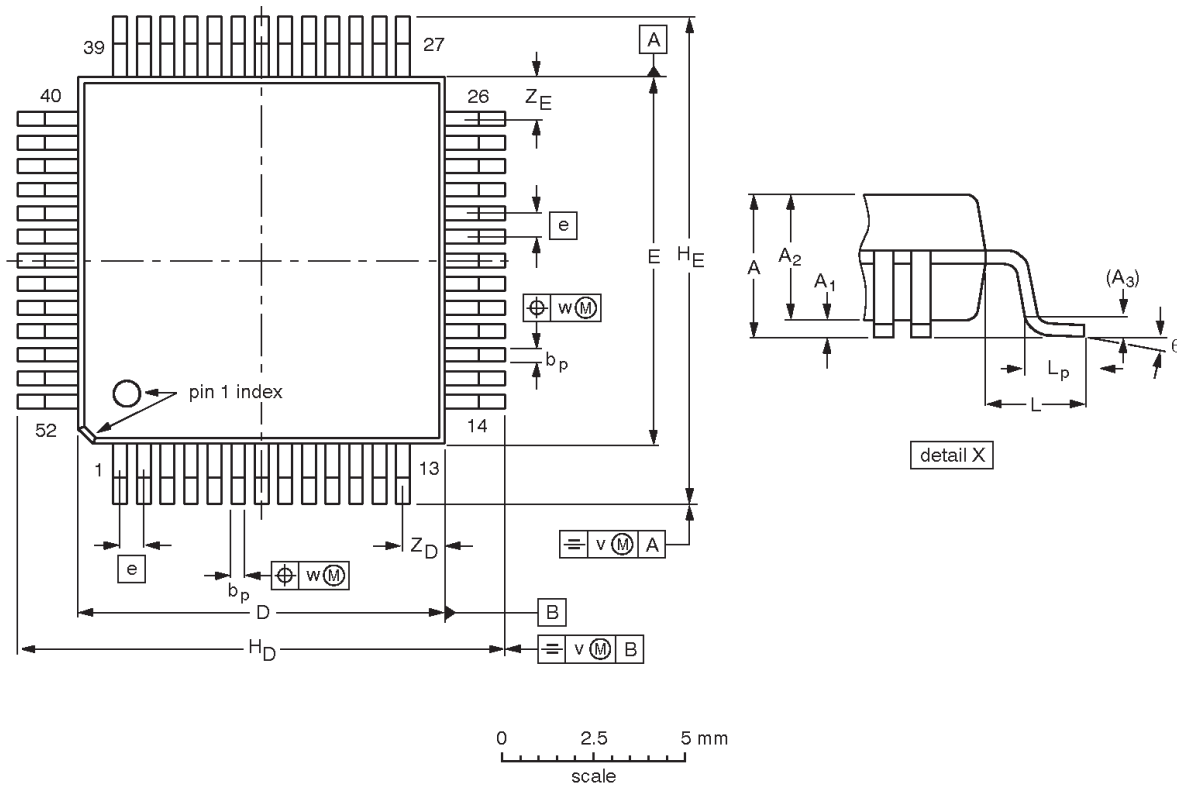
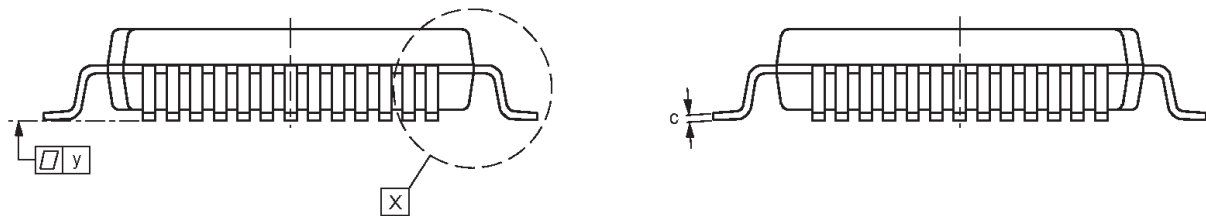
SA00146

# 10-bit BTL transceiver with registers

## 74ABTL3205

**QFP52: plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 x 10 x 2.0 mm**

**SOT379-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	2.45	0.45 0.25	2.10 1.95	0.25	0.38 0.22	0.23 0.13	10.1 9.9	10.1 9.9	0.65	13.45 12.95	13.45 12.95	1.60	0.95 0.65	0.20	0.12	0.10	1.24 0.95	1.24 0.95	7° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT379-1		MO-108			95-02-04 97-08-04

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10-bit BTL transceiver with registers

74ABTL3205

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**NOTES**

## 10-bit BTL transceiver with registers

74ABTL3205

**Data sheet status**

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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