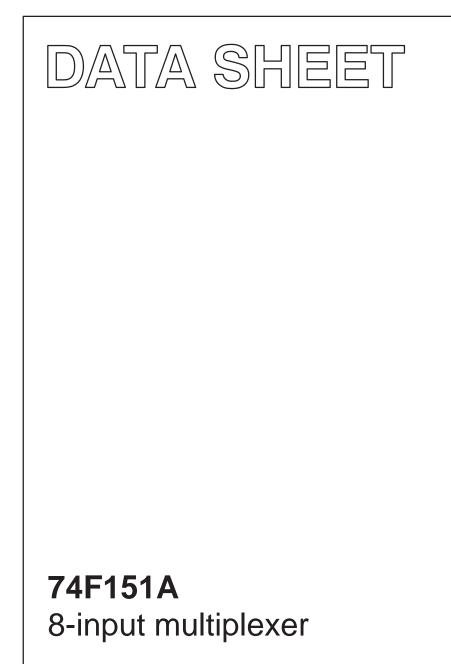
# INTEGRATED CIRCUITS



Product specification Supercedes data of 1989 Mar 03 IC15 Data Handbook

1995 Jul 17



Philips Semiconductors

# 74F151A

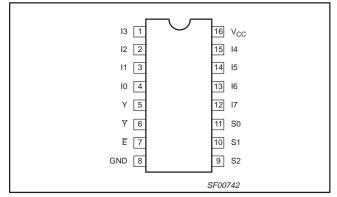
## **FEATURES**

- High speed 8-to-1 multiplexing
- On chip decoding
- Multifunction capability
- Complementary outputs

## DESCRIPTION

The 74F151A is a logic implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select (S0, S1, S2) inputs. True (Y) and complementary ( $\overline{Y}$ ) outputs are both provided. The Enable input ( $\overline{E}$ ) is active Low. When  $\overline{E}$  is High, the  $\overline{Y}$  output is High and the Y output is Low, regardless of all other inputs. In one package the 74F151A provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and the negation with correct manipulation.

## PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F151A	4.5ns	17mA

## **ORDERING INFORMATION**

	ORDER CODE		
DESCRIPTION	$\begin{array}{l} \text{COMMERCIAL RANGE} \\ \text{V}_{\text{CC}} = 5\text{V} \pm 10\%, \\ \text{T}_{\text{amb}} = 0^{\circ}\text{C to} + 70^{\circ}\text{C} \end{array}$	PKG DWG #	
16-pin plastic DIP	N74F151AN	SOT38-4	
16-pin plastic SO	N74F151AD	SOT109-1	

#### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

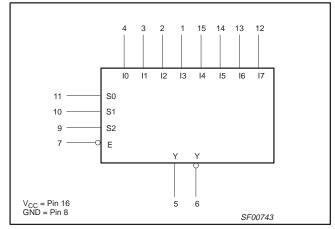
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
10–17	Data inputs	1.0/1.0	20µA/0.6mA
S0–S2	Select inputs	1.0/1.0	20µA/0.6mA
Ē	Enable input (active High)	1.0/1.0	20µA/0.6mA
Υ, Ϋ	Data outputs	150/33	3mA/20mA

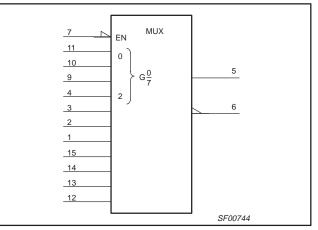
NOTE:

One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

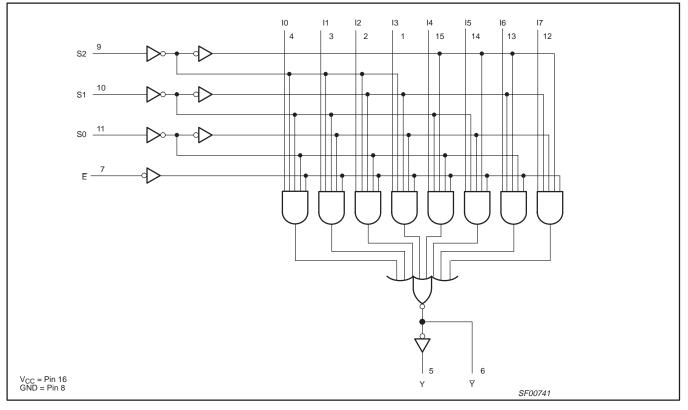
## 74F151A

## LOGIC SYMBOL





## LOGIC DIAGRAM



## **IEC/IEEE SYMBOL**

## 74F151A

#### **FUNCTION TABLE**

	INP	UTS		OUTF	PUTS
S2	S1	S0	Ē	Y	Ϋ́
Х	Х	Х	Н	L	Н
L	L	L	L	10	ĪO
L	L	Н	L	l1	Ī1
L	Н	L	L	12	Ī2
L	Н	Н	L	13	Ī3
Н	L	L	L	14	Ī4
Н	L	Н	L	15	Ī5
Н	Н	L	L	16	Ī6
Н	Н	Н	L	17	Ī7

#### NOTES:

H = High voltage level

L = Low voltage level

X = Don't care

## **ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	–0.5 to $V_{CC}$	V
I <sub>OUT</sub>	Current applied to output in Low output state	40	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature	-65 to +150	°C

## **RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER		LIMITS	LIMITS		
STWIDUL	PARAMETER	MIN	MAX	UNIT		
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V	
V <sub>IH</sub>	High-level input voltage	2.0			V	
V <sub>IL</sub>	Low-level input voltage			0.8	V	
I <sub>IK</sub>	Input clamp current			-18	mA	
I <sub>OH</sub>	High-level output current			-1	mA	
I <sub>OL</sub>	Low-level output current			20	mA	
T <sub>amb</sub>	Operating free-air temperature range	0		+70	°C	

## 74F151A

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

						LIMITS					
SYMBOL	PARAMETER\		TEST CONDITIONS <sup>NO T</sup>	AG	MIN	TYP NO TAG	МАХ	UNIT			
M			$V_{CC} = MIN, V_{IL} = MAX,$ $V_{IH} = MIN, I_{OH} = MAX$	±10%V <sub>CC</sub>	2.5			V			
V <sub>OH</sub>	High-level output voltage		$V_{IH} = MIN, I_{OH} = MAX$	$\pm$ 5%V <sub>CC</sub>	2.7	3.4		V			
Ma.			$V_{CC} = MIN, V_{IL} = MAX,$			0.30	0.50	V			
V <sub>OL</sub>	Low-level output voltage		$V_{IH} = MIN, I_{OL} = MAX$	±5%V <sub>CC</sub>		0.30	0.50	V			
V <sub>IK</sub>	Input clamp voltage		$V_{CC} = MIN, I_I = I_{IK}$			-0.73	-1.2	V			
II.	Input current at maximum inp voltage	out	$V_{CC} = MAX, V_I = 7.0V$				100	μA			
I <sub>IH</sub>	High-level input current		$V_{CC} = MAX, V_I = 2.7V$				20	μA			
IIL	Low-level input current		$V_{CC} = MAX, V_I = 0.5V$				-0.6	mA			
I <sub>OS</sub>	Short-circuit output current <sup>NC</sup>	) TAG	V <sub>CC</sub> = MAX		-60		-150	mA			
1	CC Supply current (total)		V <sub>CC</sub> = MAX			18	25	mA			
ICC						17	25	mA			

#### NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

2. All typical values are at  $V_{CC} = 5V$ ,  $T_{amb} = 25^{\circ}C$ . 3. Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last. AC ELECTRICAL CHARACTERISTICS

					LIN	<b>/</b> ITS		
SYMBOL	PARAMETER	TEST CONDITION	(	<sub>CC</sub> = +5.0 <sub>mb</sub> = +25 C <sub>L</sub> = 50pl R <sub>L</sub> = 500⊆	=	V <sub>CC</sub> = +5. T <sub>amb</sub> = 0°C C <sub>L</sub> = R <sub>L</sub> = 5	UNIT	
			MIN	TYP	MAX	MIN	MAX	1
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay In to Y	Waveform NO TAG	2.5 2.5	4.5 4.5	7.0 7.0	2.5 2.5	7.5 7.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay In to $\overline{Y}$	Waveform NO TAG	2.0 1.0	4.0 2.0	7.0 4.5	2.0 1.0	7.5 5.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Sn to Y	Waveform 1, 2	4.5 4.0	6.5 6.0	10.0 8.5	4.0 3.5	11.0 9.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Sn to $\overline{Y}$	Waveform NO TAG, NO TAG	3.5 2.5	5.5 4.5	8.5 7.0	3.0 2.0	9.5 7.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay $\overline{E}$ to Y	Waveform 1	4.0 3.0	6.5 5.0	9.0 7.0	3.5 3.0	9.5 7.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay $\overline{E}$ to $\overline{Y}$	Waveform NO TAG	2.5 2.0	4.5 3.5	6.5 5.5	2.5 1.5	7.0 6.0	ns

## **AC WAVEFORMS**

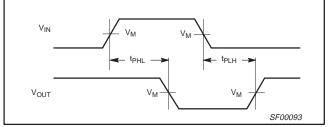
For all waveforms,  $V_M = 1.5V$ 

AMP (V)

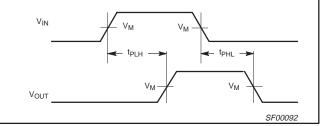
AMP (V)

0V

0V



Waveform 1. For Inverting Outputs



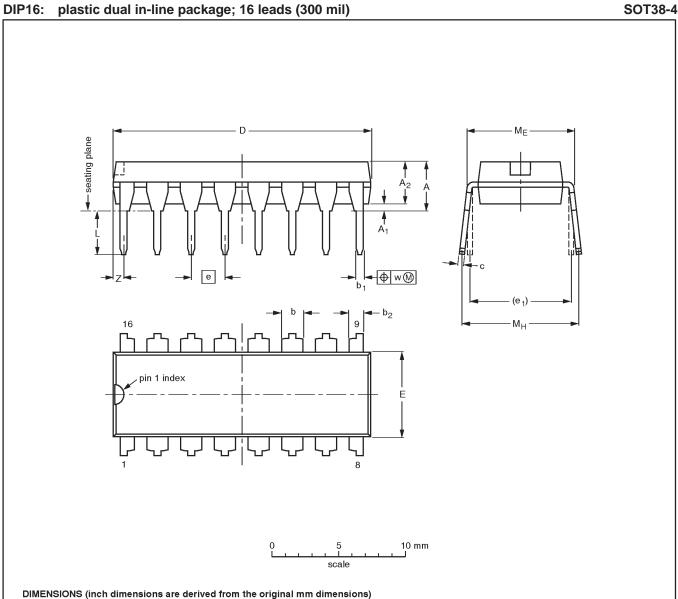


#### VCC 90% 90% NEGATIVE PULSE ٧м ٧M 10% 10% VOUT ٧IN PULSE D.U.T. $\odot$ 6 tTHL (tf) tTLH (tr) GENERATOR ≷ ₹ RL RT 市cL tTLH (tr) tTHL (tf) 90% 90% POSITIVE PULSE ÷ ٧M -= ÷ ÷ ٧м 10% Test Circuit for Totem-Pole Outputs 10% **DEFINITIONS: Input Pulse Definition** R<sub>L</sub> = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value. **INPUT PULSE REQUIREMENTS** family $C_L =$ Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value. amplitude VM rep. rate t<sub>w</sub> t<sub>TLH</sub> t<sub>THL</sub> RT = Termination resistance should be equal to Z<sub>OUT</sub> of 74F 3.0V 1.5V 1MHz 500ns 2.5ns 2.5ns pulse generators.

### **TEST CIRCUIT AND WAVEFORMS**

#### 1995 Jul 17

# 8-input multiplexer



UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	с	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

#### Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

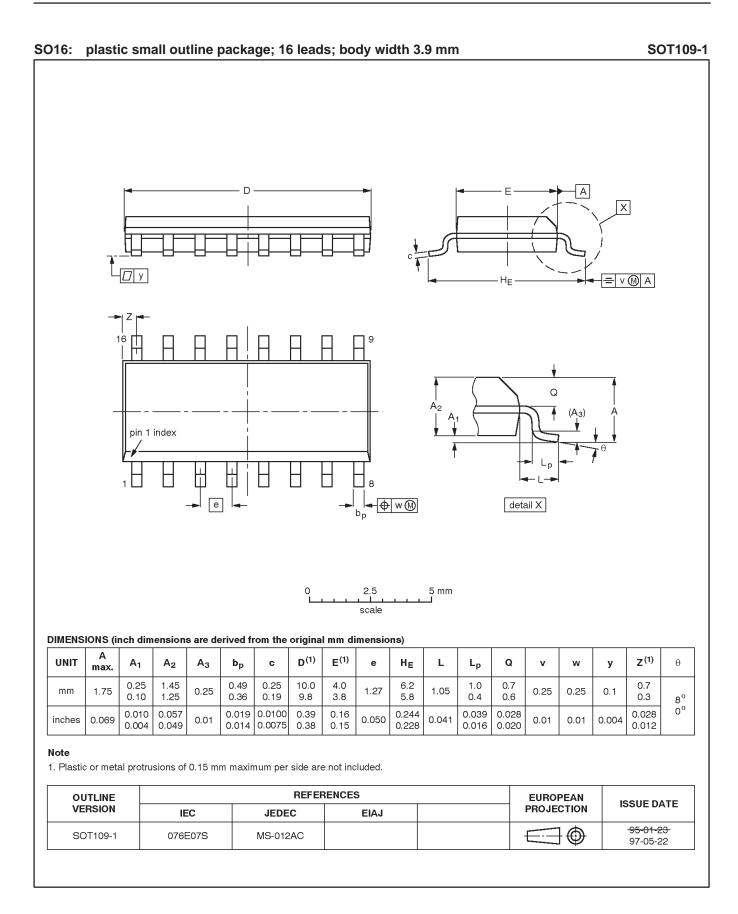
OUTLINE		REFERENCES				ISSUE DATE
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
SOT38-4						<del>-92-11-17</del> 95-01-14

#### Product specification

74F151A

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74F151A



74F151A

NOTES

#### Data sheet status

Data sheet status	Product status	Definition <sup>[1]</sup>
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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