8284A/8284A-1

Clock Generator and Driver for 8086, 8088 Processors

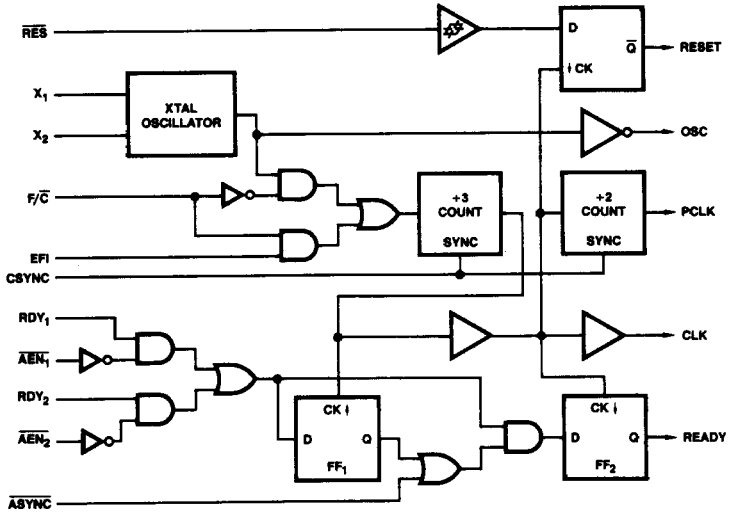
DISTINCTIVE CHARACTERISTICS

- Generates the System Clock for the 8086, 8088 Processors: 5MHz, 8MHz with 8284A; 10MHz with 8284A-1
- Uses a crystal or a TTL signal for frequency source
- Provides local READY and Multibus* READY synchronization
- Generates system reset output from Schmitt trigger input
- Capable of clock synchronization with other 8284As

GENERAL DESCRIPTION

The 8284A is a single chip clock generator/driver for the 8086, 8088 processors. The chip contains a crystal-controlled oscillator, a divide-by-three counter, complete MULTIBUS* "Ready" synchronization and reset logic.

BLOCK DIAGRAM



BD001440

RELATED AMD PRODUCTS

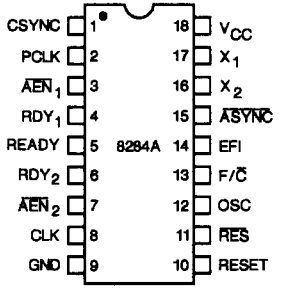
Part No.	Description
Am8086	16-Bit Microprocessor
8288	Bus Controller

*MULTIBUS is a registered trademark of Intel Corp.

Publication # 03359 | Rev. D | Amendment /0
Issue Date: April 1987

CONNECTION DIAGRAMS
Top View

DIPs



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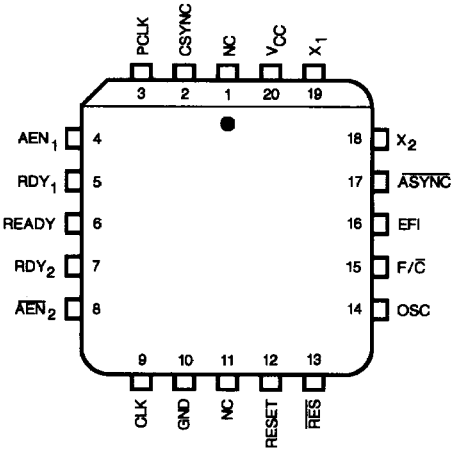

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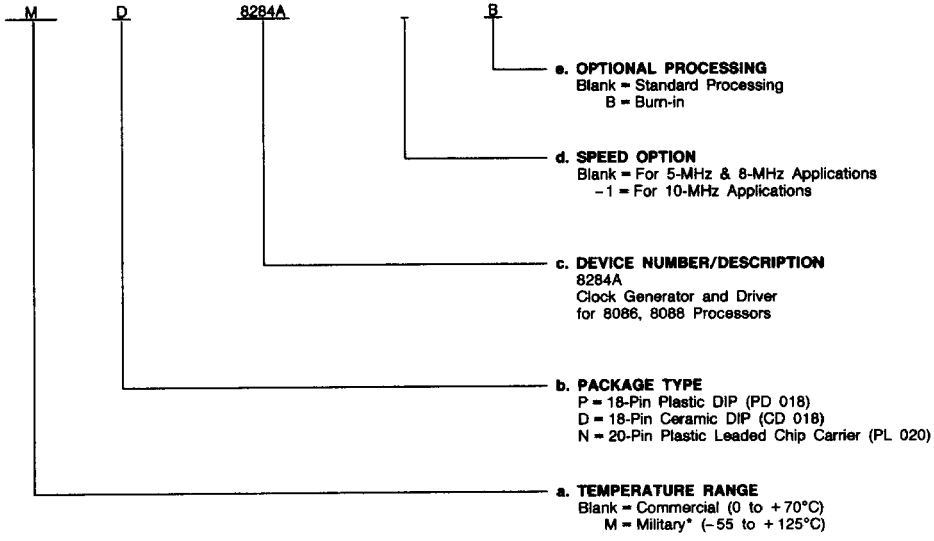
Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Temperature Range**
b. Package Type
c. Device Number
d. Speed Option
e. Optional Processing



Valid Combinations	
MD, D, P, N	8284A
MD, D, P	8284AB
D	8284A-1
	8284A-1B

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

* Military temperature range products are NPL (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
3, 7	$\overline{AEN}_1$, $\overline{AEN}_2$	I	Address Enable. The $\overline{AEN}$ signal is used to qualify the Bus Ready signal (RDY_1 or RDY_2). $\overline{AEN}_1$ validates RDY_1 while $\overline{AEN}_2$ validates RDY_2. It is possible for the processor to access two Multi-Master System Busses if you use both signals. Both signals are tied LOW in non Multi-Master Systems.
4, 6	RDY_1, RDY_2	I	Bus Ready. These signals are indications from a device located on the system bus that it is available or data has been received. RDY_1 and RDY_2 are qualified by $\overline{AEN}_1$ and $\overline{AEN}_2$ respectively.
15	$\overline{ASYNC}$	I	Ready Synchronous Select. The $\overline{ASYNC}$ signal defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is open (internal pull-up resistor is provided) or pulled HIGH, there is one stage of READY Synchronization. When $\overline{ASYNC}$ is LOW, there are two stages of READY Synchronization.
5	READY	O	Ready. READY is the synchronized RDY signal input. After the guaranteed hold time to the processor has been met, the READY signal is cleared.
7, 16	X_1,X_2	I	Crystal In. These are the input pins for the attached crystal. The crystal frequency is 3 times the desired process clock frequency.
13	F/$\overline{C}$	I	Frequency/Crystal Select. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input. When strapped LOW, the F/$\overline{C}$ allows the processor clock to be generated by the crystal.
14	EFI	I	External Frequency. Used in conjunction with a HIGH signal on F/$\overline{C}$, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
8	CLK	O	Processor Clock. CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus (including bipolar support chips and other MOS devices). An output HIGH of 4.5V (V_{CC} = 5V) is provided on this pin to drive MOS devices. The output frequency of CLK is 1/3 of the crystal on EFI input frequency and a 1/3 duty cycle.
2	PCLK	O	Peripheral Clock. This signal is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.
12	OSC	O	Oscillator Output. This signal is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
11	$\overline{RES}$	I	Reset In. This signal is used to generate a RESET. The 8284A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
10	RESET	O	Reset. This signal is used to reset the 8086 family processors.
1	CSYNC	I	Clock Synchronization. This signal is designed to allow multiple 8284As to be synchronized to provide clocks that are in phase. CSYNC HIGH will reset the internal counters, when CSYNC goes LOW the counters will resume counting. CSYNC needs to be externally synchronized to EFI. When used with the internal oscillator, CSYNC should be hard wired to ground.

DETAILED DESCRIPTION

OSCILLATOR

The oscillator circuit of the 8284A is designed primarily for use with a fundamental mode, series resonant crystal from which the operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X_1 and X_2 are the two crystal input crystal connections. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

Two 510Ω series resistors are optional for systems which have a V_{CC} ramp time greater than (or equal to) 1V/ms and/or inherent board capacitance between X_1 or X_2 exceeding 10pF. This capacitance value should not include the 8284A's pin capacitance. By limiting the stray capacitance to less than 10pF on X_1 or X_2, the deviation from the desired fundamental frequency is minimized.

CLOCK GENERATOR

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input, (CSYNC), allows the output clock to be synchronized with an external event (such as another 8284A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the 8284A (see Figure 1). This is accomplished with two Schottky flip-flops. The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/$\overline{C}$ input is a strapping pin that selects either the EFI input or the crystal oscillator as the clock for the ÷ 3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

CLOCK OUTPUTS

The CLK output is a 33% duty cycle MOS clock driver designed to drive the 8086 or 8088 processors directly. PCLK is a TTL level peripheral clock signal whose output frequency is ½ that of CLK. PCLK has a 50% duty cycle.

RESET LOGIC

Reset logic for the 8284A is provided by a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing.

The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the 8284A.

READY SYNCHRONIZATION

Two READY inputs (RDY_1, RDY_2) are provided to accommodate two Multi-Master system busses. Each input has a qualifier ($\overline{AEN}_1$ and $\overline{AEN}_2$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

To assure RDY setup and hold times are met, synchronization is required for all asynchronous active going edges of either RDY input. Inactive-going edges of RDY (in normally ready systems) do not require synchronization, but must satisfy RDY setup and hold as a matter of proper system design.

The two modes of RDY synchronization operation are defined by the $\overline{ASYNC}$ input.

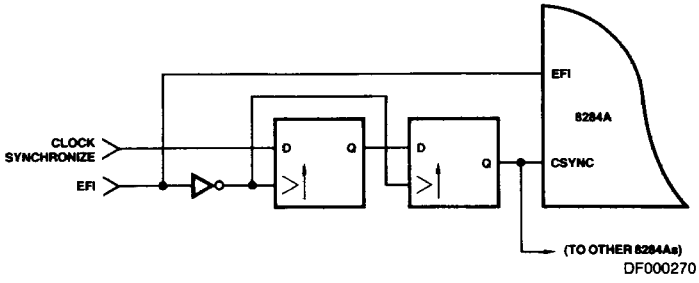
When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active RDY input signals. Positive-going asynchronous RDY inputs will first be synchronized to flip-flop one at the rising edge of CLK and then synchronized to flip-flop two at the next falling edge of CLK; after which time the READY output will go active (HIGH). Negative-going asynchro-

nous RDY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous, (normally not ready), devices in the system which cannot be guaranteed by design to meet the required RDY setup timing t_{R1VCL} on each bus cycle.

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. RDY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

$\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

Figure 1. CSYNC Synchronization



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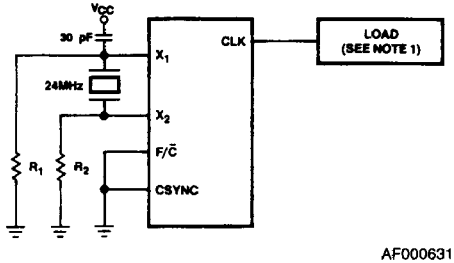
CLOCK HIGH AND LOW TIME (USING X_1, X_2)



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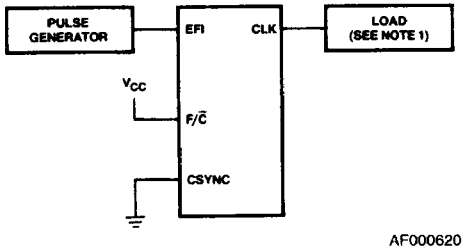
$R_1 = R_2 = 510\Omega$.

CLOCK HIGH AND LOW TIME (USING EFI)



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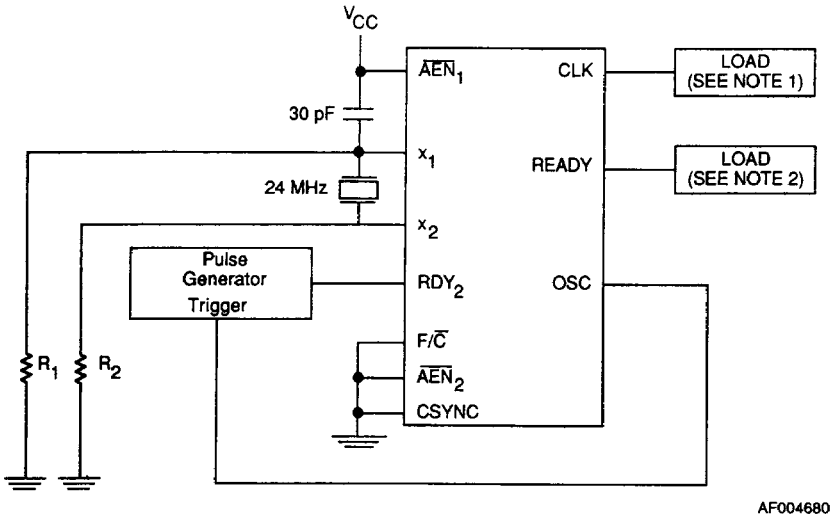
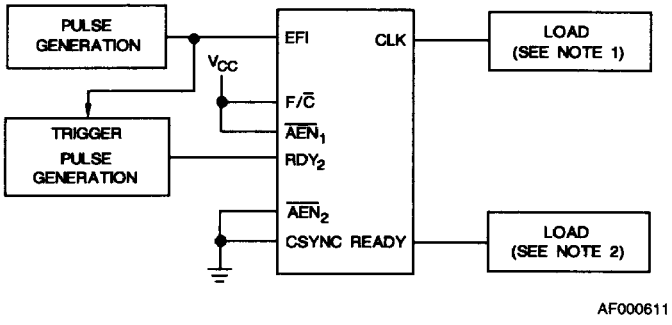
READY TO CLOCK (USING X_1, X_2)



$R_1 = R_2 = 510\Omega$.

READY TO CLOCK (USING EFI)



Notes: 1. $C_L = 100pF$
2. $C_L = 30pF$

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with Powers Applied
(COML, A-1) ..... 0°C to +70°C
(MIL) ..... −55°C to +125°C
All Output and Supply Voltages ..... −0.5V to +7.0V
All Input Voltage ..... −1.0V to +5.5V
Power Dissipation 1W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

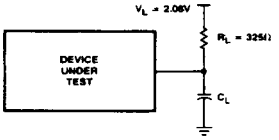
Operating ranges define those limits between which the functionality and parameters of the device are guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameters	Description	Test Conditions	Min	Max	Units
I_F	Forward Input Current ($\overline{ASYNC}$)	$V_F = 0.45V$		−1.3	mA
	Other Inputs	$V_F = 0.45V$		−0.5	
I_R	Reverse Input Current ($\overline{ASYNC}$)	$V_R = V_{CC}$		50	µA
	Other Inputs	$V_R = 5.25V$		50	
V_C	Input Forward Clamp Voltage	$I_C = -5mA$		−1.0	Volts
I_{CC}	Power Supply Current			162	mA
V_{IL}	Input LOW Voltage			0.8	Volts
V_{IH}	Input HIGH Voltage		2.0		Volts
V_{IHR}	Reset Input HIGH Voltage		2.6		Volts
V_{OL}	Output LOW Voltage	5mA		0.45	Volts
V_{OH}	Output HIGH Voltage CLK	−1mA	4.0	2.5	Volts
	Other Outputs	−1mA	2.4		
$V_{IHR}-V_{ILR}$	$\overline{RES}$ Input Hysteresis (Note 1)		0.25		Volts

Note 1. This specification is provided for reference only.

SWITCHING TESTING CIRCUIT (CLK, READY)



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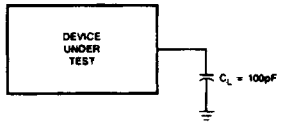
C_L = 100pF for CLK
C_L = 30pF for READY

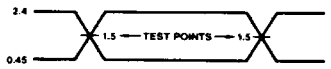
SWITCHING TESTING CIRCUIT (CLK, READY)



TC000680

C_L = 100pF

SWITCHING TESTING WAVEFORM (Input, output)



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AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 1.5V for both a logic "1" and "0".

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

TIMING REQUIREMENTS

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{EHEL}	External Frequency HIGH Time	90% – 90%V_{IN}	13			ns
t_{ELEH}	External Frequency LOW Time	10% – 10%V_{IN}	13			ns
t_{ELEL}	EFI Period	MIL (Note 1)	$t_{EHEL} + t_{ELEH} + \delta$			ns
		COM'L, A-1	33			
	XTAL Frequency		12		25	MHz
t_{R1VCL}	RDY_1, RDY_2 Active Setup to CLK	$\overline{ASYNC}$ = HIGH	35			ns
t_{R1VCH}	RDY_1, RDY_2 Active Setup to CLK	$\overline{ASYNC}$ = LOW	35			ns
t_{R1VCL}	RDY_1, RDY_2 Inactive Setup to CLK		35			ns
t_{CLR1X}	RDY_1, RDY_2 Hold to CLK		0			ns
t_{AYVCL}	$\overline{ASYNC}$ Setup to CLK		50			ns
t_{CLAYX}	$\overline{ASYNC}$ Hold to CLK		0			ns
t_{A1VR1V}	$\overline{AEN_1}$, $\overline{AEN_2}$ Setup to RDY_1, RDY_2		15			ns
t_{CLA1X}	$\overline{AEN_1}$, $\overline{AEN_2}$ Hold to CLK		0			ns
t_{YHEH}	CSYNC Setup to EFI		20			ns
t_{EHYL}	CSYNC Hold to EFI	MIL	20			ns
		COM'L, A-1	10			
t_{YHYL}	CSYNC Width		$2 \cdot t_{ELEL}$			ns
t_{I1HCL}	$\overline{RES}$ Setup to CLK	(Note 2)	65			ns
t_{CLI1H}	$\overline{RES}$ Hold to CLK	(Note 2)	20			ns
t_{ILIH}	Input Rise Time	From 0.8V to 2.0V			20	ns
t_{IHIL}	Input Fall Time	From 2.0V to 0.8V			12	ns

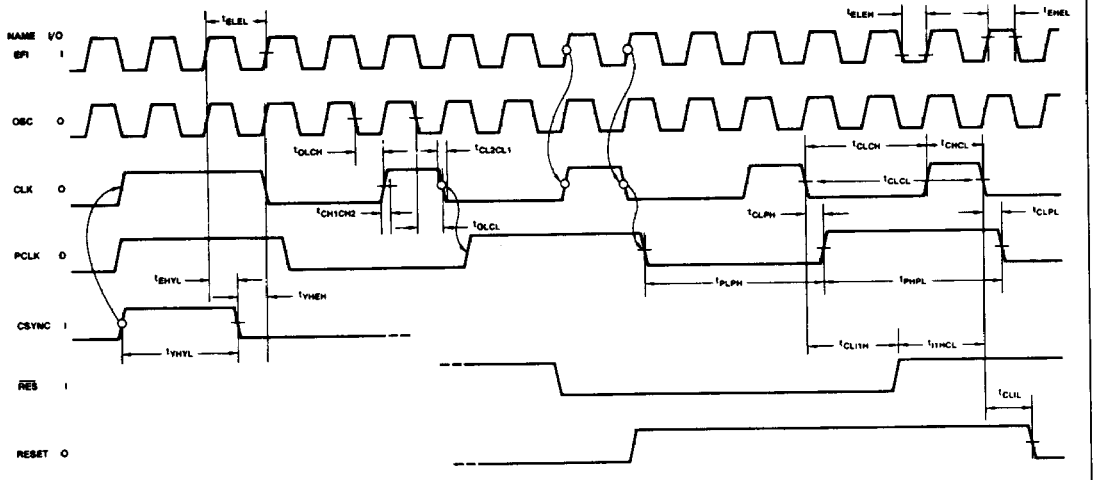
TIMING RESPONSES

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{CLCL}	CLK Cycle Period	MIL, COM'L	125			ns
		A-1	100			
t_{CHCL}	CLK HIGH Time	MIL, COM'L	(1/3 t_{CLCL}) + 2			ns
		A-1	39			
t_{CLCH}	CLK LOW Time	MIL, COM'L	(2/3 t_{CLCL}) - 15			ns
		A-1	53			
t_{CH1CH2}	CLK Rise or Fall Time	1.0V to 3.5V			10	ns
t_{CL2CL1}						
t_{PHPL}	PCLK HIGH Time		t_{CLCL} - 20			ns
t_{PLPH}	PCLK LOW Time		t_{CLCL} - 20			ns
t_{RYLCL}	Ready Inactive to CLK (See Note 4)		-8			ns
t_{RYHCH}	Ready Active to CLK (See Note 3)	MIL, COM'L	(2/3 t_{CLCL}) - 15			ns
		A-1	53			
t_{CLIL}	CLK to Reset Delay				40	ns
t_{CLPH}	CLK to PCLK HIGH Delay				22	ns
t_{CLPL}	CLK to PCLK LOW Delay				22	ns
t_{OLCH}	OSC to CLK HIGH Delay		-5		22	ns
t_{OLCL}	OSC to CLK LOW Delay		2		35	ns
t_{OLOH}	Output Rise Time (except CLK)	From 0.8V to 2.0V			20	ns
t_{OHOL}	Output Fall Time (except CLK)	From 2.0V to 0.8V			12	ns

Notes:
1. δ = EFI rise (5ns max) + EFI fall (5ns max).
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T_3 and T_W states.
4. Applies only to T_2 states.

SWITCHING WAVEFORMS

CLOCKS AND RESET SIGNALS



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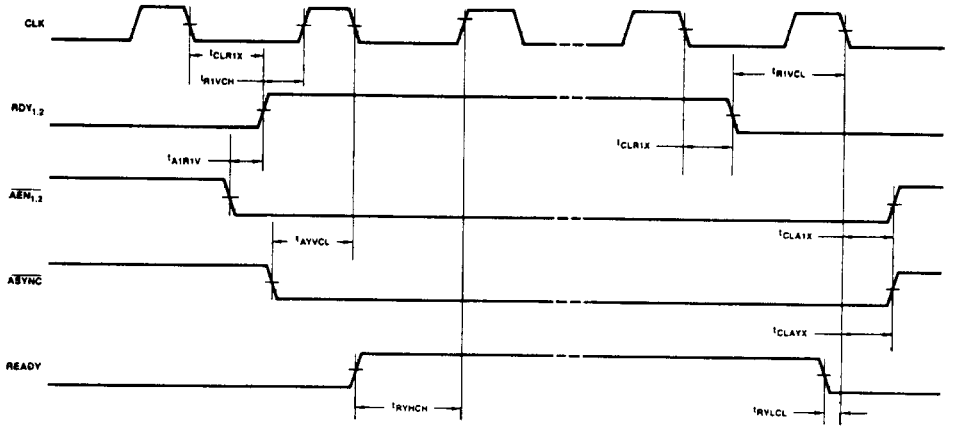
Note: All timing requirements are made at 1.5 volts, unless otherwise noted.

READY SIGNALS (FOR ASYNCHRONOUS DEVICES)



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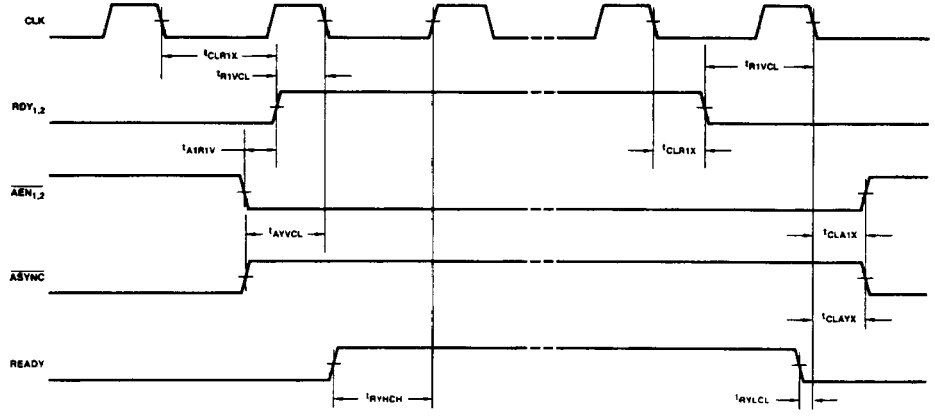
READY SIGNALS (FOR SYNCHRONOUS DEVICES)



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