Document Title

524,288 X 8 BIT CMOS MASK ROM

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	October 2, 2001	Preliminary

Preliminary

524,288 X 8 BIT CMOS MASK ROM

Features

- 524,288 x 8 bit organization
- Wide power supply range: +2.7V to +3.6V
- Access time: 150ns (max.)/3V~3.6V
  200ns (max.)/2.7V~3.3V
- Current: Operating: 15mA (max.)/3V~3.6V
  10mA (max.)/2.7V~3.3V
  Standby: 25ì A (max.)/3V~3.6V
  5ì A (max.)/2.7V~3.3V
- Mask Programmed for Chip Enable (power-down) CE/ $\overline{CE}$, Output Enable OE/ $\overline{OE}$ /NC
- Three-state outputs for wired-OR expansion
- Full static operation
- All inputs and outputs are directly TTL-compatible
- Available in 32-pin DIP, 32-pin SOP, 32-pin PLCC packages or in DICE FORM.

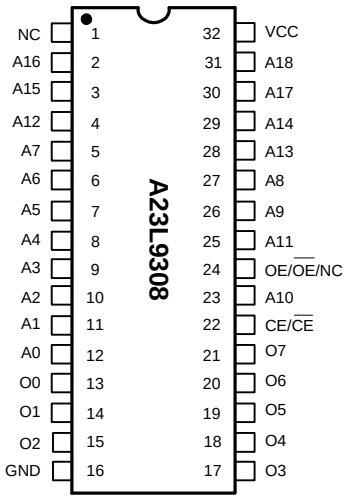
General Description

The A23L9308 high-performance Read Only Memory is configured as 524,288 x 8 bits. It is designed to be compatible with all microprocessors and similar applications where high-performance, large-bit storage, and simple interfacing are important design considerations. This device is designed for use with operating voltage from 2.7V to 3.6V.

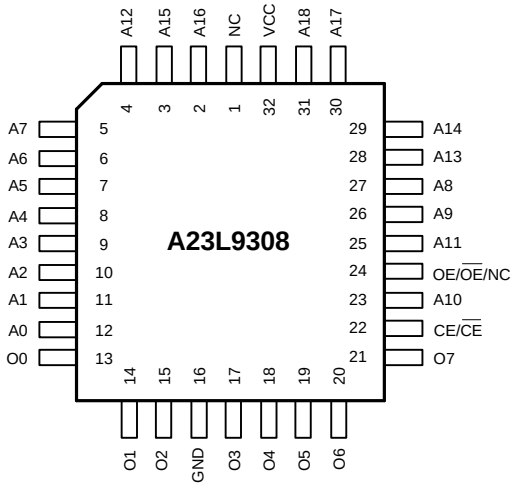
The A23L9308 offers an automatic POWER-DOWN controlled by the Chip Enable CE/ $\overline{CE}$ input. When CE/ $\overline{CE}$ goes low/high, the device will automatically POWER-DOWN and remain in a low power STANDBY mode as long as CE/ $\overline{CE}$ remains low/high. A23L9308 also offers OE/ $\overline{OE}$ /NC (Active High or Low or No Connection), which eliminates bus contention in multiple bus microprocessor systems.

Pin Configurations

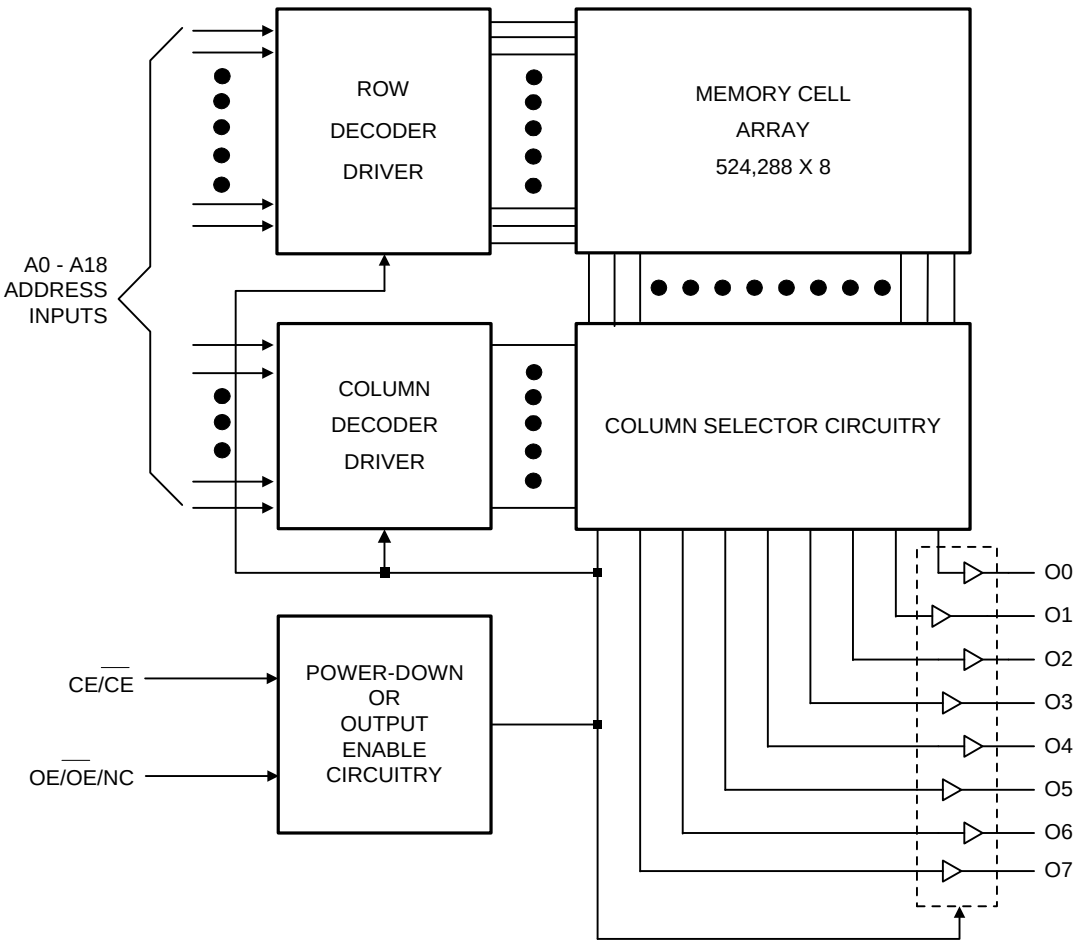
■ **P-DIP / SOP**



■ **PLCC**



Block Diagram



Pin Descriptions

Pin No.		Symbol	Description
32L DIP/SOP	32L PLCC		
2 - 12, 23, 25 - 31	2 - 12, 23, 25 - 31	A0 - A18	Address Inputs
22	22	CE/ $\overline{CE}$	Chip Enable Input (Note 1)
24	24	OE/ $\overline{OE}$ /NC	Output Enable (Note 1)
13 - 15, 17 - 21	13 - 15, 17 - 21	O0 - O7	Data Outputs
32	32	VCC	Power Supply
16	16	GND	Ground
1	1	NC	No Connection (Note 2)

Notes:
1. This pin is user-definable as active high or active low.
2. NC indicates "No Connection."

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C)

Symbol	Parameter	Min.	Max.	Unit
VCC	Supply Voltage	2.7	3.6	V
GND	Ground	0	0	V
V_{IH}	Input High Voltage	0.7* VCC	VCC+0.3	V
V_{IL}	Input Low Voltage	- 0.5	0.8	V

Absolute Maximum Ratings*

Ambient Operating Temperature . . . . . -10°C to + 80°C
Storage Temperature . . . . . -65°C to + 150°C
Supply Voltage to Ground Potential . . . . . -0.5V to + 7.0V
Output Voltage . . . . . -0.5V to VCC + 0.5V
Input Voltage . . . . . -0.5V to VCC + 0.5V
Power Dissipation 400mW

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to + 70°C, GND = 0V)

Symbol	Parameter	3V~3.6V		2.7V~3.3V		Unit	Conditions	Note
		Min.	Max.	Min.	Max.			
V_{OH}	Output High Voltage	2.15		2.15		V	I_{OH} = -0.4mA (3V)	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 1.6mA (3V)	
V_{IH}	Input High Voltage	0.7*VCC	VCC+0.5	0.7*VCC	VCC+0.5	V		
V_{IL}	Input Low Voltage	-0.5	0.6	-0.5	0.6	V		
$\lvert I_{LI} \rvert$	Input Leakage Current		+5		+5	µA	VCC = max. V_{IN} = VCC to GND	
$\lvert I_{LO} \rvert$	Output Leakage Current		+5		+5	µA	VCC = max. V_{OUT} = VCC to GND	1
I_{CC}	Operating Supply Current		15		10	mA	t_{CYC} = min.	2
I_{SB}	Standby Supply Current (TTL)		0.5		0.3	mA	$\overline{CE}$ = V_{IH}, CE = V_{IL}	
I_{SB1}	Standby Supply Current (CMOS)		25		5	µA	$\overline{CE}$ = VCC - 0.2V, CE = 0.2V	

Capacitance

Symbol	Parameter	Min.	Max.	Unit	Test Conditions	Note
C_I	Input Capacitance		10	pF	T_A = 25°C f = 1.0MHz	3
C_O	Output Capacitance		10	pF		

AC Characteristics

(T_A = 0°C to +70°C, VCC=3.0V~3.6V for -15, VCC=2.7V~3.3V for -20, GND = 0V)

Symbol	Parameter	A23L9308-15		A23L9308-20		Unit	Note
		Min.	Max.	Min.	Max.		
t_{CYC}	Cycle Time	150		200		ns	
t_{AA}	Address Access Time		150		200	ns	
t_{ACE}	Chip Enable Access Time		150		200	ns	
t_{AOE}	Output Enable Access Time		90		160	ns	
t_{OH}	Output Hold after Address Change	10		10		ns	
t_{LZ}	Output Low Z Delay	10		10		ns	4, 6
t_{HZ}	Output High Z Delay*		70		70	ns	5, 6

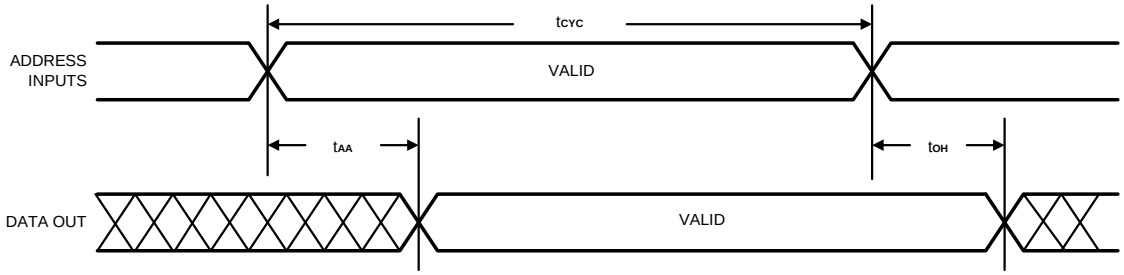
* t_{HZ} is specified from either OE / $\overline{OE}$ or CE / $\overline{CE}$ going disabled, whichever occurs first.

Notes:

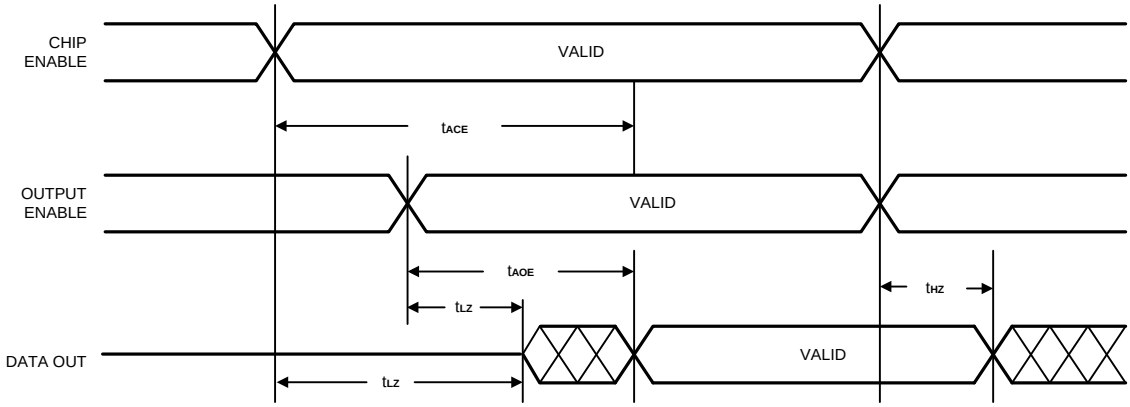
1. OE/CE = V_{IL}, $\overline{OE}$ / $\overline{CE}$ = V_{IH} (Output is unloaded)
2. V_{IN} = V_{IH}/V_{IL}, but OE/CE = V_{IH}, $\overline{OE}$ / $\overline{CE}$ = V_{IL} (Output is unloaded)
3. This parameter is periodically sampled and is not 100% tested. All pins, except pins under test, are tied to AC ground.
4. Output LOW impedance delay (t_{LZ}) is measured from $\overline{CE}$ or $\overline{OE}$ going active.
5. Output HIGH impedance delay (t_{HZ}) is measured from $\overline{CE}$ or $\overline{OE}$ going inactive.
6. This parameter is sampled and not 100% tested.

Timing Waveforms

Propagation Delay from Address (CE/ $\overline{CE}$ = Active, OE/ $\overline{OE}$ = Active)



Propagation Delay from Chip Enable or Output Enable (Address Valid)



AC Test Conditions

Applied Voltage	2.7V~3.6V
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Time	10 ns
Timing Measurement Reference Level	V_{IN} = 1.5V V_{OUT} = 1.5V
Output Load	1 TTL gate and C_L = 100pF

Function Table

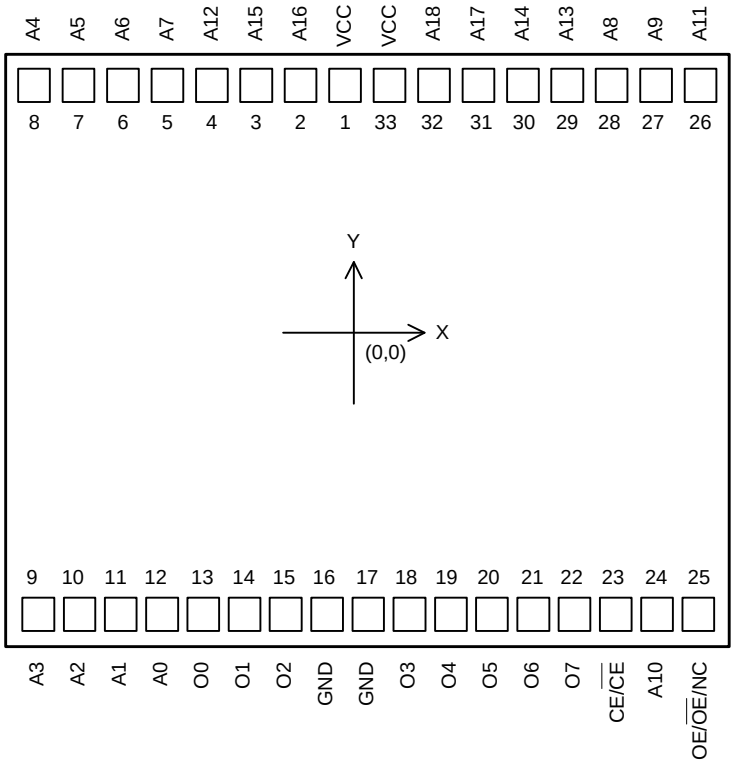
CE/ $\overline{CE}$	OE/ $\overline{OE}$ /NC	O0 - O7	Mode
A	A	Data Out	Read
I	X	Hi - Z	Power-down
A	I	Hi - Z	Output Disable

1. CE/ $\overline{CE}$ and OE/ $\overline{OE}$ /NC are mask programmable as either active low, active high, or no connection.
2. "A" means "Active," "I" means "Inactive," and "X" means "Either."

Ordering Information

Part No.	Access Time (ns)	Package
A23L9308-15	150	32L DIP
A23L9308M-15	150	32L SOP
A23L9308L-15	150	32L PLCC
A23L9308H-15	150	DICE FORM
A23L9308-20	200	32L DIP
A23L9308M-20	200	32L SOP
A23L9308L-20	200	32L PLCC
A23L9308H-20	200	DICE FORM

Pad Configurations



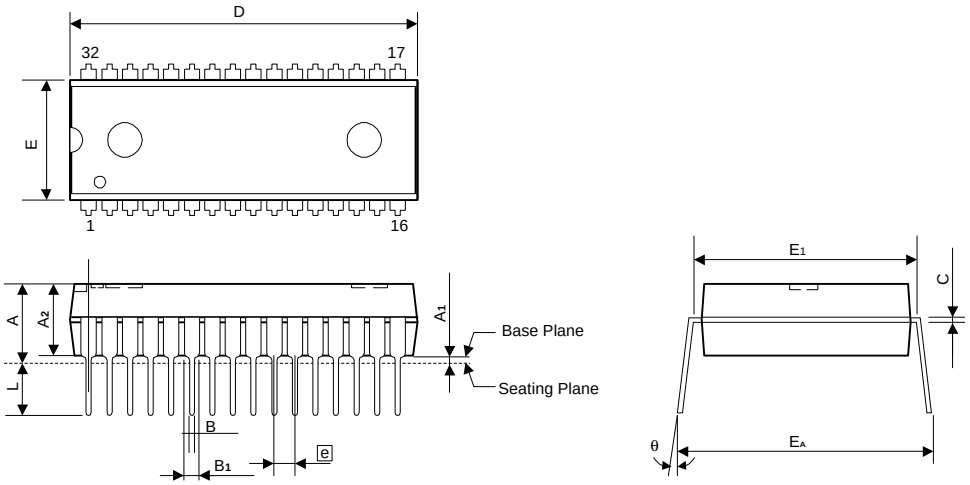
Pad Location

Pad No.	Pad Name	Coordinate (um)	
		X	Y
1	VCC	-73.6	1406.3
2	A16	-259.9	1419.2
3	A15	-409.9	1419.2
4	A12	-532.9	1419.2
5	A7	-682.9	1419.2
6	A6	-805.9	1419.2
7	A5	-955.9	1419.2
8	A4	-1078.9	1419.2
9	A3	-1079.3	-1419.7
10	A2	-956.3	-1419.2
11	A1	-806.3	-1419.2
12	A0	-683.3	-1419.2
13	O0	-529.3	-1419.7
14	O1	-406.3	-1419.7
15	O2	-254.8	-1419.7
16	GND	-131.8	-1419.7
17	GND	-8.8	-1417.7

Pad No.	Pad Name	Coordinate (um)	
		X	Y
18	O3	138.7	-1419.7
19	O4	261.7	-1419.7
20	O5	413.2	-1419.7
21	O6	536.2	-1419.7
22	O7	687.7	-1419.7
23	CE/ $\overline{CE}$	810.7	-1419.2
24	A10	960.7	-1419.2
25	OE/ $\overline{OE}$ /NC	1083.7	-1419.2
26	A11	1083.3	1419.2
27	A9	960.3	1419.2
28	A8	810.3	1419.2
29	A13	687.3	1419.2
30	A14	537.3	1419.2
31	A17	414.3	1419.2
32	A18	264.3	1419.2
33	VCC	97.1	1417.7

Package Information

P-DIP 32L Outline Dimensions unit: inches/mm



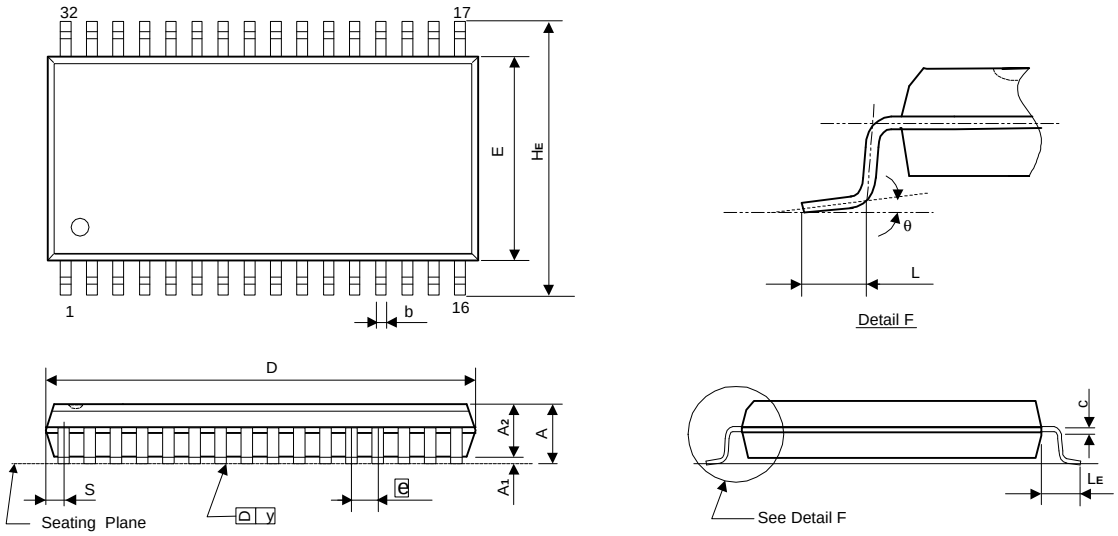
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.210	-	-	5.334
A_1	0.015	-	-	0.381	-	-
A_2	0.149	0.154	0.159	3.785	3.912	4.039
B	-	0.018	-	-	0.457	-
B_1	-	0.050	-	-	1.270	-
C	-	0.010	-	-	0.254	-
D	1.645	1.650	1.655	41.783	41.91	42.037
E	0.537	0.542	0.547	13.64	13.767	13.894
E_1	0.590	0.600	0.610	14.986	15.240	15.494
E_A	0.630	0.650	0.670	16.002	16.510	17.018
e	-	0.100	-	-	2.540	-
L	0.120	0.130	0.140	3.048	3.302	3.556
θ	0°	-	15°	0°	-	15°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.

Package Information

SOP (W.B.) 32L Outline Dimensions

unit: inches/mm

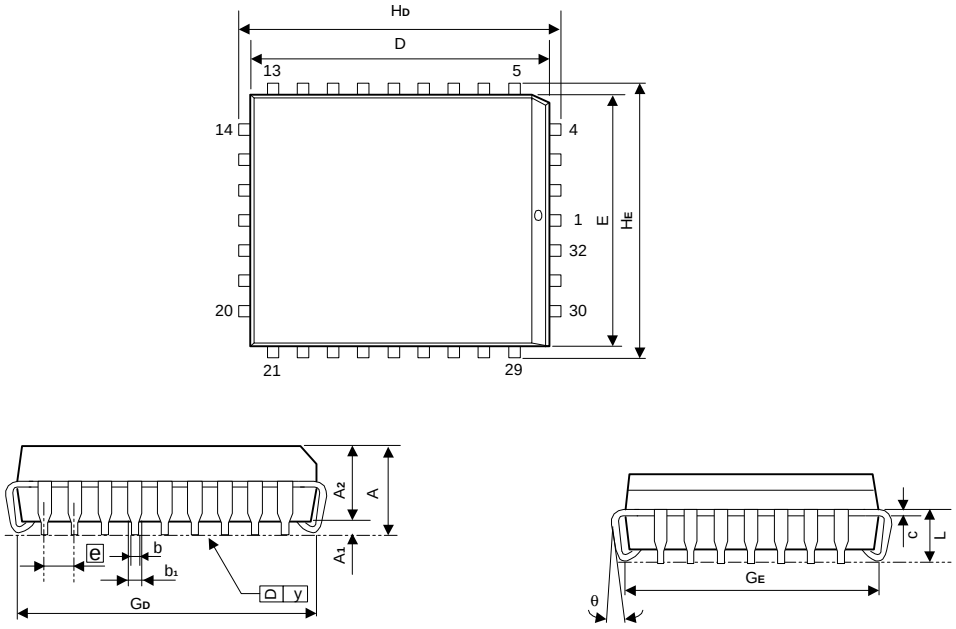


Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.118	-	-	3.00
A_1	0.004	-	-	0.10	-	-
A_2	0.101	0.106	0.111	2.57	2.69	2.82
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.006	0.008	0.012	0.15	0.20	0.31
D	-	0.805	0.817	-	20.45	20.75
E	0.440	0.445	0.450	11.18	11.30	11.43
e	0.044	0.050	0.056	1.12	1.27	1.42
H_E	0.546	0.556	0.566	13.87	14.12	14.38
L	0.023	0.031	0.039	0.58	0.79	0.99
L_E	0.047	0.055	0.063	1.19	1.40	1.60
S	-	-	0.036	-	-	0.91
y	-	-	0.004	-	-	0.10
θ	0°	-	10°	0°	-	10°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

Package Information

PLCC 32L Outline Dimension unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.134	-	-	3.40
A_1	0.0185	-	-	0.47	-	-
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.021	0.41	0.46	0.54
C	0.008	0.010	0.014	0.20	0.254	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	-	-	0.003	-	-	0.075
θ	0°	-	10°	0°	-	10°

Notes:
1. Dimensions D and E do not include resin fins.
2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.