Preliminary *256K X 16 CMOS DYNAMIC RAM WITH EDO PAGE MODE*

Document Title

256K X 16 CMOS DYNAMIC RAM WITH EDO PAGE MODE

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	January 26, 1999	Preliminary
0.1	Modify AC data	August 20, 2002	

Preliminary 256K X 16 CMOS DYNAMIC RAM WITH EDO PAGE MODE

Features

- Organization: 262,144 words X 16 bits
- Part Identification
  - A42L8316 (512 Ref.)
- Single 3.3V power supply/built-in VBB generator
- Low power consumption
  - Operating: 110mA (-30 max)
  - Standby: 2.5mA (TTL), 1.5mA (CMOS)
    1.0mA (Self-refresh current)
- High speed
  - 30/35/40 ns $\overline{RAS}$ access time
  - 16/17/18 ns column address access time
  - 9/10/11 ns $\overline{CAS}$ access time
  - 14/16/18 ns EDO Page Mode Cycle Time
- Industrial operating temperature range: -40°C to 85°C for -U
- Fast Page Mode with Extended Data Out
- Separate $\overline{CAS}$ ($\overline{UCAS}$, $\overline{LCAS}$) for byte selection
- 512 Refresh Cycle in 8ms
- Read-modify-write, $\overline{RAS}$ -only, $\overline{CAS}$ -before- $\overline{RAS}$, Hidden refresh capability
- TTL-compatible, three-state I/O
- JEDEC standard packages
  - 400mil, 40-pin SOJ
  - 400mil, 40/44 TSOP type II package

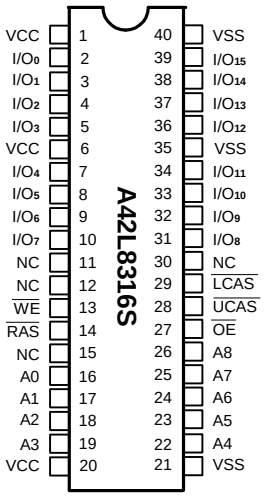
General Description

The A42L8316 is a new generation randomly accessed memory for graphics, organized in a 262,144-word by 16-bit configuration. This product can execute Byte Write and Byte Read operation via two $\overline{CAS}$ pins.
The A42L8316 offers an accelerated Fast Page Mode cycle with a feature called Extended Data Out (EDO).

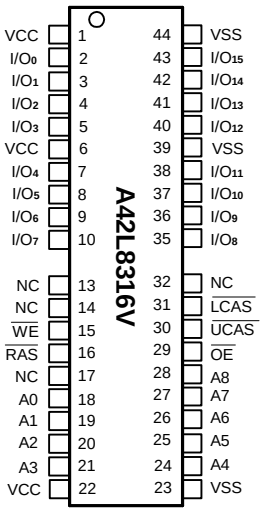
This allow random access of up to 512 words within a row at a 71/62/55 MHz EDO cycle, making the A42L8316 ideally suited for graphics, digital signal processing and high performance computing systems.

Pin Configuration

■ SOJ



■ TSOP



Pin Descriptions

Symbol	Description
A0 – A8	Address Inputs
I/O0 - I/O15	Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{LCAS}$	Column Address Strobe for Lower Byte (I/O0 – I/O7)
$\overline{UCAS}$	Column Address Strobe for Upper Byte (I/O8 – I/O15)
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	3.3V Power Supply
VSS	Ground
NC	No Connection

Selection Guide

Symbol	Description	-30	-35	-40	Unit
t_{RAC}	Maximum $\overline{RAS}$ Access Time	30	35	40	ns
t_{AA}	Maximum Column Address Access Time	16	17	18	ns
t_{CAC}	Maximum $\overline{CAS}$ Access Time	9	10	11	ns
t_{OEA}	Maximum Output Enable ($\overline{OE}$) Access Time	9	10	11	ns
t_{RC}	Minimum Read or Write Cycle Time	54	62	70	ns
t_{PC}	Minimum EDO Cycle Time	14	16	18	ns

Functional Description

The A42L8316 reads and writes data by multiplexing an 18-bit address into a 9-bit row and 9-bit column address. $\overline{RAS}$ and $\overline{CAS}$ are used to strobe the row address and the column address, respectively.

The A42L8316 has two $\overline{CAS}$ inputs: $\overline{LCAS}$ controls I/O_0-I/O_7, and $\overline{UCAS}$ controls I/O_8 - I/O_{15}, $\overline{UCAS}$ and $\overline{LCAS}$ function in an identical manner to $\overline{CAS}$ in that either will generate an internal $\overline{CAS}$ signal. The $\overline{CAS}$ function and timing are determined by the first $\overline{CAS}$ ($\overline{UCAS}$ or $\overline{LCAS}$) to transition low and by the last to transition high. Byte Read and Byte Write are controlled by using $\overline{LCAS}$ and $\overline{UCAS}$ separately.

A Read cycle is performed by holding the $\overline{WE}$ signal high during $\overline{RAS}$/$\overline{CAS}$ operation. A Write cycle is executed by holding the $\overline{WE}$ signal low during $\overline{RAS}$/$\overline{CAS}$ operation; the input data is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs later. The data inputs and outputs are routed through 16 common I/O pins, with $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{OE}$ controlling the in direction.

EDO Page Mode operation all 512 columns within a selected row to be randomly accessed at a high data rate. A EDO Page Mode cycle is initiated with a row address latched by $\overline{RAS}$ followed by a column address latched by $\overline{CAS}$. While holding $\overline{RAS}$ low, $\overline{CAS}$ can be toggled to strobe changing column addresses, thus achieving shorter cycle times.

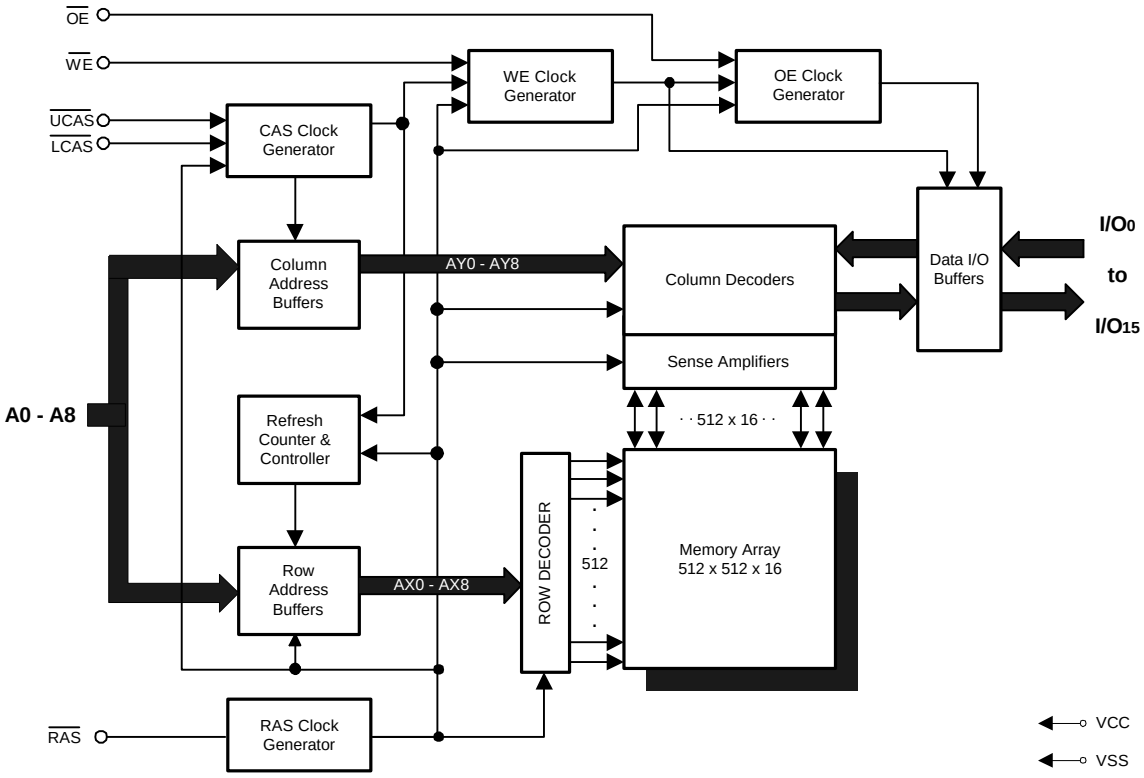
The A42L8316 offers an accelerated Fast Page Mode cycle through a feature called Extended Data Out, which keeps the output drivers on during the $\overline{CAS}$ precharge time (t_{cp}). Since data can be output after $\overline{CAS}$ goes high, the user is not required to wait for valid data to appear before starting the next access cycle. Data-out will remain valid as long as $\overline{RAS}$ and $\overline{OE}$ are low, and $\overline{WE}$ is high; this is the only characteristic which differentiates Extended Data Out operation from a standard Read or Fast Page Read.

A memory cycle is terminated by returning both $\overline{RAS}$ and $\overline{CAS}$ high. Memory cell data will retain its correct state by maintaining power and accessing all 512 combinations of the 9-bit row addresses, regardless of sequence, at least once every 8ms through any $\overline{RAS}$ cycle (Read, Write) or $\overline{RAS}$ Refresh cycle ($\overline{RAS}$-only, CBR, or Hidden). The CBR Refresh cycle automatically controls the row addresses by invoking the refresh counter and controller.

Power-On

The initial application of the VCC supply requires a 200 µs wait followed by a minimum of any eight initialization cycles containing a $\overline{RAS}$ clock. During Power-On, the VCC current is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with VCC or be held at a valid V_{IH} during Power-On to avoid current surges.

Block Diagram



Recommended Operating Conditions (Ta = 0°C to +70°C or -40°C to +85°C)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VCC	Power Supply	3.0	3.3	3.6	V	1
VSS	Input High Voltage	0.0	0.0	0.0	V	1
V_{IH}	Input High Voltage	2.0	-	VCC + 0.3	V	1
V_{IL}	Input Low Voltage	-0.5	-	0.8	V	1

Truth Table

Function	$\overline{RAS}$	$\overline{UCAS}$	$\overline{LCAS}$	$\overline{WE}$	$\overline{OE}$	Address	I/Os	Notes
Standby	H	H	H	X	X	X	High-Z	
Read: Word	L	L	L	H	L	Row/Col.	Data Out	
Read: Lower Byte	L	H	L	H	L	Row/Col.	I/O_{0-7} = Data Out I/O_{8-15} = High-Z	
Read: Upper Byte	L	L	H	H	L	Row/Col.	I/O_{0-7} = High-Z I/O_{8-15} = Data Out	
Write: Word	L	L	L	L	H	Row/Col.	Data In	
Write: Lower Byte	L	H	L	L	H	Row/Col.	I/O_{0-7} = Data In I/O_{8-15} = X	
Write: Upper Byte	L	L	H	L	H	Row/Col.	I/O_{0-7} = X I/O_{8-15} = Data In	
Read-Write	L	L	L	H→L	L→H	Row/Col.	Data Out → Data In	1,2
EDO-Page-Mode Read: Hi-Z								
-First cycle	L	H→L	H→L	H	H→L	Row/Col.	Data Out	2
-Subsequent Cycles	L	H→L	H→L	H	H→L	Col.	Data Out	2
EDO-Page-Mode Write								
-First cycle	L	H→L	H→L	L	H	Row/Col.	Data In	1
-Subsequent Cycles	L	H→L	H→L	L	H	Col.	Data In	1
EDO-Page-Mode Read-Write								
-First cycle	L	H→L	H→L	H→L	L→H	Row/Col.	Data Out → Data In	1, 2
-Subsequent Cycles	L	H→L	H→L	H→L	L→H	Col.	Data Out → Data In	1, 2
Hidden Refresh Read	L→H→L	L	L	H	L	Row/Col.	Data Out	2
Hidden Refresh Write	L→H→L	L	L	L	X	Row/Col.	Data In → High-Z	1
$\overline{RAS}$-Only Refresh	L	H	H	X	X	Row	High-Z	
CBR Refresh	H→L	L	L	X	X	X	High-Z	3
Self Refresh	H→L	L	L	H	X	X	High-Z	

Note: 1. Byte Write may be executed with either $\overline{UCAS}$ or $\overline{LCAS}$ active.
2. Byte Read may be executed with either $\overline{UCAS}$ or $\overline{LCAS}$ active.
3. Only one $\overline{CAS}$ signal ($\overline{UCAS}$ or $\overline{LCAS}$) must be active.

Absolute Maximum Ratings*

Input Voltage (Vin) . . . . . -0.5V to +4.6V
Output Voltage (Vout) . . . . . -0.5V to +4.6V
Power Supply Voltage (VCC) . . . . . -0.5V to +4.6V
Operating Temperature (T_{OPR}) . . . . . 0°C to +70°C
Storage Temperature (T_{STG}) . . . . . -55°C to +150°C
Soldering Temperature X Time (T_{SOLDER}) . . . . . 260°C X 10sec
Power Dissipation (P_D) 1W
Short Circuit Output Current (Iout) 50mA
Latch-up Current 200mA

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of these specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (VCC = 3.3V ± 0.3V, VSS = 0V, Ta = 0°C to +70°C or -40°C to +85°C)

Symbol	Parameter	-30		-35		-40		Unit	Test Conditions	Notes
		Min.	Max.	Min.	Max.	Min.	Max.			
I_{IL}	Input Leakage Current	-5	+5	-5	+5	-5	+5	µA	0V ≤ Vin ≤ VCC Pins not under Test = 0V	
I_{OL}	Output Leakage Current	-5	+5	-5	+5	-5	+5	µA	D_{OUT} disabled, 0V ≤ Vout ≤ VCC	
I_{CC1}	Operating Power Supply Current	-	110	-	105	-	100	mA	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ and Address cycling; t_{RC} = min.	1, 2
I_{CC2}	TTL Supply Current Supply Current	-	2.5	-	2.5	-	2.5	mA	$\overline{RAS} = \overline{UCAS} = \overline{LCAS} =$ V_{IH}	
I_{CC3}	Average Power Supply Current, $\overline{RAS}$ Refresh Mode	-	110	-	105	-	100	mA	$\overline{RAS}$ and Address cycling, $\overline{UCAS} = \overline{LCAS}$ = V_{IH}, t_{RC} = min.	1
I_{CC4}	EDO Page Mode Average Power Supply Current	-	110	-	105	-	100	mA	$\overline{RAS}$ and address = V_{IL}, $\overline{UCAS}$, $\overline{LCAS}$ and Address cycling; t_{PC} = min.	1, 2
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Power Supply Current	-	110	-	105	-	100	mA	$\overline{RAS}$ and $\overline{UCAS}$ or $\overline{LCAS}$ cycling; t_{RC} = min.	1
I_{CC6}	CMOS Standby Power Supply Current	-	1.5	-	1.5	-	1.5	mA	$\overline{RAS} = \overline{UCAS} = \overline{LCAS}$ = VCC - 0.2V	
I_{CC7}	Self Refresh Mode Current	-	1.0	-	1.0	-	1.0	mA	$\overline{RAS} = \overline{CAS} \leq$ VSS+0.2V All other input high levels are VCC-0.2V or input low levels are VSS +0.2V	
V_{OH}	Output Voltage	2.4	-	2.4	-	2.4	-	V	I_{OUT} = -2.0mA	
V_{OL}		-	0.4	-	0.4	-	0.4	V	I_{OUT} = 2.0mA	

AC Characteristics (VCC = 3.3V ± 0.3V, VSS = 0V, Ta = 0°C to +70°C or -40°C to +85°C)

Test Conditions:

Input timing reference level: V_{IH}/V_{IL}=2.0V/0.8V
Output reference level: V_{OH}/V_{OL}=2.0V/0.8V
Output Load: 2TTL gate + CL (50pF)
Assumed t_T=2ns

#	Std Symbol	Parameter	-30		-35		-40		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
	t_T	Transition Time (Rise and Fall)	1	50	1	50	1	50	ns	4, 5
1	t_{RC}	Random Read or Write Cycle Time	54	-	62	-	70	-	ns	
2	t_{RP}	$\overline{RAS}$ Precharge Time	20	-	23	-	26	-	ns	
3	t_{RAS}	$\overline{RAS}$ Pulse Width	30	10K	35	10K	40	10K	ns	
4	t_{CAS}	$\overline{CAS}$ Pulse Width	5	10K	6	10K	7	10K	ns	
5	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	10	21	10	25	10	29	ns	6
6	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	8	14	8	18	8	22	ns	7
7	t_{RSH}	$\overline{CAS}$ to $\overline{RAS}$ Hold Time	5	-	6	-	7	-	ns	
8	t_{CSH}	$\overline{CAS}$ Hold Time	29	-	31	-	33	-	ns	
9	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
10	t_{ASR}	Row Address Setup Time	0	-	0	-	0	-	ns	
11	t_{RAH}	Row Address Hold Time	5	-	6	-	7	-	ns	
12	t_{CLZ}	$\overline{CAS}$ to Output in Low Z	3	-	3	-	3	-	ns	8
13	t_{RAC}	Access Time from $\overline{RAS}$	-	30	-	35	-	40	ns	6,7
14	t_{CAC}	Access Time from $\overline{CAS}$	-	9	-	10	-	11	ns	6, 13
15	t_{AA}	Access Time from Column Address	-	16	-	17	-	18	ns	7, 13
16	t_{OEA}	$\overline{OE}$ Access Time	-	9	-	10	-	11	ns	
17	t_{AR}	Column Address Hold Time from $\overline{RAS}$	26	-	31	-	36	-	ns	

AC Characteristics (continued) (VCC = 3.3V ± 0.3V, VSS = 0V, Ta = 0°C to +70°C or -40°C to +85°C)

Test Conditions:
- Input timing reference level: V_{IH}/V_{IL}=2.0V/0.8V
- Output reference level: V_{OH}/V_{OL}=2.0V/0.8V
- Output Load: 2TTL gate + CL (50pF)
- Assumed t_T=2ns

#	Std Symbol	Parameter	-30		-35		-40		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
18	t_{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	
19	t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	9
20	t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$	0	-	0	-	0	-	ns	9
21	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	16	-	17	-	18	-	ns	
22	t_{COH}	Output Hold After $\overline{CAS}$ Low	3	-	3	-	3	-	ns	
23	t_{OFF}	Output Buffer Turn-Off Delay Time	-	3	-	3	-	3	ns	8, 10
24	t_{ASC}	Column Address Setup Time	0	-	0	-	0	-	ns	
25	t_{CAH}	Column Address Hold Time	5	-	6	-	7	-	ns	
26	t_{OES}	$\overline{OE}$ Low to $\overline{CAS}$ High Set Up	6	-	7	-	8	-	ns	
27	t_{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	11
28	t_{WCH}	Write Command Hold Time	5	-	6	-	7	-	ns	11
29	t_{WCR}	Write Command Hold Time to $\overline{RAS}$	26	-	31	-	36	-	ns	
30	t_{WP}	Write Command Pulse Width	5	-	6	-	7	-	ns	
31	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	9	-	10	-	11	-	ns	
32	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	7	-	7	-	7	-	ns	
33	t_{DS}	Data-in setup Time	0	-	0	-	0	-	ns	12
34	t_{DH}	Data-in Hold Time	5	-	6	-	7	-	ns	12
35	t_{DHR}	Data-in Hold Time to $\overline{RAS}$	26	-	31	-	36	-	ns	

AC Characteristics (continued) (VCC = 3.3V ± 0.3V, VSS = 0V, Ta = 0°C to +70°C or -40°C to +85°C)

Test Conditions:
- Input timing reference level: V_{IH}/V_{IL}=2.0V/0.8V
- Output reference level: V_{OH}/V_{OL}=2.0V/0.8V
- Output Load: 2TTL gate + CL (50pF)
- Assumed t_T=2ns

#	Std Symbol	Parameter	-30		-35		-40		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
36	t_{RWC}	Read-Modify-Write Cycle Time	75	-	85	-	95	-	ns	
37	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time (Read-Modify-Write)	40	-	46	-	52	-	ns	11
38	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time (Read-Modify-Write)	19	-	21	-	23	-	ns	11
39	t_{AWD}	Column Address to $\overline{WE}$ Delay Time (Read-Modify-Write)	26	-	28	-	30	-	ns	11
40	t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$	5	-	6	-	7	-	ns	
41	t_{OEP}	$\overline{OE}$ High Pulse Width	5	-	5	-	5	-	ns	
42	t_{PC}	Read or Write Cycle Time (EDO Page)	14	-	16	-	18	-	ns	14
43	t_{CPA}	Access Time from $\overline{CAS}$ Precharge (EDO Page)	-	16	-	18	-	20	ns	13
44	t_{CP}	$\overline{CAS}$ Precharge Time	5	-	6	-	7	-	ns	
45	t_{PCM}	EDO Page Mode RMW Cycle Time	37	-	40	-	43	-	ns	
46	t_{CRW}	EDO Page Mode $\overline{CAS}$ Pulse Width (RMW)	28	-	30	-	32	-	ns	
47	t_{RASP}	$\overline{RAS}$ Pulse Width (EDO Page)	30	200K	35	200K	40	200K	ns	
48	t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$)	5	-	5	-	5	-	ns	3
49	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$)	10	-	10	-	10	-	ns	3
50	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	3

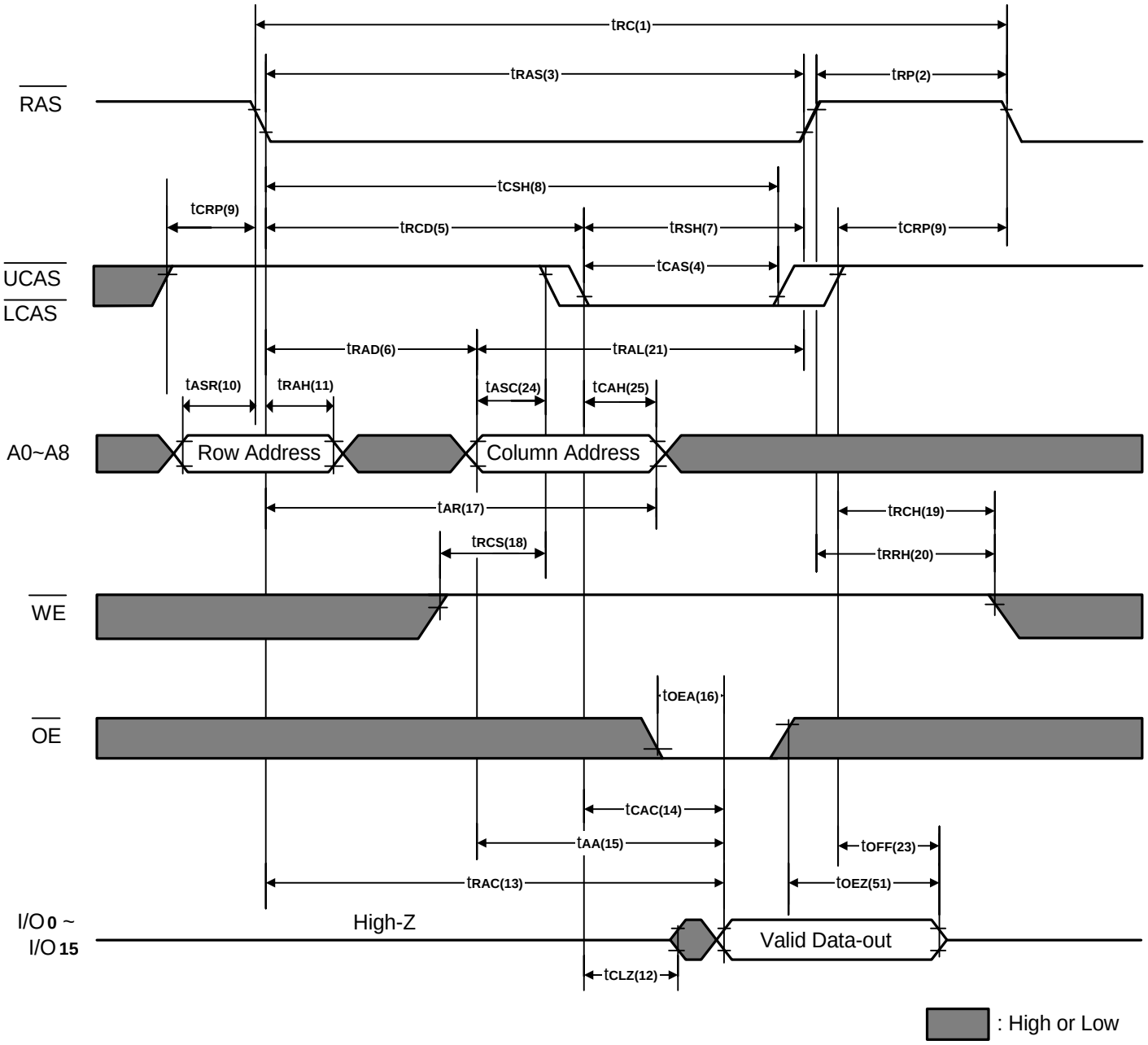
AC Characteristics (continued) (VCC = 3.3V ± 0.3V, VSS = 0V, Ta = 0°C to +70°C or -40°C to +85°C)

Test Conditions:
- Input timing reference level: V_{IH}/V_{IL}=2.0V/0.8V
- Output reference level: V_{OH}/V_{OL}=2.0V/0.8V
- Output Load: 2TTL gate + CL (50pF)
- Assumed t_T=2ns

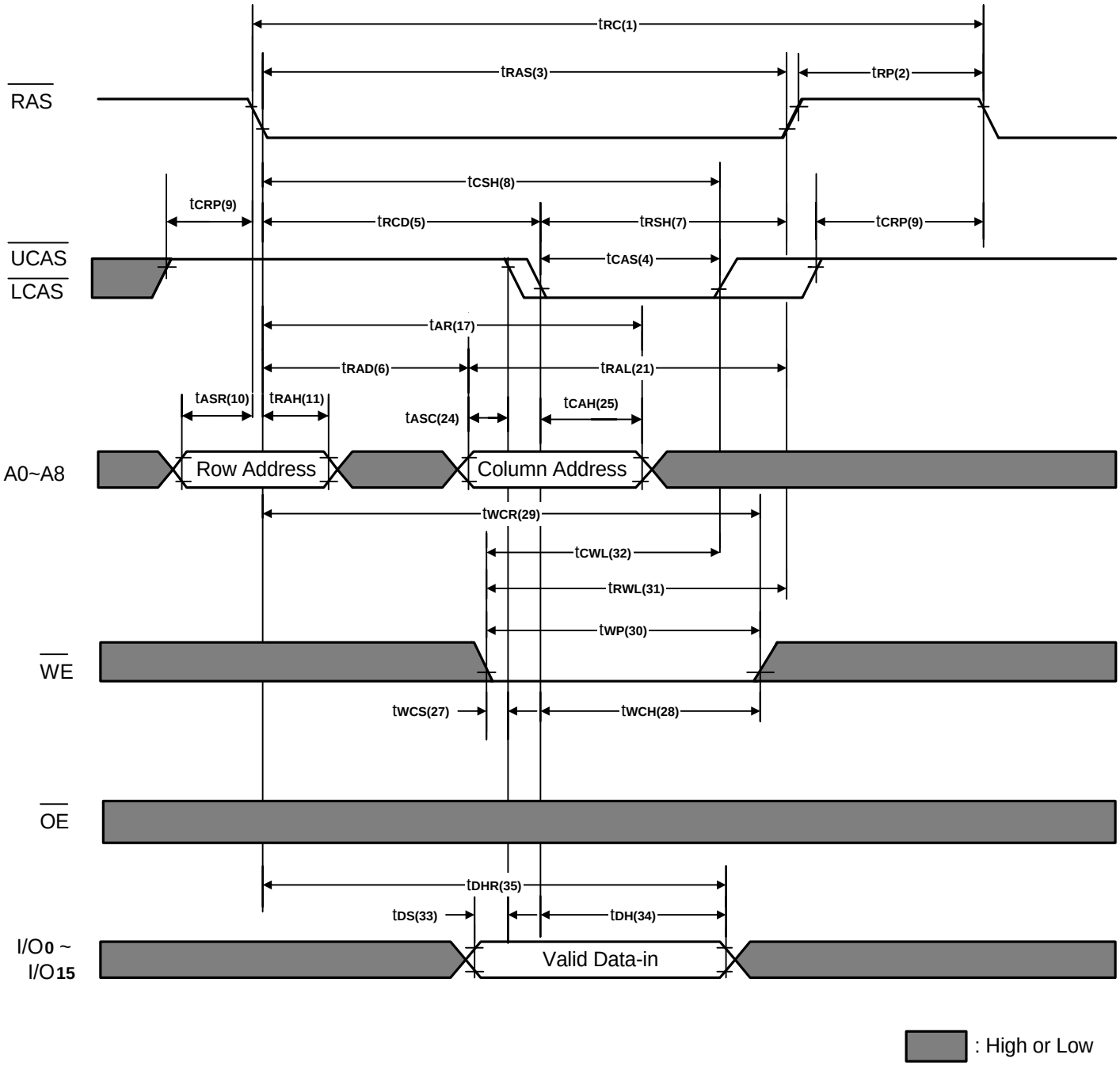
#	Std Symbol	Parameter	-30		-35		-40		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
51	t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	-	3	-	3	-	3	ns	8
52	t_{RASS}	$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	100	-	100	-	100	-	µs	
53	t_{RPS}	$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	54	-	62	-	70	-	ns	
54	t_{CHS}	$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	-50	-	-50	-	-50	-	ns	

Notes:
1. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.
3. An initial pause of 200µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required. 8 initialization cycles are required after extended periods of bias without clocks.
4. AC Characteristics assume t_T = 2ns. All AC parameters are measured with a load equivalent to two TTL loads and 50pF, V_{IL} (min.) ≥ GND and V_{IH} (max.) ≤ VCC.
5. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
7. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
8. Assumes three state test load (5pF and a 500Ω Thevenin equivalent).
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels.
11. t_{WCS}, t_{WCH}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS} ≥ t_{WCS} (min.) and t_{WCH} ≥ t_{WCH} (min.), the cycle is an early write cycle and data-out pins will remain open circuit, high impedance, throughout the entire cycle. If t_{RWD} ≥ t_{RWD} (min.) , t_{CWD} ≥ t_{CWD} (min.) and t_{AWD} ≥ t_{AWD} (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.
12. These parameters are referenced to $\overline{UCAS}$ and $\overline{LCAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
14. t_{ASC} ≥ t_{CP} to achieve t_{PC} (min.) and t_{CPA} (max.) values.

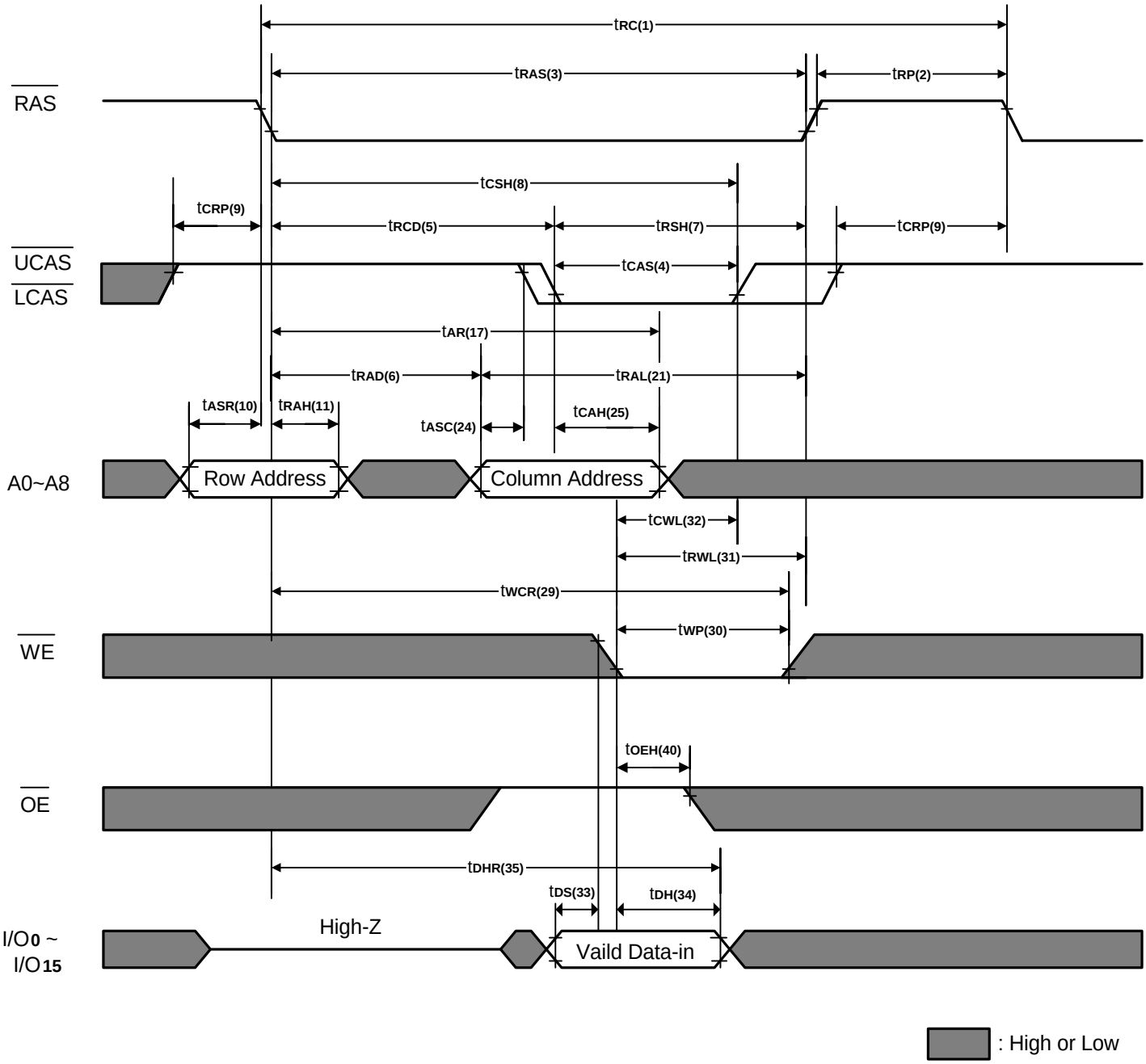
Word Read Cycle



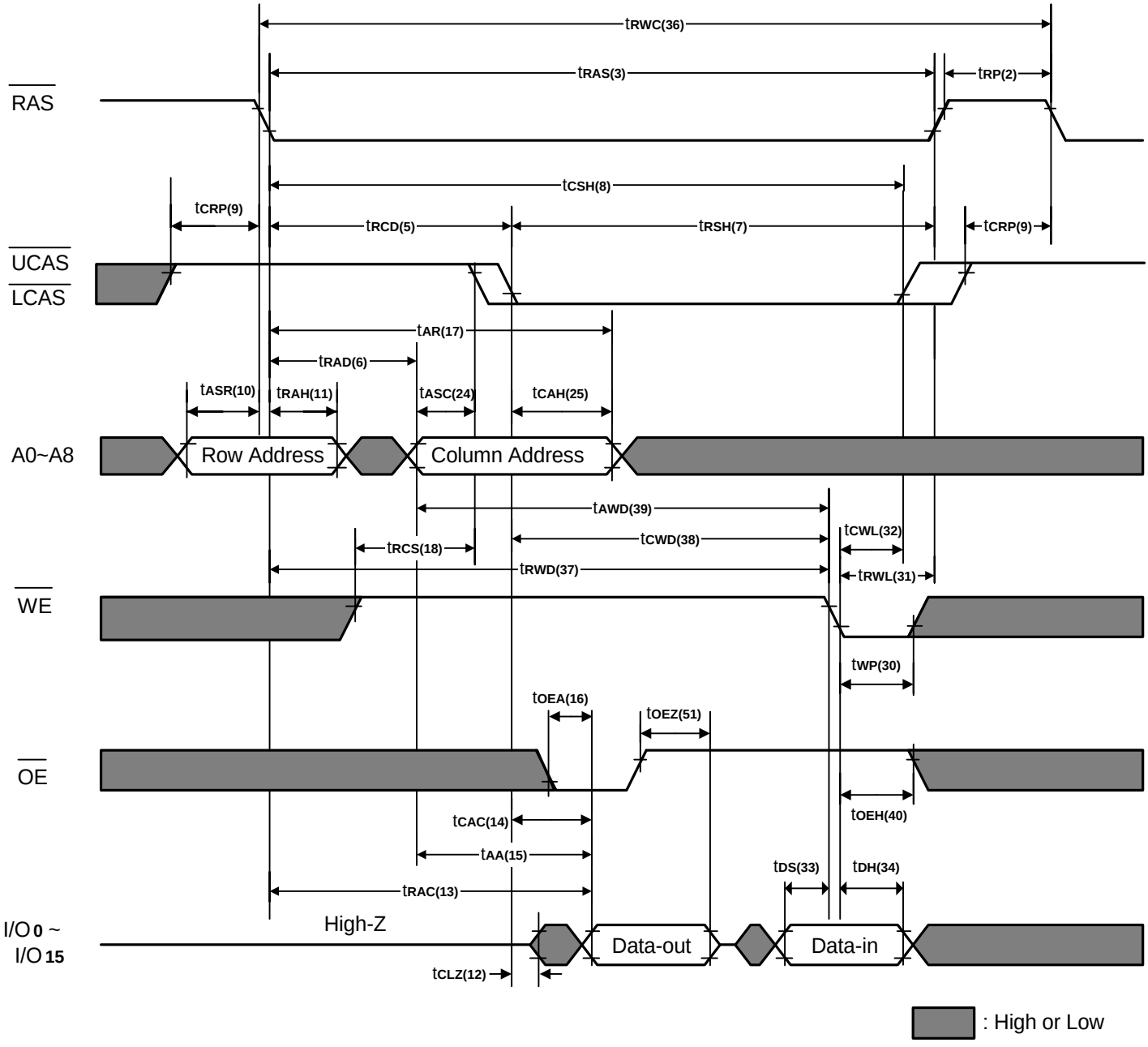
Word Write Cycle (Early Write)



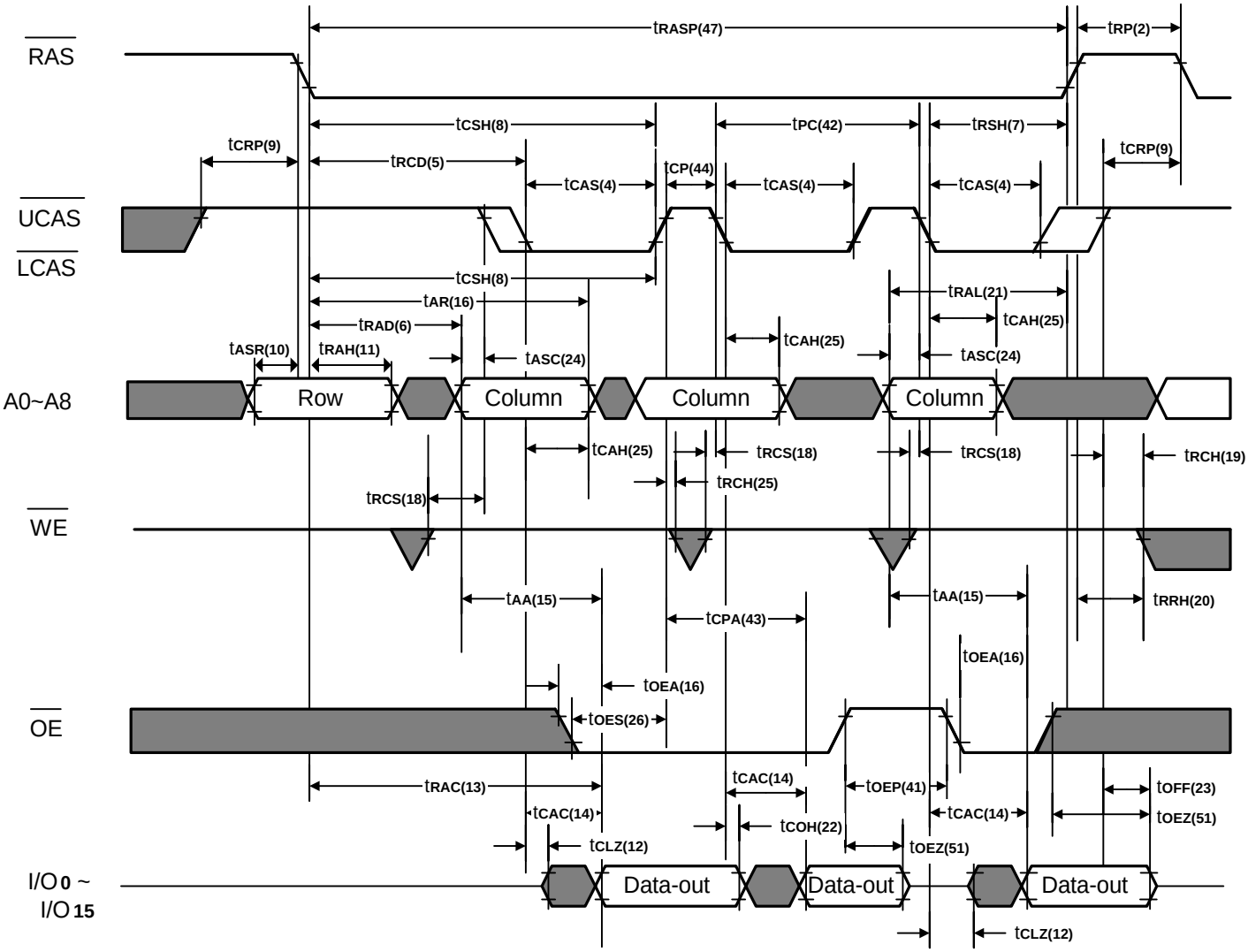
Word Write Cycle (Late Write)



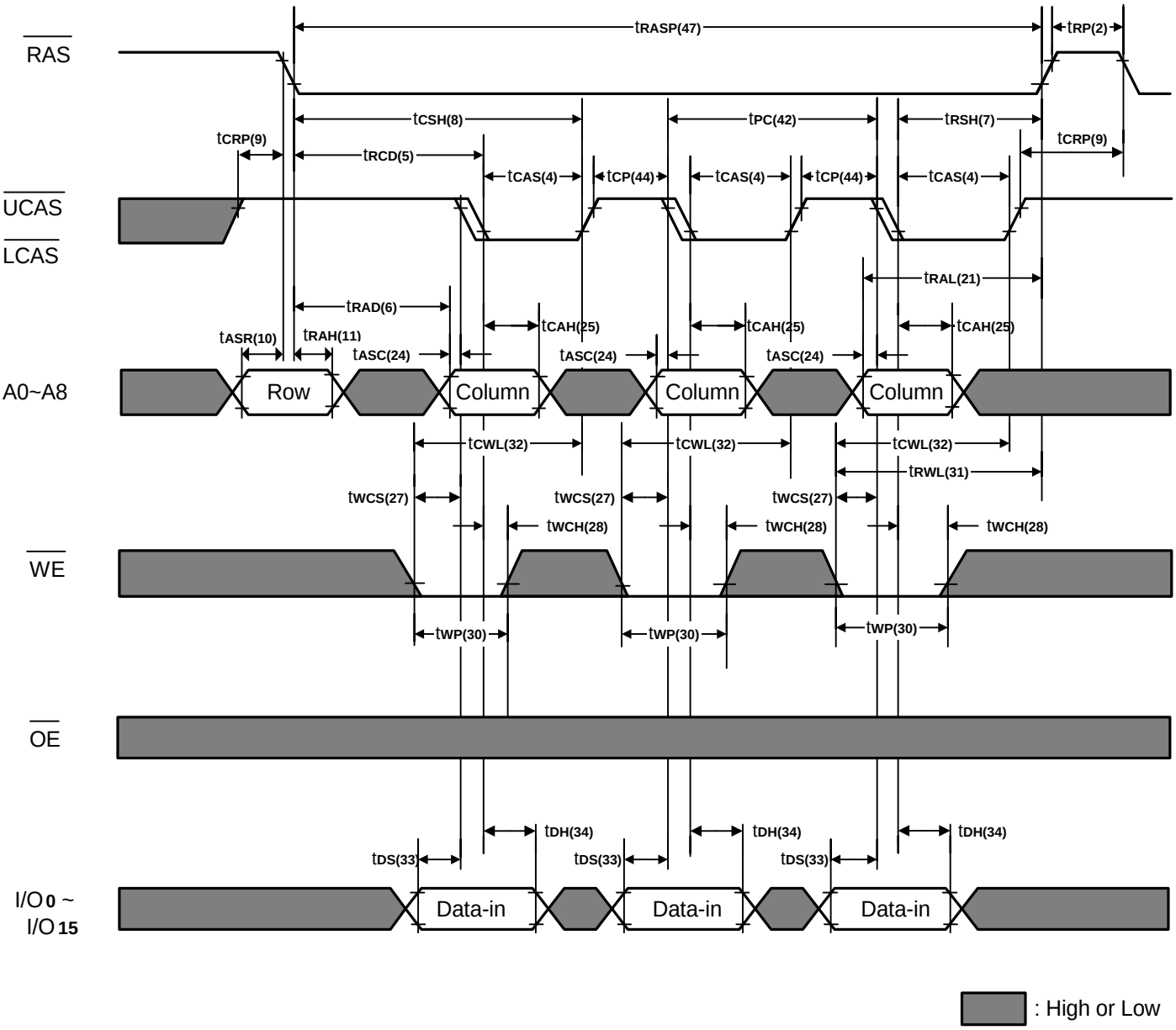
Word Read-Modify-Write Cycle



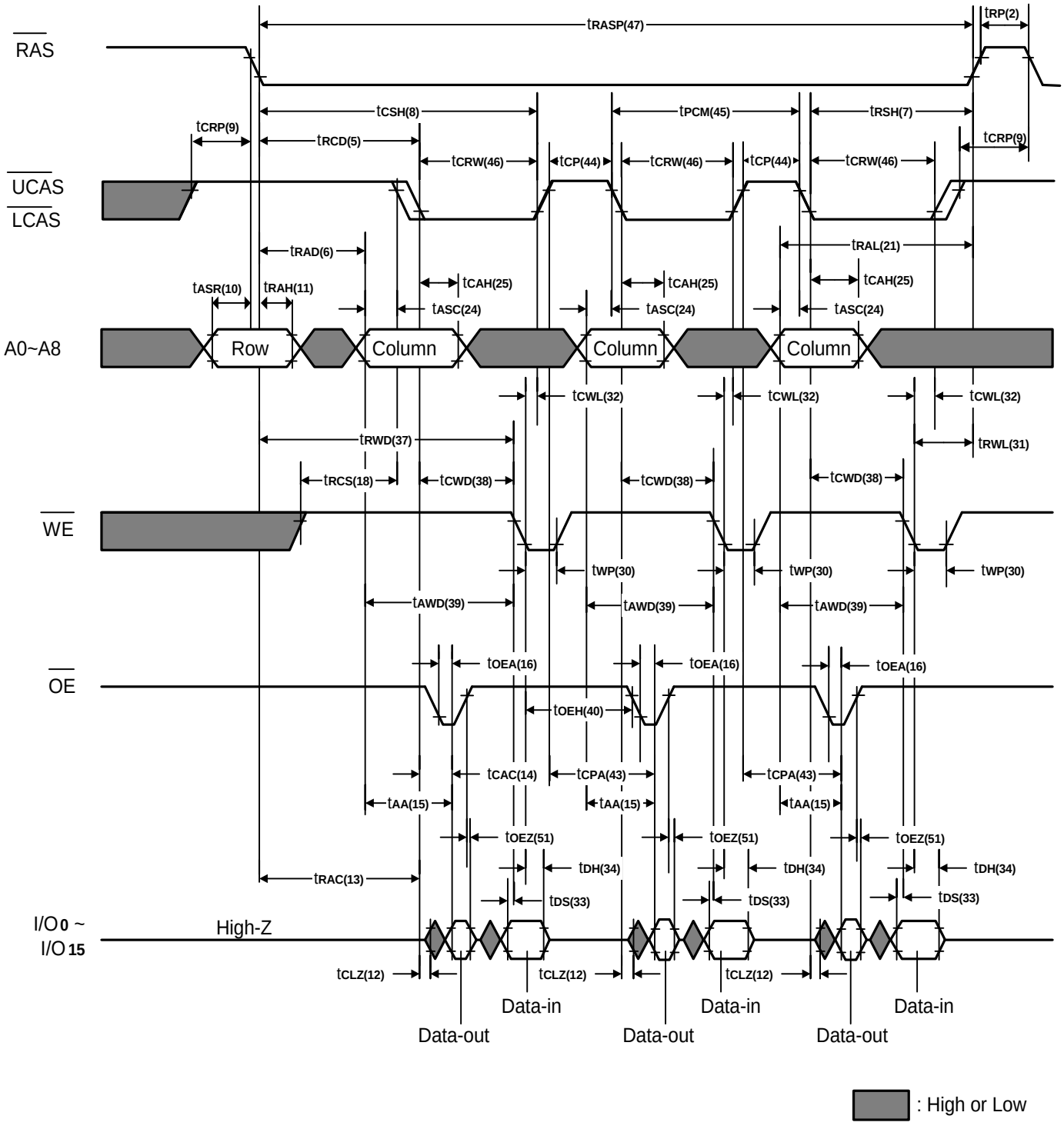
EDO Page Mode Word Read Cycle



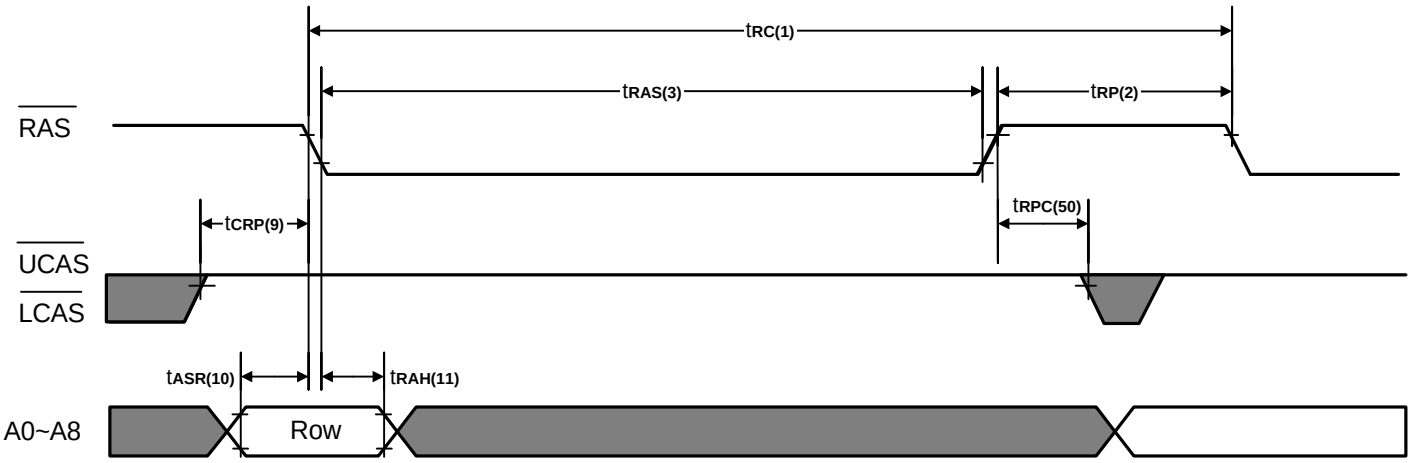
EDO Page Mode Early Word Write Cycle



EDO Page Mode Word Read-Modify-Write Cycle



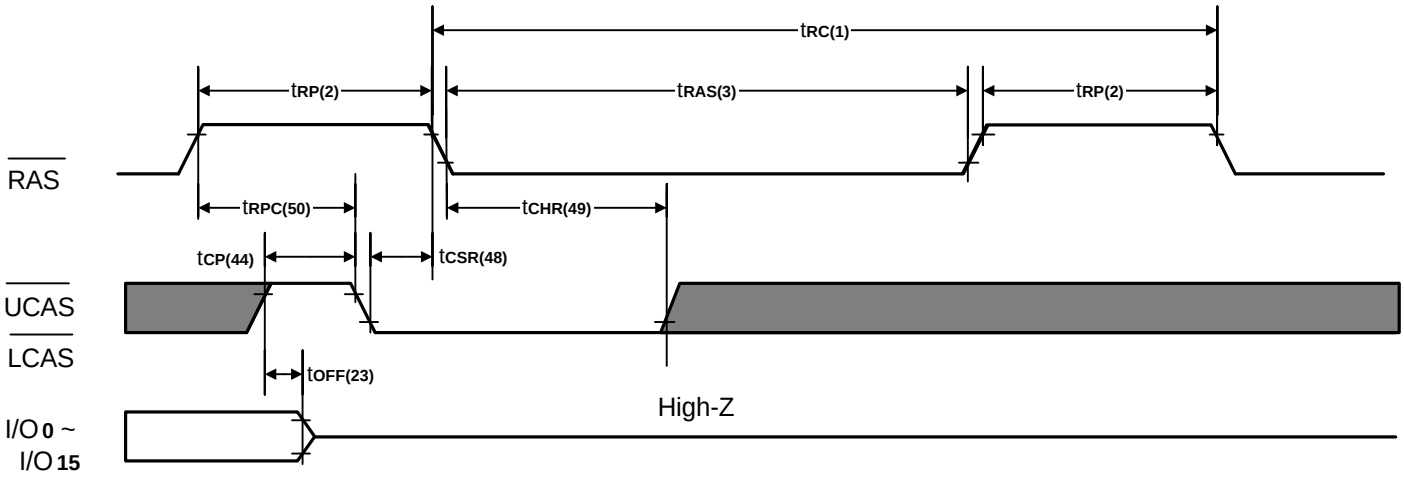
$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, $\overline{OE}$ = Don't care.

: High or Low

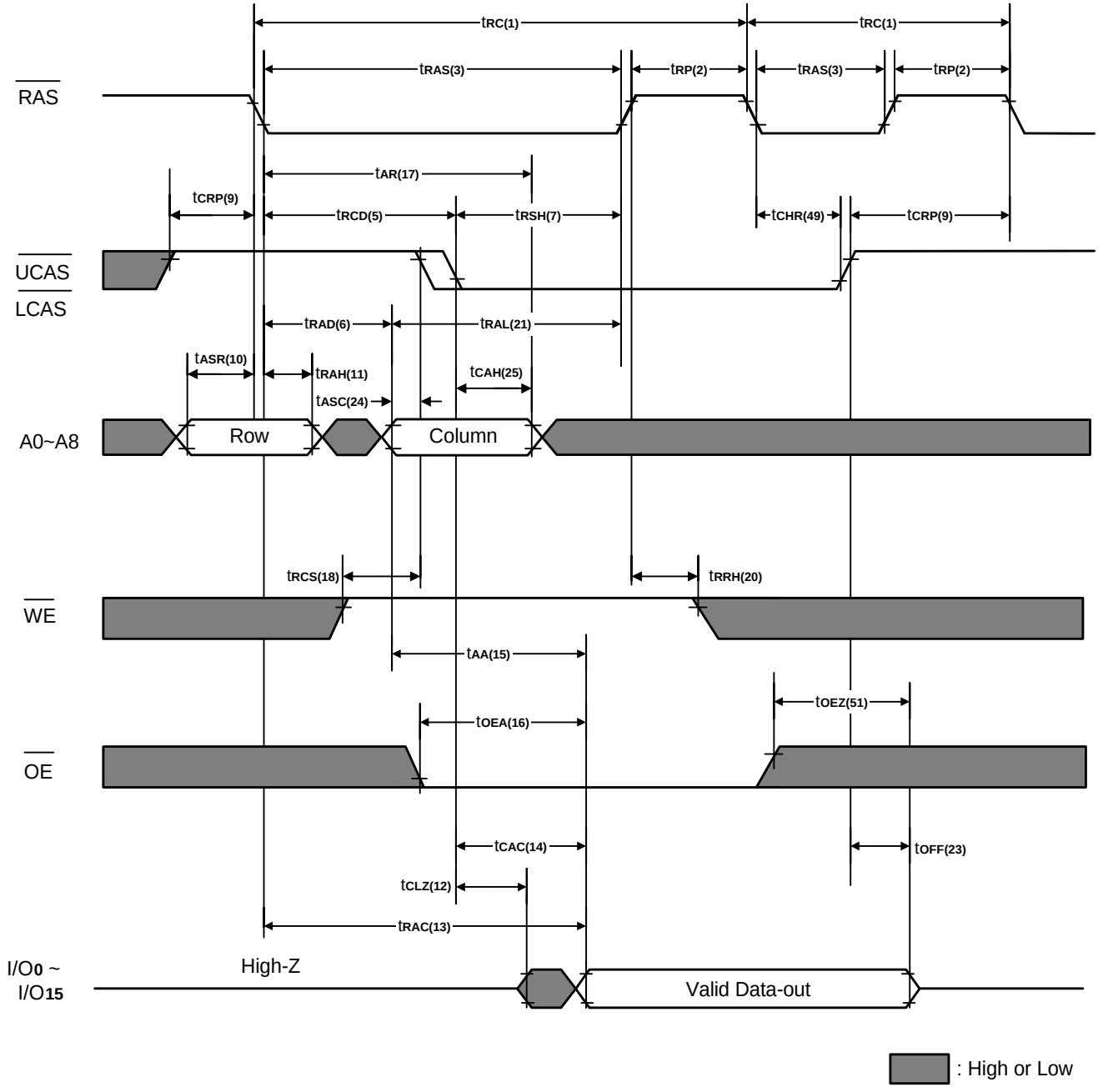
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



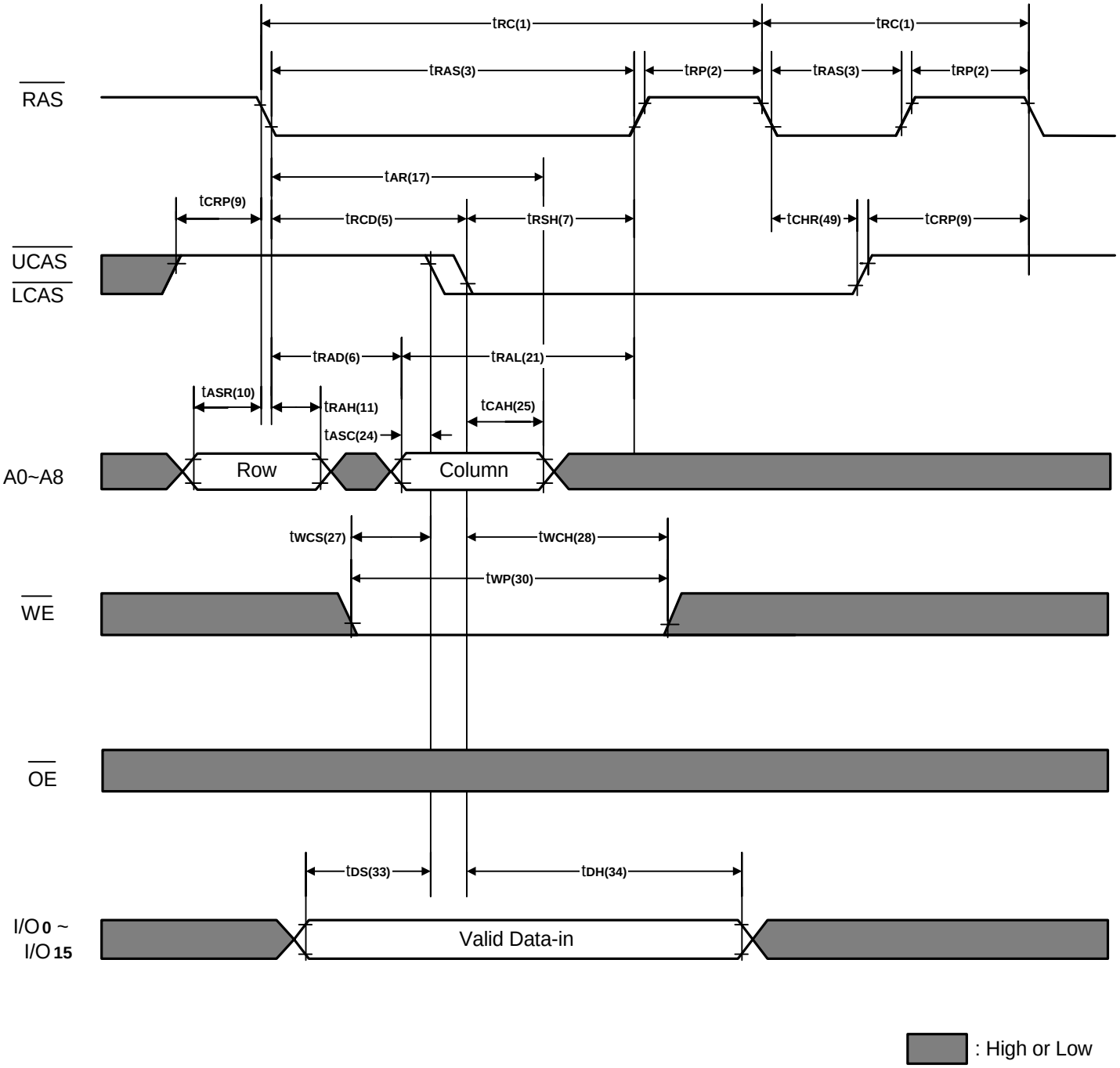
Note: $\overline{WE}$, $\overline{OE}$, Address = Don't care.

: High or Low

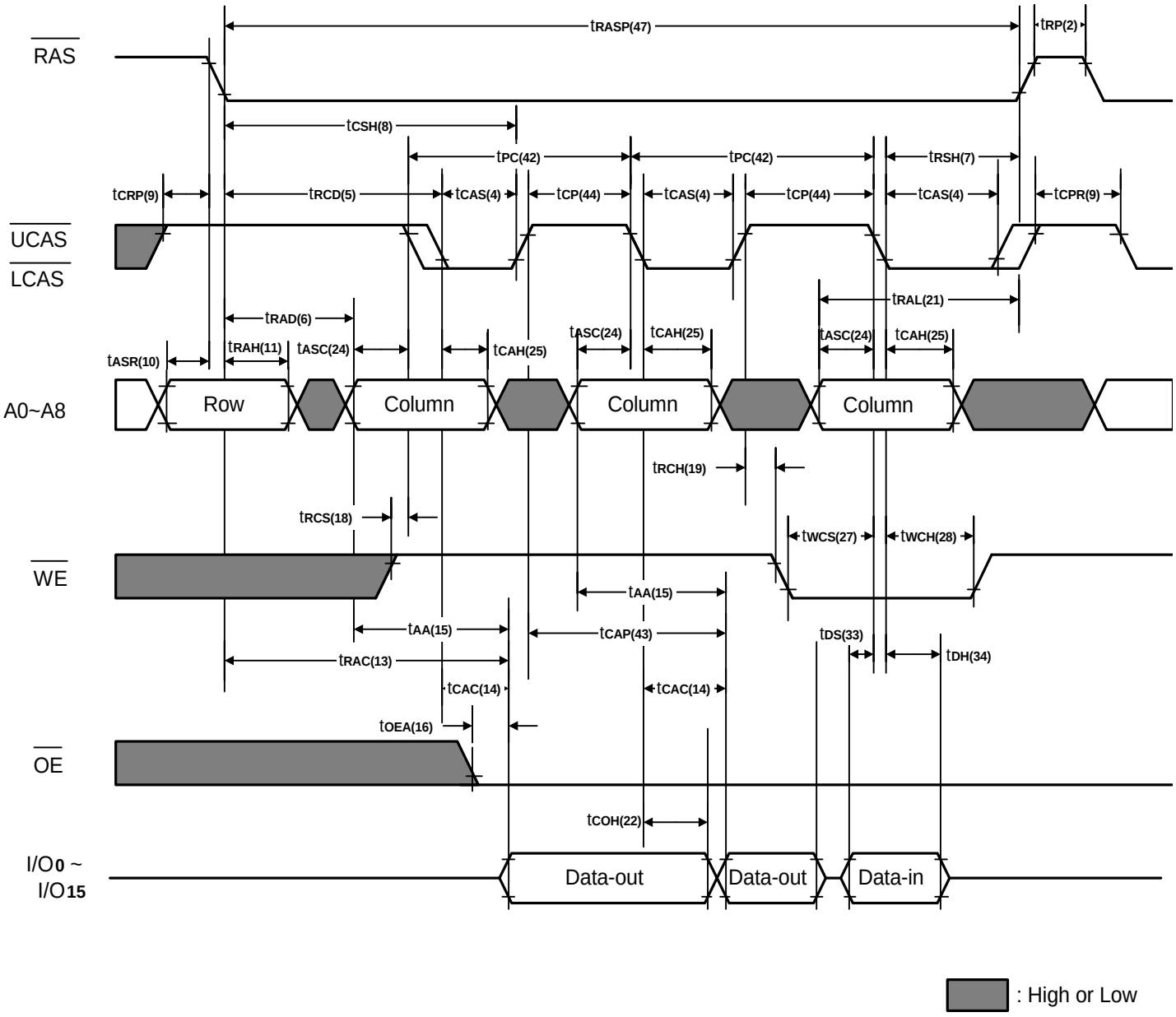
Hidden Refresh Cycle (Word Read)



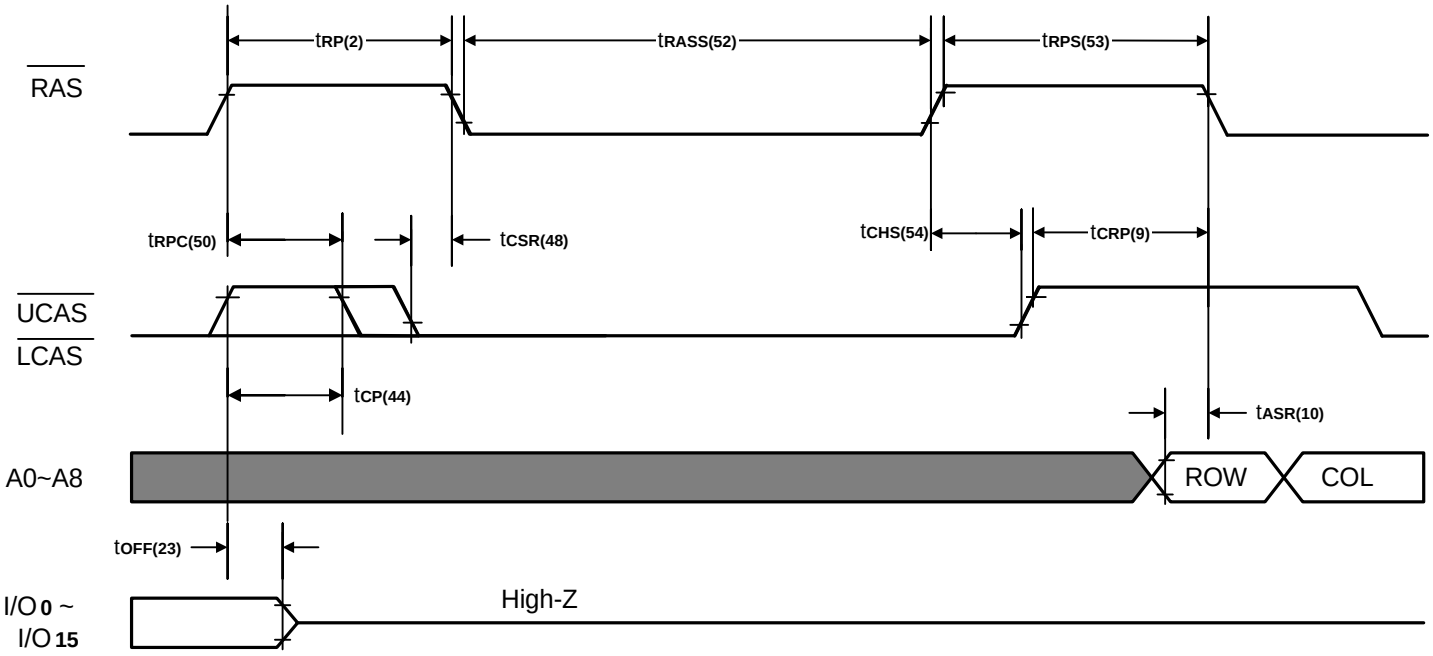
Hidden Refresh Cycle (Early Word Write)



EDO Page Mode Read-Early-Write Cycle (Pseudo Read-Modify-Write)



Self Refresh Mode



Note: $\overline{WE}$, $\overline{OE}$ = Don't care.

: High or Low

■ Self Refresh Mode.

a. Entering the Self Refresh Mode:

The A42L8316 Self Refresh Mode is entered by using $\overline{CAS}$ before $\overline{RAS}$ cycle and holding $\overline{RAS}$ and $\overline{CAS}$ signal "low" longer than 100µs.

b. Continuing the Self Refresh Mode:

The Self Refresh Mode is continued by holding $\overline{RAS}$ "low" after entering the Self Refresh Mode.

It does not depend on $\overline{CAS}$ being "high" or "low" after entering the Self Refresh Mode continue the Self Refresh Mode.

c. Exiting the Self Refresh Mode:

The A42L8316 exits the Self Refresh Mode when the $\overline{RAS}$ signal is brought "high".

Capacitance (f = 1MHz, Ta = Room Temperature, VCC = 3.3V ± 0.3V)

Symbol	Signals	Parameter	Max.	Unit	Test Conditions
C_{IN1}	A0 - A8	Input Capacitance	5	pF	Vin = 0V
C_{IN2}	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$		7	pF	Vin = 0V
$C_{I/O}$	I/O_0 - I/O_{15}	I/O Capacitance	7	pF	Vin = Vout = 0V

Ordering Codes

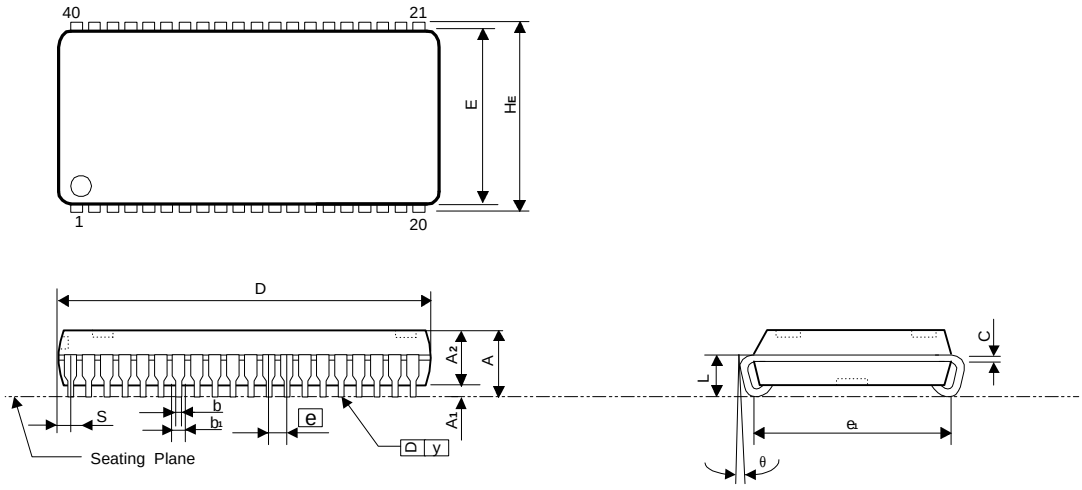
Package $\overline{RAS}$ Access Time	30ns	35ns	40ns	Self-Refresh
SOJ 40L (400mil)	A42L8316S-30	A42L8316S-35	A42L8316S-40	Yes
TSOP 40/44 L type II (400mil)	A42L8316V-30	A42L8316V-35	A42L8316V-40	Yes
TSOP 40/44 L type II (400mil)	A42L8316V-30U	A42L8316V-35U	A42L8316V-40U	Yes

Note: -U is for industrial operating temperature range.

Package Information

SOJ 40L (400mil) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.144	-	-	3.66
A_1	0.025	-	-	0.64	-	-
A_2	0.105	0.110	0.115	2.67	2.79	2.92
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
C	0.008	0.010	0.014	0.20	0.25	0.36
D	1.020	1.025	1.030	25.91	26.04	26.16
E	0.395	0.400	0.405	10.03	10.16	10.29
e	0.044	0.050	0.056	1.12	1.27	1.42
e_1	0.355	0.366	0.376	9.114	9.383	9.652
H_E	0.430	0.440	0.450	10.92	11.18	11.43
L	0.081	0.093	0.105	2.083	2.39	2.70
S	-	-	0.050	-	-	1.27
y	-	-	0.004	-	-	0.10
θ	0°	-	10°	0°	-	10°

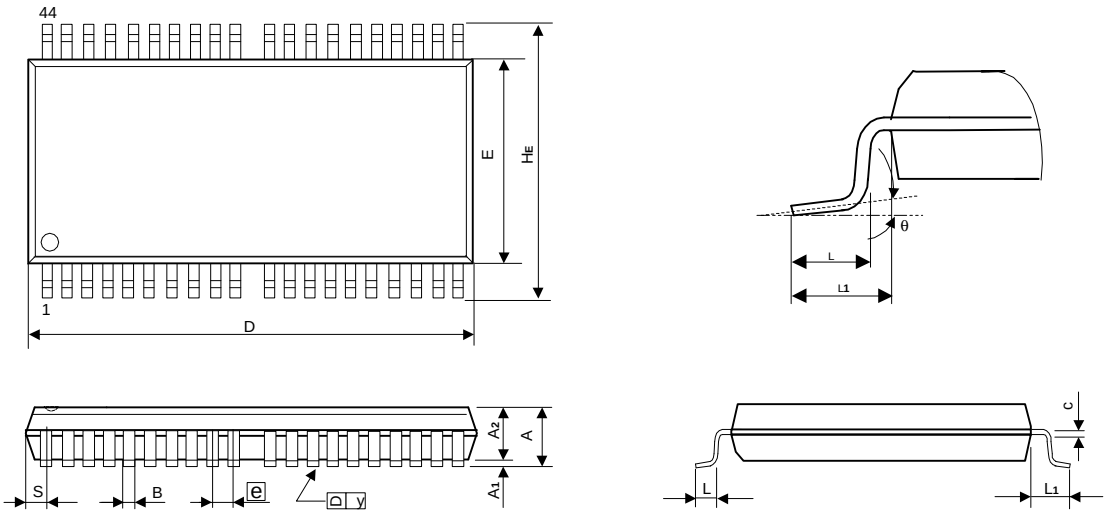
Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Package Information

TSOP 40/44L (Type II) (400mil) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.013	0.015	0.017	0.32	0.37	0.42
c	0.003	0.005	0.009	0.08	0.13	0.23
D	0.720	0.725	0.730	18.28	18.41	18.54
E	0.395	0.400	0.405	10.03	10.16	10.29
e	0.031 BSC			0.80 BSC		
H_E	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L_1	-	0.031	-	-	0.80	-
S	-	-	0.035	-	-	0.90
y	-	-	0.004	-	-	0.10
θ	1°	3°	5°	1°	3°	5°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.