ACT4525

Rev 3, 06-Jan-2017

FEATURES

- Pass Apple MFi Test
- 40V Input Voltage Surge
- 4.5V-36V Operational Input Voltage
- Dual 5.1V Outputs with 1% Accuracy
- Up to 3.5A Output Current
- 2.65A Constant Current Regulation for VOUT1
- 1.2A Constant Current Regulation for VOUT2
- USB Auto-detect Support Apple 2.4A, Samsung and BC1.2 Devices
- Hiccup Mode Protection at Output Short
- 90% Efficiency at Full Load
- 0.5mA Low Standby Input Current
- 5.7V Output Over Voltage Protection
- Cord Voltage Drop Compensation
- Meet EN55022 Class B Radiated EMI Standard
- 8kV ESD HBM Protection on DP and DM
- SOP-8EP Package

APPLICATIONS

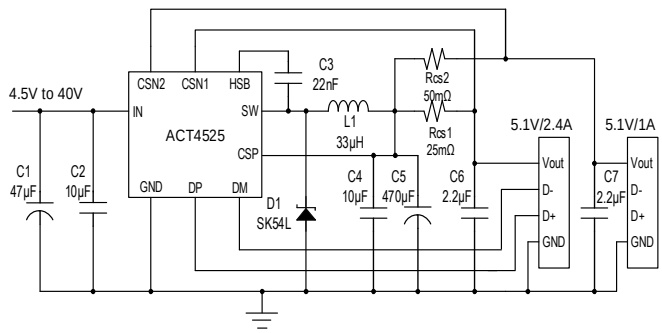
- Car Charger
- Cigarette Lighter Adaptor (CLA)
- Rechargeable Portable Device
- CV/CC regulation DC/DC converter

GENERAL DESCRIPTION

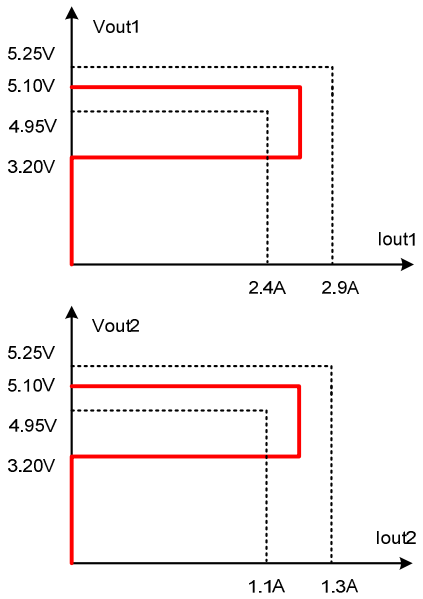
ACT4525 is a wide input voltage, high efficiency step-down DC/DC converter that operates in either CV (Constant Output Voltage) mode or CC (Constant Output Current) mode. ACT4525 has separated output current limits for dual port CLA applications. With the separated current limits, the CLA can meet Apple's MFi standard. ACT4525 provides up to 3.5A output current at 125kHz switching frequency. ACT4525 builds in USB auto-detect algorithms to recognize Apple, Samsung, and BC1.2 devices to ensure maximum charge current to attached devices. ACT4525 utilize adaptive drive technique to achieve good EMI performance while main 90% efficiency at full load for mini size CLA designs. ACT4525 also built in output short circuit protection with hiccup mode. The average output current is reduced to below 6mA when output is shorted to ground. Other features include output over voltage protection and thermal shutdown.

The devices are available in a SOP-8EP package and require very few external devices for operation.

Typical Application Circuit



V/I Profile

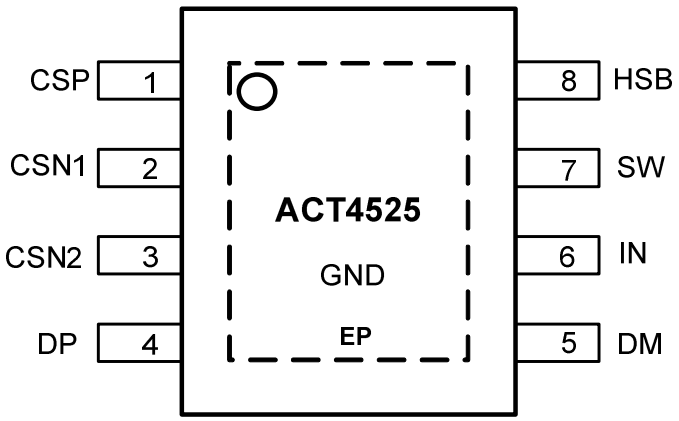


* Patent Pending

ORDERING INFORMATION

PART NUMBER	OPERATION TEMPERATURE RANGE	PACKAGE	FREQUENCY	CORD COMP	PACKING
ACT4525YH-T	-40°C to 85°C	SOP-8EP	125kHz	100mV	TAPE & REEL
ACT4525YH-T0001	-40°C to 85°C	SOP-8EP	125kHz	200mV	TAPE & REEL

PIN CONFIGURATION



SOP-8EP

Top View

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	CSP	Voltage Feedback Input. Connect to node of the inductor and output capacitor. CSP, CSN1 and CSN2 Kevin sensing is recommended.
2	CSN1	Output current sense negative input. Connect to the negative terminal of current sense resistor for VOUT1.
3	CSN2	Output current sense negative input. Connect to the negative terminal of current sense resistor for VOUT2.
4	DP	Data Line Positive Input. Connected to D+ of attached portable device data line. This pin passes 8kV HBM ESD.
5	DM	Data Line Negative Input. Connected to D- of attached portable device data line. This pin passes 8kV HBM ESD.
6	IN	Power Supply Input. Bypass this pin with a 10μF ceramic capacitor to GND, placed as close to the IC as possible.
7	SW	Power Switching Output to External Inductor.
8	HSB	High Side Bias Pin. This provides power to the internal high-side MOSFET gate driver. Connect a 22nF capacitor from HSB pin to SW pin.
9	GND	Ground and Heat Dissipation Pad. Connect this exposed pad to large ground copper area with copper and vias.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
IN to GND	-0.3 to 40	V
SW to GND	-1 to V_{IN} +1	V
HSB to GND	V_{SW} - 0.3 to V_{SW} + 7	V
CSP, CSN1, CSN2, DP , DM to GND	-0.3 to +6	V
Junction to Ambient Thermal Resistance	46	°C/W
Operating Junction Temperature	-40 to 150	°C
Storage Junction Temperature	-55 to 150	°C
Lead Temperature (Soldering 10 sec.)	300	°C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified.)

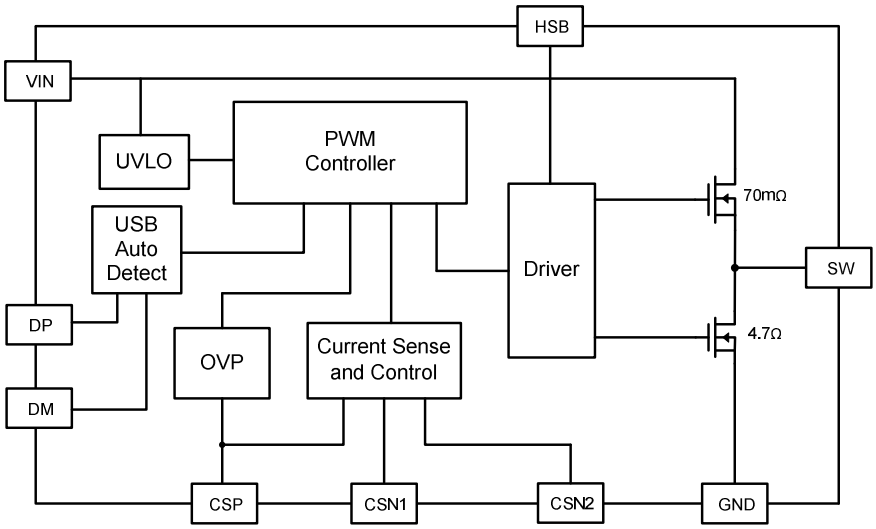
Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Over Voltage Protection	VIN_OVP	Rising	40	42	44	V
Input Over Voltage Hysteresis				4		V
Input Over Voltage Response Time	T_VIN_OVP	VIN step from 30V to 45V		250		ns
Input Under Voltage Lockout (UVLO)	VIN	Rising		4.5		V
Input UVLO Hysteresis				200		mV
Input Voltage Power Good Deglitch Time		No OVP		40		ms
Input Voltage Power Good Deglitch Time		No UVP		10		us
Input Standby Current		Vin=12V, Vout=5.1V, Iload=0		500		uA
Output Voltage Regulation	CSP		5.05	5.1	5.15	V
Output Over Voltage Protection (OVP)		Output rising		5.7		V
Output Over Voltage Deglitch Time				1.0		us
Output Voltage Cord Compensation		ACT4525-T Iout=2.4A	-15%	100	+15%	mV
		ACT4525-T0001 Iout=2.4A	-15%	200	+15%	mV
Output Under Voltage Protection (UVP)	VOUT	VOUT falling	-10%	3.2	10%	V
UVP Hysteresis	VOUT	VOUT rising		0.2		V
UVP Deglitch Time	VOUT			10		us
UVP Blanking Time at Startup				3.5		ms
Output Constant Current Limit	CC1	Rcs=25mΩ	2.50	2.65	2.80	A
	CC2	Rcs=50mΩ	1.1	1.2	1.3	A
Hiccup Waiting Time				4.13		s
Top FET Cycle by Cycle Current Limit			4.5	5.8		A
Top FET Rdson				70		mΩ
Bottom FET Rdson				4.7		Ω
Maximum Duty Cycle			99			%
Switching Frequency			-10%	125	+10%	kHz
Soft-start Time				2.0		ms

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Out Voltage Ripples		Cout=470uF/22uF ceramic		80		mV
Line Transient Response		Input 12V-40V-12V with 1V/us slew rate, Vout=5V, Iload=0A and 2.4A	4.75		5.25	V
Load Transient Response	Vout=5V	80mA-1.0A-80mA load with 0.1A/us slew rate	4.9	5.15	5.4	V
Thermal Shut Down				160		°C
Thermal Shut Down Hysteresis				30		°C
ESD of DP, DM		HBM		8		kV

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Output Current Sensing and Regulation

Sense resistor is connected to CSP and CSN1, CSN2 respectively. The sensed differential voltages are compared with interval references to regulate currents. CC loop and CV loop are in parallel. The current loop response is allowed to have slower response compared to voltage loop. However, during current transient response, the inductor current overshoot/undershoot should be controlled within +/-25% to avoid inductor saturation.

Cycle-by-Cycle Current Control

The conventional cycle-by-cycle peak current mode is implemented with high-side FET current sense.

Input Over Voltage Protection

The converter is disabled if the input voltage is above 42V (+/-2V). Device resumes operation automatically 40ms after OVP is cleared.

Output Over Voltage Protection

Device stops switching when output over-voltage is sensed, and resumes operation automatically when output voltage drops to OVP - hysteresis.

Output Under-Voltage Protection / Hiccup Mode

There is a under voltage protection (UVP) threshold. If the UVP threshold is hit for 10us, an over current or short circuit is assumed, and the converter goes into hiccup mode by disabling the converter and restarts after hiccup waiting period.

Cord Compensation

In some applications, the output voltage is increased with output current to compensate the potential voltage drop across output cable. The compensation is based on the high side feedback resistance.

The compensation voltage is derived as:

$\Delta Vout = (V_{CSP}-V_{CSN})*K$

ACT4525YH-T K=1.515

ACT4525YH-T0001 K=3.030

This voltage difference could be added on the reference or turning the (V_{CSP}-V_{CSN}) voltage into a sink current at FB pin to pull Vout higher than programmed voltage.

The cord compensation loop should be very slow to avoid potential disturbance to the voltage loop. The voltage loop should be sufficiently stable on various cord compensation setting.

Thermal Shutdown

If the T_J increases beyond 160°C, ACT4525 goes into HZ mode and the timer is preserved until T_J drops by 30°C.

APPLICATIONS INFORMATION

Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value.

Higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{LOADMAX} K_{RIPPLE}} \quad (1)$$

Where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, $I_{LOADMAX}$ is the maximum load current, and K_{RIPPLE} is the ripple factor. Typically, choose K_{RIPPLE} = 30% to correspond to the peak-to-peak ripple current being 30% of the maximum load current.

With a selected inductor value the peak-to-peak inductor current is estimated as:

$$I_{LPK-PK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times V_{IN} \times f_{SW}} \quad (2)$$

The peak inductor current is estimated as:

$$I_{LPK} = I_{LOADMAX} + \frac{1}{2} I_{LPK-PK} \quad (3)$$

The selected inductor should not saturate at I_{LPK}. The maximum output current is calculated as:

$$I_{OUTMAX} = I_{LIM} - \frac{1}{2} I_{LPK-PK} \quad (4)$$

L_{LIM} is the internal current limit.

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 10µF. The best choice is the ceramic type. However, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and GND pins of the IC, with the shortest traces possible. In the case of tantalum or electrolytic types, a ceramic capacitor is recommended to parallel with tantalum or electrolytic capacitor, which should be placed right next to the IC.

Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{OUTMAX} K_{RIPPLE} R_{ESR} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{8 \times f_{SW}^2 L C_{OUT} \times V_{IN}} \quad (5)$$

Where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR of the output capacitor, f_{SW} is the switching frequency, L is the inductor value, and C_{OUT} is the output capacitance. In the case of ceramic output capacitors, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic capacitors, the ripple is dominated by R_{ESR} multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

For ceramic output capacitor, typically choose a capacitance of about 22µF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50mΩ ESR. If an 330µF or 470µF electrolytic capacitor is used, where ripple is dominantly caused by ESR, an 2.2uF ceramic in parallel is recommended.

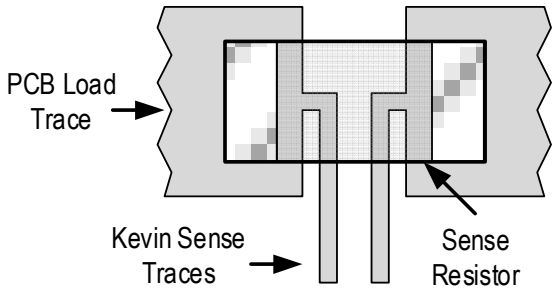
Rectifier Schottky Diode

Use a Schottky diode as the rectifier to conduct current when the High-Side Power Switch is off. The Schottky diode must have current rating higher than the maximum output current and a reverse voltage rating higher than the maximum input voltage. Further more, the low forward voltage Schottky is preferable for high efficiency and smoothly operation.

APPLICATIONS INFORMATION

Current Sense Resistor

The traces leading to and from the sense resistor can be significant error sources. With small value sense resistors, trace resistance shared with the load can cause significant errors. It is recommended to connect the sense resistor pads directly to the CSP and CSN pins using “Kelvin” or “4-wire” connection techniques as shown below.



Current Limit Setting

If output current hits current limit, output voltage drops to keep the current to a constant value.

The following equation calculates the constant current limit.

For output1:

$$ILimit\ (A) = \frac{66\,mV}{Rcs\ (m\Omega)} \qquad (6)$$

For output2:

$$ILimit\ (A) = \frac{60\,mV}{Rcs\ (m\Omega)} \qquad (7)$$

Where Rcs is current sense resistor.

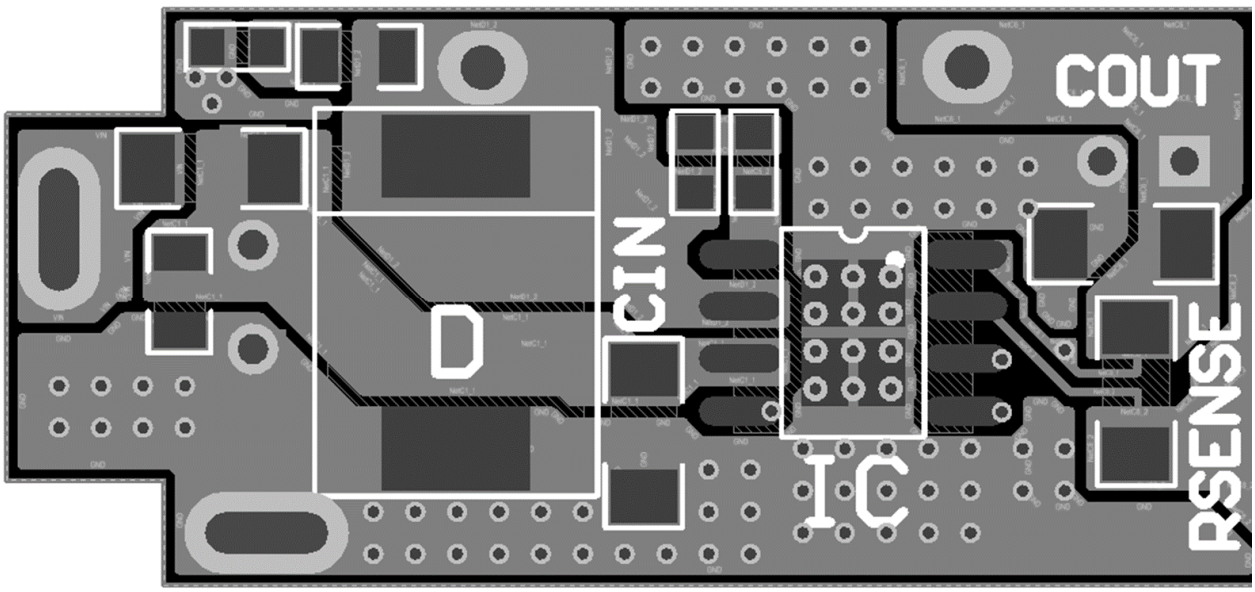
APPLICATIONS INFORMATION

PCB Layout Guidance

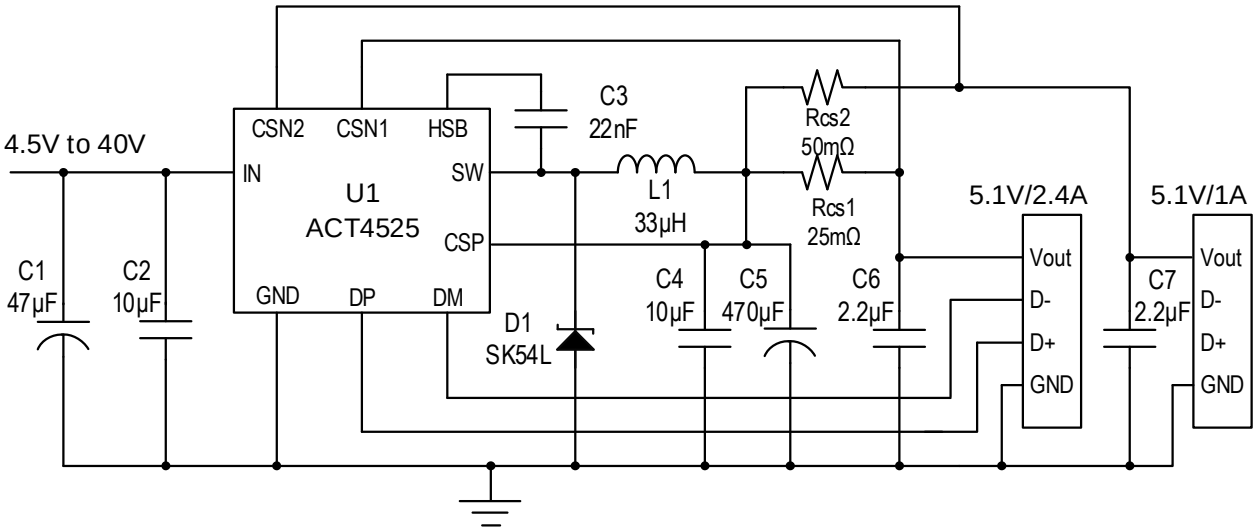
When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

1) Arrange the power components to reduce the AC loop size consisting of C_{IN}, V_{IN} pin, SW pin and the Schottky diode.
2) The high power loss components, e.g. the controller, Schottky diode, and the inductor should be placed carefully to make the thermal spread evenly on the board.
3) Place input decoupling ceramic capacitor C_{IN} as close to VIN pin as possible. C_{IN} should be connected to power GND with several vias or short and wide copper trace.
4) Schottky anode pad and IC exposed pad should be placed close to ground clips in CLA applications.
5) Use “Kelvin” or “4-wire” connection techniques from the sense resistor pads directly to the CSP and CSN1, CSN2 pins. The CSP and CSN1, CSN2 traces should be in parallel to avoid interference.
6) Place multiple vias between top and bottom GND planes for best heat dissipation and noise immunity.
7) Use short traces connecting HSB-C_{HSB}-SW loop.
8) SW pad is noise node switching from V_{IN} to GND. It should be isolated away from the rest

Example PCB Layout



Typical Application Circuit for 5V/3.4A Car Charger



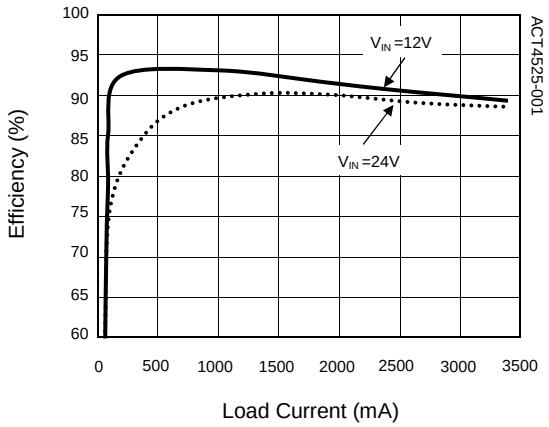
BOM List for 5V/3.4A Car Charger

ITEM	REFERENCE	DESCRIPTION	MANUFACTURER	QTY
1	U1	IC, ACT4525, SOP-8EP	Active-Semi	1
2	C1	Capacitor, Electrolytic, 47µF/35V	Murata, TDK	1
3	C2	Capacitor, Ceramic, 10µF/25V, 1206, SMD	Murata, TDK	1
4	C3	Capacitor, Ceramic, 22nF/25V, 0603, SMD	Murata, TDK	1
5	C4	Capacitor, Ceramic, 10µF/10V, 1206, SMD	Murata, TDK	1
6	C5	Capacitor, Electrolytic, 470µF/10V	Murata, TDK	1
7	C6,C7	Capacitor, Ceramic, 2.2µF/10V, 0805, SMD	Murata, TDK	2
8	L1	Inductor, 33µH, 4.5A, 20%,		1
9	D1	Diode, Schottky, 40V/5A, SK54L	Panjit	1
10	Rcs1	Chip Resistor, 25mΩ, 1206, 1/2W, 1%	SART	1
11	Rcs2	Chip Resistor, 50mΩ, 1206, 1/2W, 1%	SART	1

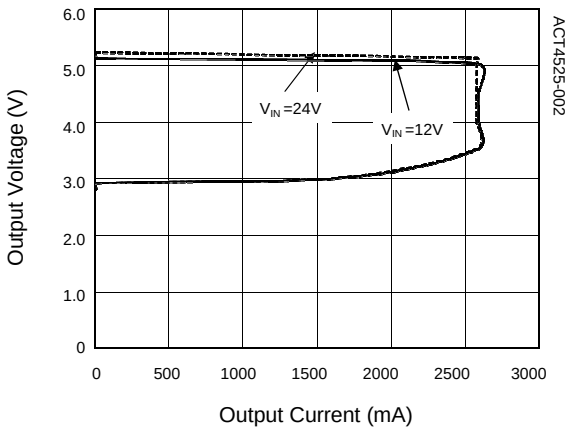
TYPICAL PERFORMANCE CHARACTERISTICS

(Schematic as show in typical application circuit, Ta = 25°C, unless otherwise specified)

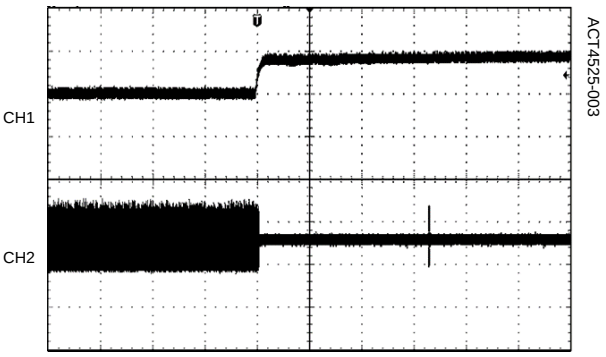
Efficiency vs. Load current



Output1 CC/CV Curve

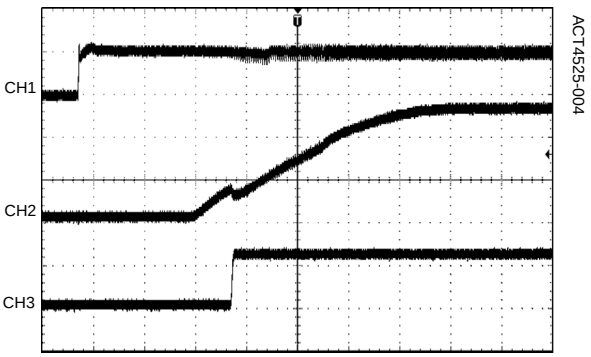


Output Over Voltage (5V Vout)



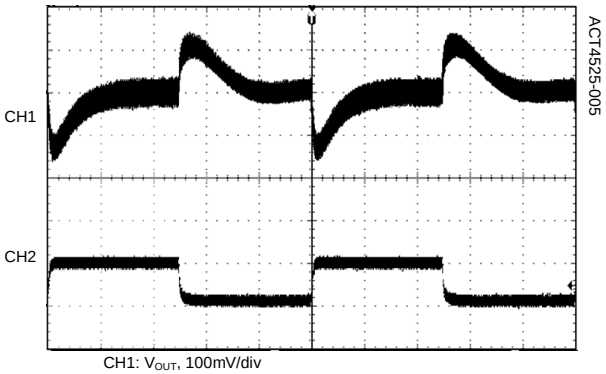
CH1: V_{OUT}, 1V/div
CH2: SW, 10V/div
TIME: 1ms/div

Start up into CC Mode



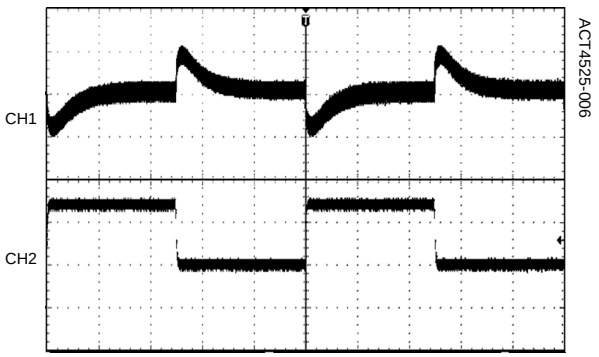
CH1: V_{IN}, 10V/div
CH2: V_{OUT}, 2V/div
CH3: I_{OUT}, 2A/div
TIME: 400μs/div

Load Transient (80mA-1A-80mA)
Vin=12V, Vout=5V



CH1: V_{OUT}, 100mV/div
CH2: I_{OUT}, 1A/div
TIME: 400us//div

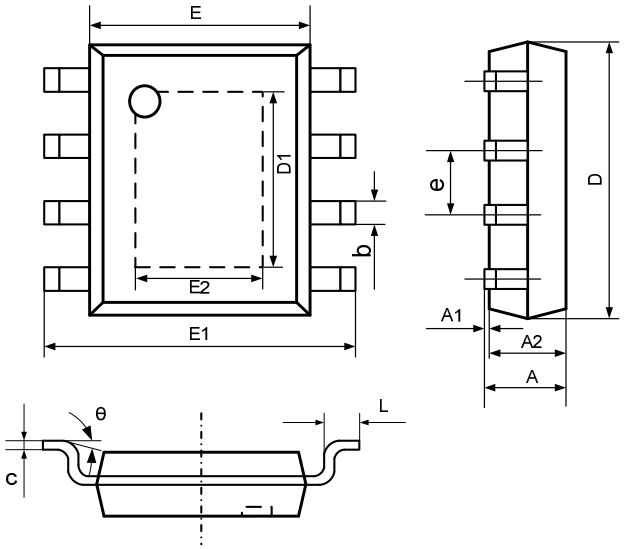
Load Transient (1A-2.4A-1A)
Vin=12V, Vout=5V



CH1: V_{OUT}, 200mV/div
CH2: I_{OUT}, 1A/div
TIME: 400us//div

PACKAGE OUTLINE

SOP-8EP PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.727	0.053	0.068
A1	0.000	0.152	0.000	0.006
A2	1.245	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.734	4.000	0.147	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 TYP		0.050 TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°