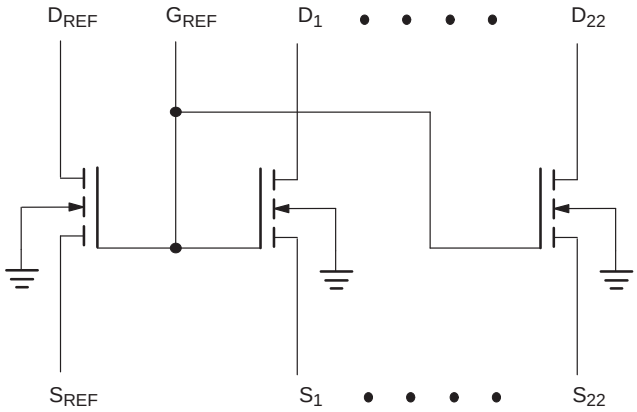
APPLICATION NOTE



ABSTRACT

Philips Semiconductors Gunning Transceiver Logic Translator Voltage Clamp (GTL-TVC) bi-directional low voltage translators are used in bi-directional signaling voltage level translation applications. Voltage translation can be from any voltage between 1.0 V to 5.0 V to any voltage between 1.0 V to 5.0 V without need for directional control. Device operation, resistor sizing and typical applications are discussed in this application note.

AN10145

Bi-directional low voltage translators

GTL2000, GTL2002, GTL2010

Supersedes data of 2002 Dec 16

2004 Aug 11

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Specialty Logic Product Line
Interface Products Business Line

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OVERVIEW

Description

Within the semiconductor world, there are many I/O standards that have different voltage level requirements for the input voltage (V_{IH} or V_{IL}) and output voltage (V_{OH} or V_{OL}) typically based on the device operating voltage. These voltage levels define how the device communicates with other devices and the voltage levels are expressed as a bus standard. A few of these bus standards include 5 V CMOS, 5 V TTL, 3.3 V LVTTL, 2.5 V AGP graphics port and 1.5 V GTL+ host bus. Providing a migration path is important in all industry segments because system components used in new designs must communicate with components using the existing bus infrastructure even if they are operating at higher voltage levels. Since new devices are designed and produced with advanced sub-micron semiconductor process technologies, there has to be an easy way to prevent damage to the new device and translate voltage switching levels of the higher voltage legacy device.

The Philips Semiconductors Gunning Transceiver Logic Translator Voltage Clamp (GTL-TVC) family of bi-directional low voltage translators is designed in a BiCMOS process for protecting the sensitive I/Os on new advanced sub micron components. The GTL-TVC devices protect these new devices from the over voltage and ESD conditions applied by the older, legacy devices and translate the V_{IH} and V_{OH} switching levels. The information presented in this application note describes the I/O-protection applications and voltage translations of the GTL-TVC family and will enable the design engineer to successfully interface devices with different I/O voltage levels.

Applications

Voltage Level Shifting

The GTL-TVC devices can be used to interface between devices I/Os operating at different voltage levels. Since the GTL-TVC device is open drain on both sides, pull up resistors may be needed depending on the I/O interface type (totem pole or open drain) and the translation direction (High to Low, Low to High, or bi-directional). The GTL-TVC devices allow translations between any voltages from 1.0 V to 5.0 V as long as the voltage difference between the Gate and Source voltages is maintained at about 1 V. The recommended circuit in Figure 1 connects the gate (GREF) and reference drain (DREF) together through a 200 k Ω resistor to a voltage, **which should be at least 1.5 V above the reference Source (SREF) level**. This circuit biases the gate to a threshold above the reference source voltage and compensates for part-to-part threshold variations. Since the gate threshold voltage can vary between 0.6 V and 1 V, if the GREF to SREF voltage is less than 1 V, the low voltage side high level may be degraded below the SREF voltage because it can only pull up to a threshold below the GREF voltage.

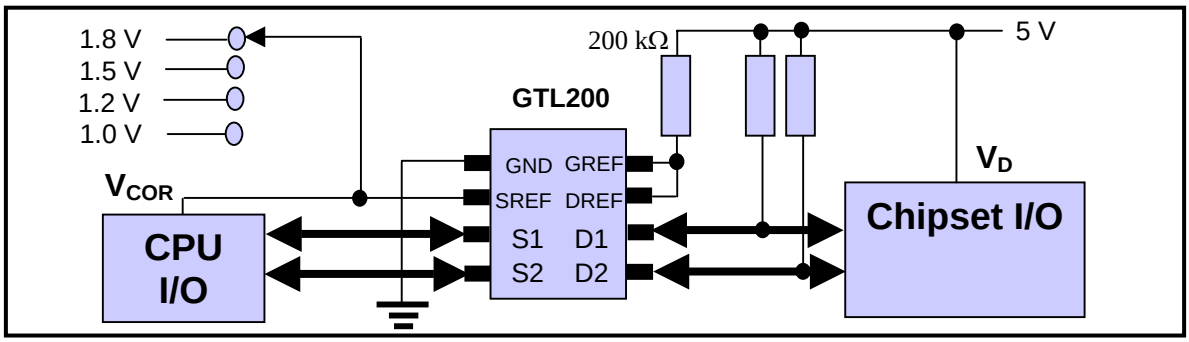


Figure 1. Typical Two-bit bi-directional application

1. **Bi-directional Translation**
   For bi-directional translation, the drivers on both sides of the GTL-TVC device must be open drain outputs or at least they must be controlled in such a way that contention between a High level on an output driver on one side and a Low level on an output driver on the other side is prevented. The easiest solution is to use open drain devices (the standard GTL and I^2C/SMBus outputs are open drain outputs).
   When using open drain devices, it is necessary to use pull up resistors, and they must be sized so as not to overload the output drivers nor exceed the 15 mA recommended current for use of a GTL-TVC device in a translation application. If the device is used for I^2C bus translation, the resistors must be sized to provide less than 3 mA of current (I^2C devices are specified to drive 3 mA max at 0.4 V).

When the GTL-TVC device is used as described in Figure 1, it is not necessary to have pull up resistors on the lower voltage side because the GTL-TVC device will pass up to the reference Source voltage. With a 200 kΩ resistor connected to the reference Drain (DREF) and the reference Gate (GREF) and pulled up to a supply voltage **that is at least 1.5 V higher than the reference Source (SREF) level**, about 2.5 μA will pass to the lower voltage side at the reference Source voltage value. If the low voltage side is known to be leaky (more than the 2.5 μA described above), it is necessary to include a pull up resistor on the low voltage side as well as the high voltage side to provide the required current value.

2. **Down Translation**
When doing down translation, since there is no driver on the lower voltage side, the higher voltage driver may be either totem pole without any pull up resistor or open drain with a pull up resistor, and **no resistor pull up is needed on the low voltage side** unless it has excessive leakage (more than the 2.5 μA described in the paragraph above).

3. **Up Translation**
A pull up resistor is **always** required on the higher voltage side to get the full high level, since the GTL-TVC device will only pass the reference source voltage as a high when doing a up translation. A full CMOS driver or an open drain driver with or without a pull up resistor on the low voltage side may be used. The resistor values must be chosen so as not to overload the pull down driver nor the 15 mA limit of the GTL-TVC devices.

4. **Multiple Voltage Bi-Directional Translation**
The channel pass transistors are constructed such that the gate of the reference transistor (GREF) pin is used to limit the maximum high voltage that will be passed by the device. This allows the use of different bus voltages on each source to drain channel so that for example, a 1.5 V device can communicate with 2.5 V, 3.3 V or 5 V devices without any additional protection. Figure 2 shows how the GTL2010 can be used in a bi-directional I^2C application where two ASIC's I^2C ports (left side) operating at 1.5 V can interface to higher voltage devices (right side) operating at 3.3V and 5.0 V.
   - One of the ASIC ports (MDDC on S1 & S2) only needs to interface with 5 V I^2C devices.
   - The other ASIC port (MI2C on S3 & S4 and S5 & S6) needs to interface with both 3.3 V SMBus and 5.0 V I^2C devices.

Since the voltage difference between the low voltage (1.5V, left side) and the voltage on the resistor for the GREF (Gate pull-up) is higher than 1.5V (5.0V in the figure), pull up resistors on the low voltage side (1.5V) are optional.

Note:
Pull up resistors on the low voltage side are required if:
- **Te difference between the external voltage applied on the resistor for the Gate reference (GREF) and the voltage on the low side is lower than 1.5V**
- **The device in the low voltage side has a leakage current value higher than 2.5 μA**

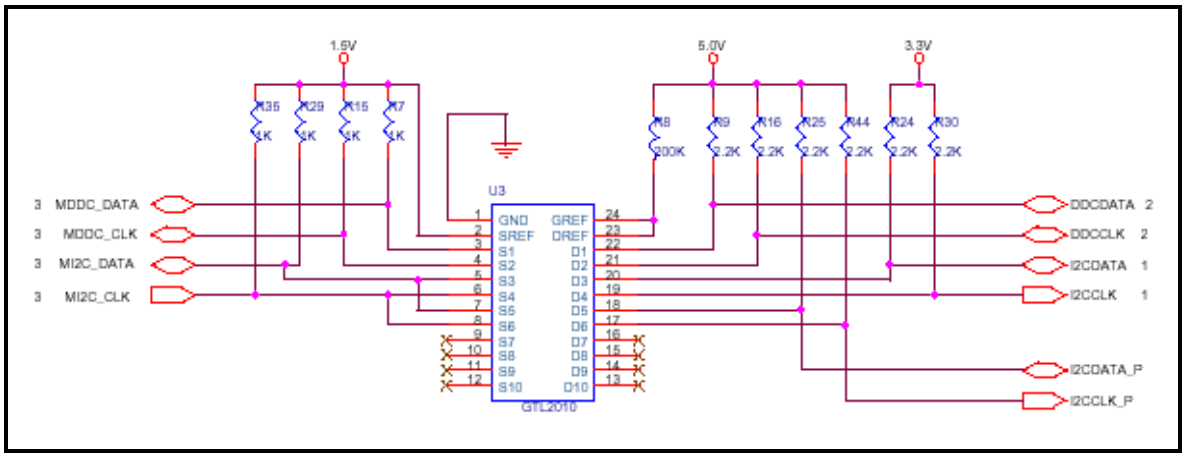


Figure 2. Bi-directional Multiple Voltage I^2C Application

Cross-Bar Technology (CBT) Like Behavior

The large NMOS pass transistors used in the GTL-TVC devices are very similar to the large NMOS pass transistors used in CBT devices. However unlike the CBT devices that use internal drivers to control the gate of the NMOS pass transistor, the gate pin of the GTL-TVC devices is directly connected to the gate of each transistor. In principle the GTL-TVC devices can be used like CBT devices except that the gate input capacitance is much larger than a normal CBT device. When using the GTL-TVC devices as CBT devices, the gate pin (GREF) is driven by external logic to the power supply, to enable it, or to ground to disable it, and the SREF and DREF pins can be used as an additional channel as shown in Figure 3.

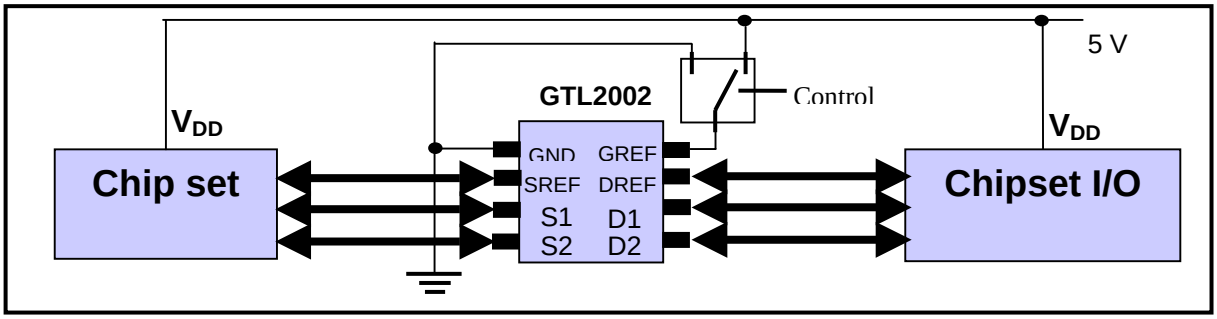


Figure 3. Cross Bar Technology like Application

Note: If a 5 V to 3.3 V translation is wanted, best results are achieved using the bias circuit of the GTL-TVC with the SREF at 3.3 V. Additionally, when used as a CBT function with the gate at V_{DD} and the input at $V_{DD,}$ the maximum pass voltage will be ~ V_{DD} – 1 V because the output is shifted down by a threshold compared to the gate voltage.

Features

The GTL-TVC family has several features that benefit a system designer when designing an interface between devices with different I/O voltage levels.

Device Construction – The GTL-TVC devices are of a very simple design. The only required connections are GND, gate of the reference transistor (GREF), drain of the reference transistor (DREF) and source of the reference transistor (SREF) and then any of the Dn/Sn I/O pairs needed for voltage level translations.

- Any transistor Dn or Sn I/O pair can be used as the source or drain of the reference transistor (SREF or DREF). This makes it easier to route signals to and from the device.
- All the transistors are on one die, which is manufactured with very tight process control. This provides a very low spread of V_O relative to SREF or DREF.
- It is easy to change the SREF voltage allowing the system designer an easy migration path to even lower voltages (e.g. 1.5 V or 1.2 V).
- Dn /Sn I/O pairs are matched on either side of the devices (e.g., flow through pinout) which offers easy trace routing.

No Active Control Logic – As shown in Figure 4, the GTL-TVC is a passive device and there is no active control logic. This means there is no supply power (V_{DD}) required for device operation.

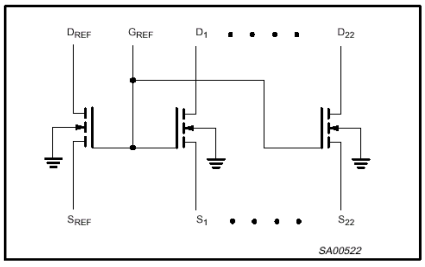


Figure 4. GTL20XX Logic Diagram

Wide Range of Bit Widths and Packages – The GTL-TVC devices are offered in a wide range of bit widths and packages as shown in table 1. They are available in 2, 10 or 22 bit widths and package sizes ranging from the SO and TSSOP packages to the small HVQFN and VSSOP packages. This allows the designer the maximum flexibility in picking the bit width and package that is best suited for them, should the concern be easy soldering or small form factor or wider bit width.

DEVICE NAME	# of I/O pairs	PACKAGES					
		PIN COUNT	SO	SSOP	TSSOP	VSSOP	HVQFN
GTL2000	22	48		DL	DGG		
GTL2002	2	8	D		DP	DC	
GTL2010	10	24			PW		BS

Table 1. GTL20XX Selection Table

Operating Characteristics

- 1.0 V to 5.0 V voltage translation range
- 5.5 V tolerant I/O ports
- -40 ºC to 85 ºC operating temperature range
- ESD protection exceeds:
  - 2000 V HBM per JESD22-A114
  - 200 V MM per JESD22-A115
  - 1000 V CDM per JESD22-C101
- Latch-up is not possible because there is no V_{DD} pin.
- Manufactured in a high volume BiCMOS process for robust ESD performance.

Device Pinout

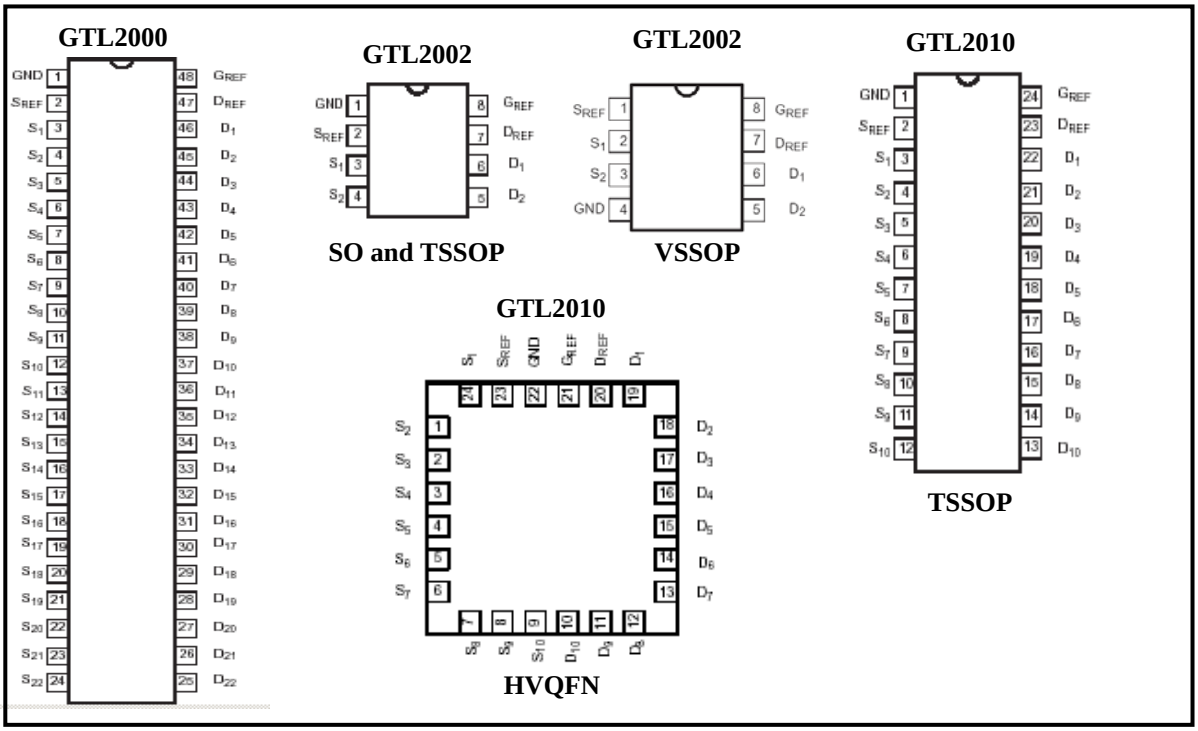


Figure 5. GTL20XX SO, SSOP, TSSOP, VSSOP and HVQFN Pin Outs

All the devices operate exactly the same and vary only on the number of I/O available. Any matched set of Sn and Dn pins can be used as SREF and DREF (e.g., pin 12 and 13 on the GTL2010 can be used for SREF and DREF instead of pins 2 and 23 which revert to S10 and D10).

Ordering Information

Package	Container	GTL2000	GTL2002	GTL2010
SO	Tube		GTL2002D	-
	T & R		GTL2002D-T	-
SSOP	Tube	GTL2000DL	-	-
	T & R	GTL2000DL-T	-	-
TSSOP	Tube	GTL2000DGG	-	GTL2010PW
	T & R	GTL2000DGG-T	GTL2002DP-T	GTL2010PW-T
VSSOP	T & R	-	GTL2002DC-T	
HVQFN	T & R	-	-	GTL2010BS-T

Table 2. GTL20xx Ordering Information

Data Sheets and IBIS Models

Data sheets and IBIS models can be downloaded from www.philipslogic.com

TECHNICAL INFORMATION

Block Diagram

GTL-TVC voltage-limiting application

In voltage-limiting applications, the common GREF input must be connected to one side (Sn or Dn) of any of the transistors (see Figure 6). This connection determines the DREF input of the reference transistor. The DREF and GREF inputs are connected together through a pull up resistor (typically 200 kΩ) to the V_{DD} supply. A filter capacitor (typically 0.1 µF) on DREF is recommended. Associated with the 200 kΩ resistor, the RC time constant is equal to 20 ms. The larger the capacitor, the less the gate node will move, the slower it will rise on power up.

The opposite side of the reference transistor is used as the reference voltage SREF connection. The SREF input should be less than V_{DD} – 1.5 V to insure that the reference transistor is properly biased into conduction. If the SREF is set to less than 1.5 V below Vdd, the maximum pass voltage may be less than the SREF voltage because the threshold voltage (the minimum gate to source voltage necessary for conduction) may be limiting the pass voltage rather than the SREF voltage. The gate to source threshold voltage will vary from part to part but will not vary within a package. The reference transistor regulates the gate voltage (GREF) of all the pass transistors in the package when properly biased, as described above.

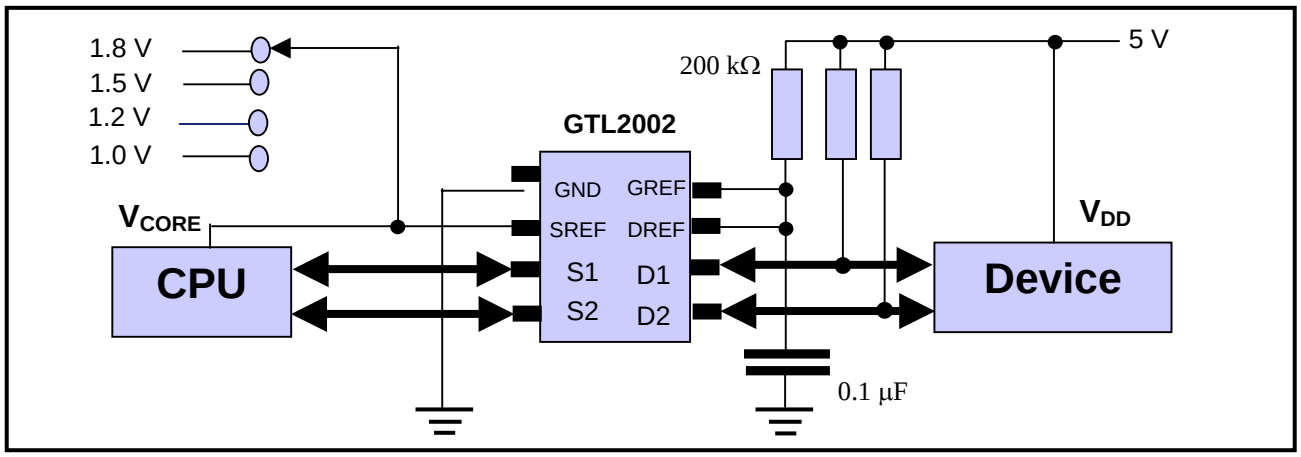


Figure 6 – GTL-TVC Typical Application Circuit

Propagation delay

Propagation delay for the GTL-TVC devices is problematic to define because, like the CBT functions, it is very small across the transistor. The rise time is dominated by the RC time constant of the node, and the fall time is dominated by the pull down driver, the total capacitance and the pull up resistor. The propagation delay is normally measured from ½ the swing on the lower voltage side to ½ the swing on the higher voltage side or vice versa. For a 0 V to 3 V transition on the input with a 1 ns edge rate to a 0 V to 3 V output, the measurement points on both sides would be 1.5 V and the propagation delay would be less than 1 ns. However, for a GTL+ to 5 V translation, where the pull up on the 5 V side is 2.2 k Ω and the total capacitance is 100 pF, the rising edge propagation would be measured from the 1 V point on the GTL+ side to 2.5 V on the 5 V side and would measure about 95 ns because of the RC time constant.

GTL-TVC Electrical characteristics

The typical electrical characteristics of the GTL-TVC NMOS transistors as measured over temperature using the test configuration shown in Figure 7 are included in Figures 8 to 13.

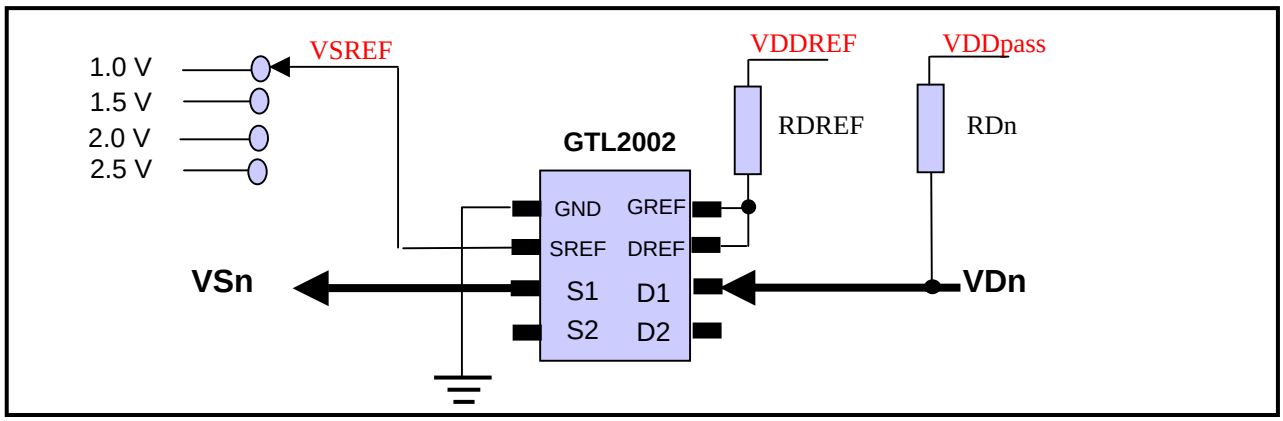


Figure 7. GTL-TVC Test Set Up

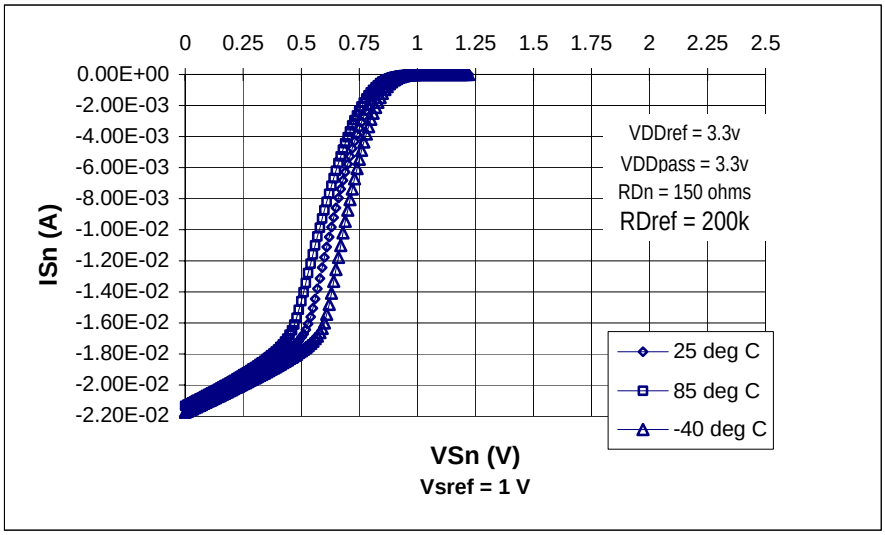


Figure 8. V – I Electrical Chacteristics at V_{SREF} = 1.0 Volt

As can be seen in Figure 8, the current is controlled by the 150 Ω resistor on the drain (RDn) until the source voltage is within about 0.5 volts of the SREF voltage where the pass transistor resistance increases rapidly to the point that the current through the pass transistor is just a few μA. This occurs as the source (Sn) voltage reaches the SREF voltage.

In any system, or logic level definition, there is a maximum low level input voltage (Vil) specified for the device. When a GTL-TVC device is used, the series combination of the driver and GTL-TVC device must not exceed the maximum Vil allowed for the logic family. Normally the allowed low level voltage is divided between the driver and the GTL-TVC device. If the driver is weak or the allowed low level voltage is small, it would be necessary to operate at a lower current than 15 mA. For example, if the GTL-TVC device is used as a translator for an I^2C bus, the current would be limited to 3 mA. On the other hand, if the driver is very strong and/or the allowed low level is large, it may be possible to operate the GTL-TVC device at currents higher than 15 mA, but in this case, it must be remembered that the voltage drop across the device will be greater than the 0.175 V maximun specified in the electrical characteristics of the data sheet.

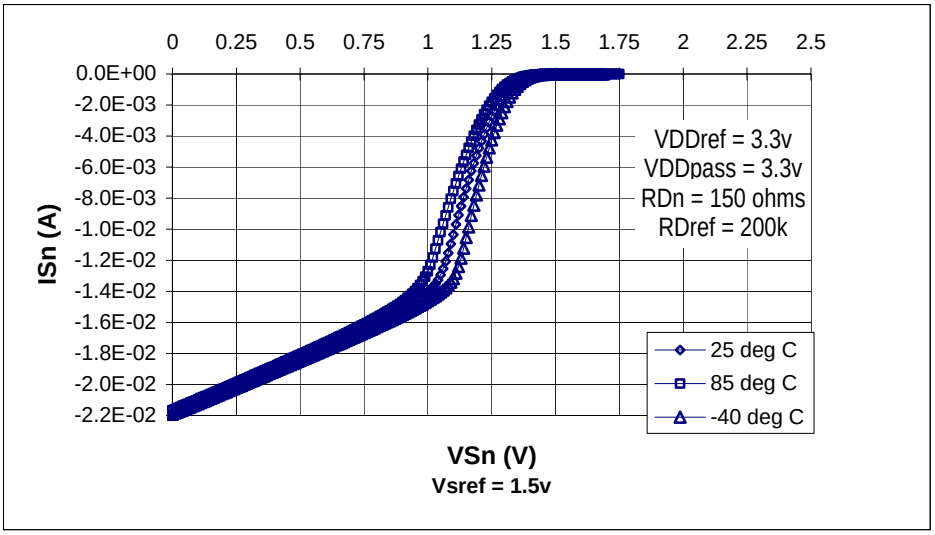


Figure 9. V-I Electrical Characteristics at V_{SREF} = 1.5 Volt

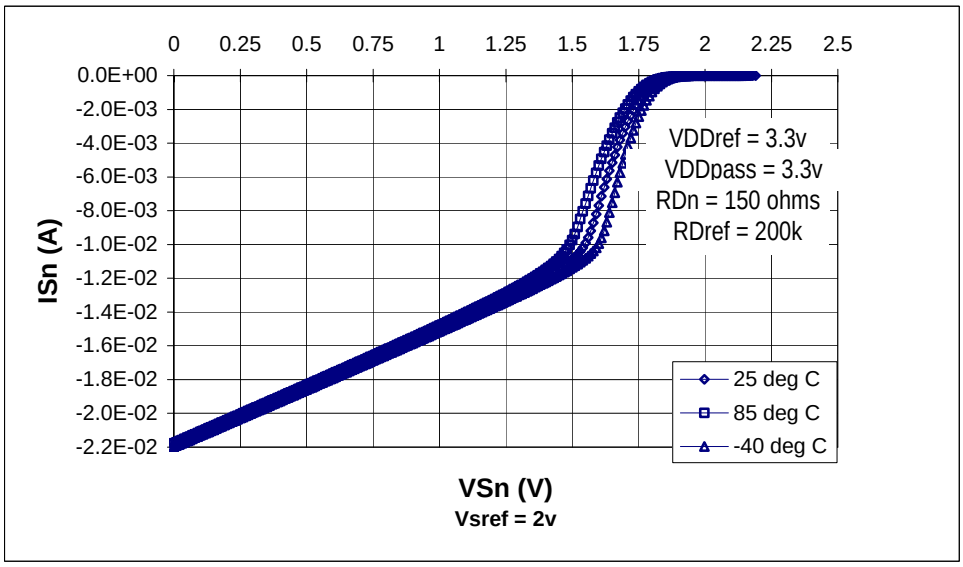


Figure 10. V-I Electrical Characteristics at V_{SREF} = 2.0 Volt

Figures 9 and 10 show the SREF at 1.5 V and 2.0 V respectively. The same behavior is observed where the current shuts off quickly as the source voltage gets within about 0.5 V of the SREF voltage.

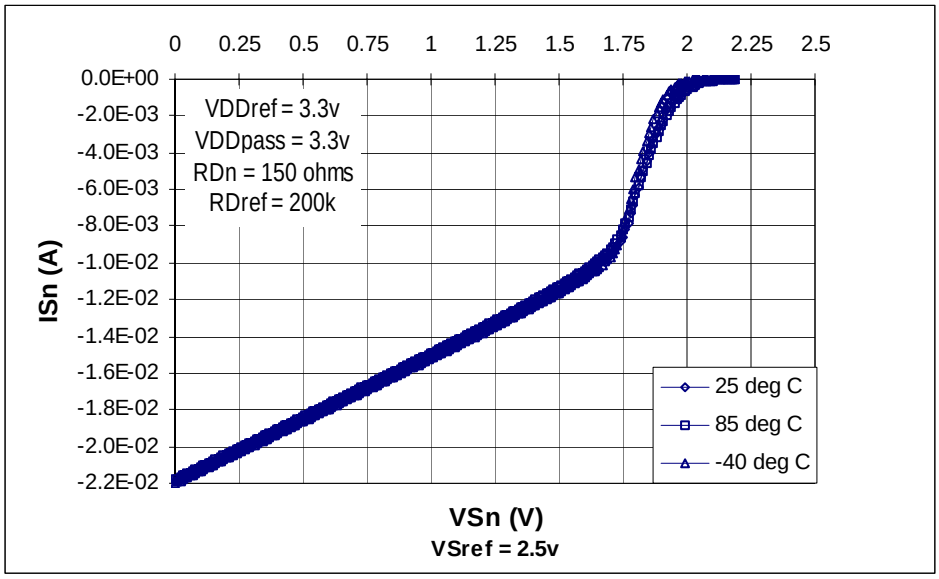


Figure 11. V-I Electrical Characteristics at V_{SREF} = 2.5 Volt and V_{DDREF} = 3.3 Volt

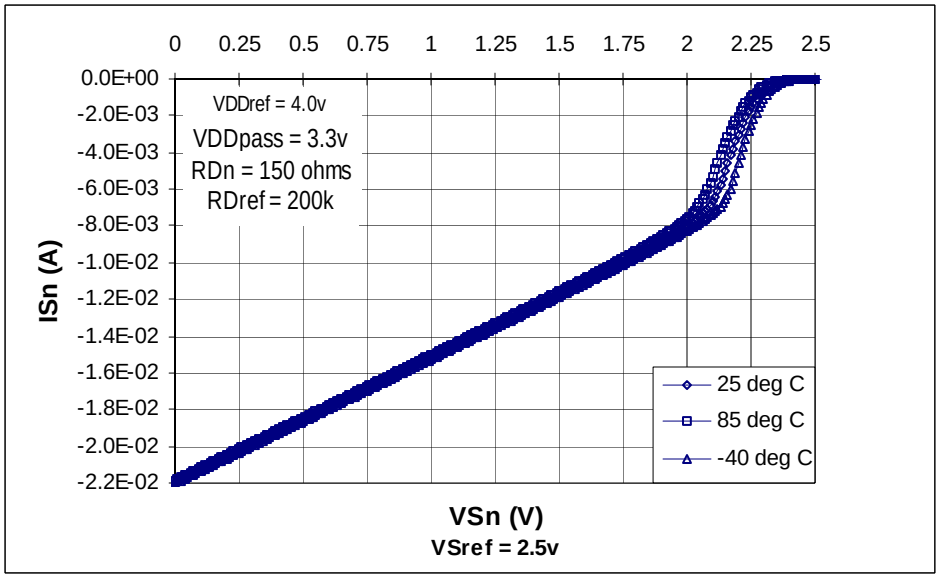


Figure 12. V-I Electrical Characteristics at V_{SREF} = 2.5 Volt and V_{DDREF} = 4.0 Volt

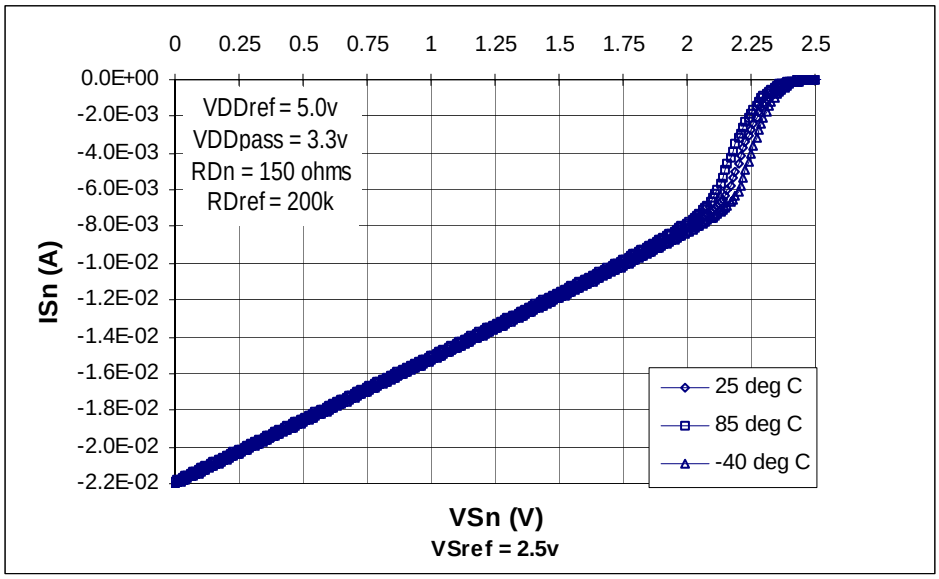


Figure 13. V-I Electrical Characteristics at V_{SREF} = 2.5 Volt and V_{DDREF} = 5.0 Volt

Figures 11, 12 and 13 show the SREF at 2.5 V with V_{DDREF} voltages of 3.3 V, 4.0 V, and 5.0 V respectively. Note that when V_{DDREF} is 3.3 V, with only 0.8 V between V_{DDREF} and the SREF voltage, the cold temperature curve turns off before the source voltage reaches the SREF voltage. With V_{DDREF} voltages of 4.0 V and 5.0 V, the behavior returns to normal where the turn off point is the SREF voltage, independent of temperature. The same pass transistor at hot temperatures has a higher on resistance so it starts to shut off sooner as the source voltage approaches the SREF voltage.

CBT Like Electrical characteristics

CBT like characteristics are tested using a setup as shown in Figure 14.

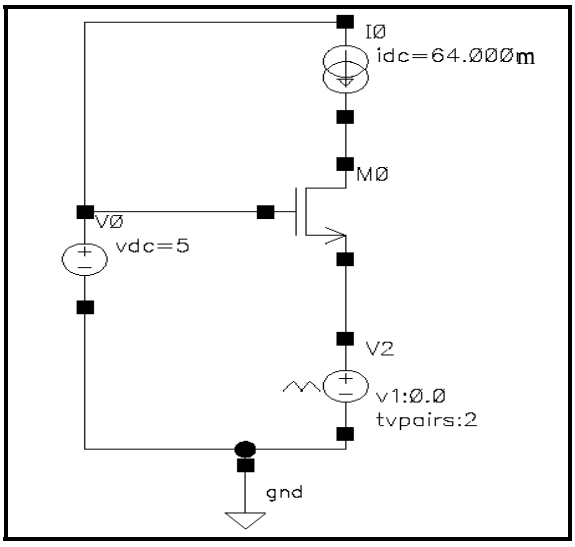


Figure 14 – CBT like Test Set Up

Figure 15 shows typical pass transistor on resistance (R_{ON}) as a function of source voltage with the gate at 5 V and I_{source} = 64 mA, Figure 16 shows R_{ON} with I_{source} = 15 mA. As can be clearly seen in these figures, the R_{ON} changes only slightly as long as the source voltage is less than the gate to source voltage necessary to conduct an Idsat equal to the current source current (64 mA for Figure 15 and 15 mA for Figure 16). The R_{ON} increases rapidly as the transistor is unable to conduct the high current. CBT functions are generally used with dynamic currents rather than static currents.

Figure 15 shows that a driver capable of first reflected wave switching can propagate its transition through the GTL-TVC device as a first reflected wave because, at 64 mA, the resistance is still low (~ 8 Ω at 2.5 V) and only 50 mA is required to impose a 2.5 V transition into a 50 Ω line (the voltage doubles at the end to 5 V).

Caution: It may be necessary to include a resistor in series with the driver if its pull up is stronger than a first reflected wave driver, to prevent over shoot and ringing in an unterminated transmission line.

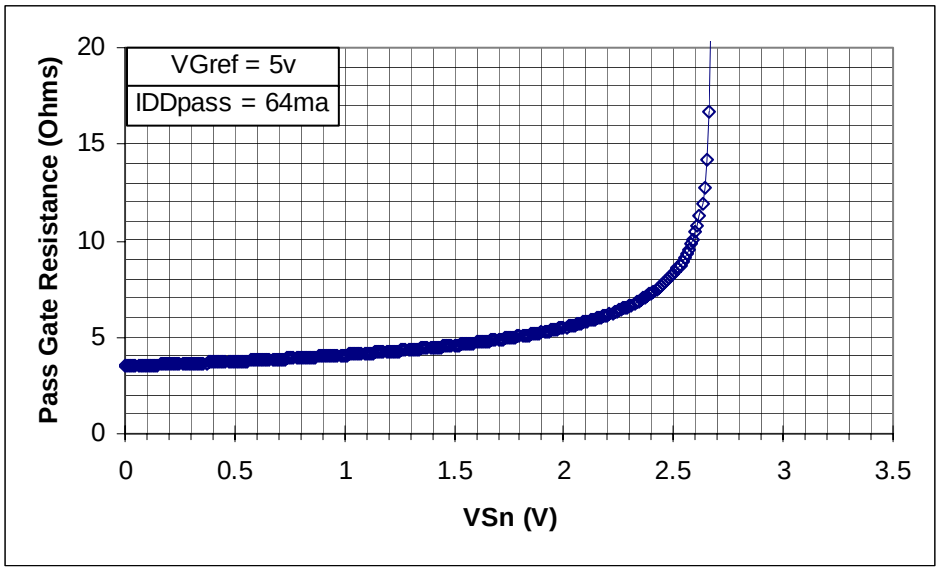


Figure 15. Electrical Characteristics as a CBT like function, resistance – source voltage with the gate at 5.0 V and 64 mA pass current.

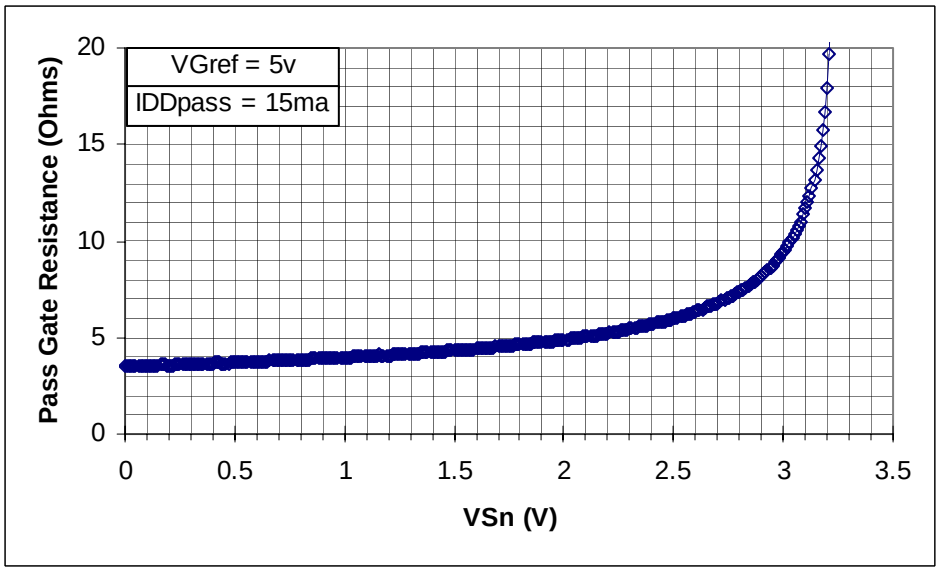


Figure 16. Electrical Characteristics as a CBT like function, resistance – source voltage with the gate at 5.0 V and 15 mA pass current.

Calculating Pull-Up Resistor Values

The pull-up resistor value needs to limit the current through the pass transistor when it is in the "on" state to about 15 mA. This will guarantee a pass voltage of 260 to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage will also be higher in the "on" state. To set the current through each pass transistor at 15 mA, calculate the pull-up resistor value as follows:

$$\text{Resistor Value (in } \Omega) = \frac{V_{pull\text{-}up} \text{ (in V)} - 0.350 \text{ V}}{0.015 \text{ A}}$$

Table 3 below summarizes resistor values for various reference voltages and currents at 15 mA and also at 10 mA and 3 mA. The resistor value shown in the highlighted box or a larger value should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the GTL-TVC device at 0.175 V, although the 15 mA only applies to current flowing through the GTL-TVC device.

Pull Up Resistor value (ohms)						
Voltage	**15 mA**		**10 mA**		**3 mA**	
	Nominal	**+ 10 %**	**Nominal**	**+ 10 %**	**Nominal**	**+ 10 %**
5.0 V	**310**	**341**	**465**	**512**	**1550**	**1705**
3.3 V	**197**	**217**	**295**	**325**	**983**	**1082**
2.5 V	**143**	**158**	**215**	**237**	**717**	**788**
1.8 V	**97**	**106**	**145**	**160**	**483**	**532**
1.5 V	**77**	**85**	**115**	**127**	**383**	**422**
1.2 V	**57**	**63**	**85**	**94**	**283**	**312**

1) Calculated for Vol = 0.35 V
2) Assumes output driver Vol = 0.175 V at stated current.
3) + 10 % to compensate for V_{DD} range and resistor tolerance.

Table 3. Pull Up Resistor Values

Alternate Sources

The Texas Instruments TVC devices operate the same as the Philips Semiconductors GTL-TVC devices but have different names for the connections as shown in table 4. The data sheet specifications are marginally different. The Texas Instruments TVC devices are CMOS construction.

Philips Semiconductors GTL-TVC	Texas Instruments TVC
GREF	GATE
DREF	Vbias
SREF	Vref

Table 4. Device Pin Name Comparison

APPLICATIONS

Voltage Level Translation

Figure 17 shows an application similar to the one shown in Figure 2 but with only one ASIC I^2C port that has to interface with both the 3.3 V and 5 V I^2C devices. Since the voltage difference between the low voltage (1.5V, left side) and the voltage on the resistor for the GREF (Gate pull-up) is higher than 1.5V, the resistors R30 and R25 are not required unless the devices on MI2C_CLK are leaky.

Note: Pull up resistors on the low voltage side are required if the difference between the voltage applied on the Gate reference (GREF) pull up resistor and the low side voltage is lower than 1.5 V.

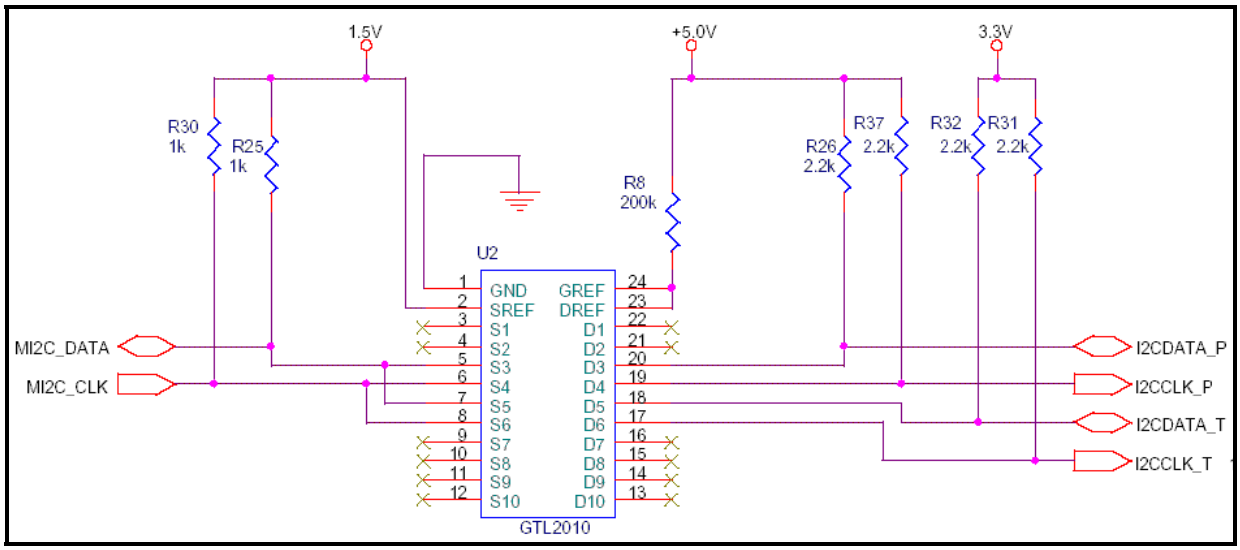


Figure 17. Example of 1.5 V I^2C Bus to both 3.3V SMBus and 5.0 V I^2C Bus

Note: Figure 2 and Figure 17 are from the Intel reference design. Resistor sizing works fine but is not in accordance with the recommendations in this application note.

FREQUENTLY ASKED QUESTIONS

Device

1. **Question:** The GTL-TVC schematic makes these parts look like an array of NMOS transistors?
   Answer: Yes, the GTL 2000, 2010 and 2002 are arrays of NMOS transistors with a common gate. These parts could be used as one large NMOS transistor by wiring all the sources together and all the drains together. However, they were designed as level shifters /clamps where the inherent matching is used by making one transistor a reference and the remaining transistors as level shifters/clamps. Not shown in the schematic are the ESD protection devices between each pin and ground.

2. **Question:** Can any transistor in the array be used as the reference transistor?
   Answer: Yes, any transistor can be used as long as its Dn pin is connected to the GREF pin and its associated Sn is used as the SREF. However, the DREF pin is probably the easiest to use because of its close proximity to the GREF pin.

3. **Question:** Are the Sn and Dn pins interchangeable?
   Answer: Yes, the Sn and Dn labels are merely for convenience in thinking about the devices. A Sn pin could be used as a drain and the corresponding Dn pin used as a source. The n indicates a number, which identifies a transistor. Thus, S1 and D1 correspond to transistor 1.

4. **Question:** Are both the Sn and Dn ports 5-V I/O tolerant?
   Answer: Yes, both the ports are 5.5 V tolerant, and the GREF is also 5.5 V tolerant.

5. **Question:** Do the GTL-TVC devices isolate the capacitance in the line?
   Answer: No, the devices don't have this capability since the device is basically an array of NMOS transistors.

6. **Question:** What will be the typical propagation delay for GTL2000 device family?
   Answer: The GTL2000 family of devices have the propagation delay associated with a 5 Ω wire for much of the swing. Thus with a 50 pF load and a low resistance driver driving the transition and measuring both sides at the same voltage level i.e. 1.5 V, the delay is about 0.25 ns. If the delay wanted is from one side GTL+ where the measurement point is 1 V to CMOS at 5 V in the other side, with a 2.5 V measurement voltage, then the delay is not the 0.25 ns of the GTL2000 family part. It is rather primarily the delay of the system, that is the RC time constant of the pull-up and the line capacitance, which determine the rise time between 1 V and 2.5 V. The fall time is not affected as much because the driver's effective resistance is very low compared to the pull-up so the 2.5 V to 1 V transition is much faster than the rising transition. For a 3 V to 5 V level translation, the measurement point difference is much less so the propagation delay is shorter. If the 5 V part is TTL input then the measurement points are the same.

7. **Question:** I am using a 3.3 V FPGA with a GTL device on some pins. The GTL device does the level conversion, either down to 1.8V or up to 5V. The pins from the GTL device go to a connector. There is a possibility that a human being touches it and there a ESD can occur. Will GTL prevent the FPGA from ESD? I think that the GTL device is ESD protected, am I right?
   Answer: The GTL2000/10/02 devices all have ESD protection > 2kV HBM and they should absorb most of the energy from an ESD event. The GTL part on the connector will absorb the primary ESD energy but we cannot guarantee that this will always protect the FPGA. Very little of the ESD energy should reach the FPGA however.

8. **Question:** Due to the requirement of the voltage for the 200 kΩ pull-up at both the GREF and DREF pins that has to be at least 1.5V more than the SREF voltage (1.8V in this case), the voltage at the 200 kΩ resistor need to be at least 3.3V. The design does not have such voltage provided other than 1.8V and 3.0V. Can the GTL2010 be used?
   Answer: The device will work with 1.2V differential but the actual voltage seen on the lower side may not be what SREF sets. Example would be one side at 5V and the other at 3V; you will always seen 5V and 3V. If one side is at 5V and the other at3.8V, then you will always seen 5V but may see > 3.8V on the other side depending on current flow. The higher voltage may not matter much unless the device in not tolerant to the higher voltage. You could also adjust the SREF to the low side of the band so that the overshoot doesn't over stress the device. The problem is not that the 3.8 V side would be above 3.8 V but rather that it might only get as high as 3.5 V and that the exact value will vary from part to part and would be between 3.5 V and 3.8 V. Or in the specific case the 1.8 V side high may

only pull up to 1.5 V when biased with the 3 V supply. If the 1.5 V level is not high enough a high value pull-up resistor could be used to the 1.8 V supply to make certain that it gets to 1.8 V.

Connecting the device to the right voltages/components

1. **Question:** In the recommended operating conditions table of the data sheet, the typical DREF is 3.3 V. Should DREF be equal to or greater than SREF on the reference transistor?
   Answer: The SREF and DREF can be equal, however, for best results the DREF should be connected through a 200 kΩ resistor to a power supply level that is at least 1.5 V above SREF. If the SREF is less than 1 V below the DREF, the maximum pass voltage may be limited to a voltage below SREF by the threshold of the transistor (e.g. DREF = 2.5 V and SREF = 1.8 V). When the SREF and DREF are equal, the threshold of the transistor determines the maximum pass voltage. Although the threshold variation within a package is small, the part-to-part variation can be larger. If the part-to-part threshold variation is acceptable, then the gate (GREF) could be tied directly to the power supply and the reference transistor used as one more pass transistor.

2. **Question:** You said "You can use SREF to clamp the Sn port at 1.5 V so you can feed in the 3.3 V signal on the Dn port side and clamp it at 1.5 V without having to use any pull up resistors on the lower voltage side, but going from 1.5 V to the 3.3 V you have to use pull up resistors on the 3.3 V Dn port side". My understanding is that going from a higher voltage (3.3 V PCI) to a lower voltage (1.5V AGP) doesn't need to use any pull-up resistors unless the logic used is based in pull-up resistors (like GTL). So in our case (push-pull logic) we don't need pull-ups on the AGP side. Am I right?
   Answer: If it is a uni-directional signal going from the 3.3 V PCI side (push-pull) to the 1.5 V AGP side (which is push pull logic so it doesn't need pull up resistors but operates in input mode only) then you don't need pull up resistors on the 3.3 V or 1.5V side except for the DREF pin which sets the reference voltage.

3. **Question:** We use only 3 bits on the GTL2010. Seven of the bits are No Connect (Dn and Sn is open). Is this OK or should they be tied to GREF?
   Answer: There are several acceptable ways of dealing with unused data paths and treating them as no connects is probably the easiest. It is recommended that pads be included on the circuit board for the unused pins so that after soldering the part will be firmly attached. Alternatively, the unused Dn and Sn pins can be connected together and tied to GND. It is not recommended connecting unused paths to GREF.

4. **Question:** I use three GTL2000 devices for translating 66 signals from 3.3 V to 1.8 V. Can the 200 kΩ resistor be shared by all three GTL2000 GREF and DREF pins or do I need three 200 kΩ resistors? What is the recommended value for the capacitor next to the 200 kΩ resistor?
   Answer: It would be best to use 3 different resistors, because different packages may not have identical characteristics and separate resistors / biasing allows the circuit to compensate for these differences. Sharing one resistor would not work well. If the characteristics matched perfectly they would be biased with an effective 600 kΩ resistor and if not perfectly matched one would be biased correctly and the other two would have too low of a gate voltage.
   For the capacitor, we usually recommend a 0.1 μF value. Note that the capacitor stabilizes the gate node but also slows its power up: with a 200 kΩ resistor, it will take on the order of 100 ms to get to the correct clamp level with a 0.1 μF capacitor. Since the gate node has over 100 pF capacitance the capacitor needs to be in at least the nF range to do anything. If you do not have any speed constraint at power up, then 0.1 μF would be safe enough.

5. **Question:** Is it possible to use a GTL2010 to perform bi-directional voltage translation between a 1.8V device and a 3.0V device B using the 3.0V device B supply for the 200 kΩ pull-up at both the GREF and DREF pins of GTL2010? As I understand from the GTL2010 datasheet, the pull-up supply has to be at least 1.5V more than the SREF voltage (1.8V in this case)). How should I connect the different pins of the GTL2010?
   Answer: Tie the 1.8 V signal to S side. And connect the 3.0 V signal to D side.
   The pull-up resistor is dependant on the driving current and signal level.
   For a 3.0 V signal and a 15 mA driving current, the pull-up resistor value is 177 Ω (normal) to 195 Ω (max) as indicated in page 6 of the GTL2010 data sheet.

6. **Question:** I am experiencing a problem with the GTL2000 when I reference the SREF input to the voltage supply of the CPU (1.1 V). The problem is sending a signal from the low I/O voltage device to the high I/O device. With input

S1 switching from High to Low and input S2 switching from Low to High, output D1's waveform is markedly different from D1's output when S1 and S2 both switch from High to Low. The waveform looks a lot better with SREF (1.3 V) greater than the CPU I/O voltage (1.1 V), but because of process reliability issues the Serf" voltage cannot be greater than the CPU supply voltage.

Answer: The GTL2000 is specified at 15.2 mA with the SREF at 1.365 V with the Dn at 0.175 V. When the SREF is at 1.1 V, the on resistance of the channel is degraded. The observation being referred to is that if both channels make a high to low transition at the same time the fall time of the Dn side is slower than if one is falling and the other is rising.

There are 2 reasons for this observation:

1. First is that there is some capacitive coupling between the drain and the gate and between the source and the gate. When the channels have opposite transitions, the coupled charges cancel out. When they are in the same direction they perturb the voltage on the GREF node making the channels weaker to pull the Dn nodes down. Role of the capacitor on the GREF node is to minimize this effect, however because the GREF pin has package inductance and the ESD protection includes some series resistance, the decoupling capacitor benefit is limited.
2. Second is that a SREF at 1.1 V results in an effective lower gate overdrive voltage, so the on resistance is higher. The 300 kΩ resistor to the 3.3 V supply biases the GREF to just a threshold above the SREF voltage. In the case of SREF = 1.1 V rather than SREF = 1.365 V the GREF will be 0.265 V lower.

Possible techniques to improve the behavior:

1. Include larger decoupling capacitor. This slows down the RC time constant of the GREF node.
2. Lower the value of the bias resistor so that it provides more charging current for the GREF node. It will also increase the leakage current at Sn = SREF.
3. Decrease the Sn low voltage to compensate for the higher on resistance.
4. Operate the channel at a lower current by raising the high voltage side resistor. This trades High to Low for Low to High delay.
5. Double up on channels (combine two I/Os), this increases the capacitance at the level shifter because of the two channels and reduces the on resistance.

7. **Question:** Why did we use GREF at 3.3V and inputs on that side at 2.5V for the timing test setup and why not 2.5V on GREF and the inputs to 1.5V SREF or 3.3V GREF and inputs to 1.5V SREF?

   Answer: The Vref or SREF for the test circuit is 1.365 V to 1.635 V, with the GREF and DREF connected together and tied through a 200 kΩ resistor to 3.3 V so the difference is 1.66 V which satisfies the 1.5 V requirement and the translation is 1.5 V (1.365 - 1.635) to 2.5 V. For the 2.5 to 3.3 V case, the resistor to GREF should be to 4 V or higher if 3.3 V is used the low side high voltage will be degraded below the 2.5 V on the SREF.

Applications

1. **Question:** Can I use the GTL2010 to level shift from 1.5 V to 3.3 V and from 1.5 V to 5 V at the same time?

   Answer: Yes, as long as the low side high voltage is the same for both translations, in this case 1.5 V. In this case, the SREF can be connected to 1.5 V and different transistors used, i.e. source side on the 1.5 V level and the drain of one at 3.3 V and the drain of the other at 5.0 V as shown in Figure 16. The Pull up resistors would need to be sized so as not to exceed the maximum allowed current (i.e., 15 mA) for the GTL-TVC device.

2. **Question:** How does the GTL-TVC device act like a termination for the GTL line?

   Answer: GTL and GTL+ logic families rely on incident wave switching which require the line to be terminated at the end with a resistor equal to the effective Z_0 of the line to prevent reflections. The line in GTL /GTL+ systems is generally used point to point with one termination resistor but could be use on a bus with multiple drivers, so it is driven from the middle and termination is required at both ends. The GTL-TVC device can be used in place of the termination at an end by sizing the resistor on the high voltage side (Dn side) to provide the same low state current that the termination resistor would have provided (i.e., GTL/GTL+ is about 15 mA).

3. **Question:** I have worked with the Intel 845 Northbridge chipset and I'm trying to use the GTL-TVC translators to interface a standard 3.3V PCI chip to the 1.5 V AGP bus of the i845. Any information related to my application would be appreciated.

   Answer: The Intel reference design doesn't use the same resistor values as we recommend. They use 1 kΩ for the 1.5 V side and 2.2 kΩ for the 3.3 V and 5 V side. GREF and DREF are connected together with a 200 kΩ resistor.

Use SREF to clamp the Sn port at 1.5 V so the 3.3 V Dn port side signal is clamped at 1.5V without having to use any pull up resistors on the lower voltage side. When going from 1.5 V to 3.3 V a pull up resistor has to be used on the 3.3 V Dn port side. The GTL-TVC devices don't have a direction pin that makes them very nice for bi-directional level translation.
The timing budget in AGP is quite tight so devices have to be as fast as possible. Both AGP and PCI do not have a signal to control the direction of the data so devices that don't have a direction pin (e.g., GTL-TVC) are very convenient.
Regarding the pull-up on the PCI side, in a typical PCI environment, only the control signals need pull-ups and those are provided by the motherboard. The stability of the rest of the signals is guaranteed by parking the bus. In the case where the PCI chip is not connected to the motherboard PCI bus, pull-up resistors on the control signals are required.

4. **Question:** Both the PCI 3.3 V and AGP 1.5 V are push-pull logic and most of the signals are bi-directional. For me it's clear that going from AGP 1.5 V to PCI 3.3 V needs pull up resistors to pull the signals up, so I need pull-ups on the PCI side. From the PCI 3.3 V side to the AGP 1.5 V we only need to clamp signals so my question is: Can I save the pull-ups on the AGP side?
   Answer: Yes, a pull-up is not required on the AGP 1.5 V side unless there are reflection related noise problems. If this is a GTL application with incident wave switching where typically both ends of the bus are terminated with the characteristic impedance of the bus, the GTL-TVC translator will replace one of the terminations. Unless the AGP edge rates are fast enough or the data rate is so high that the line needs to be terminated at both ends, the GTL20XX translators can provide the pull-up using current from the 3.3 V side and no pull up resistors are needed on the 1.5 V side.

5. **Multi-part Question :**
   We want to use the Philips GTL2010 for level shifting between Intel GMCH DVO @ 1.5 V and our TV Encoder @ 3.3 V. The diagram shown in Figure 17 is the reference circuit recommended by the TV encoder vendor. In the recommended circuit, there are two levels of voltage shifting, 1.5 V to 3.3 V and 1.5 V to 5 V. We will only use the level shifting of 1.5 V to 3.3 V by putting GREF (pin 24) and DREF (pin 23) to 3.3 V_{DD}. The signal running through the GTL2010 is the Open Drain I^2C Bus, bi-directional for the I^2C data and uni-directional for the I^2C clock.

   Question A: Do you think that the circuit shown in Figure 17 is well designed? Do you have an advice for the design?
   Answer A: You could try removing the pull up resistors on the 1.5 V side since the 3.3 V pull ups pass through the device and will pull the 1.5 V line high to the clamping voltage of 1.5 V. You can also leave them on since it will not hurt.

   Question B: VSn (ON-state) = 0.2 V max, VDn (ON-state) = 0.4 V max. Is this the input specification?
   Answer B: VSn is describing an input condition, VDn is describing the corresponding output condition. That is if a low of 0.2 V is forced on the Sn pin the corresponding Dn will be 0.4 V or less (but not less than Sn) for the pull-up currents within the data sheet.

   Question C: If 0.5 V is applied to the Sn, doesn't the FET become ON-state because VSn (ON-state) is 0.2 V maximum?
   Answer C: The data path is a large NMOS transistor, where the gate is nominally biased to a threshold above the reference source. Anytime that an Sn pin is forced to a voltage below the SREF the NMOS transistor will be on. The lower the Sn voltage the lower the on resistance. That is if the SREF is at 1.5 V and the GREF and DREF are connected together and a current limiting resistor of 200 kΩ connects between a 3.3 V supply and the GREF/DREF node. Then, if an Sn pin is pulled below 1.5 V the corresponding Dn will start to pull current. The closer to 0.0 V that the Sn gets the more current the Dn will pull, or, described as on-resistance, the lower the Sn voltage the lower the on-resistance.
   Note: the lower the SREF voltage the higher the effective on-resistance, because the effective VGS - Vt is less since the VG follows the SREF voltage.

   Question D: The On-state values are not dependant on Vs-ref but on the current through the device. I do not understand why on-state value is not dependant on Vs-ref. Could you tell me the reason in detail? I think that if Vs-ref is up, then Vg of the FET is up and then voltage difference between Vg and Vsn will become large, therefore the Vsn maximum voltage is more than 0.2 V.

Answer D: The voltage drop between Sn and Dn depends upon both current and the difference between Vs-ref and the voltage at Sn. For a specific selection of Vs-ref and Vsn, the voltage at Dn depends on the current. If the voltage of the SREF pin is raised, the necessary voltage on the Sn pin will rise if the same current and voltage drop between Sn and Dn are considered. If the voltage at Dn is considered fixed and the same current is needed, the Sn can only move up slightly even if the SREF is raised substantially.

Question E: When voltage of Sn is more than Vs-ref (V), the FET is high impedance and when voltage of Sn is less than 0.2V, the FET is low impedance. Is this correct? By the way, I would like to know the relationship between FET impedance versus voltage of Sn (or Dn) or FET impedance versus current through the FET. Do you have any measurement data?
Answer E: Yes, see Figures 8 to 13. When Sn = SREF, the bias circuit sets the current to a few microamperes, thus off, and for any Sn voltage above SREF, the leakage decreases.

Question F: Please see the DC specification of our product circuit. Could you tell me your opinion whether this circuit works correctly? If not, could you advise?
Answer F: The TV Encoder's Vol of 0.4 V @ 2.0 mA limits the resistor choices because the current on the TV Encoder side must not exceed 2.0 mA. If the 2.0 mA is divided into equal contributions from both the 1.5 V and 3.3 V sides, a minimum value of 1.1 kΩ on the 1.5 V side and a minimum value of 3 kΩ on the 3.3 V side are needed. Higher value resistors could be used at the expense of increasing the RC time constants. If the power supply ranges were ± 10 % (i.e., 3.3 V ± 0.3 V) then the minimum resistor value would be set by the high supply limits (3.3 kΩ on the 3.6 V (max) and 1.2 kΩ on the 1.65 V (max) side).

6. **Question:** On the GTL2002 parts, if you have a uni-directional signal that is being driven by an OR gate, can this net be put directly into the part on the TTL side, or do you have to have the inputs all open drain with pull-up resistors? I would expect this be all right since there is no way the microprocessor will drive this signal low and short a ground to a driven signal.
   Answer: The only possible problem is if the OR gate output drive is very strong (i.e. fast edge rates), it may be desirable to add a series termination resistor to the output of the OR gate to prevent ringing and an over voltage at the microprocessor caused by ringing. If the OR gate does not have fast edge rates there should be no problems. The GTL2002 will prevent any static over voltage of the microprocessor input but if the edge rate is too fast there may be some dynamic over voltage. Configuration is as following: SREF connected to the microprocessor power supply, DREF connected to GREF and to a high value resistor (200 kΩ) to a power supply at least 1.5 V above the microprocessor supply, and uni-directional down translation).

7. **Question:** We need a translator to convert signals from 5V to 3.3V and vice-versa. But the drivers are not open-drain. In this case, can I use GTL2000?
   Answer: If the drivers are not open drain, you system needs to integrate some flag between the driving devices so there is no conflict by having one device driving a high level while at the same time the other one is driving a low level. There needs to be a way to prevent bus contention otherwise the devices would be damaged. With that in mind, the GTL2000 can be used.

8. **Question:** Is the GTL2000/02/10 capable of supporting I^2C voltage level shifting in the Standard-speed mode (100kbits/s), Fast-speed mode (400kbit/s) and/or High-speed mode (3.4Mbits/s)?
   Answer: The GTL bi-directional voltage level translators are essentially frequency independent. So they should work at all three speeds. However, in addition to some series resistance, it also adds some capacitance to the wire. This is not a problem for the Standard mode or Fast mode, although it needs to be added to the total line capacitance. For the High-speed mode, the extra capacitance is probably undesirable, but the translators will communicate the signal if the rest of the capacitance is small enough.
   Note: During a low to high event in the High-speed mode, the master's current source pull up will not up translate through the GTL voltage level translators. That is if the master is on the low voltage side of the translator, the current source pull-up (active pull-up) will only pull-up the low voltage side of the bus because on the high voltage side of the translator, the high speed current source pull-up will cut off just below the clamp voltage (SREF), leaving only the normal pull up resistor on the high voltage side to complete the low to high transition (SREF to Vcc).

9. **Question:** GTL20xx in AGP applications. So far, the AGP specification is version 2.0 and the signal is specified at 1.5V. In AGP specification 3.0, the signal will migrate to a 0.8V swing and I think this will be a problem using the GTL20xx devices. Why was the low limit of the GTL20xx set at 1V? Could it be used at 0.8V?

Answer:: The low voltage limit is not in the DC specifications but the bullet under "Features" states level translation down to 1 V. The GTL20xx devices SREF is not recommended below 1 V to insure a low on resistance. The problem with a SREF voltage lower than 1V is that the gate overdrive, or the amount that the gate voltage is above the threshold, decreases as the SREF voltage is lowered. This means that the NMOS transistor does not turn on as hard and so the on resistance increases. Once you get below a certain gate overdrive, the on resistance increases rapidly. The part will still be functional, but the on resistance will be higher.

10. **Question**: We want to use the GTL2010 to translate signals from 1.5 V to 3.3 V so our settings will be V_{SREF} = 1.5V, V_{DREF} = 3.3V. But we use only 6-bits of the 10-bit GTL2010, so there are 4-bits unused. We plan to use these other 4-bits for signal translation from 3.3V to 5V. Looking through the application note we know that if the V_{DREF} is changed to 5V, then the GTL2010 can support both 3.3V and 5V output mix on the D side. But is it suitable for V_{SREF} to be changed to 3.3V so that the input will support both a 1.5V and 3.3V input mix on the S side?

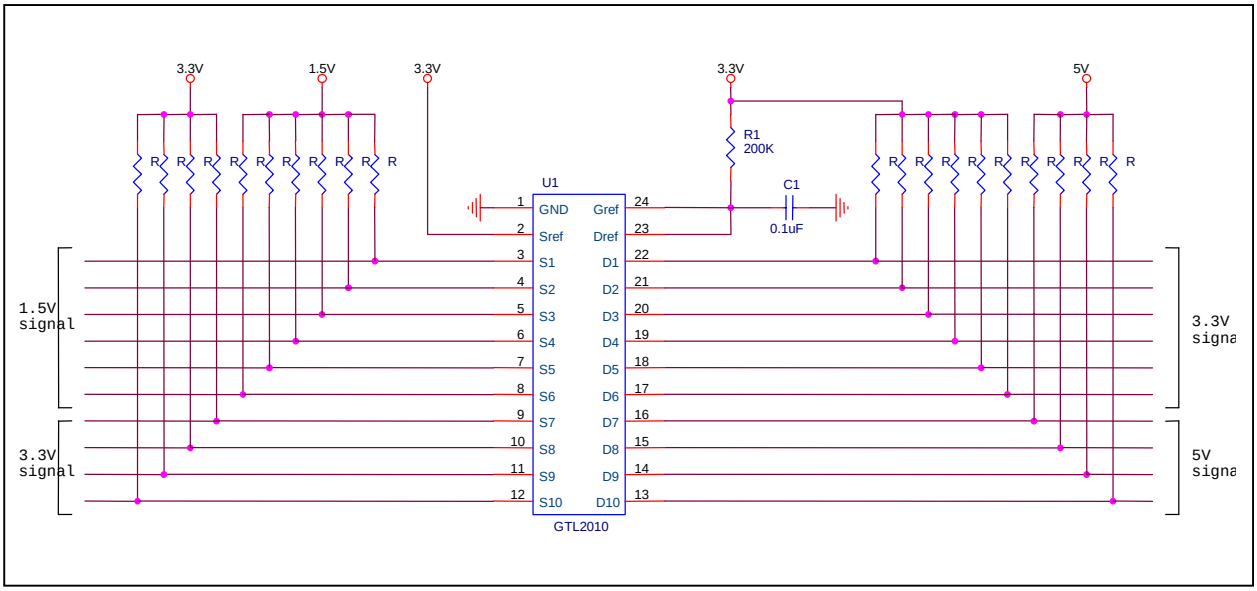


Figure 18. Application Diagram

Answer: To protect the 1.5 V parts the SREF must stay at 1.5 V and you will have to rely on the 3.3 V pull-up on the S side and the 5 V pull-up on the D side to get the high levels since the path will be essentially cut off above 1.5 V. It is possible to mix the voltages as proposed but the SREF must be 1.5 V and the resistors on both the 3.3 V and 5 V sides determine the highs with the low being passed through the GTL2010.

11. **Multi-part Question:**
I have a design where I need to translate voltage levels. My design needs fix 3.3V levels on D side.
Voltage levels on S side vary from 1.8V to 5V. So I did the following:
    1. SREF to 1.8 V, GREF+DREF through R = 200 kΩ to 5 V, D pins pull-ups to 3.3 V. This is 1.8 V compliant on S side.
    2. SREF to 3.3 V, GREF+DREF through R = 200 kΩ to 5 V, D pins pull-ups to 3.3 V. This is 3.3 V compliant on S side.
    3. SREF+GREF through R=200 kΩ to 5 V, DREF to 3.3 V, D pins pull-ups to 3.3 V. S pins pull-up to 5 V. I assume that DREF pin is now Vreference so it should not exceed 4.4V and should be 1.5 V below GREF. This is 5.0 V compliant on S side. The level on D side is 3.3 V.
    Question A: Am I right for the last assumption and is my design correct?
    Answer A: We assume that you are describing three different parts or at least three different jumper configurations, that is the 1.8 V, 3.3 V, and 5 V are not all present on different sources and drains at the same time because the level shift can only be down to one low voltage level per part/configuration.
    The answer to 3 is yes, the S and D are labels, the electrical characteristics are identical so connecting the SREF and GREF together and using a 200 kΩ resistor to 5 V to bias them with the DREF at 3.3 V is equivalent to connecting the DREF and GREF together and biasing them through the 200 K ohm resistor to 5 V, with the

SREF at 3.3 V. The effect is that the maximum high level that will be passed by the clamp is slightly above 3.3 V, whether the 5 V signals are applied to Sn or Dn pins.

Question B: Due to battery operation, we cannot afford to have 16mA pull-up current on 48 signals as this would result to current >700mA under certain conditions, so we opt for 3 to 4 mA per signal as a maximum.

- How would that influence the speed?
- What speed can I expect (in terms of rising/falling edges and frequency) and is the speed dependant on the value of pull-up resistors (higher resistors than recommended are used)?
- Is the speed influenced by $R_{PULL\text{-}UP}$ x C_{TOTAL} or is the matter more complex?
- I use a FPGA that is 3.3V device with 5 V tolerant I/O's. It has internal (active) pull-ups. Can I rely on them (use them) when translating from 1.8V to 3.3V (up conversion) or from 5V to 3.3V (down conversion)?

Answer B: The speed, that is the rise time is directly the RC product, so higher resistors will result in a slower behavior. For bi-directional signal operation it is necessary to use passive pull-ups or have an external circuit prevent contention between a low on one side with a high on the other side. If signals are flowing in only one direction on some lines the active pull-up on those lines cannot result in a contention because only one side has a driver. If the signal is being driven from the higher voltage logic to the lower voltage logic input the active pull-up is all that is needed, however if the low voltage logic is the driver, it will be necessary to use a pull-up on the high voltage logic side in order for the high level to reach a full high. An open drain bus is the easiest way to handle bidirectional signals, however it requires passive pull-ups. A more exotic alternative to resistors is use of current sources because they give a faster rise for the same worst-case maximum current.

12. **Question:** Is it possible to have the GTL2000 with 2.5V and 3.3V on one side and 5V on the other side?
    Answer: Yes, if the 2.5 V and 3.3V low side voltages are present at different times / applications, the SREF could be used to connect to the current low side voltage. If both 2.5 V and 3.3 V voltages are present at the same time on the low voltage side with 5.0 V on the high voltage side, the SREF will need to be connected to the lowest voltage, 2.5 V in this case, and the voltage that will be passed on the 3.3 V pins would be 2.5 V. Pull up resistors could be used on the 3.3 V pins to achieve 3.3 V. The unidirectional or bidirectional voltage can be applied on a per channel basis. The idea of bi-directional is that there are drivers on both sides of the GTL2000 that can be active, so the signal can flow in either direction. If the outputs are totem pole outputs, some mechanism is required to prevent the contention of a high level on one side with a low level on the other. The use of open drain outputs eliminates the possibility of such a contention. Uni-directional means only one side of each channel has a driver so contention is not possible. Different channels in the same GTL2000 can be operated as bi-directional, uni-directional up translation or uni-directional down translation, and the high side voltages can differ, but the SREF must be connected to the low side voltage in order to clamp to that voltage.

13. **Multi-part Question:**
    Question A: I have been looking at using the GTL2000 for a 2.5-V FPGA to 5-V Sensor drive.
    Here's my configuration: the FPGA has to drive 17 control signals to a 5 V part. The 5 V part has 2 outputs that connect to the FPGA. The FPGA is NOT 5 V tolerant and cannot be configured to have open drain outputs. What configuration would be best for me to use?
    Answer A: The clamp voltage would be set at 2.5 V and then each Sn/Dn pair can be used in a uni-directional (either direction) or bi-directional mode where you just need to treat each Sn/Dn pair individually. So the seventeen 2.5 V to 5 V signals would have no resistors on the 2.5 V side that are driven with the totem pole outputs and you would need to put pull up resistors on the 5 V side so the sensor input would see 5 V H (high) when the FPGA is driving high or L (low) when the FPGA is driving low. The 2 5 V to 2.5 V signals would not need the pull ups on the 5 V side if the sensor has totem pole outputs and you don't need pull up resistors on the 2.5 V side if you don't have too much leakage.

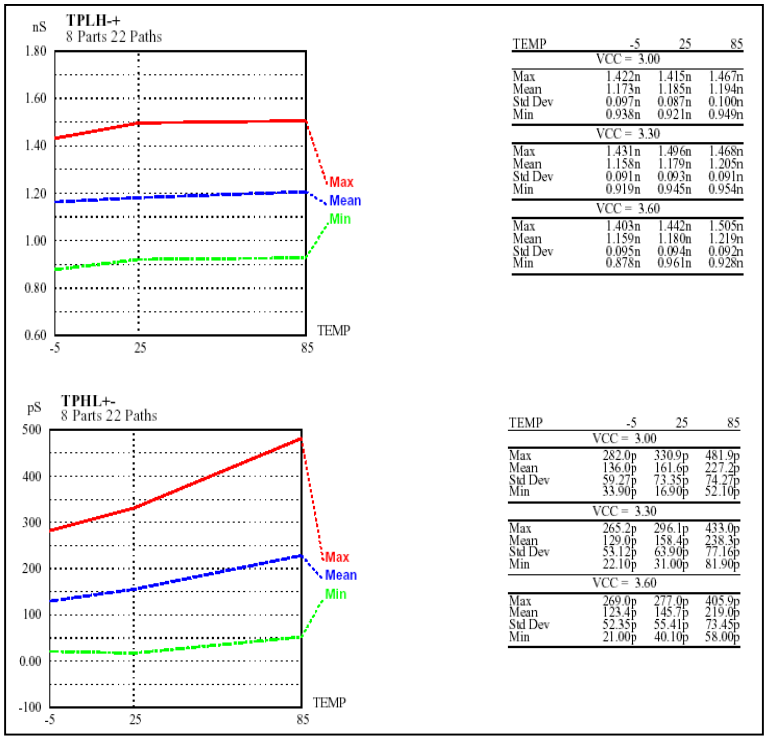
    Question B: What if I was to up the FPGA output voltage and input tolerance to 3.0 V or even 3.3 V? Would the configuration be the same except for SREF being pulled to 3.3 V instead of 2.5 V?
    Answer B: Yes, this is correct.

14. **Question:** I want to use the GTL2010 as unidirectional conversion from 3.3 V to 1.5 V on some control signals to a CPU. I also want to have jumper override on these signals, so I want to put on the low side an option to either pull the signal up through a 2.2 kΩ resistor or pull down through a 2.2 kΩ resistor. If the high side is driving high and the low side is pulled down with the 2.2 kΩ resistor, is it like having a 200 kΩ resistor pulling up with a 2.2 kΩ resistor pulling down (200 kΩ connected between GREF, DREF to 3.3 V) thus getting a logical Low on the Low side?
    I cannot connect the low side directly to GND or 1.5V.

Answer: The jumper probably needs to disconnect the 3.3 V side. If the 3.3 V side driver is a push pull type driver it must be disconnected before the low side resistor jumpers can be effective. If it is open drain (NMOS) then the pull down jumper would form a resistor divider with the pull up resistor (probably should still disconnect the 3.3 V side), if the pull-up resistor is a sufficiently high value it will look low. If the driver is strong it will pull the 2.2 kΩ pull-up low through the GTL2010. Please note that grounding SREF will disconnect the 3.3 V side for all channels.
I think that the bottom line is that the 3.3 V side needs to be disconnected in order for the 2.2 kΩ jumpers to work because the on resistance of the GTL2010 is only a few ohms when either side is low and it only rises slowly as the low voltage rises until it is within less than 1 V below the SREF then it rises like 1/(V applied - V of SREF)**2 to about 200 kΩ when V applied = V of SREF and then increases exponentially. So the low could be pulled up by the 3.3 V side to above 0.75 V and a low on the 3.3 V side would certainly pull the 2.2 kΩ pull-up resistor on the 1.5 V side low.

15. **Multi-part Question:**
We intend to use the GTL2000 for a PCI to AGP converter. The device will bi-directionally translate 1.5 V to 3.3 V.
Question A: Pull up resistors: We would like to be sure they are not needed on both sides of the device. Our guess would be that they are needed only on the High side but they want to be sure.
Answer A: No pull-up is required on the low voltage side unless that side is known to have a significant leakage to ground i.e. >10 µA.

Question B: Propagation delay: spec says between 0.5 and 5.5 ns. They would like to have more info on that like simulations or characterization results if possible.
Answer B: The GTL2000 (and GTL2002 and 10) can be thought of as acting like a wire, with a little resistance and some capacitance. The characterization data that can be found in Figure 19 shows the following:
- The high to low transition is less than 1 ns with a strong pull-down driver driving through the GTL2000.
- The low to high transition is determined by the RC time constant. The ~1.2 ns in the characterization represents the added delay because of the capacitance of the GTL2000. The actual low to high transition time in the system is determined by the total RC time constant and the relevant pick off points. For example if the pull-up is 200 Ω and the total capacitance is 100 pF, the time constant would be 20 ns and for a pick off point that is 1/2 the swing the delay would be ~14 ns.



TEMP	-5	25	85
VCC = 3.00			
Max	1.422n	1.415n	1.467n
Mean	1.173n	1.185n	1.194n
Std Dev	0.097n	0.087n	0.100n
Min	0.938n	0.921n	0.949n
VCC = 3.30			
Max	1.431n	1.496n	1.468n
Mean	1.158n	1.179n	1.205n
Std Dev	0.091n	0.093n	0.091n
Min	0.919n	0.945n	0.954n
VCC = 3.60			
Max	1.403n	1.442n	1.505n
Mean	1.159n	1.180n	1.219n
Std Dev	0.095n	0.094n	0.092n
Min	0.878n	0.961n	0.928n

TEMP	-5	25	85
VCC = 3.00			
Max	282.0p	330.9p	481.9p
Mean	136.0p	161.6p	227.2p
Std Dev	59.27p	73.35p	74.27p
Min	33.90p	16.90p	52.10p
VCC = 3.30			
Max	265.2p	296.1p	433.0p
Mean	129.0p	158.4p	238.3p
Std Dev	53.12p	63.90p	77.16p
Min	22.10p	31.00p	81.90p
VCC = 3.60			
Max	269.0p	277.0p	405.9p
Mean	123.4p	145.7p	219.0p
Std Dev	52.35p	55.41p	73.45p
Min	21.00p	40.10p	58.00p

Figure 19. Propagation delay characterization results

16. **Multi-part Question :**
We are using the GTL2000 for the one-way level shifting from 3.3V -> 1.8V.
Question A: let us know the set up time and the hold time of GTL2000.
Answer A: "Set up and hold" are usually referring to flip flop or latch parts, so they have no meaning with respect to the GTL2000 parts.

Question B: When the transistor is off and the GREF and DREF are Low, it is specified that the input and the output are don't care. When GTL2000 becomes this state, is this correct that all input and output of the GTL2000 become the high impedance. Please let us know the maximum voltage we can induce to the I/O of GTL2000 when it is the high impedance. Can we induce the 5.5V max to the I./O ?
Answer B: If the GREF pin is at ground the transistors in the GTL2000 are off and the path from each D to its S is high impedance.
Note: If the intent is to switch the GREF pin the enable time and the disable time will depend upon how quickly the GREF pin voltage transitions between ground and the bias voltage for the appropriate level shift conditions.
For example, let assume that the 200 kΩ pull-up resistor is used to connect the GREF and DREF to the 3.3 V power supply and a 1 μF capacitor is used for decoupling between the GREF and DREF node and ground. The RC time constant of the GREF node would be 0.2 s meaning that the enable time would be on the order of 0.2 s. The disable time if the SREF is connected to ground or if the GREF is connected to ground by a transistor or open drain or open collector gate would be the delay of the gate because the internal time constant is only about 5 ns as soon as the GREF falls below about 0.5 V the transistors are off.

If the need is for the GTL2000 to enable and disable quickly about the best solution that could be recommended would be to use a high drive CMOS gate (with a minimum high level drive current maximum of at least 15 mA), a series 50 ohm resistor between the CMOS gate and the GREF pin of the GTL2000 and a diode with its anode on the GREF and 50 ohm resistor node and its anode to the 1.8 V power supply. This solution is fast ~ 10 ns at the expense of wasting about 15 mA of current and doing a less than perfect translation. This will also require pull-up resistors on the low voltage side as well as the high voltage side because the diode forward does not match the threshold of the NMOS transistors in the GTL2000. Increasing the 50 ohm resistor if slower enable and disable times can be tolerated can reduce power.

ADDITIONAL INFORMATION

The latest datasheets for the GTL2000/02/10 Bi-Directional Low Voltage Translators and other Specialty Logic products can be found at the Philips Semiconductors website: www.philipslogic.com

Additionnal technical support for GTL2000/02/10 Bi-Directional Low Voltage Translator devices can be provided by e-mailing the question to: I2C.support@philips.com

Bi-directional low voltage translators AN10145

REVISION HISTORY

Rev	Date	Description
_2	20040811	**Application note (9397 750 13933). Supersedes data of 16 December 2002.**
_1	20021216	**Application note; initial version.**

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Date of release: 08-04

Document order number: 9397 750 13933

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