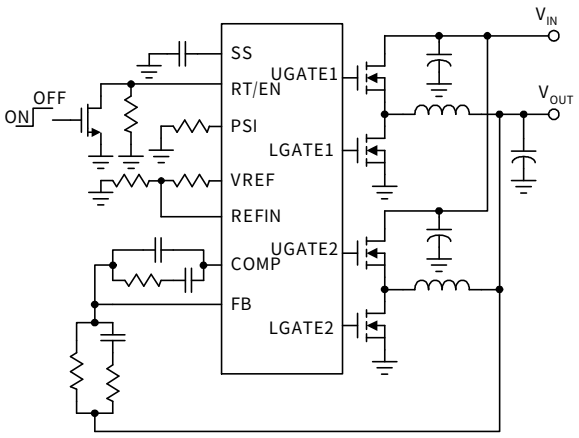
Dual-Phase Synchronous-Rectifier Buck Controller

Features

- **Voltage-Mode Operation with Current Sharing**
- **Operate with 4.5V~13.2V Supply Voltage**
- **Support Single and Two-Phase Operations**
- **±2% Reference Voltage Accuracy Over Temperature**
- **Loss-Less Inductor DCR Current Sensing**
- **Adjustable Over Current Protection use DCR Current Sensing**
- **Programmable PWM Switching Frequency from 100kHz to 800kHz**
- **Dynamic Output Voltage Adjustment**
- **Adjustable Soft-start**
- **QFN4x4-24 Package**
- **Halogen and Lead Free Available (RoHS Compliant)**

Simplified Application Circuit



General Description

The APW8700, two-phase PWM control IC, provides a precision voltage regulation system for advanced graphic card and motherboard applications. The integration of power MOSFET drivers into the controller IC and reduces the number of external parts for a cost and space saving power management solution.

The APW8700 uses a voltage-mode PWM architecture, operating with adjust frequency from 100kHz to 800kHz. The device uses the voltage across the DCRs of the inductors for current sensing achieves high efficiency. The device integrates adjustable load line voltage positioning (droop) and adopts low side R_{DS_ON} for channel-current balance.

The automatic phase reduction and over-current protection are accomplished through continuous inductor DCRs current sensing.

The APW8700 also implement a one-bit VID control operation in which the feedback voltage is regulated and tracks external input reference voltage.

This controller protection features include over-temperature(OTP), over-voltage(OVP), under-voltage (UVP) and over-current protections (OCP).

The device also provides a power-on-reset function and a programmable soft-start to prevent wrong operation and limit the input surge current during power-on or start-up. The APW8700 is available in QFN4x4-24 packages.

Applications

- **VGA**
- **Mother Board**

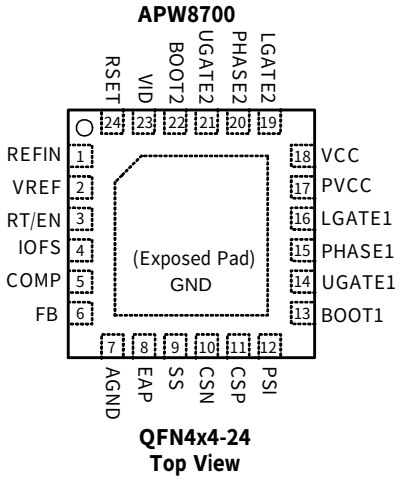
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APW8700 □□□ – □□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QA : QFN4x4-24 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW8700 QA : 	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



QFN4x4-24
Top View

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{VCC}	Input Supply Voltage (V_{VCC} to GND)		-0.3 ~ 16	V
V_{PVCC}	Gate Driver Supply Voltage (V_{PVCC} to GND)		-0.3 ~ V_{VCC}+1	V
	BOOT1/2 to PHASE1/2 Voltage		-0.3 ~ 16	V
	BOOT1/2 to GND Voltage		-0.3 ~ 30	V
	UGATE1/2 to PHASE1/2 Voltage	> 200ns	-0.3 ~ $V_{BOOT1/2}$+0.3	V
		< 200ns	-5 ~ $V_{BOOT1/2}$+5	V
$V_{LGATE1/2}$	LGATE1/2 to GND Voltage	> 200ns	-0.3 ~ V_{VCC}+0.3	V
		< 200ns	-5 ~ V_{VCC}+5	V
$V_{PHASE1/2}$	PHASE1/2 to GND Voltage	> 200ns	-0.3 ~ 16	V
		< 200ns	-10 ~ 30	V
	REFIN, VREF, RT/EN, IOFS, COMP, FB, EAP, SS, CSP, CSN, PSI, VID, RSET to AGND Voltage		-0.3 ~ 7	V
	AGND to GND		-0.3 +0.3	V
P_D	Power Dissipation		2.5	W

Absolute Maximum Ratings (Cont.) (Note 1)

Symbol	Parameter	Rating	Unit
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	QFN4x4-24	41	°C/W
θ_{JC}	Junction-to-Case Resistance	QFN4x4-24	9	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{VCC}	VCC Supply Voltage (V_{VCC} to GND)	4.5 ~ 13.2	V
V_{OUT}	V_{OUT} to GND	0.6 ~ 5.5	V
V_{IN}	Converter Input Voltage	2 ~ 13.2	V
F_{OSC}	Oscillator Frequency	100 ~ 800	kHz
I_{OUT}	Converter Output Current	0 ~ 60	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the application circuit for further information.

Electrical Characteristics

Refer to figure 1 in the "Typical Application Circuits". These specifications apply over V_{VCC} = 12V, TA= 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8700			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
VCC	Supply Voltage Range		4.5	-	13.2	V
I_{DD_SD}	Input DC Bias Current	No switching, RT/EN=GND	-	4	5	mA
I_{DD}		UGATE1/2, LGATE1/2 open, switching	-	5	7	mA
V_{PVCC}	Regulated Supply Voltage	RT/EN=GND, I_{PVCC}=0mA	8	9	10	V
	POR Threshold of VCC		3.8	4.1	4.4	V
	POR Hysteresis		0.3	0.5	0.6	V
	POR Threshold of PVCC		3.8	4.1	4.4	V
	POR Hysteresis		0.3	0.5	0.6	V

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Electrical Characteristics (Cont.)

Refer to figure 1 in the "Typical Application Circuits". These specifications apply over V_{VCC} = 12V, TA= 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8700			Unit
			Min.	Typ.	Max.	
CHIP ENABLE/FREQUENCY SETTING						
$I_{RT/EN}$	RT/EN Source Current	RT/EN=GND	-	-	120	μA
	RT/EN Shutdown Threshold		0.45	0.5	0.55	V
	Enable Debounce time	RT/EN high debounce	-	200	-	μs
$V_{RT/EN}$	RT/EN Voltage	$R_{RT/ENB}$=33kΩ	-	1	-	V
	Switching Frequency Setting Range		100	-	800	kHz
F_{OSC}	Free Run Switching Frequency	$R_{RT/EN}$=33kΩ	255	300	345	kHz
ΔF_{OSC}	Switching Frequency Accuracy	F_{OSC}=200kHz~500kHz	-15	-	15	%
SOFT-START						
I_{SS}	Soft-start Current	During Soft-start	-	20	-	μA
	SS Source/Sink Current Capability	After Soft-start	-	200	-	μA
OSCILLATOR						
	Maximum Duty Cycle		-	85	-	%
	Minmum Duty Cycle		-	0	-	%
ΔV_{OSC}	Ramp Amplitude	V_{VCC}=12V	-	1.5	-	V
POWER SAVING MODE						
V_{PSI}	Threshold Voltage to Enter Dual Phase	V_{PSI} Rising	0.55	0.6	0.65	V
ΔV_{PSI}	Hysteresis to Enter Single Phase	V_{PSI} Falling	-	0.2	-	V
	2 Phase to single phase debounce	Continuously	-	0.2	-	ms
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage Accuracy	I_{REF}=100μA, T_J= -20°C ~ 70°C	1.98	2.00	2.02	V
	VREF Maximum Output Current	VREF=GND	20	-	-	mA
ΔV_{REF}	Reference Voltage Load Regulation	I_{REF}=0~2mA	-5	-	5	mV
V_{FB}	Output Voltage Accuracy	V_{REFIN}-V_{FB}, V_{REFIN}=0.8V~2V, R_{DRP}=0Ω	-5	-	5	mV
		V_{FB} operating range	0.2	-	V_{REF}	V
ERROR AMPLIFIER						
	Open-Loop DC Gain (Note 4)	R_L = 10kΩ, C_L =10pF	-	80	-	V/V
	Open-Loop Bandwidth (Note 4)	R_L = 10kΩ, C_L =10pF	-	20	-	MHz
	Slew Rate (Note 4)	R_L = 10kΩ, C_L =10pF	-	8	-	V/μs
	FB Input Leakage Current	V_{FB}=1V	-	0.1	0.5	μA
V_{COMP}	COMP High Voltage	R_L = 10kΩ, C_L =10pF	-	4.8	-	V/μs
	COMP Low Voltage	R_L = 10kΩ, C_L =10pF	-	0.2	-	μA
I_{COMP}	Maximum COMP Source Current	V_{COMP}=2V	-	2	-	mA
	Maximum COMP Sink Current	V_{COMP}=2V	-	2	-	mA

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Electrical Characteristics (Cont.)

Refer to figure 1 in the "Typical Application Circuits". These specifications apply over V_{VCC} = 12V, TA= 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8700			Unit
			Min.	Typ.	Max.	
TOTAL CURRENT SENSE						
I_{CSN_MAX}	Maximum Sourcing Current		100	-	-	µA
	GM Amplifier Offset		-5	-	5	mV
I_{CSN_OCP}	Over-Current Protection Threshold Level		55	60	65	µA
	Droop Accuracy	I_{DRP}/I_{CSN}	90	100	110	%
	PSI Accuracy	I_{PSI}/I_{CSN}	90	100	110	%
PHASE CURRENT SENSE						
gm	Trans-conductance		-	1.0	-	mA/V
V_{IOFS}	IOFS Voltage	100kΩ from IOFS to VREF	1.425	1.5	1.575	V
		100kΩ from IOFS to GND	0.475	0.5	0.525	V
VID CONTROL INPUT						
V_{IH}	Logic High Threshold Level		1.2	-	-	V
V_{IL}	Logic Low Threshold Level		-	-	0.4	V
R_{RSET}	On Resistance of RSET MOSFET	VID=High	-	20	-	Ω
I_{RSET}	Leakage Current of RSET Pin	V_{RSET}=2V, VID=GND	-	-	0.1	µA
Gate Driver						
R_{UG_SRC}	Upper Side Gate Sourcing	I_{UGATE}=100mA Sourcing	-	2	4	Ω
R_{UG_SNK}	Upper Side Gate Sinking	I_{UGATE}=100mA Sinking	-	1.5	3	Ω
R_{LG_SRC}	Low Side Gate Sourcing	I_{LGATE}=100mA Sourcing	-	2	4	Ω
R_{LG_SNK}	Low Side Gate Sinking	I_{LGATE}=100mA Sinking	-	1	2	Ω
T_{DT}	Dead-time		-	30	-	ns
PROTECTION						
	Over Voltage Protection (OVP)	V_{FB}/V_{EAP}	125	130	135	%
	Over Voltage Hysteresis		-	20	-	%
	Under Voltage Protection (UVP)	V_{FB}/V_{EAP}	45	50	55	%
	Over Current Protection (OCP)	I_{CSN}	55	60	65	µA
	Over Temperature Protection (OTP)		-	150	-	°C
	Over Temperature Hysteresis		-	20	-	°C

Note 4: Guarantee by design, not production test

Pin Description

PIN	NAME	FUNCTION
1	REFIN	External Reference Input. This is input pin of external reference voltage. Connect a voltage divider from VREF to REFIN to AGND to set the reference voltage.
2	VREF	Reference Voltage Output. This is the output pin of high precision 2V reference voltage. Bypass this pin with a 1μF ceramic capacitor to AGND.
3	RT/EN	Operation Frequency Setting. Connecting a resistor between this pin and AGND to set the operation frequency. Pull this pin to ground to shut down the APW8700.
4	IOFS	Current Balance Adjustment. Connect a resistor from this pin to VREF or GND to adjust the current sharing.
5	COMP	Error Amplifier Output. Use this pin in combination with the FB pin to compensate the voltage-control feedback loop of the converter.
6	FB	Feedback Voltage. This pin is the inverting input to the error amplifier. Use this pin in combination with the COMP pin to compensate the voltage control feedback loop of the converter.
7	AGND	Analog Ground. Connect this pin to the GND pin where the output voltage is to be regulated.
8	EAP	Non-Inverting Input of Error Amplifier. Connect a resistor to SS pin to set the droop slope.
9	SS	Soft Start Output. Connect a capacitor to GND to set the soft start interval.
10	CSN	Inverting Input of Current Sensing Amplifier.
11	CSP	Non-Inverting Input of Current Sensing Amplifier.
12	PSI	Power Saving Indicator. Connect a resistor from PSI to AGND to set the power saving mode threshold current level. Connect this pin to VREF for always two phases operation. Short this pin to ground for always single-phase operation. Don't left this pin floating.
13	BOOT1	Bootstrap Supply for the floating high-side gate driver of channel 1. Connect the Bootstrap capacitor between the BOOT1 pin and the PHASE1 pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the high-side MOSFET. Typical values for CBOOT range from 0.1μF to 1μF.Ensure that CBOOT is placed near the IC.
14	UGATE1	Upper Gate Driver Output for channel 1. Connect this pin to the gate of high-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off.
15	PHASE1	Switch Node for Channel 1. Connect this pin to the source of high-side MOSFET and the drain of the low-side MOSFET. This pin is used as sink for UGATE1 driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off.
16	LGATE1	Low-side Gate Driver Output for Channel 1. Connect this pin to the gate of low-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the low-side MOSFET has turned off.
17	PVCC	Supply Voltage for Gate Driver. This pin is the output of internal 9V LDO. It provides current for gate drives. Bypass this pin with a minimum 1μF ceramic capacitor. If VCC below 7V, connect this pin to VCC is recommended.
18	VCC	Supply Voltage. This pin provides current for internal control circuit and 9V LDO. Bypass this pin with a minimum 1μF ceramic capacitor next to the IC.
19	LGATE2	Low-side Gate Driver Output for Channel 2. Connect this pin to the gate of low-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the low-side MOSFET has turned off.
20	PHASE2	Switch Node for Channel 2. Connect this pin to the source of high-side MOSFET and the drain of the low-side MOSFET. This pin is used as sink for UGATE2 driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off.
21	UGATE2	Upper Gate Driver Output for channel 2. Connect this pin to the gate of high-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off.

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Pin Description(Cont.)

PIN	NAME	FUNCTION
22	BOOT2	Bootstrap Supply for the floating high-side gate driver of channel 2. Connect the Bootstrap capacitor between the BOOT2 pin and the PHASE2 pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the high-side MOSFET. Typical values for CBOOT range from 0.1µF to 1µF.Ensure that CBOOT is placed near the IC.
23	VID	VID Input. This pin is used to adjust reference voltage. Logic high turns on the internal MOSFET connected to RSET pin.
24	RSET	Reference Voltage Setting. This pin is an open drain output that is pulled low when VID = high. Connect a resistor from this pin to REFIN pin to set the reference voltage.
Exposed Pad	GND	Power Ground. Tie this pad to the ground island/plane through the lowest impedance connection available.

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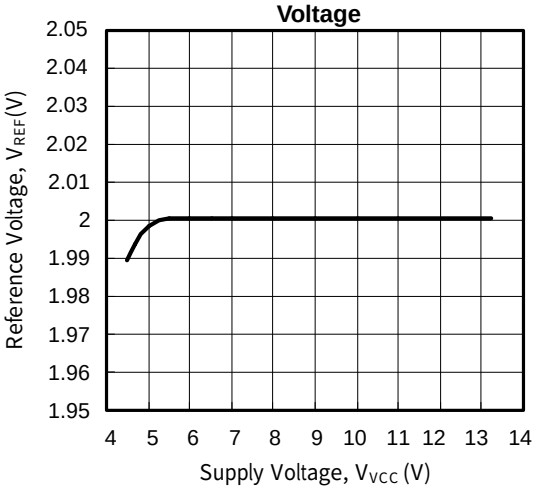
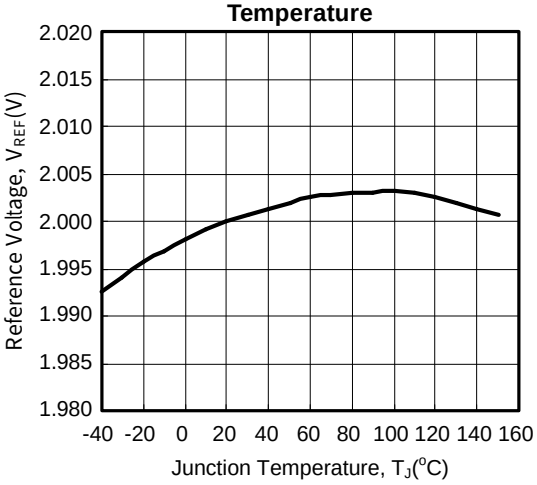
Typical Operating Characteristics

Refer to the "Typical Application Circuits", V_{IN}=12V, V_{OUT}=1.05V, T_A=25°C unless otherwise specified

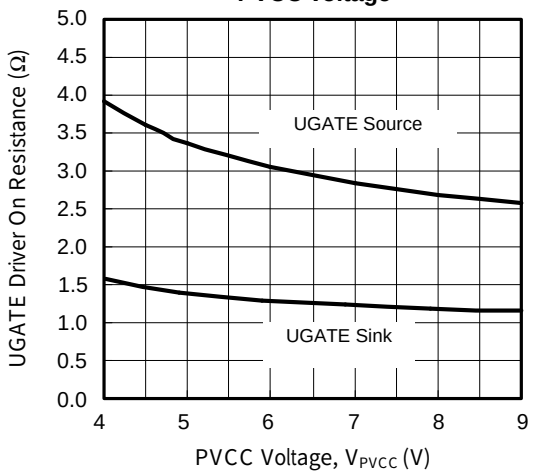
Reference Voltage vs. Supply Voltage



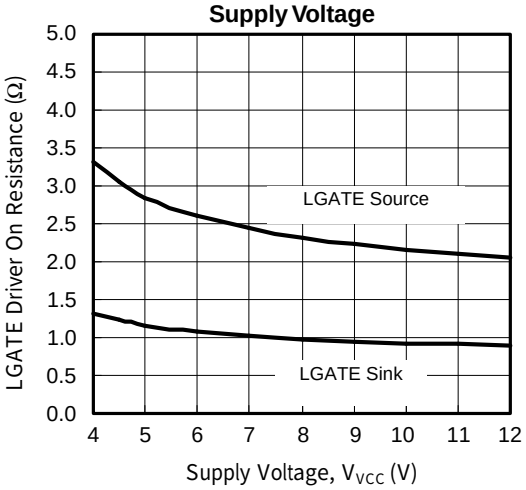
Reference Voltage vs. Junction Temperature



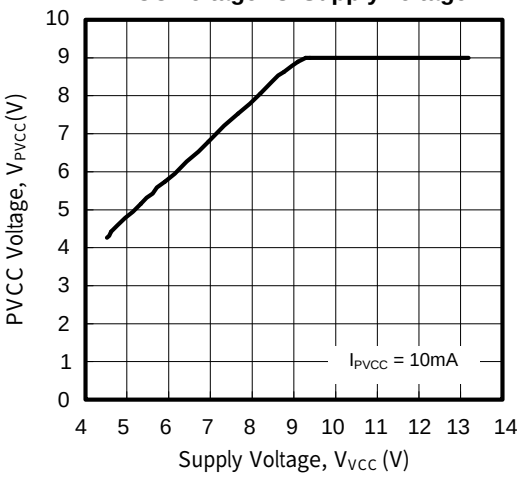
UGATE Driver On Resistance vs. PVCC Voltage



LGATE Driver On Resistance vs. Supply Voltage



PVCC Voltage vs. Supply Voltage



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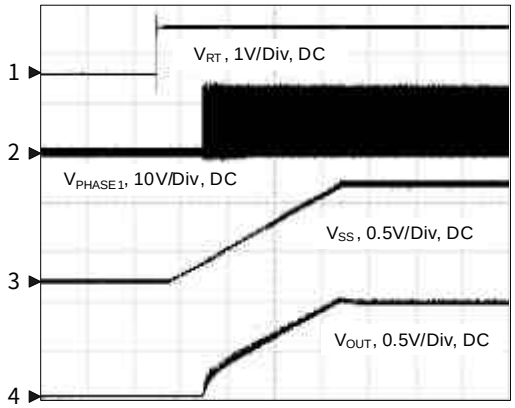
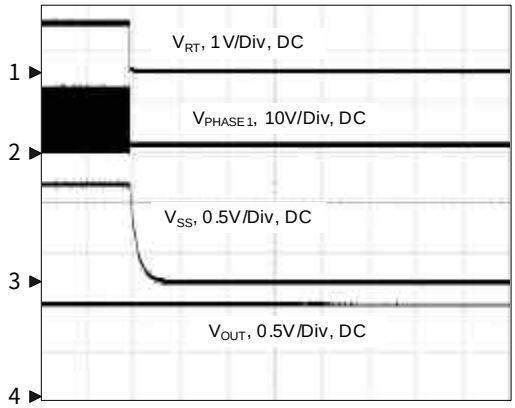
Operating Waveforms

Enable



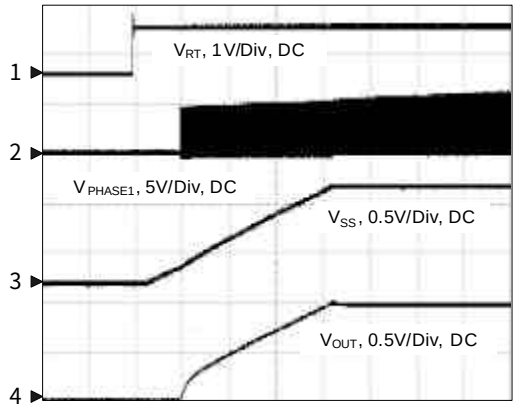
Time: 500µs/Div

Shutdown



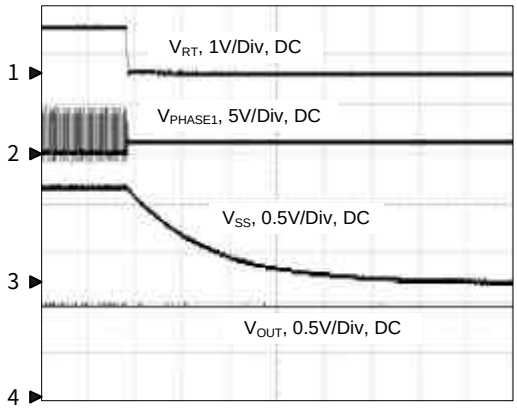
Time: 500µs/Div

Power ON



Time: 500µs/Div

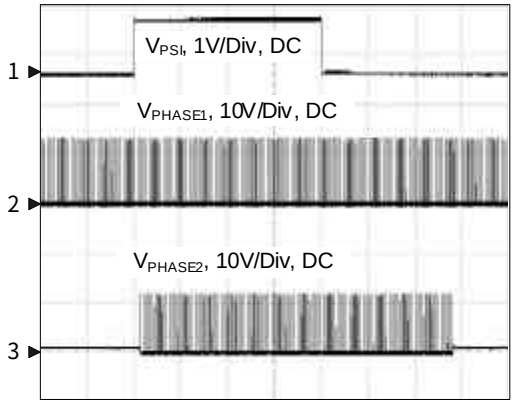
Power OFF



Time: 50µs/Div

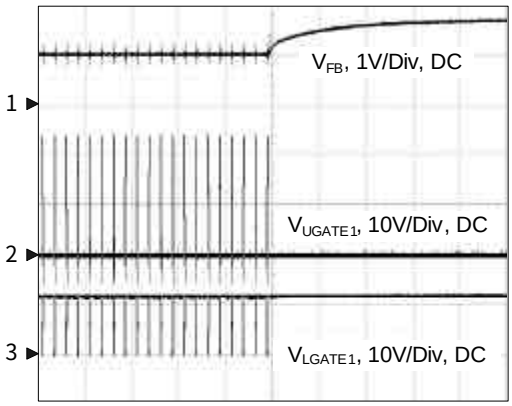
Operating Waveforms

PSI



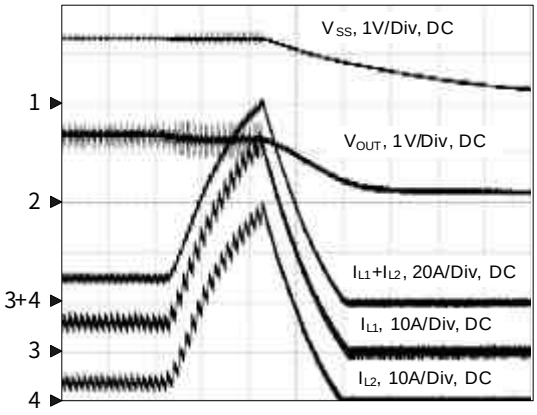
Time: 50µs/Div

OVP



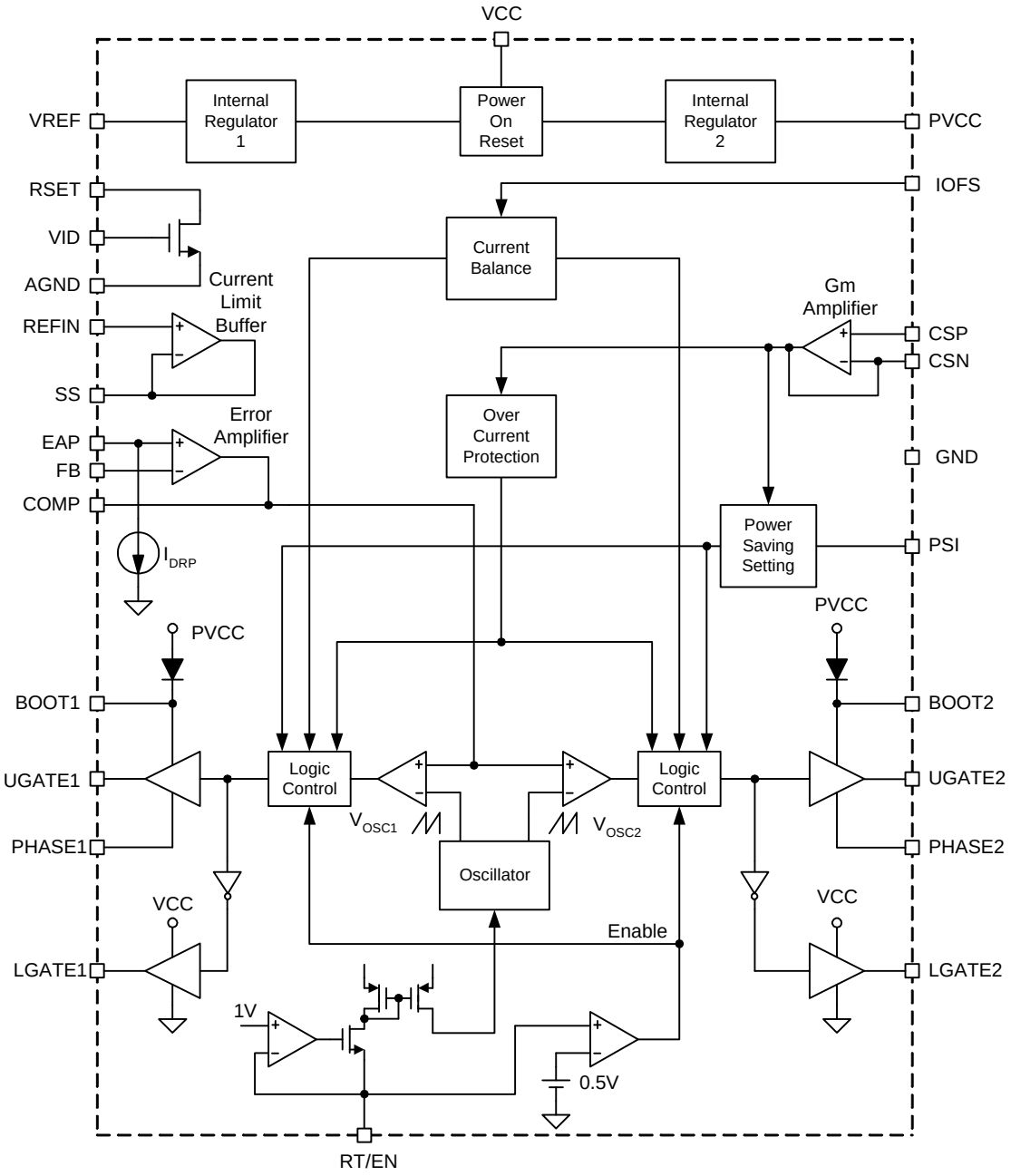
Time: 10µs/Div

OCP

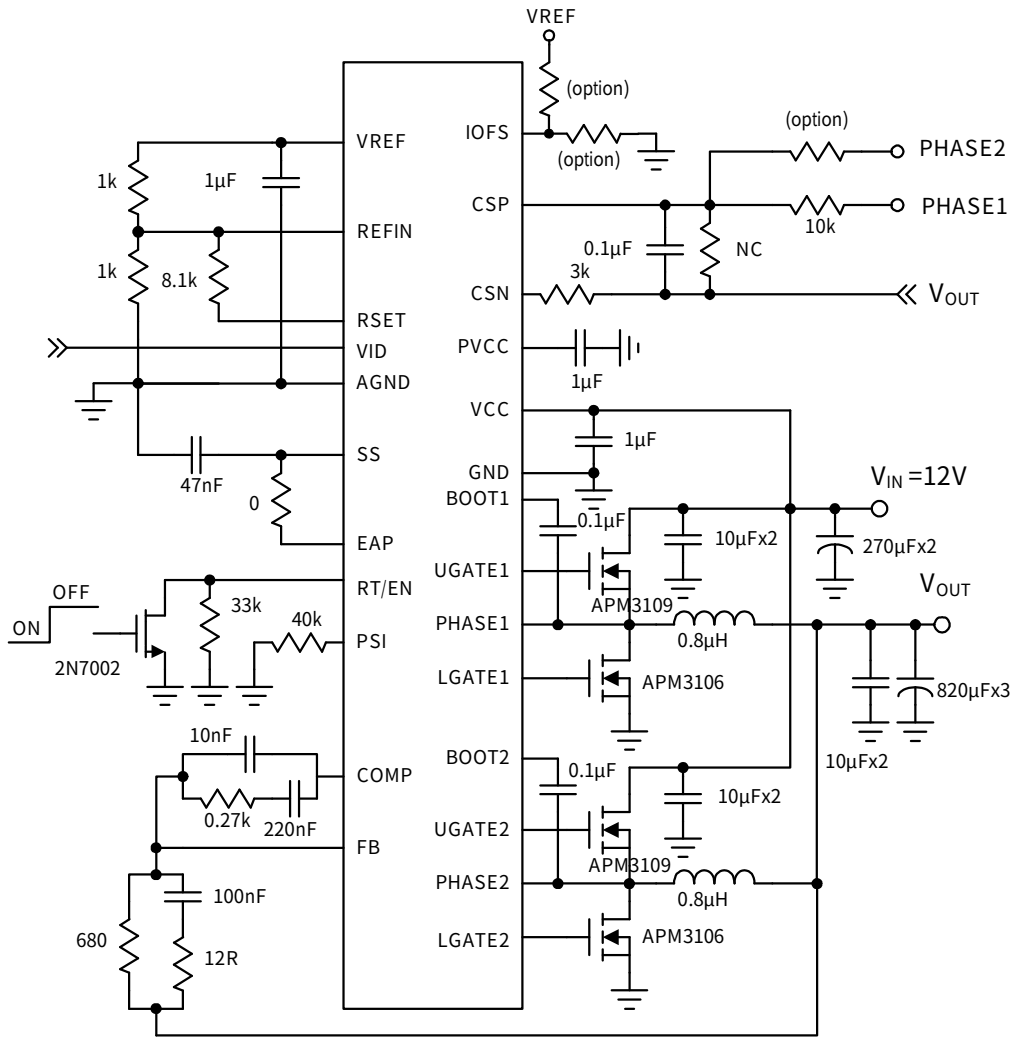


Time: 20µs/Div

Block Diagram



Typical Application Circuit



Function Description

VCC Power-On-Reset (POR)

The Power-On-Reset (POR) circuit compares the input voltage at VCC with the POR threshold (4.1V rising, typical) to ensure the input voltage is high enough for reliable operation. The 0.5V (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the POR rising threshold, startup begins. When the input voltage falls below the POR falling threshold, the controller turns off the converter.

VREF

This is the output pin of high precision 2V reference voltage. Bypass this pin with a 1µF ceramic capacitor to AGND. The VREF have capability to drive 20mA output current.

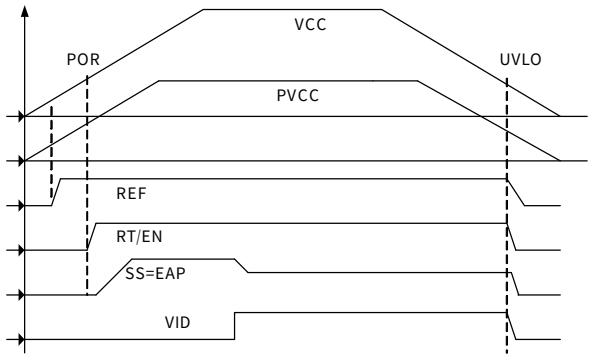


Figure 1. Power on/off sequence

Soft-start

After the VCC voltage exceeds the POR voltage threshold and the RT/EN voltage exceeds 0.5V, the device initials a start-up process and then ramps up the output voltage to the setting of output voltage. A 20µA current source starts to charge the capacitor (C_{SS}) connected with SS and AGND pins. Connect error amplifier non-inverting input, EAP, to SS. The V_{FB} starts to rise with the same rate as the soft-start voltage. Once the SS voltage reaches 80% of VREFIN, the soft-start process is completed after 3ms. After the soft-start process is completed, the SS could source/sink 200µA.

$$\frac{dV_{SS}}{dt} = \frac{I_{SS}}{C_{SS}} = \frac{20\mu A}{C_{SS}} \qquad \text{During soft-start}$$

$$\frac{dV_{SS}}{dt} = \frac{I_{SS}}{C_{SS}} = \frac{200\mu A}{C_{SS}} \qquad \text{After soft-start}$$

Figure 2 shows the simplified voltage control loop of APW8700. VREF is a reference voltage output with 1% accuracy and up to 20mA sourcing capability. RSET is an open drain output that is controlled by VID pin. RSET is pulled to FBRTN when VID = 1 and is set high impedance when VID = 0.

$$V_{SS} = V_{REF} \times \frac{R2}{R1+R2} \qquad \text{VID=0}$$

$$V_{SS} = V_{REF} \times \frac{R2//R3}{R1+(R2//R3)} \qquad \text{VID=1}$$

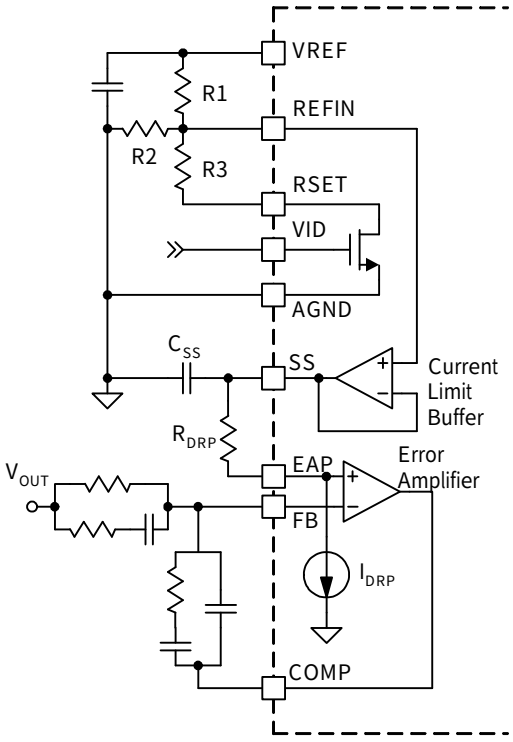


Figure 2. Simplified voltage control loop

Function Description (Cont.)

Shutdown Control and Frequency Setting

RT/EN is a multi function pin. Pull RT/EN below 0.5V to shuts down the device. Connecting a resistor between this pin and GND to set the operation frequency. The operation frequency range could be set from 100kHz to 800kHz. In shutdown mode, the UGATEx and LGATEx are pulled to PHASEx and GND respectively. When the pull-down device is released, the APW8700 initiate a soft-start process.

The switching frequency, F_{OSC}, could be calculated as:

$$F_{OSC} = \frac{10000}{R_{RT}(k\Omega)}(kHz)$$

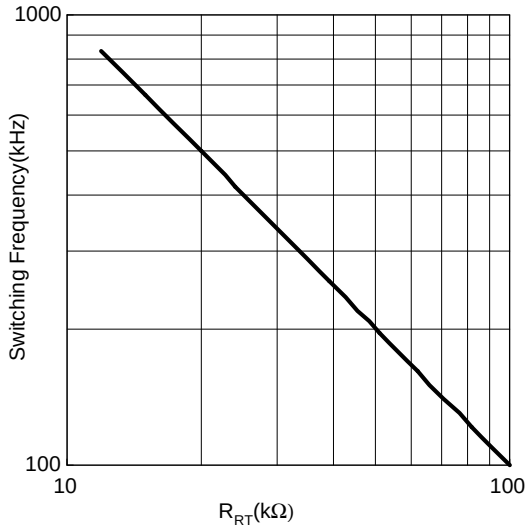


Figure 3. Switching Frequency vs. RT resistance

Current Balancer

The APW8700 adopts parasitic on-resistance of the lower switches current balance as show in figure 4. When the lower switches turn on, the GM amplifier senses the voltage drop across the lower switches and converts it into current signal each time it turns on. The sampled and held current is expressed as:

$$I_{SENx} = \frac{IL_X \cdot R_{DS(ON)}}{R_X} + \frac{V_{OFFSET}}{R_X}$$

The differential current of the current balance control circuit (I_{SEN1}-I_{SEN2}) is used to fine-tune the COMP1/2 voltage. The V_{COMP1} and V_{COMP2} will increase or decrease because of these two currents. For example, when I_{SEN1}>I_{SEN2}, the V_{COMP1} will decrease and the V_{COMP2} will increase. Therefore, the duty of PWM1 will decrease and the duty of PWM2 will increase. Then, the device will reduce I_{L1} current and increase I_{L2} current for current sharing, vice verse.

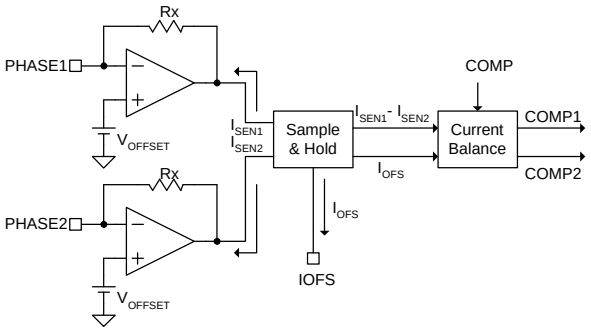


Figure 4. Current balance scheme

Current Sense

Below shows the circuit of sensing inductor current. Connecting a series resistor (R_S) and a capacitor (C_S) network in parallel with the inductor and measuring the voltage (V_C) across the capacitor can sense the inductor current.

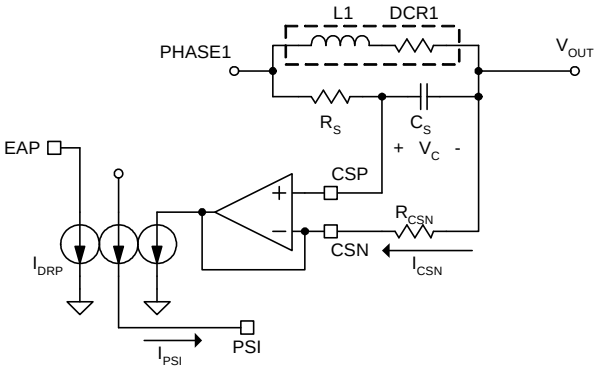


Figure 5. DCR current sense scheme

Function Description (Cont.)

The equations of the sensing network are:

$$V_{L1}(s) = I_{L1}(s) \times (sL1 + DCR1)$$

$$V_C(s) = V_{L1}(s) \times \frac{1}{1 + sR_SC_S} = \frac{I_{L1}(s) \times (sL1 + DCR1)}{1 + sR_SC_S}$$

Take

$$R_SC_S = \frac{L1}{DCR1}$$

If the above is true, the voltage across the capacitor C_S equal to voltage drop across the inductor DCR1, and the voltage V_C is proportional to the inductor current I_{L1}.

$$V_C = DCR1 \times I_{L1}$$

$$I_{CSN} = \frac{V_C}{R_{CSN}} = \frac{I_{L1} \times DCR1}{R_{CSN}}$$

where

I_{L1} is the inductor current of phase 1

DCR1 is the inductor resistance of phase 1

Due to the APW8700 implement current balance circuit. At two phase operation, the I_{L1} equal half of output current, I_{OUT}.

$$I_{CSN} = \frac{I_{OUT} \times DCR1}{2 \times R_{CSN}}$$

Over Current Protection (OCP)

The APW8700 feature an over current protection adopt current sensing. When I_{CSN} exceed 60μA at operation, the over current occurs. In over-current protection, the IC shuts off the converter. The I_{CSN} can be describe as:

$$I_{CSN} = \frac{V_C}{R_{CSN}} = \frac{I_{OUT} \times DCR1}{2 \times R_{CSN}}$$

The APW8700 initial a soft-start process until recycle POR or EN/RT.

Automatic Phase Reduction

The APW8700 implements automatic phase reduction that turns off phase 2 at light load condition and reduces both switching and conduction losses. The automatic phase reduction maintains high power conversion efficiency over the output current range. The output current is sensed and mirrored to PSI pin as:

$$I_{PSI} = I_{CSN} = \frac{I_{OUT} \times DCR1}{2 \times R_{CSN}}$$

The I_{PSI} creates a voltage V_{PSI} as:

$$V_{PSI} = R_{PSI} \times I_{PSI} = \frac{I_{OUT} \times DCR1 \times R_{PSI}}{2 \times R_{CSN}}$$

The APW8700 operates at dual phase if V_{PSI} exceeds 0.6V and at single phase at V_{PSI} below 0.4V. There is a 200mV hystersis at the phase change threshold. There is a 0.2ms delay when entering single phase operation and no time delay when entering dual phase operation. When operating single phase, both UGATE2 and LGATE2 are turned off.

Droop Setting

In some high current applications, a requirement on precisely controlled output impedance is imposed. This dependence of output voltage on load current is often termed droop regulation. As shown in figure 4, the droop control block generates a voltage through external resistor R_{DRP} and then set the droop voltage. The droop voltage, V_{DRP}, is proportional to the total current in two channels. As shown in the following equation:

$$V_{FB} = V_{SS} - I_{DRP} \times R_{DRP}$$

where

I_{DRP} is the droop current that mirrored from I_{CSN}.

The output voltage also can be describe as:

$$V_{FB} = V_{SS} - I_{DRP} \times R_{DRP} = V_{SS} - \frac{I_{OUT} \times DCR1 \times R_{DRP}}{2 \times R_{CSN}}$$

Function Description (Cont.)

Offset Current Adjust

The APW8700 integrated IOFS allows the offset current to adjust phase current. The IOFS pin voltage is nominal 0.5V when connecting a resistor to GND and 1.5V when connecting a resistor to VREF. Connecting a resistor from IOFS pin to GND generate a current source as:

I_{OFS}= 0.5V/R_{IOFS}

This current is add to phase 1 current signal I_{SEN1} for current balance. Consequently, phase 2 will share more percentage of output current. Connecting a resistor from IOFS pin to VREF generates a current source as:

I_{OFS}= (2V-1.5V) /R_{IOFS}

This current is add to phase 2 current signal I_{SEN2} for current balance. Consequently, phase 1 will share more percentage of output current.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW8700. When the junction temperature exceeds 150°C, a thermal sensor pulls UGTAEx and LGATEx low, allowing the devices to cool. The thermal sensor allows the converters to start a soft-start process and regulates the output voltage again after the junction temperature cools by 20°C. The OTP is designed with a 20°C hysteresis to lower the average Junction Temperature (T_J) during continuous thermal overload conditions increasing the lifetime of the device.

OVP

The over-voltage protection (OVP) circuit monitors the FB (V_{FB}) voltage to prevent the output from over-voltage. When the V_{FB} rises to 130% of the EAP voltage (V_{EAP}), the APW8700 turns off high-side and turn on low-side MOSFETs to sink output voltage (V_{OUT}). As soon as the V_{FB} falls below 110% of V_{EAP}, the OVP comparator is disengaged. The chip will restore its normal operation.

UVP

The under-voltage protection circuit monitors the voltage on FB (V_{FB}) by Under-Voltage (UV) comparator to protect the PWM converter against short-circuit conditions. When the V_{FB} falls below the falling UVP threshold (50% V_{EAP}), a fault signal is generated and the device turns off high-side and low-side MOSFETs. The converter shuts down and the output is latched to be floating. The APW8700 will initials a soft-start process until re-cycle RT/EN or VCC

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Application Information

PWM Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with -40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network among COMP, FB, and V_{OUT} should be added. The compensation network is shown in Figure 9. The output LC filters consists of the output inductors and output capacitors. For two-phase convertor, when assuming $V_{IN1}=V_{IN2}=V_{IN}$, L1=L2=L, the transfer function of the LC filter is given by:

$$GAIN_{LC} = \frac{1+s\times ESR\times C_{OUT}}{s^2\times\frac{1}{2}L\times C_{OUT}+s\times ESR\times C_{OUT}+1}$$

The poles and zero of this transfer functions are:

$$F_{LC} = \frac{1}{2\times\pi\times\sqrt{\frac{1}{2}L\times C_{OUT}}}$$

$$F_{ESR} = \frac{1}{2\times\pi\times ESR\times C_{OUT}}$$

The F_{LC} is the double-pole frequency of the two-phase LC filters, and F_{ESR} is the frequency of the zero introduced by the ESR of the output capacitors.

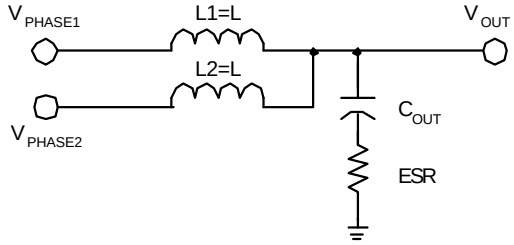

Figure 6. The Output LC Filter

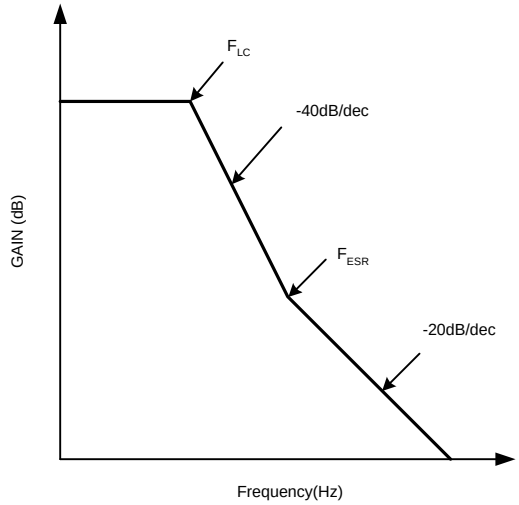

Figure 7. Frequency Resopnse of the LC filters

The PWM modulator is shown in figure 8. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by :

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

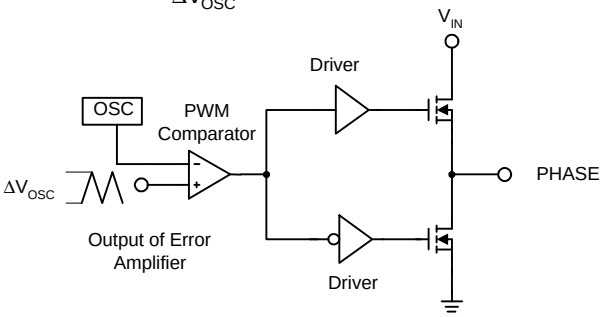

Figure 8. The PWM Modulator

The compensation network is shown in figure 9. It provides a close loop transfer function with the highest zero crossover frequency and sufficient phase margin.

The transfer function of error amplifier is given by :

$$GAIN_{AMP} = \frac{V_{COMP}}{V_{OUT}} = \frac{\frac{1}{sC1}//\left(R2+\frac{1}{sC2}\right)}{R1//\left(R3+\frac{1}{sC3}\right)}$$

$$= \frac{R1+R3}{R1\times R3\times C1}\times\frac{\left(s+\frac{1}{R2\times C2}\right)\times\left(s+\frac{1}{(R1+R3)\times C3}\right)}{s\left(s+\frac{C1+C2}{R2\times C1\times C2}\right)\times\left(s+\frac{1}{R3\times C3}\right)}$$

The pole and zero frequencies of the transfer function are:

$$F_{Z1} = \frac{1}{2\times\pi\times R2\times C2}$$

$$F_{Z2} = \frac{1}{2\times\pi\times(R1+R3)\times C3}$$

$$F_{P1} = \frac{1}{2\times\pi\times R2\times\left(\frac{C1\times C2}{C1+C2}\right)}$$

$$F_{P2} = \frac{1}{2\times\pi\times R3\times C3}$$

Application Information (Cont.)

PWM Compensation (Cont.)

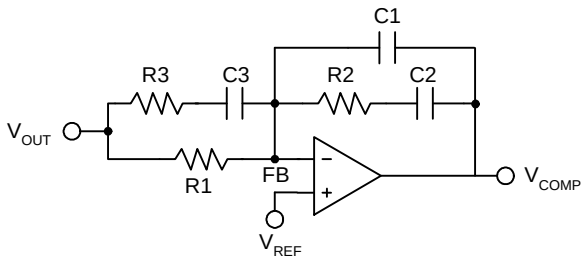

Figure 9. Compensation Network

The closed loop gain of the converter can be written as:

$$GAIN_{LC} X\, GAIN_{PWM} X\, GAIN_{AMP}$$

Figure 10. shows the asymptotic plot of the closed loop converter gain, and the following guidelines will help to design the compensation network. Using the below guidelines should give a compensation similar to the curve plotted. A stable closed loop has a -20dB/ decade slope and a phase margin greater than 45 degree.

1. Choose a value for R1, usually between 1K and 5K.

2. Select the desired zero crossover frequency

F_O= (1/5 ~ 1/10) X F_{SW}

Use the following equation to calculate R2:

$$R2 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{F_O}{F_{LC}} \times R1$$

3. Place the first zero F_{Z1} before the output LC filter double pole frequency F_{LC}.

F_{Z1} = 0.75 X F_{LC}

Calculate the C2 by the equation:

$$C2 = \frac{1}{2 \times \pi \times R2 \times F_{LC} \times 0.75}$$

4. Set the pole at the ESR zero frequency F_{ESR}:

F_{P1} = F_{ESR}

Calculate the C1 by the following equation:

$$C1 = \frac{C2}{2 \times \pi \times R2 \times C2 \times F_{ESR} - 1}$$

5. Set the second pole F_{P2} at the half of the switching frequency and also set the second zero F_{Z2} at the output LC filter double pole F_{LC}. The compensation gain should not exceed the error amplifier open loop gain, check the compensation gain at F_{P2} with the capabilities of the error amplifier.

F_{P2} = 0.5 X F_{SW}

F_{Z2} = F_{LC}

Combine the two equations will get the following component calculations:

$$R3 = \frac{R1}{\frac{F_{SW}}{2 \times F_{LC}} - 1}$$

$$C3 = \frac{1}{\pi \times R3 \times F_{SW}}$$

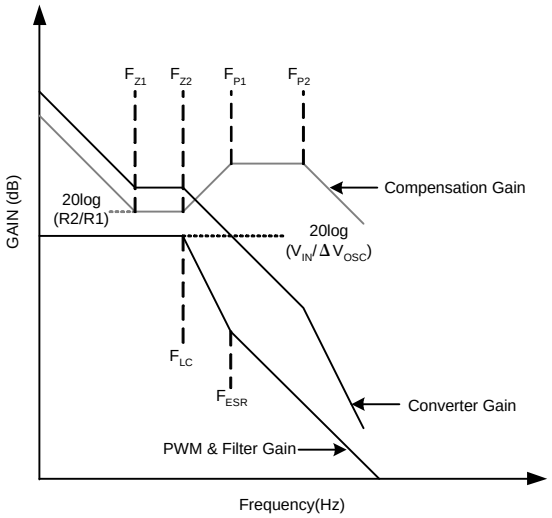

Figure 10. Converter Gain and Frequency

Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

Application Information (Cont.)

Output Inductor Selection (Cont.)

$$D = \frac{V_{OUT}}{V_{IN}}$$

For two-phase converter, the inductor value (L) determines the sum of the two inductor ripple currents, ΔI_{P-P}, and affects the load transient reponse. Higher inductor value reduces the output capacitors' ripple current and induces lower output ripple voltage. The ripple current can be approxminated by:

$$\Delta I_{P-P} = \frac{V_{IN} - 2V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator. Although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting output capacitors. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop ΔV_{COUT} and ESR voltage drop ΔV_{ESR} caused by the AC peak-to-peak sum of the inductor's current. The ripple voltage of output capacitors can be represented by:

$$\Delta V_{COUT} = \frac{\Delta I_{P-P}}{8 \times C_{OUT} \times F_{SW}}$$

$$\Delta V_{ESR} = \Delta I_{P-P} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered.

To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change. For getting same load transient response, the output capacitance of two-phase converter only needs around half of output capacitance of single-phase converter.

Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from overheating.

Input Capacitor Selection

Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the surge current needed each time high-side MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of high-side MOSFET and the source of low-side MOSFET.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. For two-phase converter, the

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Application Information (Cont.)

Input Capacitor Selection (Cont.)

RMS current of the bulk input capacitor is roughly calculated as the following equation :

$$I_{RMS} = \frac{I_{OUT}}{2} \times \sqrt{2D \cdot (1-2D)}$$

For a through hole design, several electrolytic capacitors may be needed. For surface mount design, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating.

MOSFET Selection

The APW8700 requires two N-Channel power MOSFETs on each phase. These should be selected based upon $R_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection, and heatsink are the dominant design factors. The power dissipation includes two loss components, conduction loss, and switching loss. The conduction losses are the largest component of power dissipation for both the high-side and the low-side MOSFETs. These losses are distributed between the two MOSFETs according to duty factor (see the equations below). Only the high-side MOSFET has switching losses since the low-side MOSFETs body diode or an external Schottky rectifier across the lower MOSFET clamps the switching node before the synchronous rectifier turns on. These equations assume linear voltage-current transitions and do not adequately model power loss due the reverse-recovery of the low-side MOSFET body diode. The gate-charge losses are dissipated by the APW8700 and don't heat the MOSFETs. However, large gate-charge increases the switching interval, t_{SW} which increases the high-side MOSFET switching losses. Ensure that all MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

For the high-side and low-side MOSFETs, the losses are approximately given by the following equations:

$$P_{high\text{-}side} = I_{OUT}^{2}(1+TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_{SW}$$

$$P_{low\text{-}side} = I_{OUT}^{2}(1+TC)(R_{DS(ON)})(1-D)$$

where

I_{OUT} is the load current
TC is the temperature dependency of $R_{DS(ON)}$
F_{SW} is the switching frequency
t_{SW} is the switching interval
D is the duty cycle

Note that both MOSFETs have conduction losses while the high-side MOSFET includes an additional transition loss. The switching interval, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The (1+TC) term is a factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs. Temperature" curve of the power MOSFET.

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the low side MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. Besides, signal and power grounds are to be kept separating and finally combined using ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Figure 11. illustrates the layout, with bold lines indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed lose together. Below is a checklist for your layout:

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Application Information (Cont.)

Layout Consideration (Cont.)

- Keep the switching nodes (UGATEx, LGATEx, BOOTx, and PHASEx) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.
- The signals going through theses traces have both high dv/dt and high di/dt with high peak charging and discharging current. The traces from the gate drivers to the MOSFETs (UGATEx and LGATEx) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node. In addition, the large layout plane between the drain of the MOSFETs (V_{IN} and PHASEx nodes) can get better heat sinking.
- For experiment result of accurate current sensing, the current sensing components are suggested to place close to the inductor part. To avoid the noise interference, the current sensing trace should be away from the noisy switching nodes.
- Decoupling capacitors, the resistor-divider, and boot capacitor should be close to their pins. (For example, place the decoupling ceramic capacitor close to the drain of the high-side MOSFET as close as possible).
- The input bulk capacitors should be close to the drain of the high-side MOSFET, and the output bulk capacitors should be close to the loads. The input capacitor's ground should be close to the grounds of the output capacitors and low-side MOSFET.
- Locate the resistor-divider close to the FB pin to minimize the high impedance trace. In addition, FB pin traces can't be close to the switching signal traces (UGATEx, LGATEx, BOOTx, and PHASEx).

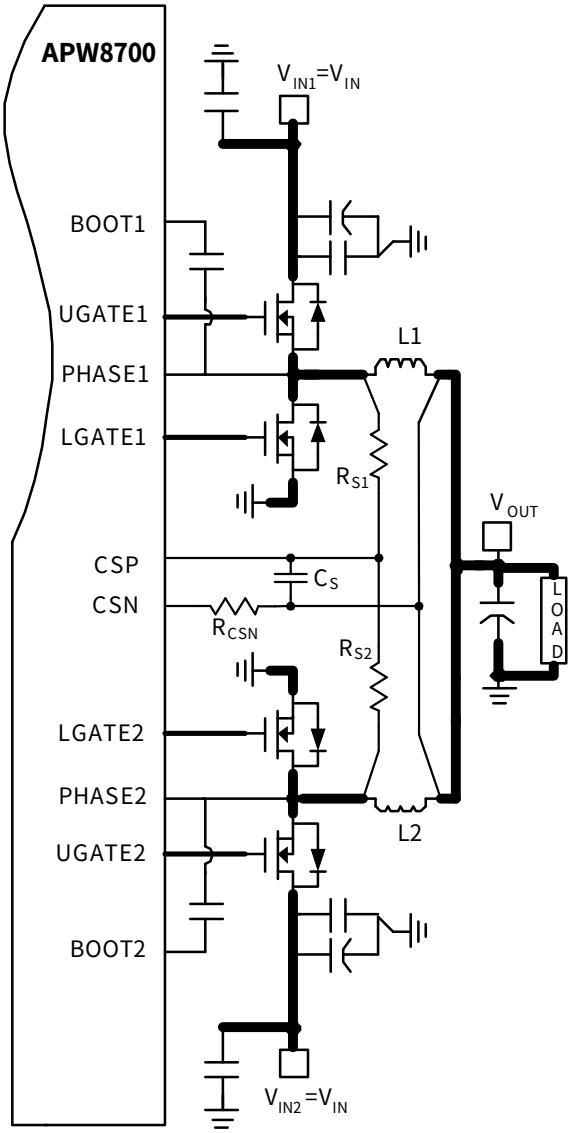
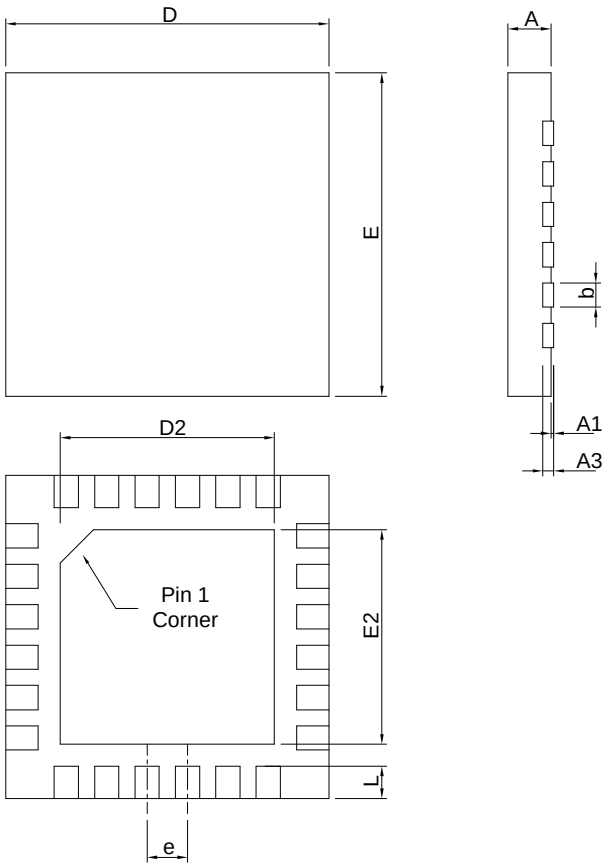


Figure 11. Layout Guidelines

Package Information

QFN4x4-24



SYMBOL	QFN4x4-24			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.008	0.012
D	4.00 BSC		0.157 BSC	
D2	2.50	2.80	0.098	0.110
E	4.00 BSC		0.157 BSC	
E2	2.50	2.80	0.098	0.110
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018

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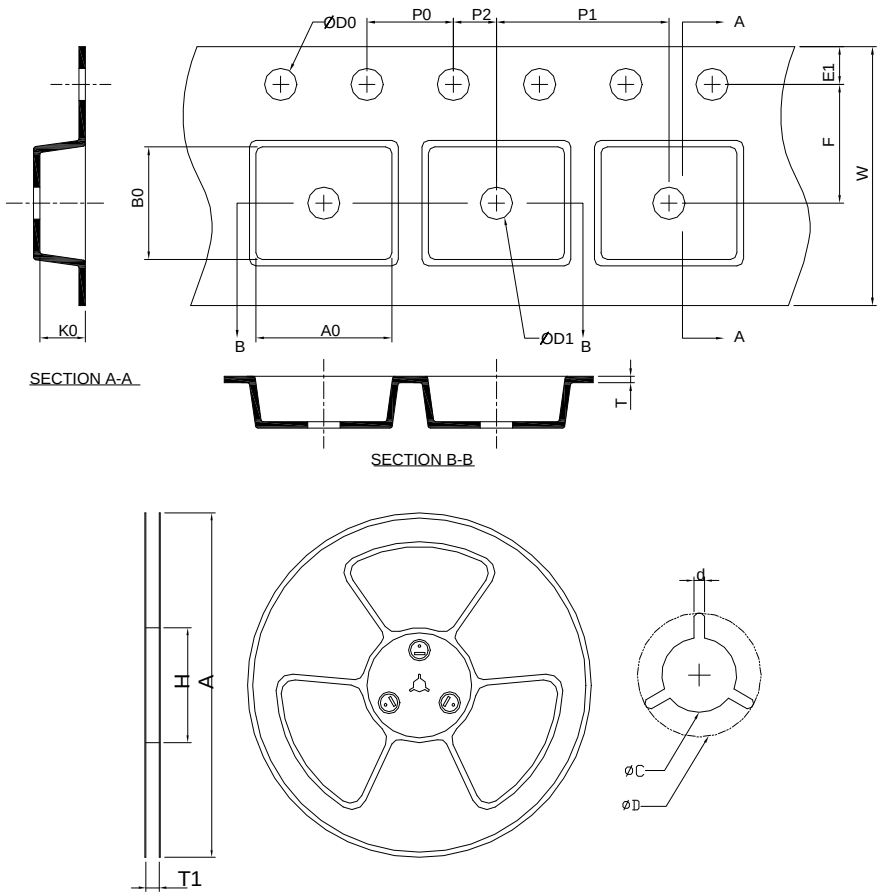
Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
QFN4x4-24	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.30±0.20

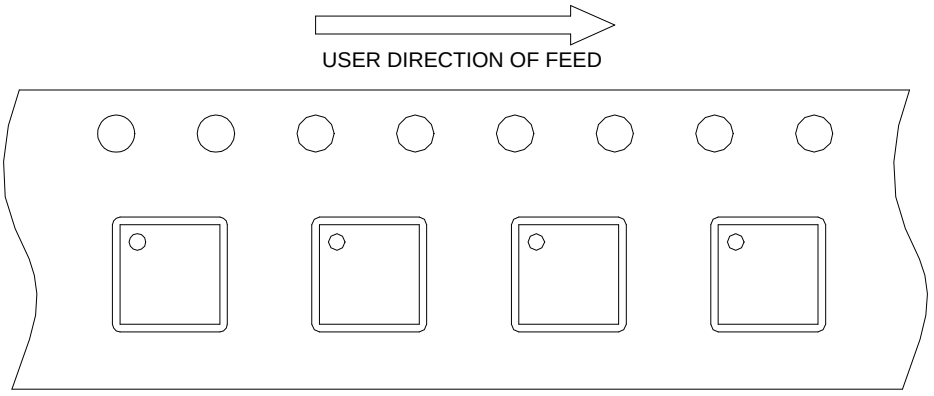
(mm)

Devices Per Unit

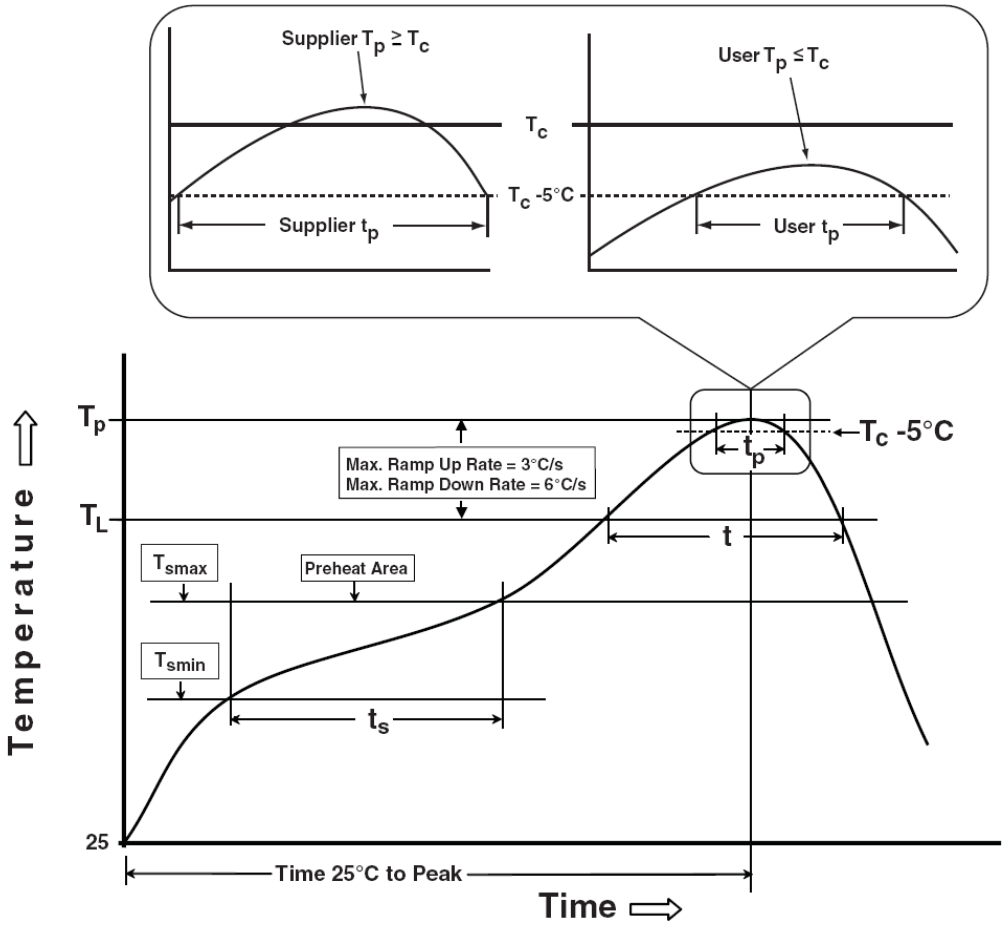
Package Type	Unit	Quantity
QFN4x4-24	Tape & Reel	3000

Taping Direction Information

QFN4x4-24



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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