

5V/3.3V 64K×16 CMOS SRAM

Features

- AS7C1026 (5V version)
- AS7C31026 (3.3V version)
- Industrial and commercial versions
- Organization: 65,536 words x 16 bits
- Center power and ground pins for low noise
- High speed

Logic block diagram

- 12/15/20 ns address access time
- 6,7,8 ns output enable access time
- Low power consumption: ACTIVE
- 880 mW (AS7C1026) / max @ 12 ns
- 396 mW (AS7C31026) / max @ 12 ns

- Low power consumption: STANDBY
 28 mW (AS7C1026) / max CMOS I/O
 - 18 mW (AS7C31026) / max CMOS I/O
- 2.0V data retention
- Easy memory expansion with \overline{CE} , \overline{OE} inputs
- TTL-compatible, three-state I/O
- JEDEC standard packaging
 - 44-pin 400 mil SOJ
 - 44-pin 400 mil TSOP II
 - 48-ball 6 mm \times 8 mm CSP mBGA
- ESD protection \geq 2000 volts
- Latch-up current $\geq 200 \text{ mA}$

A0 V_{CC} A1 Row decoder A2 $64K \times 16$ GND A3 Array A4 A5 A6 A7 I/O0–I/O7 I/O buffer Control circuit I/O8–I/O15 Column decoder WE A9 A10 A11 A12 A12 A13 A14 A15 UB OE LB CE

44-Pin SOJ	i, TSOP	II (400 mil)
A4 1 A3 2 A2 3 A1 4 A0 5 CE 6 I/00 7 I/01 8 I/02 9 I/03 14 Vccc 1 I/04 1 I/05 14 I/06 1 I/07 14 A15 14 A13 22 NC 2	1 0 6 8 2 9 2 4 5 2 1 0 2 6 4 2 0 2 6 4 2 0 2 6 4 2 7 2 0 2 6 4 2 7 2 1 0 2 6 4 2 7 2 3 1 0 2 6 4 2 7 2 3 1 0 2 6 4 2 7 2 3 1 0 2 6 4 2 7 2 3 1 0 2 6 4 2 7 2 3 1 0 2 6 4 2 7 2 3 1 0 2 6 4 2 7 2 3 1 0 2 6 4 2 7 2 7 3 1 0 2 6 4 2 7 2 7 3 1 0 2 6 4 2 7 2 7 3 1 0 2 6 4 2 7 2 7 3 1 0 2 6 4 2 7 7 3 1 0 2 6 4 2 7 7 3 1 0 2 6 4 2 7 7 3 1 0 2 6 4 2 7 7 3 1 0 2 6 4 2 7 7 3 1 0 2 6 4 2 7 7 3 1 0 2 6 4 2 7 7 3 1 0 2 6 4 2 7 7 3 1 0 2 6 4 2 7 7 3 1 0 2 6 4 2 7 7 3 1 0 2 6 4 2 7 7 3 1 0 2 6 4 2 7 7 3 1 0 2 6 4 2 7 7 3 1 0 2 6 4 2 7 7 3 1 0 2 6 4 2 7 7 3 1 0 2 7 7 3 1 0 2 7 7 3 1 0 2 7 7 3 1 0 2 7 7 3 1 0 2 7 7 3 1 0 2 7 7 3 1 0 2 7 7 3 1 0 2 7 7 3 1 0 2 7 7 3 1 0 2 7 7 3 1 0 2 7 7 3 1 0 2 7 7 3 1 0 2 7 7 3 1 0 2 7 7 3 1 0 2 7 7 3 1 0 2 7 7 3 1 0 2 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	44 A5 43 A6 42 A7 41 OE 40 UB 39 IB 38 I/O15 37 I/O14 36 I/O12 34 GND 33 V _{CC} 32 I/O11 31 I/O101 30 I/O9 29 I/O8 28 NC 27 A8 26 A9 25 A10 24 A11 23 NC

Pin arrangement

48-CSP mini Ball-Grid-Array Package

					0	
	1	2	3	4	5	6
А	LB	OE	A ₀	A ₁	A ₂	NC
В	I/08	UB	A3	A4	CE	I/O0
С	I/09	I/O10	A5	A6	I/O1	I/O2
D	V _{SS}	I/O11	NC	A7	I/O3	V _{DD}
Е	V _{DD}	I/O12	NC	NC	I/O4	V _{SS}
F	I/O14	I/O13	A14	A15	I/O5	I/O6
G	I/O15	NC	A12	A13	WE	I/07
Η	NC	A8	A9	A10	A11	NC
Η	NC	A8	A9	A10	A11	NC

Selection guide

8					
		AS7C1026-12 AS7C31026-12	AS7C1026-15 AS7C31026-15	AS7C1026-20 AS7C31026-20	Unit
Maximum address access time		12	15	20	ns
Maximum output enable access time		6	8	10	ns
Manianana ana sina ana sina a	AS7C1026	160	150	140	mA
Maximum operating current	AS7C31026	110	100	90	mA
Mayimum CMOS standby sument	AS7C1026	10	10	15	mA
Maximum CMOS standby current	AS7C31026	10	10	15	mA

Shaded areas indicate preliminary information.

Functional description

The AS7C1026 and AS7C31026 are high-performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) devices organized as 65,536 words x 16 bits. They are designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA} , t_{RC} , t_{WC}) of 12/15/20 ns with output enable access times (t_{OE}) of 6,7,8 ns are ideal for high-performance applications.

When $\overline{\text{CE}}$ is high the devices enter stanby mode. The AS7C1026 is guaranteed not to exceed 28 mW power consumption in CMOS standby mode. The devices also offer 2.0V data retention.

A write cycle is accomplished by asserting write enable (\overline{WE}) and chip enable (\overline{CE}). Data on the input pins I/O0–I/O15 is written on the rising edge of \overline{WE} (write cycle 1) or \overline{CE} (write cycle 2). To avoid bus contention, external devices should drive I/ O pins only after outputs have been disabled with output enable (\overline{OE}) or write enable (\overline{WE}).

A read cycle is accomplished by asserting output enable (\overline{OE}) and chip enable (\overline{CE}), with write enable (\overline{WE}) high. the chips drive I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

The devices provide multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. \overline{LB} controls the lower bits, I/O0–I/O7, and \overline{UB} controls the higher bits, I/O8–I/O15.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5V supply (AS7C1026) or 3.3V supply (AS7C31026). the device is packaged in common industry standard packages. Chip scale BGA packaging, easy to use in manufacturing, provides the smallest possible footprint. This 48-ball JEDEC-registered package has a ball pitch of 0.75 mm and external dimensions of 8 mm × 6 mm.

Parameter		Symbol	Min	Max	Unit
Veltere en V. relative to CND	AS7C1026	V _{t1}	-0.50	+7.0	V
Voltage on V _{CC} relative to GND	AS7C31026	V _{t1}	-0.50	+5.0	V
Voltage on any pin relative to GND		V _{t2}	-0.50	V _{CC} +0.50	V
Power dissipation		P _D	—	1.0	W
Storage temperature (plastic)		T _{stg}	-65	+150	°C
Ambient temperature with VCC applied		T _{bias}	-55	+125	°C
DC current into outputs (low)		I _{OUT}	_	20	mA

Absolute maximum ratings

Note: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

CE	WE	ŌĒ	LB	UB	I/O0–I/O7	I/O8–I/O15	Mode
Н	Х	Х	Х	Х	High Z	High Z	Standby (I _{SB}), I _{SBI})
L	Н	L	L	Н	D _{OUT}	High Z	Read I/O0–I/O7 (I _{CC})
L	Н	L	Н	L	High Z	D _{OUT}	Read I/O8–I/O15 (I _{CC)}
L	Н	L	L	L	D _{OUT}	D _{OUT}	Read I/O0–I/O15 (I _{CC})
L	L	Х	L	L	D _{IN}	D _{IN}	Write I/O0–I/O15 (I _{CC})
L	L	Х	L	Н	D _{IN}	High Z	Write I/O0–I/O7 (I _{CC})



CE	WE	ŌĒ	LB	UB	I/O0–I/O7	I/O8–I/O15	Mode
L	L	Х	Н	L	High Z	D _{IN}	Write I/O8–I/O15 (I _{CC})
L L	H X	H X	X H	X H	High Z	High Z	Output disable (I _{CC})

Key: H = High, L = Low, X = don't care.

Recommended operating conditions

Parameter		Device	Symbol	Min	Тур	Max	Unit
		AS7C1026	V _{CC}	4.5	5.0	5.5	V
Supply voltage		AS7C31026 (-10)	V _{CC}	3.15	3.3	3.6	V
		AS7C31026 (12/15/20)	V _{CC}	3.0	3.3	3.6	V
	AS7C1026	V _{IH}	2.2	_	$V_{CC} + 0.5$	V	
Input voltage		AS7C31026	V _{IH}	2.0	_	$V_{CC} + 0.5$	V
			V _{IL}	-0.5^{\dagger}	—	0.8	V
	commercial		T _A	0	_	70	°C
Ambient operating temperature	industrial		T _A	-40	-	85	°C

[†] V_{IL} min = -3.0V for pulse width less than $t_{RC}/2$.

DC operating characteristics (over the operating range)^I

				-	12	-	15	-2	.0	
Parameter	Sym	Test conditions	Device	Min	Max	Min	Max	Min	Max	Unit
Input leakage current	I _{LI}	$V_{CC} = Max$ $V_{IN} = GND$ to V_{CC}		-	1	-	1	-	1	μΑ
Output leakage current	I _{LO}	$V_{CC} = Max$ $\overline{CE} = V_{IH},$ $V_{OUT} = GND \text{ to } V_{CC}$		_	1	_	1	_	1	μΑ
Operating power	_	$V_{CC} = Max, \overline{CE} \le V_{IL}$	AS7C1026	—	160	—	150	-	140	mA
supply current	I _{CC}	outputs open, $f = f_{Max} = 1/t_{RC}$	AS7C31026	_	110	_	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	mA		
		$V_{CC} = Max, \overline{CE} \le V_{IL},$	AS7C1026	-	50	-	50	-	50	
Standby	I _{SB}	outputs open, $f = f_{Max} = 1/t_{RC}$	AS7C31026	- 110 - 100 - 90 mA - 50 - 50 - 50	mA					
current		$V_{CC} = Max, \overline{CE} \ge V_{CC} - 0.2V,$	AS7C1026	-	10	-	10	-	15	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	_	15	mA							
Output	V _{OL}	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min}$		-	0.4	-	0.4	—	0.4	V
voltage	V _{OH}	$I_{OH} = -4 \text{ mA}, V_{CC} = Min$		2.4	—	2.4	_	2.4	_	V

Shaded areas indicate preliminary information.

Capacitance (f = 1MHz, $T_a = 25$ °C, $V_{CC} = \text{NOMINAL})^2$

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C _{IN}	A, $\overline{\text{CE}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$	$V_{IN} = 0V$	5	pF
I/O capacitance	C _{I/O}	I/O	$V_{IN} = V_{OUT} = 0V$	7	pF

3/23/01; v.1.0



		-]	2	-]	5	-2	20		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t _{RC}	12	-	15	-	20	-	ns	
Address access time	t _{AA}	_	12	_	15	_	20	ns	3
Chip enable (\overline{CE}) access time	t _{ACE}	_	12	_	15	_	20	ns	3
Output enable (\overline{OE}) access time	t _{OE}	-	6	-	7	-	8	ns	
Output hold from address change	t _{OH}	4	-	4	-	4	-	ns	5
\overline{CE} Low to output in low Z	t _{CLZ}	0	_	0	_	0	-	ns	4,5
\overline{CE} High to output in high Z	t _{CHZ}	_	6	_	6	_	8	ns	4,5
\overline{OE} Low to output in low Z	t _{OLZ}	0	-	0	-	0	-	ns	4,5
Byte select access time	t _{BA}	-	6	-	7	-	8	ns	
Byte select Low to low Z	t _{BLZ}	0	-	0	-	0	-	ns	4,5
Byte select High to high Z	t _{BHZ}	-	6	-	6	-	8	ns	4,5
\overline{OE} High to output in high Z	t _{OHZ}	-	6	-	6	-	8	ns	4,5
Power up time	t _{PU}	0	-	0	-	0	-	ns	4,5
Power down time	t _{PD}	-	12	-	15	—	20	ns	4,5

Read cycle (over the operating range)^{3,9}

Shaded areas indicate preliminary information.

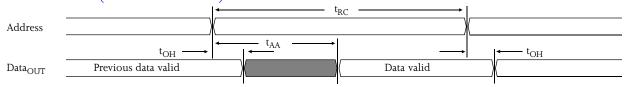
Key to switching waveforms

Rising input

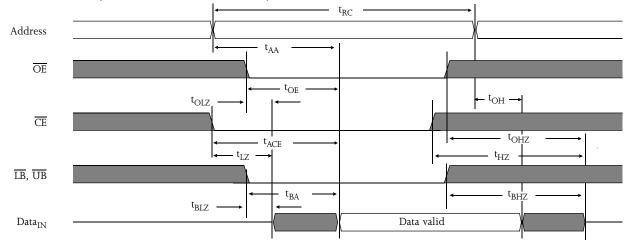
____ Falling input

Undefined output/don't care

Read waveform 1 (address controlled)^{3,6,7,9}



Read waveform 2 (OE, CE, UB, LB controlled)^{3,6,8,9}



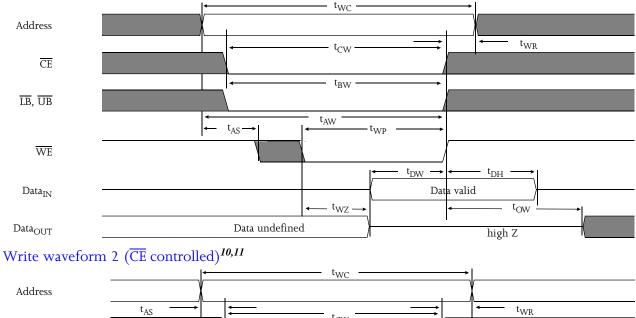


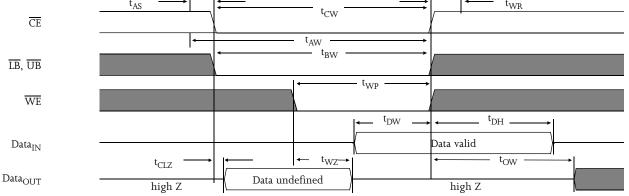
Write cycle (over the operating range) ¹¹

		- 1	-12		5	-20			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t _{WC}	12	—	15	—	20	—	ns	
Chip enable (\overline{CE}) to write end	t _{CW}	8	-	12	_	13	_	ns	
Address setup to write end	t _{AW}	9	_	10	—	12	-	ns	
Address setup time	t _{AS}	0	_	0	—	0	-	ns	
Write pulse width	t _{WP}	8	_	10	—	12	-	ns	
Address hold from end of write	t _{AH}	0	_	0	—	0	-	ns	
Data valid to write end	t _{DW}	6	_	8	—	10	-	ns	
Data hold time	t _{DH}	0	_	0	—	0	-	ns	5
Write enable to output in high Z	t _{WZ}	_	6	_	6	—	8	ns	4,5
Output active from write end	t _{OW}	1	-	1	-	2	-	ns	4,5
Byte select low to end of write	t _{BW}	8	—	9	—	12	-	ns	

Shaded areas indicate preliminary information.

Write waveform 1 ($\overline{\text{WE}}$ controlled)^{10,11}



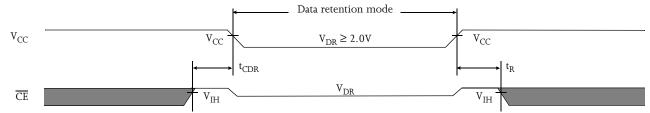




Parameter	Symbol	Test conditions	Min	Max	Unit
V _{CC} for data retention	V _{DR}		2.0	-	V
Data retention current	I _{CCDR}	$\frac{V_{CC} = 2.0V}{CE} \ge V_{CC} - 0.2V$	_	1	ma
Chip deselect to data retention time	t _{CDR}	$CE \ge V_{CC} - 0.2V$ $V_{IN} \ge V_{CC} - 0.2V \text{ or}$	0	_	ns
Operation recovery time	t _R	$V_{\rm IN} \leq V_{\rm CC} = 0.2 V$ of $V_{\rm IN} \leq 0.2 V$	t _{RC}	-	ns
Input leakage current	I _{LI}		_	1	μΑ

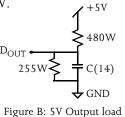
Data retention characteristics (over the operating range)¹³

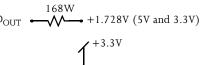
Data retention waveform

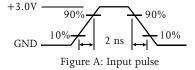


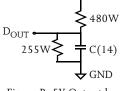
AC test conditions

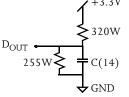
- Output load: see Figure B or Figure C, except as noted.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.











Thevenin Equivalent:

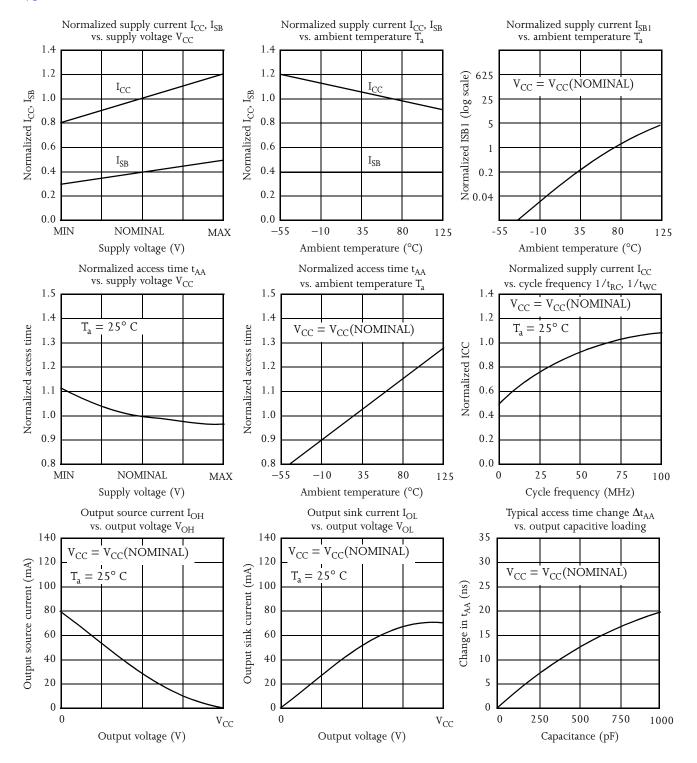
Figure C: 3.3V Output load

Notes

- During V_{CC} power-up, a pull-up resistor to V_{CC} on \overline{CE} is required to meet I_{SB} specification. 1
- This parameter is sampled, but not 100% tested. 2
- 3 For test conditions, see AC Test Conditions, Figures A, B, and C.
- These parameters are specified with $C_L = 5pF$, as in Figures B or C. Transition is measured \pm 500 mV from steady-state voltage. 4
- 5 This parameter is guaranteed, but not tested.
- 6 $\overline{\text{WE}}$ is High for read cycle.
- $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are Low for read cycle. 7
- Address valid prior to or coincident with \overline{CE} transition Low. 8
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 CE or WE must be High during address transitions. Either CE or WE asserting high terminates a write cycle.
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12 Not applicable.
- 13 2V data retention applies to commercial temperature range operation only.
- 14 C=30pF, except all high Z and low Z parameters where C=5pF.

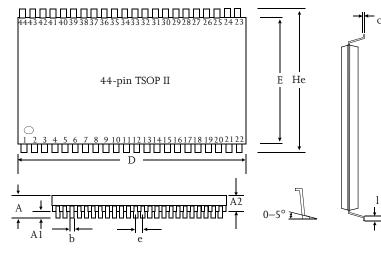


Typical DC and AC characteristics

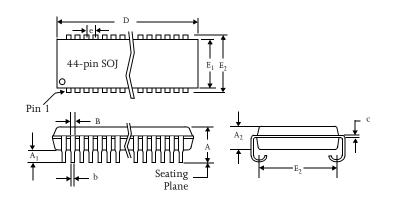




Package dimensions



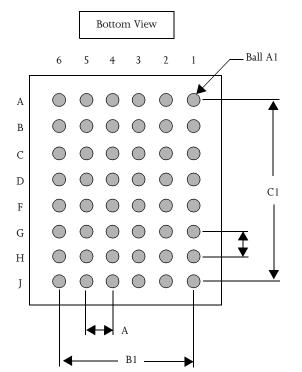
	44-pin TSOP II		
	Min (mm)	Max (mm)	
А		1.2	
A1	0.05		
A2	0.95	1.05	
b	0.30	0.45	
С	0.127 (typical)		
D	18.28 18.54		
Е	10.03	10.29	
He	11.56	11.96	
e	0.80 (typical)		
1	0.40	0.60	

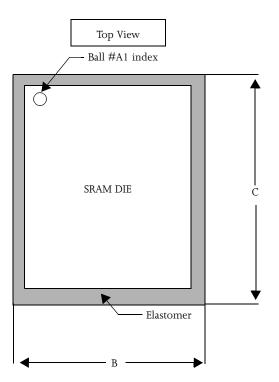


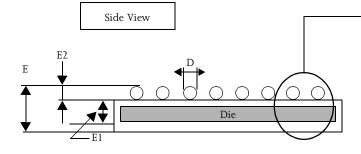
	44-pin SOJ		
	400 mL		
	Min	Max	
А	0.128	0.148	
A ₁	0.025	_	
A ₂	1.105	1.115	
В	0.026	0.032	
b	0.015	0.020	
С	0.007	0.013	
D	1.120	1.130	
Е	0.370 NOM		
E ₁	0.395	0.405	
E ₂	0.435	0.445	
е	0.050 NOM		



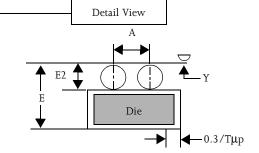
48-ball FBGA







	Minimum	Typical	Maximum
А	-	0.75	—
В	5.90	8.00	8.10
B1	-	3.75	—
С	7.90	8.00	8.10
C1	-	5.25	-
D	-	0.35	-
E	-	_	1.20
E1	_	0.68	_
E2	0.22	0.25	0.27
Y	_	_	0.08



Notes

- 1 Bump counts: 48 (8 row x 6 column).
- 2 Pitch: (x,y) = 0.75 mm x 0.75 mm (typ).
- 3 Units: millimeters.
- 4 All tolerance are +/- 0.050 unless otherwise specified.
- 5 Typ: typical.
- 6 Y is coplanarity: 0.08 (max).

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Ordering codes

Package \ Access time	Volt/Temp	12 ns	15 ns	20 ns
	5V commercial	AS7C1026-12JC	AS7C1026-15JC	AS7C1026-20JC
Plastic SOJ, 400 mil	5V industrial	AS7C1026-12JI	AS7C1026-15JI	AS7C1026-20JI
	3.3V commercial	AS7C31026-12JC	AS7C31026-15JC	AS7C31026-20JC
TSOP II, 18.4×10.2 mm	5V commercial	AS7C1026-12TC	AS7C1026-15TC	AS7C1026-20TC
	3.3V commercial	AS7C31026-12TC	AS7C31026-15TC	AS7C31026-20TC
	3.3V industrial	AS7C31026-12TI	AS7C31026-15TI	AS7C31026-20TI
	5V commercial	AS7C1026-12BC	AS7C1026-15BC	AS7C1026-20BC
CSP BGA, 8×6 mm	3.3V commercial	AS7C31026-12BC	AS7C31026-15BC	AS7C31026-20BC
	3.3V industrial	AS7C31026-12BI	AS7C31026-15BI	AS7C31026-20BI

NA: not available.

Shaded areas indicate preliminary information.

Part numbering system

AS7C	Х	1026	-XX	Х	С
SRAM prefix	Blank=5V CMOS 3=3.3V CMOS	Device number	Access time	Package: J=SOJ 400 mil T=TSOP type 2, 18.4 × 10.2 mm B=CSP BGA, 8 × 6 mm	Temperature range, C=Commercial: 0° C to 70° C I=Industrial: -40° C to 85° C

3/23/01; v.1.0

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