

AZ10EL32 AZ100EL32

ECL/PECL ÷ 2 Divider

FEATURES

- 510ps Propagation Delay
- 3.0GHz Toggle Frequency
- High Bandwidth Output Transitions
- 75kΩ Internal Input Pulldown Resistors
- Direct Replacement for ON Semiconductor MC10EL32 & MC100EL32

PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING
SOIC 8	AZ10EL32D	AZM10EL32
SOIC 8 T&R	AZ10EL32DR1	AZM10EL32
SOIC 8 T&R	AZ10EL32DR2	AZM10EL32
SOIC 8	AZ100EL32D	AZM100EL32
SOIC 8 T&R	AZ100EL32DR1	AZM100EL32
SOIC 8 T&R	AZ100EL32DR2	AZM100EL32
TSSOP 8	AZ10EL32T	AZTEL32
TSSOP 8 T&R	AZ10EL32TR1	AZTEL32
TSSOP 8 T&R	AZ10EL32TR2	AZTEL32
TSSOP 8	AZ100EL32T	AZHEL32
TSSOP 8 T&R	AZ100EL32TR1	AZHEL32
TSSOP 8 T&R	AZ100EL32TR2	AZHEL32

DESCRIPTION

The AZ10/100EL32 is an integrated ÷2 divider. The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flop will attain a random logic state; the reset allows for the synchronization of multiple EL32's in a system.

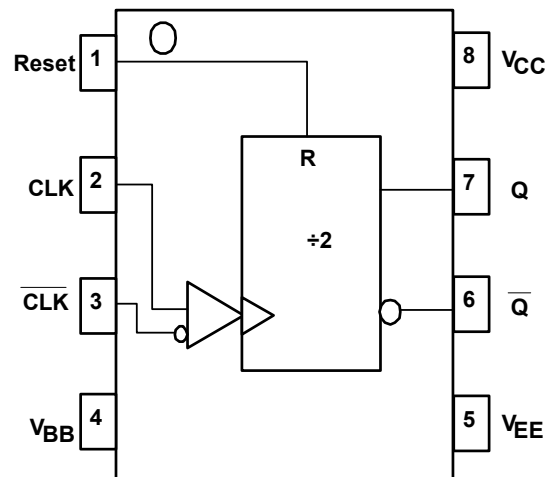
The EL32 provides a V_{BB} output for single-ended use or a DC bias reference for AC coupling to the device. For single-ended input applications, the V_{BB} reference should be connected to one side of the CLK/CLK differential input pair. The input signal is then fed to the other CLK/CLK input. The V_{BB} pin should be used only as a bias for the EL32 as its sink/source capability is limited. When used, the V_{BB} pin should be bypassed to ground via a 0.01μF capacitor.

NOTE: Specifications in ECL/PECL tables are valid when thermal equilibrium is established.

LOGIC DIAGRAM AND PINOUT ASSIGNMENT

PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{\text{CLK}}$	Clock Inputs
Reset	Asynch Reset
V_{BB}	Reference Voltage Output
Q, \overline{Q}	Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply



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Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V _{CC}	PECL Power Supply (V _{EE} = 0V)	0 to +8.0	Vdc
V _I	PECL Input Voltage (V _{EE} = 0V)	0 to +6.0	Vdc
V _{EE}	ECL Power Supply (V _{CC} = 0V)	-8.0 to 0	Vdc
V _I	ECL Input Voltage (V _{CC} = 0V)	-6.0 to 0	Vdc
I _{OUT}	Output Current --- Continuous --- Surge	50 100	mA
T _A	Operating Temperature Range	-40 to +85	°C
T _{STG}	Storage Temperature Range	-65 to +150	°C

10K ECL DC Characteristics (V_{EE} = -4.75V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ¹	-1080		-890	-1020		-840	-980		-810	-910		-720	mV
V _{OL}	Output LOW Voltage ¹	-1950		-1650	-1950		-1630	-1950		-1630	-1950		-1595	mV
V _{IH}	Input HIGH Voltage	-1230		-890	-1170		-840	-1130		-810	-1060		-720	mV
V _{IL}	Input LOW Voltage	-1950		-1500	-1950		-1480	-1950		-1480	-1950		-1445	mV
I _{IH}	Input HIGH Current			150			150			150			150	μA
I _{IL}	Input LOW Current	0.5			0.5			0.5			0.5			μA
V _{BB}	Output Reference Voltage	-1430		-1300	-1380		-1270	-1350		-1250	-1310		-1190	mV
I _{EE}	Power Supply Current		25	30		25	30		25	30		25	30	mA

- Each output is terminated through a 50Ω resistor to V_{CC} - 2V.

10K PECL DC Characteristics (V_{EE} = GND, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	3920		4110	3980		4160	4020		4190	4090		4280	mV
V _{OL}	Output LOW Voltage ^{1,2}	3050		3350	3050		3370	3050		3370	3050		3405	mV
V _{IH}	Input HIGH Voltage ¹	3770		4110	3830		4160	3870		4190	3940		4280	mV
V _{IL}	Input LOW Voltage ¹	3050		3500	3050		3520	3050		3520	3050		3555	mV
I _{IH}	Input HIGH Current			150			150			150			150	μA
I _{IL}	Input LOW Current	0.5			0.5			0.5			0.5			μA
V _{BB}	Output Reference Voltage	3570		3700	3620		3730	3650		3750	3690		3810	mV
I _{EE}	Power Supply Current		25	30		25	30		25	30		25	30	mA

- For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
- Each output is terminated through a 50Ω resistor to V_{CC} - 2V.

100K ECL DC Characteristics (V_{EE} = -4.2V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ¹	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	-1025	-955	-880	mV
V _{OL}	Output LOW Voltage ¹	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	-1810	-1705	-1620	mV
V _{IH}	Input HIGH Voltage	-1165		-880	-1165		-880	-1165		-880	-1165		-880	mV
V _{IL}	Input LOW Voltage	-1810		-1475	-1810		-1475	-1810		-1475	-1810		-1475	mV
I _{IH}	Input HIGH Current			150			150			150			150	μA
I _{IL}	Input LOW Current	0.5			0.5			0.5			0.5			μA
V _{BB}	Output Reference Voltage	-1380		-1260	-1380		-1260	-1380		-1260	-1380		-1260	mV
I _{EE}	Power Supply Current		25	30		25	30		25	30		29	35	mA

- Each output is terminated through a 50Ω resistor to V_{CC} - 2V.

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100K PECL DC Characteristics ($V_{EE} = \text{GND}$, $V_{CC} = +5.0\text{V}$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage ^{1,2}	3915	3995	4120	3975	4045	4120	3975	4045	4120	3975	4045	4120	mV
V_{OL}	Output LOW Voltage ^{1,2}	3170	3305	3445	3190	3295	3380	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage ¹	3835		4120	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage ¹	3190		3525	3190		3525	3190		3525	3190		3525	mV
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			μA
V_{BB}	Output Reference Voltage	3620		3740	3620		3740	3620		3740	3620		3740	mV
I_{EE}	Power Supply Current		25	30		25	30		25	30		29	35	mA

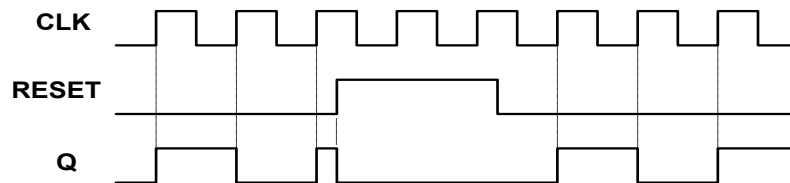
- For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
- Each output is terminated through a 50Ω resistor to $V_{CC} - 2V$.

AC Characteristics ($V_{EE} = 10E(-4.75\text{V to } -5.5\text{V})$, $100E(-4.2\text{V to } -5.5\text{V})$; $V_{CC} = \text{GND}$ or $V_{EE} = \text{GND}$, $V_{CC} = 10E(+4.75\text{V to } +5.5\text{V})$, $100E(+4.2\text{V to } +5.5\text{V})$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	2.2	3.0		2.6	3.0		2.6	3.0		2.6	3.0		GHz
$t_{\text{PLH}}/t_{\text{PHL}}$	Propagation Delay CLK to Q Reset to Q	360 390	500 540	640 690	410 440	500 540	590 640	420 440	510 540	600 640	450 450	540 550	630 650	ps
$V_{\text{PP}}(\text{AC})$	Minimum Input Swing ¹	150			150			150			150			mV
V_{CMR}	Common Mode Range ²	$V_{CC} - 2.5$		$V_{CC} - 0.4$	$V_{CC} - 2.5$		$V_{CC} - 0.4$	$V_{CC} - 2.5$		$V_{CC} - 0.4$	$V_{CC} - 2.5$		$V_{CC} - 0.4$	V
t_r / t_f	Output Rise/Fall Times Q (20% - 80%)	100		350	100		350	100		350	100		350	ps

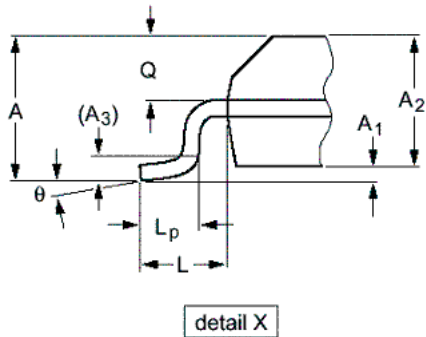
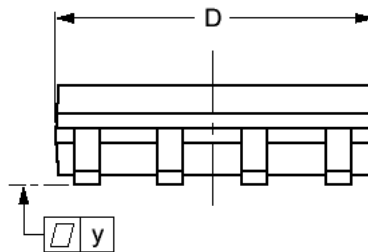
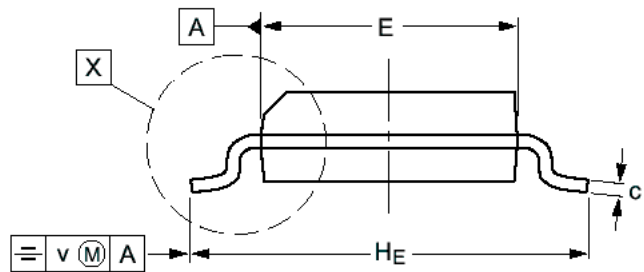
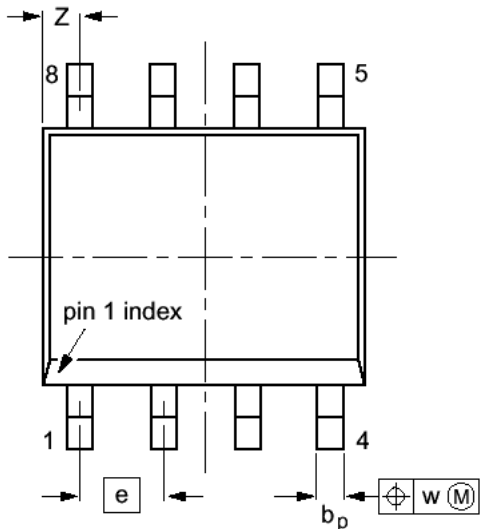
- V_{PP} is the minimum peak-to-peak differential input swing for which AC parameters are guaranteed.
- V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to $V_{\text{PP}}(\text{min})$.

Figure 1: Timing Diagram



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**PACKAGE DIAGRAM
SOIC 8**



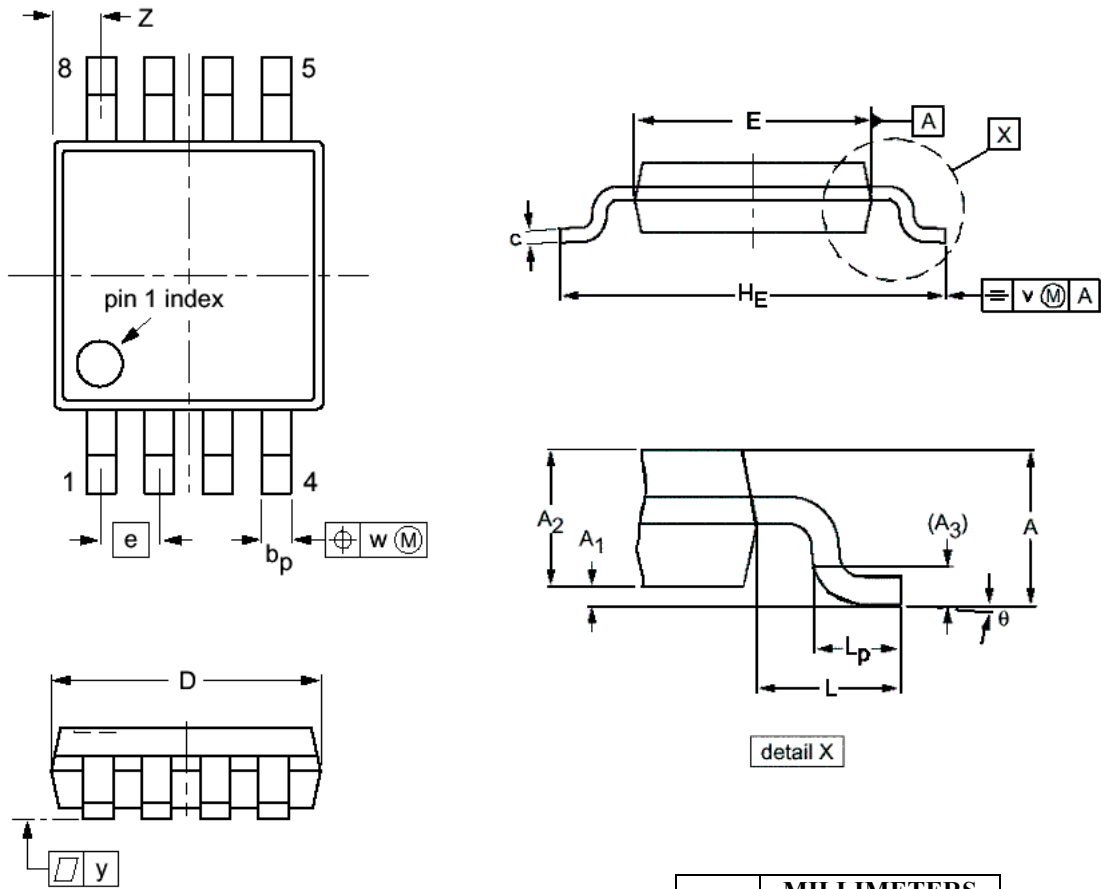
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A		1.75	0.069	
A ₁	0.10	0.25	0.004	0.010
A ₂	1.25	1.45	0.049	0.057
A ₃	0.25		0.01	
b _p	0.36	0.49	0.014	0.019
c	0.19	0.25	0.0075	0.0100
D	4.8	5.0	0.19	0.20
E	3.8	4.0	0.15	0.16
e	1.27		0.050	
H _E	5.80	6.20	0.228	0.244
L	1.05		0.041	
L _p	0.40	1.00	0.016	0.039
Q	0.60	0.70	0.024	0.028
v	0.25		0.01	
w	0.25		0.01	
y	0.10		0.004	
Z	0.30	0.70	0.012	0.028
θ	0°	8°	0°	8°

NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

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**PACKAGE DIAGRAM
TSSOP 8**



NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

DIM	MILLIMETERS	
	MIN	MAX
A		1.10
A ₁	0.05	0.15
A ₂	0.80	0.95
A ₃	0.25	
b _p	0.25	0.45
c	0.15	0.28
D	2.90	3.10
E	2.90	3.10
e	0.65	
H _E	4.70	5.10
L	0.94	
L _p	0.40	0.70
v	0.10	
w	0.10	
y	0.10	
Z	0.35	0.70
θ	0°	6°

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