

## *PicoGuard XS™ eXtreme Speed* ESD Clamp Array For High Speed Data Line Protection

### Features

- ESD protection for 4 pairs of differential channels
- ESD protection to IEC61000-4-2 Level 4 at  $\pm 8\text{kV}$  contact discharge
- Pass-through impedance matched clamp architecture
- Flow-through routing for high-speed signal integrity
- Minimal line capacitance change with temperature and voltage
- $100\Omega$  matched impedance for each paired differential channel
- Each I/O pin can withstand over 1000 ESD strikes\*
- RoHS compliant (lead-free) TDFN-16 package

### Applications

- DVI ports, HDMI ports in notebooks, set top boxes, digital TVs, LCD displays
- General purpose high-speed data line ESD protection

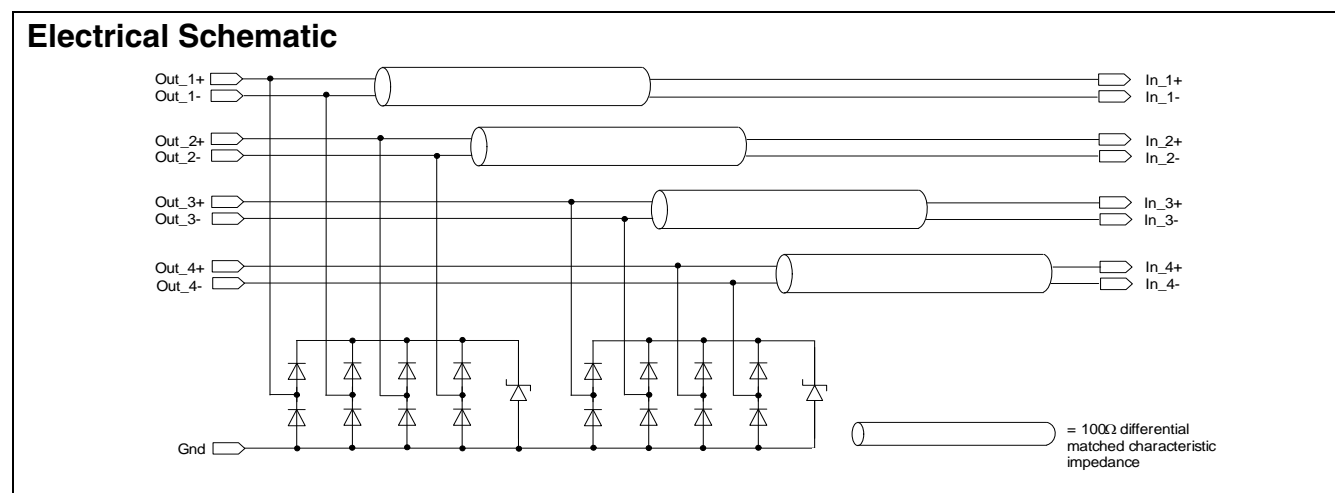
### Product Description

The *PicoGuard XS (eXtreme Speed)* protection family is specifically designed for next generation deep sub-micron high speed data line protection.

The CM1233 is ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading and tightly controlled signal skews (with channel-to-channel matching at 2% max deviation).

The device is particularly well-suited for protecting systems using high-speed ports such as DVI or HDMI, along with corresponding ports in removable storage, digital camcorders, DVD-RW drives and other applications where extremely low loading capacitance with ESD protection are required.

The CM1233 also features easily routed "pass-through" pinouts in a RoHS compliant (lead-free), 16-lead TDFN, small footprint package.



\*Standard test condition is IEC61000-4-2 level 4 test circuit with each pin subjected to  $\pm 8\text{kV}$  contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.

## PicoGuard XS ESD Protection Architecture

Conceptually, an ESD protection device performs the following actions upon an ESD strike discharge into a protected ASIC (see Figure 1):

1. When an ESD potential is applied to the system under test (contact or air-discharge), Kirchoff's Current Law (KCL) dictates that the Electrical Overstress (EOS) currents will immediately divide throughout the circuit, based on the dynamic impedance of each path.
2. Ideally, the classic shunt ESD clamp will switch within 1ns to a low-impedance path and return the majority of the EOS current to the chassis shield/reference ground. In actuality, if the ESD component's response time ( $t_{CLAMP}$ ) is slower than the ASIC it is protecting, or if the Dynamic Clamping Resistance ( $R_{DYN}$ ) is not significantly lower than the ASIC's I/O cell circuitry, then the ASIC will have to absorb a large amount of the EOS energy, and be more likely to fail.
3. Subsequent to the ESD/EOS event, both devices must immediately return to their original specifications, and be ready for an additional strike. Any deterioration in parasitics or clamping capability

should be considered a failure, since it can then affect signal integrity or subsequent protection capability. (This is known as "multi-strike" capability.)

In the CM1233 *PicoGuard XS* architecture, the signal line leading the connector to the ASIC routes through the CM1233 chip which provides  $100\Omega$  matched differential channel characteristic impedance that helps optimize  $100\Omega$  load impedance applications such as the HDMI high speed data lines.

Note: When each of the channels are used individually for single-ended signal lines protection, the individual channel provides  $50\Omega$  characteristic impedance matching.

The load impedance matching feature of the CM1233 helps to simplify system designer's PCB layout considerations in impedance matching and also eliminates associated passive components.

The route through the *PicoGuard XS* architecture enables the CM1233 to provide matched impedance for the signal path between the connector and the ASIC. Besides this function, this circuit arrangement also changes the way the parasitic inductance interacts with the ESD protection circuit and helps reduce the  $I_{RESIDUAL}$  current to the ASIC.

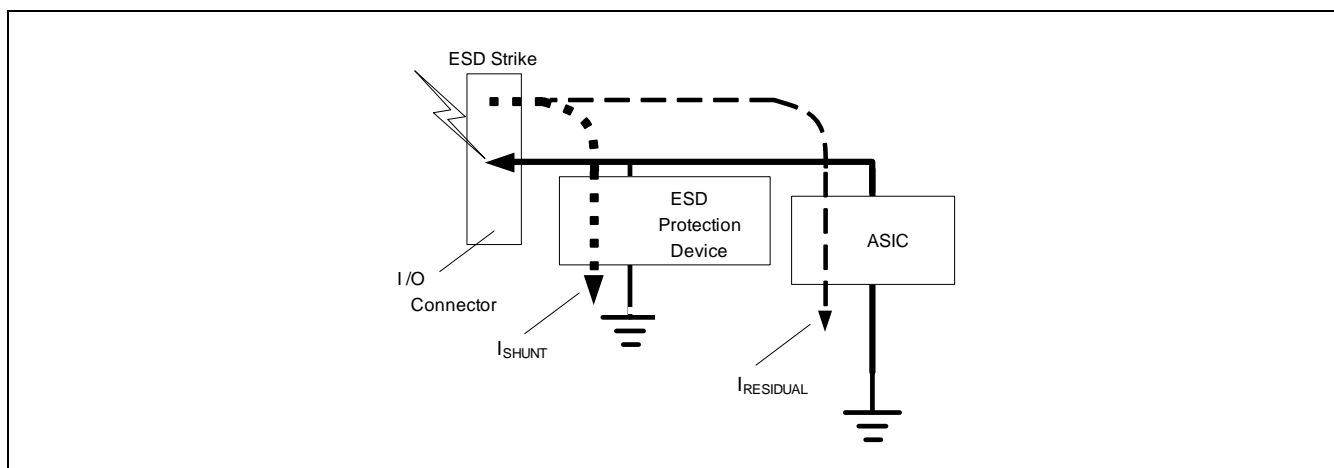
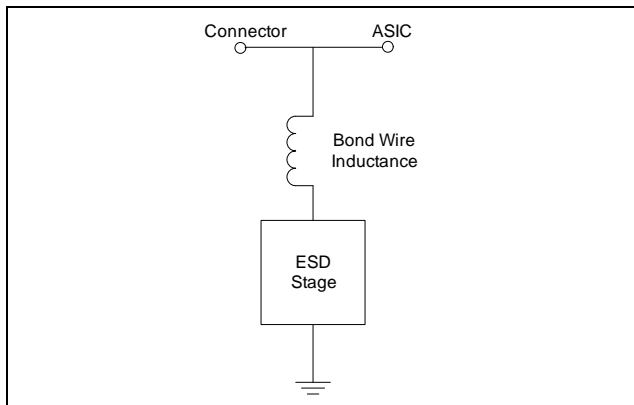


Figure 1. Standard ESD Protection Device Block Diagram

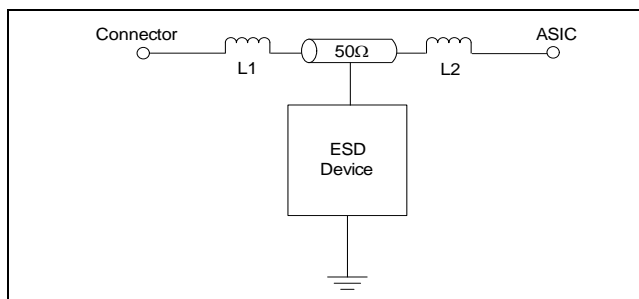
### The *PicoGuard XS* Architecture Advantages

Figure 2 illustrates a standard ESD protection device. The inductor element represents the parasitic inductance arising from the bond wire and the PCB trace leading to the ESD protection diodes.



**Figure 2. Standard ESD Protection Model**

Figure 3 illustrates one of the channels. Similarly, the inductor elements represent the parasitic inductance arising from the bond wire and PCB traces leading to the ESD protection diodes as well.



**Figure 3. CM1233 *PicoGuard XS* ESD Protection Model**

### CM1233 Inductor Elements

In the CM1233 *PicoGuard XS* architecture, the inductor elements and ESD protection diodes interact differently compared to the standard ESD model.

In the standard ESD protection device model, the inductive element presents high impedance against high slew rate strike voltage, i.e. during an ESD strike. The impedance increases the resistance of the conduction path leading to the ESD protection

element. This limits the speed that the ESD pulse can discharge through the ESD protection element.

In the *PicoGuard XS* architecture, the inductive elements are in series to the conduction path leading to the protected device. The elements actually help to limit the current and voltage striking the protected device.

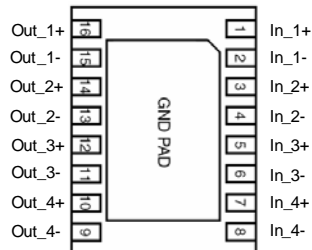
First the reactance of the inductive element, L1, on the connector side when an ESD strike occurs, acts in the opposite direction of the ESD striking current. This helps limit the peak striking voltage. Then the reactance of the inductive element, L2, on the ASIC side forces this limited ESD strike current to be shunted through the ESD protection diodes. At the same time, the voltage drop across both series element acts to lower the clamping voltage at the protected device terminal.

Through this arrangement, the inductive elements also tune the impedance of the ESD protection element by cancelling the capacitive load presented by the ESD diodes to the signal line. This improves the signal integrity and makes the overall ESD protection device more transparent to the high bandwidth data signals passing through the channel.

The innovative *PicoGuard XS* architecture turns the disadvantages of the parasitic inductive elements into useful components that help to limit the ESD current strike to the protected device and also improves the signal integrity of the system by balancing the capacitive loading effects of the ESD diodes. At the same time, this architecture provides an impedance matched signal path for 50Ω loading applications.

Board designs can take advantage of precision internal component matching for improved signal integrity, which is not otherwise possible with discrete components at the system level. This helps to simplify the PCB layout considerations by the system designer and eliminates the associated passive components for load matching that is normally required with standard ESD protection circuits.

Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to either the Zener diode or to ground. This embedded Zener diode also serves to eliminate the need for a separate bypass capacitor to absorb positive ESD strikes to ground. The CM1233 protects against ESD pulses up to ±8kV contact per the IEC 61000-4-2 standard.

**PACKAGE / PINOUT DIAGRAMS**
**Bottom View (Solder Side)**


Note:

1) This drawing is not to scale.

**PIN DESCRIPTIONS**

Pin	Name	Description
1	In_1+	Bidirectional Clamp to ASIC (inside system)
2	In_1-	Bidirectional Clamp to ASIC (inside system)
3	In_2+	Bidirectional Clamp to ASIC (inside system)
4	In_2-	Bidirectional Clamp to ASIC (inside system)
5	In_3+	Bidirectional Clamp to ASIC (inside system)
6	In_3-	Bidirectional Clamp to ASIC (inside system)
7	In_4+	Bidirectional Clamp to ASIC (inside system)
8	In_4-	Bidirectional Clamp to ASIC (inside system)
9	Out_4-	Bidirectional Clamp to Connector (outside system)
10	Out_4+	Bidirectional Clamp to Connector (outside system)
11	Out_3-	Bidirectional Clamp to Connector (outside system)
12	Out_3+	Bidirectional Clamp to Connector (outside system)
13	Out_2-	Bidirectional Clamp to Connector (outside system)
14	Out_2+	Bidirectional Clamp to Connector (outside system)
15	Out_1-	Bidirectional Clamp to Connector (outside system)
16	Out_1+	Bidirectional Clamp to Connector (outside system)
PAD	GND	Ground return to shield

**Ordering Information**
**PART NUMBERING INFORMATION**

PIN	PACKAGE	ORDERING PART NUMBER (LEAD-FREE FINISH)	PART MARKING
16	TDFN-16	CM1233-08DE	CM1233-08

Note 1: Parts are shipped in Tape &amp; Reel form unless otherwise specified.

## Specifications

### ABSOLUTE MAXIMUM RATINGS\*

PARAMETER	RATING	UNITS
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
Breakdown Voltage (Positive)	6	V

\*Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN}$	I/O Voltage Relative to GND		-0.5		5.5	V
$I_{IN}$	Continuous Current through signal pins (IN to OUT) 1000 Hr			100		mA
$I_F$	Channel Leakage Current	$T_A = 25^\circ\text{C}$ ; $V_{IN} = 5\text{V}$		$\pm 0.1$	$\pm 1.0$	$\mu\text{A}$
$V_{ESD}$	ESD Protection - Peak Discharge Voltage at any channel input, in system: Contact discharge per IEC 61000-4-2 Standard	$T_A = 25^\circ\text{C}$ ; Note 2	$\pm 8$			kV
$I_{RES}$	Residual ESD Peak Current on RDUP (Resistance of Device Under Protection)	IEC 61000-4-2 8kV; RDUP = $5\Omega$ , $T_A = 25^\circ\text{C}$ ; Note 2 and <a href="#">Figure 6</a>		3.2		A
$V_{CL}$	Channel Clamp Voltage (Channel clamp voltage per IEC 61000-4-5 Standard) Positive Transients Negative Transients	$I_{PP} = 1\text{A}$ , $T_A = 25^\circ\text{C}$ , $t_P = 8/20\mu\text{S}$ ; Note 2		+10 -1.8		V V
$R_{DYN}$	Dynamic Resistance Positive Transients Negative Transients	$I_{PP} = 1\text{A}$ , $T_A = 25^\circ\text{C}$ , $t_P = 8/20\mu\text{S}$ ; Note 2		0.9 0.55		$\Omega$ $\Omega$
$Z_o$	Differential Channels pair characteristic impedance	$T_R = 200\text{ps}$ ; Note 2		100		$\Omega$
$\Delta Z_o$	Channel-to-Channel Impedance Match (Differential)	$T_R = 200\text{ps}$ ; Note 2		2		%
$Z_{CHANNEL}$	Individual Channel Characteristic Impedance in Single-ended Connection	$T_R = 200\text{ps}$ ; Note 2		50		$\Omega$
$\Delta Z_{CHANNEL}$	Channel-to-Channel Impedance Match (Individual)	$T_R = 200\text{ps}$ ; Note 2		2		%

Note 1: All parameters specified at  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise noted.

Note 2: This parameter is guaranteed by design and verified by device characterization

## Performance Information

### Graphical Comparison and Test Setup

Figure 4 shows that the CM1233 (*PicoGuard XS* ESD protector) lowers the peak voltage and clamping voltage by 45% across a wide range of loading conditions in comparison to a standard ESD protection device. Figure 5 also indicates that the DUP/ASIC protected by the CM1233 dissipates less energy than a standard ESD protection device. This data was derived using the test setups shown in Figure 6.

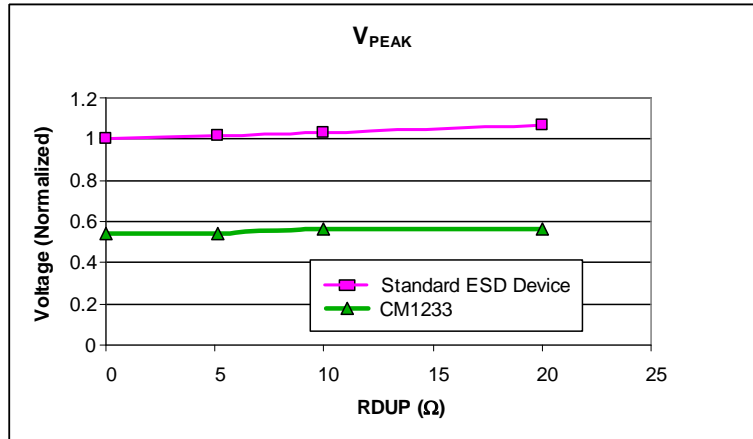


Figure 4. VPeak (8KV IEC-61000 4-2 ESD Contact Strike) and VClamp vs. Loading (RDUP)\*

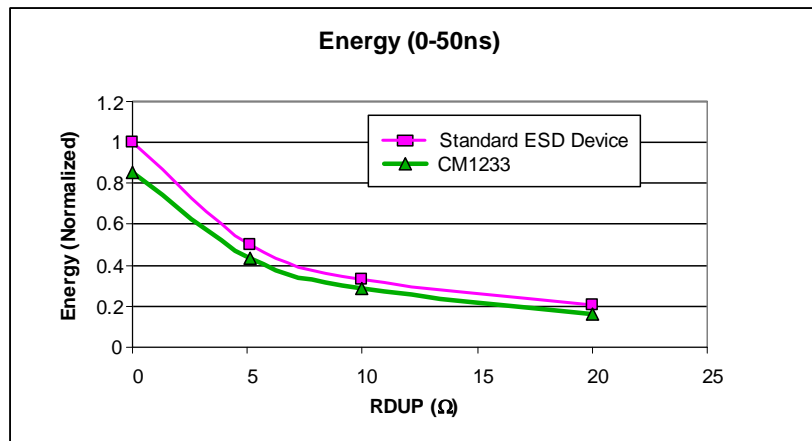
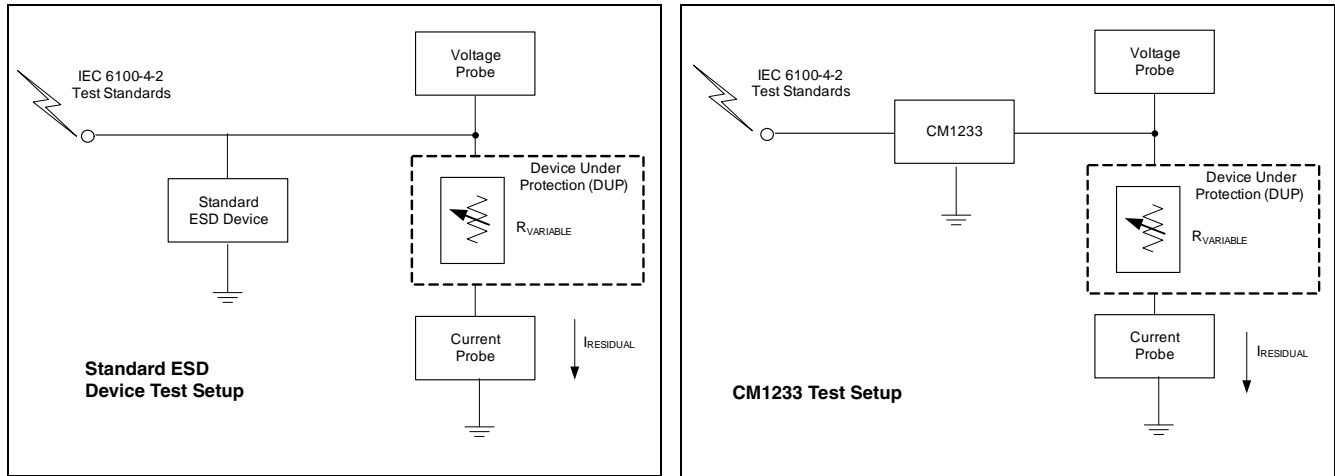
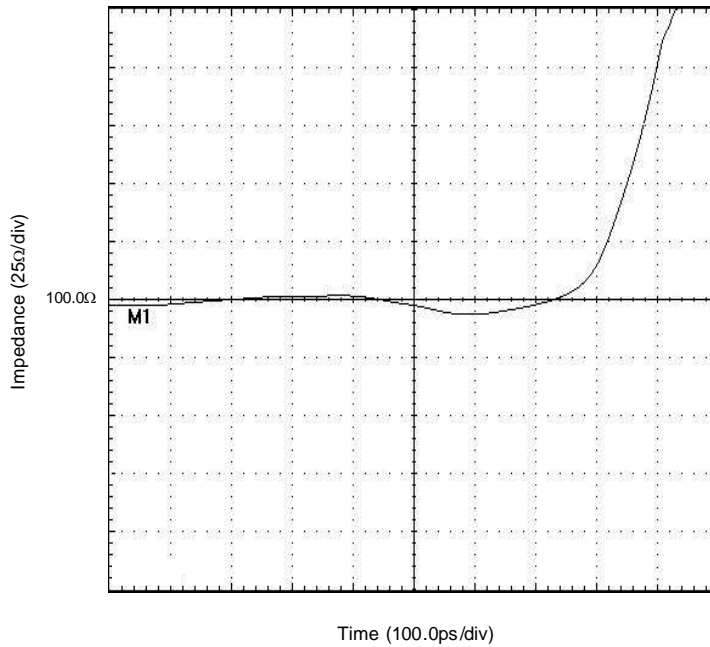


Figure 5. Energy Dissipated in DUP vs RDUP\*

\* RDUP is the emulated Dynamic Resistance (load) of the Device Under Protection (DUP). See Figure 6.



**Figure 6. Test Setups: Standard Device (Left) and CM1233 (Right)**



**Figure 7. Typical Channel TDR Measured Across Out\_x and In\_x Per Each Differential Channels Pair (Typical 200ps Incident Rise Time)**

## Application Information

### CM1233 Application and Guidelines

As a general rule, the CM1233 ESD protection array should be located as close as possible to the point of entry of expected electrostatic discharges with minimum PCB trace lengths to the ground planes and between the signal input and the ESD device to minimize stray series inductance.

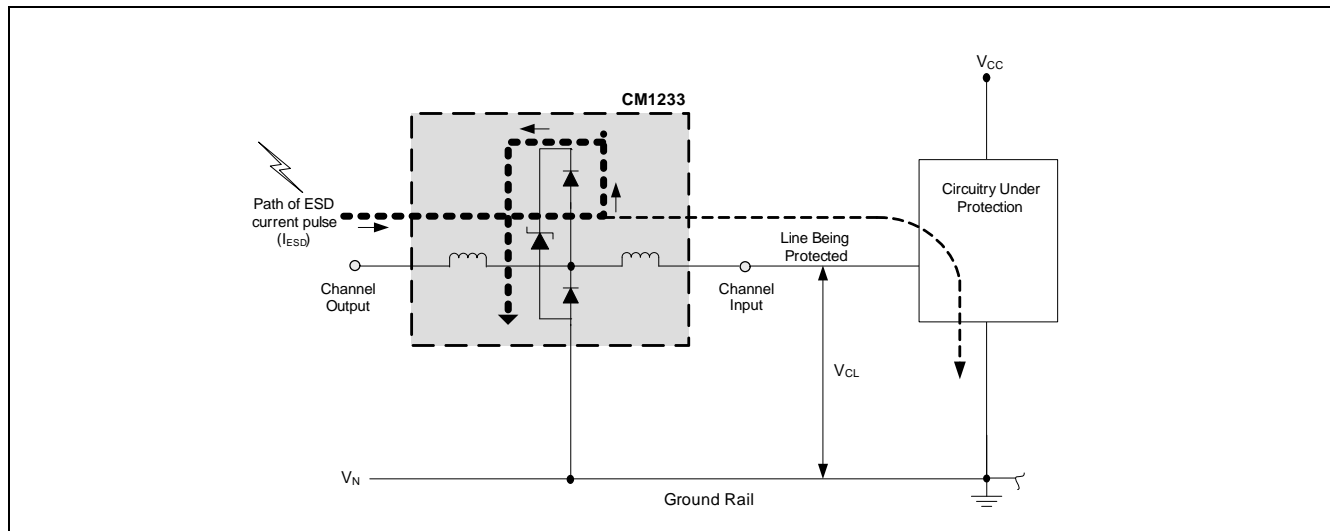


Figure 8. Application of Positive ESD Pulse Between Input Channel and Ground

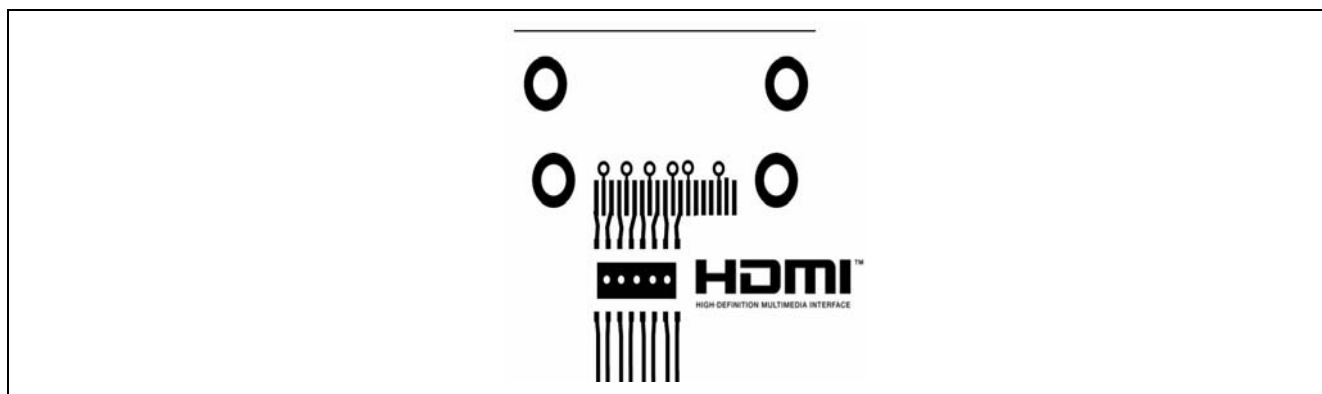


Figure 9. Typical PCB Layout

### Additional Information

See also California Micro Devices Application Note AP209, "Design Considerations for ESD Protection," in the Applications section at [www.calmicro.com](http://www.calmicro.com).



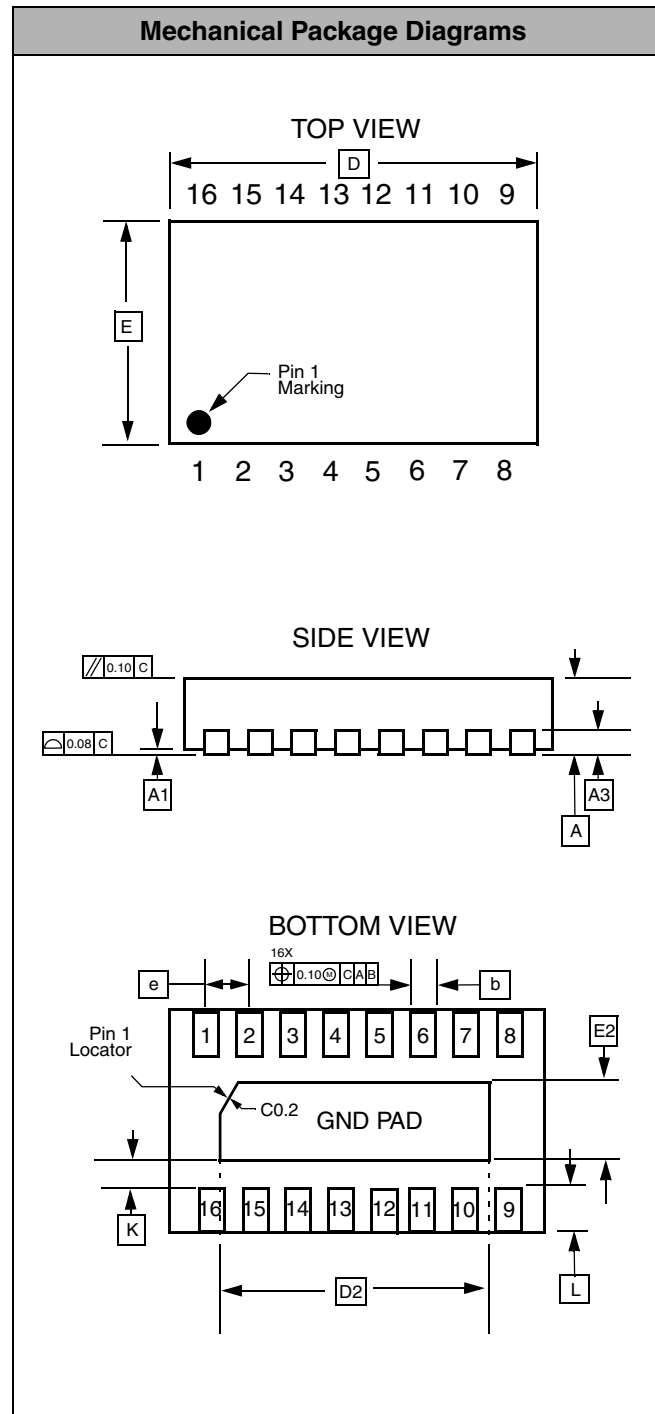
## Mechanical Details

### TDFN-16 Mechanical Specifications, 0.75mm

The 16-lead, 6.0x4.0mm, 0.75mm pitch TDFN package dimensions are presented below.

PACKAGE DIMENSIONS						
Package	TDFN					
JEDEC No.	MO-229C*					
Leads	16					
Dim.	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
<b>A</b>	0.70	0.75	0.80	0.028	0.030	0.031
<b>A1</b>	0.00	0.02	0.05	0.000	0.001	0.002
<b>A3</b>	0.175	0.200	0.225	0.007	0.008	0.009
<b>b</b>	0.20	0.25	0.30	0.008	0.010	0.012
<b>D</b>	5.90	6.00	6.10	0.232	0.236	0.240
<b>D2</b>	5.05	5.10	5.15	0.199	0.201	0.203
<b>E</b>	3.90	4.00	4.10	0.153	0.157	0.161
<b>E2</b>	1.75	1.80	1.85	0.012	0.016	0.020
<b>e</b>	0.75 BSC			0.029 BSC		
<b>K</b>	0.70 REF			0.028 REF		
<b>L</b>	0.35	0.40	0.45	0.014	0.016	0.018
<b># per tape and reel</b>	3000 pieces					
Controlling dimension: millimeters						

\* This package is compliant with JEDEC standard MO-229C with the exception of the D, D2, E, E2, K and L dimensions as called out in the table above.



**Dimensions for 16-Lead, 0.75mm pitch TDFN package**

**Tape and Reel Specifications**

PART NUMBER	PACKAGE SIZE (mm)	POCKET SIZE (mm) $B_0 \times A_0 \times K_0$	TAPE WIDTH W	REEL DIAMETER	QTY PER REEL	$P_0$	$P_1$
CM1233	6.00 X 4.00 X 0.75	6.30 X 4.30 X 1.10	12mm	330mm (13")	3000	4mm	8mm

