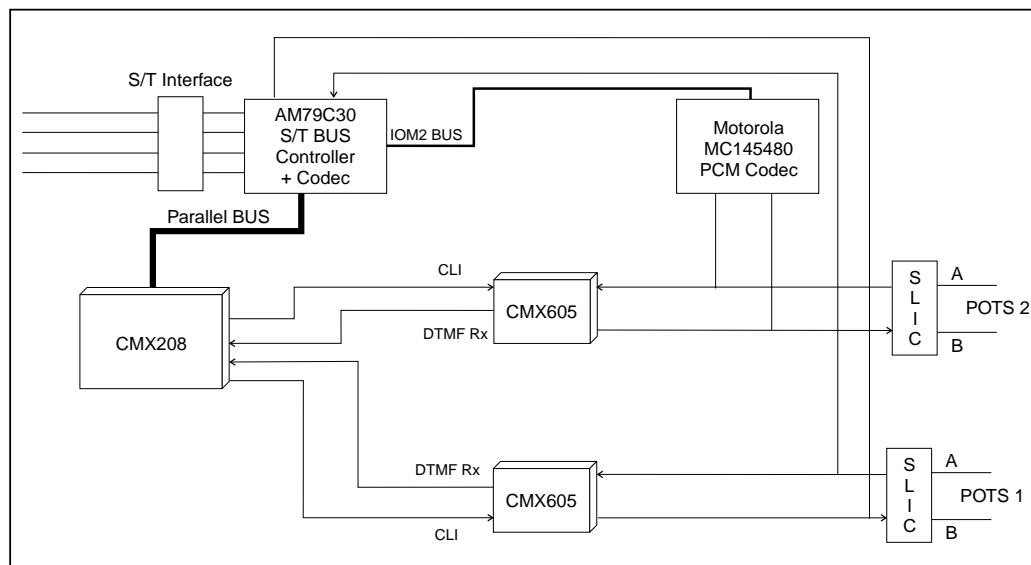


Features

- Supports ITU Specifications ¹
- Supports Incoming and Outgoing Calls
- Independent Port Configuration
- Supports CTR3 Approval
- Full API Available

Applications

- Feature Phones
- Pay-Phones
- PABX Telephones
- Reference Designs Available



The CMX208 is an ISDN telephony protocol engine which implements the lower level ISDN interface and communicates with the CMX605 and other standard devices to form a fully integrated ISDN chipset for voice communications. The CMX208 puts all the main data processing elements in a single device. No ISDN software has to be written and simple 'Plug and Play' design results. This reduces development time and provides a highly cost-effective hardware solution. By using proven circuit designs, the designer can move quickly from initial concept through design in to manufacture.

The CMX208 supports two voice ports over the ISDN Line, which can be used to provide ISDN telephony services or POTS line interfaces, and has independent keypad-configuration of these services for each port. The CMX208's feature set and architecture allow most analog systems to be converted to an ISDN equivalent with enhanced features.

The CMX208 is designed to work with the AMD 79C30 S/T bus interface, the Siemens PSB-21525 HDLC formatter, the Motorola MC145480 PCM codec and the MX-COM CMX605 POTS interface circuit, and also comes complete with embedded applications software. To support the CMX208, MX-COM can also provide licensed reference designs on user request. A flexible Applications Program Interface (API) allows users to customize the features and operation of their own design. The CMX208 is available in an 80-pin QFP (CMX208S1) package.

¹ The CMX208 is a data processor integrated circuit that supports the protocol layers 1, 2 and 3 of the ISDN protocol stack in accordance with the specifications of CCITT (now ITU). These specifications, which are widely used around the world, might not be supported within the U.S.

CONTENTS

Section	Page
1. Block Diagram.....	3
2. Signal List.....	4
3. External Components.....	7
4. General Description.....	8
4.1 Glossary	9
4.2 Initialization	10
4.3 ISDN Interface.....	10
4.3.1 Activation.....	10
4.3.2 De-activation or Line Disconnection.....	10
4.3.3 Line Failure Detection	10
4.3.4 Incoming Calls.....	10
4.3.5 Multiple Subscriber Numbering	11
4.3.6 Channel Mapping	11
4.4 POTS Configuration	12
4.4.1 Configuration and Control via DTMF Keypad.....	12
4.5 POTS Operation.....	13
4.5.1 Keypad Operation	13
4.5.2 Incoming POTS Calls	13
4.5.3 Outgoing POTS Calls	13
4.5.4 Connected Calls	14
4.5.5 Call Clearing.....	14
4.6 Application Programmer's Interface	14
4.7 Hardware Description.....	15
4.7.1 LED Status Indicators (LED1 to LED9, and ILFI).....	15
5. Application Notes	16
5.1 General	16
5.2 Approvals	16
6. Performance Specification.....	17
6.1 Electrical Performance	17
6.1.1 Absolute Maximum Ratings.....	17
6.1.2 Operating Limits	17
6.1.3 Operating Characteristics.....	18
6.2 Packaging	22

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1. Block Diagram

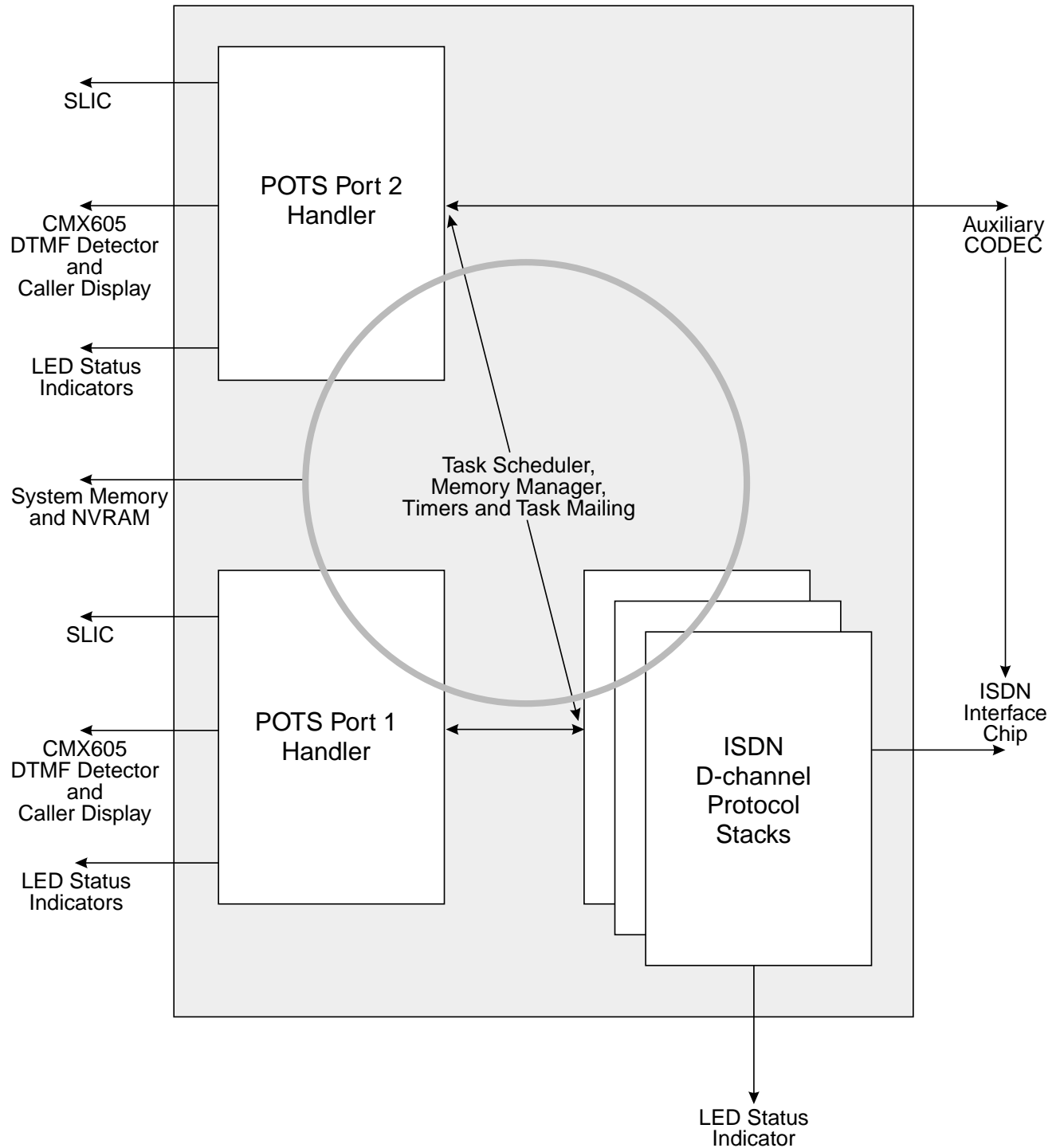


Figure 1: Block Diagram

2. Signal List

S1 Package Pin No.	Signal		Description
	Name	Type	
1	SCL	output	EEPROM - Serial Clock
2	SDA	bi-directional	EEPROM - Serial Data
3	ISDNRST	output	ISDN S-interface Chip Reset
4	N/C	output	Do not make any connection to this pin
5	N/C	output	Do not make any connection to this pin
6	N/C	output	Do not make any connection to this pin
7	$\overline{\text{RST}}$	input	CMX208 Chip Reset (active low)
8	DV _{DD1}	power	The digital positive supply rail. Levels and voltages are dependent upon this supply. This pin should be decoupled to DV _{SS} by a capacitor
9	$\overline{\text{XTAL}}$	output	The output of the on-chip Xtal oscillator inverter
10	XTAL	input	The input to the oscillator inverter from the Xtal circuit
11	DV _{SS1}	power	The digital negative supply rail (ground)
12	LED1	output	POTS Port 1 Off-Hook Indicator (HK1)
13	LED2	output	POTS Port 2 Off-Hook Indicator (HK2)
14	N/C	output	Do not make any connection to this pin
15	LED4	output	POTS Port 2 Call Connected Indicator (CN2)
16	N/C	output	Do not make any connection to this pin
17	N/C	output	Do not make any connection to this pin
18	N/C	output	Do not make any connection to this pin
19	LED8	output	ISDN Line Activated Indicator (AR)
20	$\overline{\text{ST}}$	output	Watchdog Timer Stimulus
21	LED9	output	POTS Port 1 Call Connected Indicator (CN1)
22	$\overline{\text{WR}}$	output	Memory Write Access Strobe
23	$\overline{\text{RD}}$	output	Memory Read Access Strobe
24	A19	output	Memory and Peripheral Address Bus
25	A18	output	Memory and Peripheral Address Bus
26	A17	output	Memory and Peripheral Address Bus
27	A16	output	Memory and Peripheral Address Bus
28	A15	output	Memory and Peripheral Address Bus
29	A14	output	Memory and Peripheral Address Bus
30	A13	output	Memory and Peripheral Address Bus
31	A12	output	Memory and Peripheral Address Bus
32	A11	output	Memory and Peripheral Address Bus
33	A10	output	Memory and Peripheral Address Bus
34	A9	output	Memory and Peripheral Address Bus
35	A8	output	Memory and Peripheral Address Bus
36	A/D7	bi-directional	Memory and Peripheral Address and Data Bus
37	A/D6	bi-directional	Memory and Peripheral Address and Data Bus
38	A/D5	bi-directional	Memory and Peripheral Address and Data Bus

S1 Package Pin No.	Signal		Description
	Name	Type	
39	A/D4	bi-directional	Memory and Peripheral Address and Data Bus
40	A/D3	bi-directional	Memory and Peripheral Address and Data Bus
41	A/D2	bi-directional	Memory and Peripheral Address and Data Bus
42	A/D1	bi-directional	Memory and Peripheral Address and Data Bus
43	A/D0	bi-directional	Memory and Peripheral Address and Data Bus
44	ASTB	output	Address/Data Bus Strobe (data bus selected if low)
45	DV _{SS0}	power	The digital negative supply rail (ground)
46	~	input	For manufacturer's use only. Connect to DV _{SS} directly
47	PSBRES	output	HDLC Chip Reset
48	RING2	output	POTS Port 2 Ringing Generator (low when not ringing)
49	$\overline{\text{RING2}}$	output	POTS Port 2 Ringing Generator (high when not ringing)
50	API-RXD	input	API/RS232 Port Rx Data (inactive = high)
51	API-TXD	output	API/RS232 Port Tx Data (high when inactive)
52	CLIP2	output	POTS Port 2 Line Voltage Adjustment (low when sending FSK to a Caller Display unit. If low, it makes the SLIC present a high impedance to the POTS line)
53	B1/B2	output	B-channel Select (high selects channel B1).
54	ILFI	output	ISDN Line Failure Indicator
55	DV _{DD0}	power	The digital positive supply rail. Levels and voltages are dependent upon this supply. This pin should be decoupled to DV _{SS} by a capacitor
56	RING1	output	POTS Port 1 Ringing Generator (low when not ringing)
57	$\overline{\text{RING1}}$	output	POTS Port 1 Ringing Generator (high when not ringing)
58	CLIP1	output	POTS Port 1 Line Voltage Adjustment (low when sending FSK to a Caller Display unit. If low, it makes the SLIC present a high impedance to the POTS line)
59	ILINE1	input	POTS Port 1 Hook Switch Status Detector (on-hook = low)
60	ILINE2	input	POTS Port 2 Hook Switch Status Detector (on-hook = low)
61	REPLY	input	CMX605 C-BUS Interface - Reply Data
62	CMD-DATA	output	CMX605 C-BUS Interface - Command Data
63	SER-CLK	output	CMX605 C-BUS Interface - Serial Clock
64	AV _{DD}	power	The positive analog supply rail. Levels and voltages are dependent upon this supply. This pin should be decoupled to AV _{SS} by a capacitor
65	AV _{REF1}	power	A/D Reference Voltage. Connect to AV _{DD} directly
66	AV _{SS}	power	The negative analog supply rail (ground)
67	$\overline{\text{CS1}}$	output	CMX605 C-BUS Interface (chip select POTS Port 1)
68	$\overline{\text{CS2}}$	output	CMX605 C-BUS Interface (chip select POTS Port 2)
69	AV _{REF2}	power	D/A Reference Voltage. Connect to AV _{DD} directly
70	AV _{REF3}	power	D/A Reference Voltage. Connect to AV _{SS} directly

S1 Package Pin No.	Signal		Description
	Name	Type	
71	NMI	input	For manufacturer's use only. Connect to DV _{SS} directly
72	API-INT	input	API Interrupt (inactive = high)
73	$\overline{\text{IRQ}}$	input	CMX605 C-BUS Interface - Interrupt (inactive = high)
74	PSBINT	input	HDLC Chip Interrupt
75	~	input	For manufacturer's use only. Connect to DV _{DD} directly
76	~	input	For manufacturer's use only. Connect to DV _{DD} directly
77	ISDNINT	input	ISDN S-interface Chip Interrupt
78	~	input	For manufacturer's use only. Connect to DV _{DD} directly
79	~		For manufacturer's use only. Connect to DV _{DD} directly
80	N/C	output	Do not make any connection to this pin

Table 1: Signal List

3. External Components

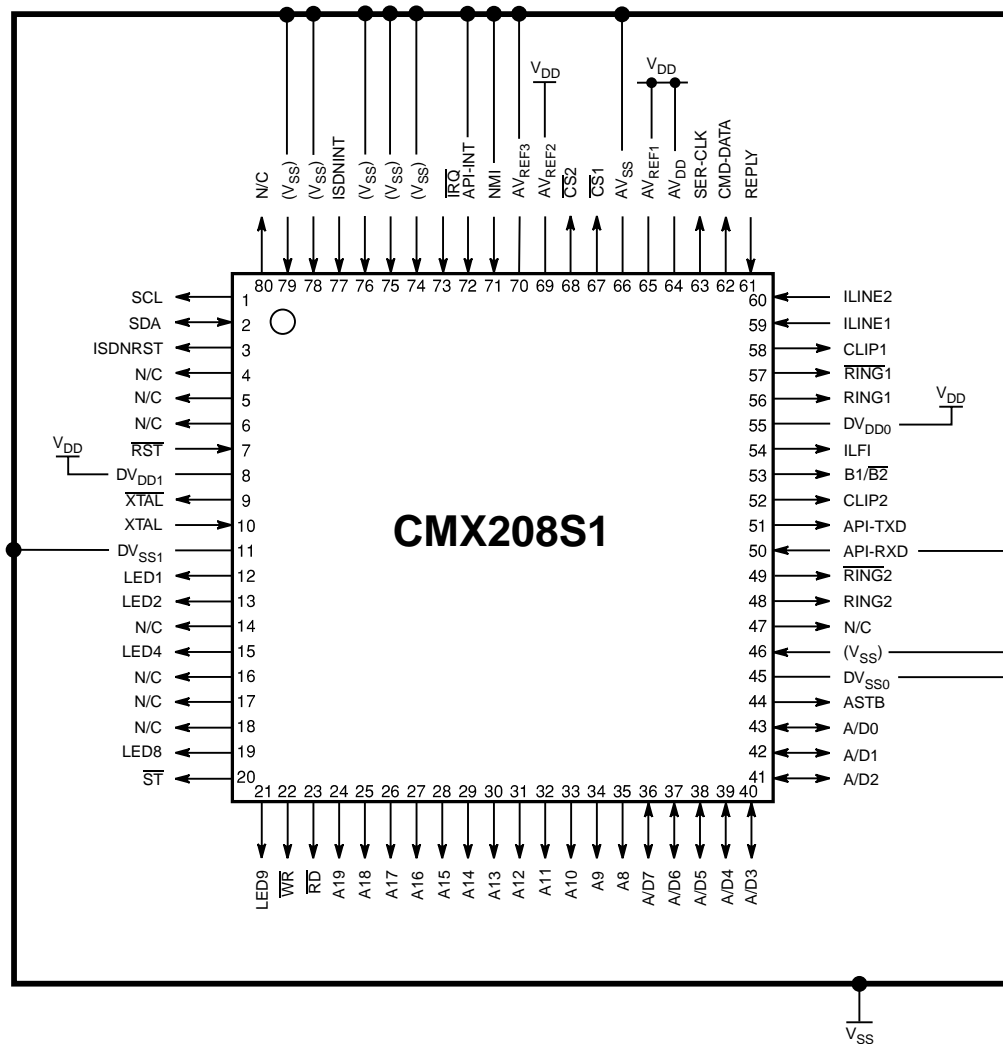


Figure 2: CMX208 Pin-Out

Note: This product is to be used as part of a chip-set. Please refer to the Applications Section (Section 5) for details of the recommended chip-set.

4. General Description

The CMX208 is a single-chip data processor which has been mask programmed with firmware to implement an ISDN protocol stack. This enables the CMX208 to interface two analog (POTS) ports to an ISDN S-bus network connection. Key variables are stored in an external EEPROM and the user can provide additional features by adding external ROM and RAM. Access to the firmware Application Programmer's Interface (API) facilitates the seamless integration of the user's additional features with the pre-programmed ISDN to POTS interfaces.

The CMX208 is intended for use as part of an ISDN chipset and all descriptions in this data sheet refer to this implementation, which is shown in Figure 3. The use of alternative chipsets is not supported.

The firmware supports connection to an ISDN S-bus network interface via the Siemens PSB21525 HDLC controller and the AMD AM79C30 ST controller with integral PCM codec for a single POTS port. An auxiliary Motorola MC145480 PCM codec will need to be added for the second POTS port.

The CMX208 interfaces with up to two CMX605 Tone Generator and DTMF Receiver chips, which decode incoming DTMF tones and generate certain call progress signals (e.g. busy tone) normally originating from an analog telephone exchange. The firmware translates the CMX605 data into ISDN D-channel commands and vice versa to support both incoming and outgoing calls. For the ISDN interface, D-channel commands sufficient for standard telephony applications are implemented. With the aid of a small amount of discrete circuitry, exchange battery voltage, ringing current, line reversal and off-hook detection are also supported, to complete the POTS interface. The CMX208 has dedicated outputs for visible indicators (LEDs) that can be used to provide information on the call status. Support for Multiple Subscriber Numbering is also included in the firmware.

The CMX208 can be configured by means of keypad programming via either POTS port. Configuration parameters allow the user to change (for example) the format and cadence of the ringing signal, so as to facilitate use of the CMX208 in different countries. Each POTS interface is able to configure the variables relevant to its own use.

An Application Programmer's Interface (API) is available and is described separately in Section 4.6. Further details are available on completion of a Non-Disclosure Agreement. Please contact MX-COM directly for further details.

The firmware and finite state machine embedded in the CMX208 have been used in products that have gained ETSI CTR3 approval.

4.1 Glossary

ACCM	Asynchronous Control Character Map
API	Application Programmer's Interface
CIDCW	Caller Identification During Call Waiting
CLI	Calling Line Identification
CRC	Cyclic Redundancy Check
CTS	Clear to Send
DCD	Data Carrier Detect
DDI	Direct Dialing Inwards
DTE	Data Terminal Equipment
DTMF	Dual Tone Multiple Frequency
DTR	Data Terminal Ready
HDLC	High Level Data Link Control
IA5	International Alphabet No 5
IE	Information Element
ILFI	ISDN Line Failure Indicator
ISDN	Integrated Services Digital Network
LAPB	Link Access Procedure – Balanced
LAPD	Link Access Procedure on the D-Channel
LCGN	Logical Channel Group Number
LED	Light Emitting Diode
LLI	Logical Link Identifier
MFO	Multiple Frame Operation
MSN	Multiple Subscriber Numbering
NUA	Network User Address
NUI	Network User Identification
PAD	Packet Assembler/Disassembler
PC	Personal Computer
PCM	Pulse Code Modulation
POTS	Plain Old (Analog) Telephone Service
PPP	Point to Point Protocol
PVC	Permanent Virtual Circuit
RI	Ring Indication
RNR	Receiver Not Ready
RR	Receiver Ready
RTS	Ready to Send
SABM	Set Asynchronous Balanced Mode
SABME	Set Asynchronous Balanced Mode Extended
SLIC	Subscriber Line Interface Circuit
SPM	Subscriber Pulse Metering
SVC	Switched Virtual Circuit
TEI	Terminal Endpoint Identifier

4.2 Initialization

On power-up, the CMX208 assumes its default values, which are factory programmed into the firmware. It then performs a self-test, during which all of the LED pins and the ILFI pin are held high for 3 seconds. If the test is unsuccessful, the CMX208 remains in this condition.

If the test is successful, the CMX208 reads its preset values from the attached EEPROM and examines the state of the ISDN link (i.e. Layer 1) before commencing normal operation. On power-up, the ISDN link is deactivated; the POTS ports are assumed to be on-hook and ringing is disabled.

4.3 ISDN Interface

Two simultaneous voice calls are possible. Incoming calls are firstly checked for other calls present, then the MSN is checked for validity, then the channel mapping, so that responses will be handled accordingly.

When channel mapping is enabled, outgoing calls will request the channel enabled. When not enabled, a request for any channel is made. If no free channels are available for outgoing calls, a locally generated busy tone is returned to the analog port.

4.3.1 Activation

Activation occurs in the following circumstances:

- The ISDN network activates.
- The device connected to the analog port goes off hook.

The Terminal Endpoint Identifier (TEI) is negotiated. Line powering of the CMX208 is not supported.

The 'AR' indicator (LED8) toggles between high and low states when the CMX208 is powered up, and remains constantly low once the CMX208 identifies an activated ISDN line.

ISDN line power detection is not implemented and the CMX208 will negotiate a new TEI on any new network activation.

4.3.2 De-activation or Line Disconnection

De-activation or line disconnection causes the TEI to be removed. Upon re-connection the CMX208 will only be re-activated and request a new TEI when one of the conditions in the above section is met.

4.3.3 Line Failure Detection

If the line failure detection parameter is enabled (via either POTS port) the CMX208 will check that Layer 2 communications are active every sample period of 30 seconds. If Layer 2 communications are not active, the CMX208 will attempt to activate them. If they remain inactive for 2 sample periods, the line is deemed to have failed, so then the ILFI pin is set high and RING1, $\overline{\text{RING1}}$, RING2 and $\overline{\text{RING2}}$ pins are set low. The CMX208 continues to attempt to activate the line and if it becomes active and stays active for 2 sample periods, then the ILFI pin is set low and RING1, $\overline{\text{RING1}}$, RING2 and $\overline{\text{RING2}}$ pins are restored to their default settings.

4.3.4 Incoming Calls

Incoming voice calls and calls from analog lines are directed to the analog ports and all other incoming calls are ignored.

4.3.5 Multiple Subscriber Numbering

Multiple Subscriber Numbering (MSN) enables each POTS port of the CMX208 to have its own telephone number. Up to 23 digits can be saved as the MSN for each port.

All incoming SETUP messages will be checked for the presence of a Called Party Number Information Element (IE). If one is present it is compared with the saved MSN number (if present), starting with the last digit of both numbers. Comparison continues until there are no more numbers in the MSN saved number or the incoming Called Party Number or there is a difference between the numbers. The MSN is said to match if the saved MSN and the incoming calls' Called Party Number are the same for the duration of the shorter number (i.e. if the digit '1' is saved and the received Called Party Number is 654321, then the MSN matches). If there is no saved MSN, the Called Party Number is ignored and call processing continues.

When there is a saved MSN and the Calling Party Number transmit is enabled, all outgoing call SETUP messages will contain a Calling Party Number Information Element.

Note:

1. When a CMX208 with MSN saved and Calling Party Number transmit enabled is connected to some exchanges, no dial tone is heard when going off-hook.
2. Disabling the Calling Party Number transmit will mean that the called party may not receive the Calling Line Identification (CLI), or if they do receive a CLI it will probably be the base number and not the number specific to the calling telephone.

4.3.6 Channel Mapping

It is possible to configure the CMX208 so that the analog ports will only originate calls to and respond to calls from a specific ISDN B-channel. This is a useful feature if, for example, you wish to have a Hunt Group on your ISDN line and only want one voice port to ring on an incoming call.

4.4 POTS Configuration

4.4.1 Configuration and Control via DTMF Keypad

Configuration can be carried out at any time by causing the POTS port to go off-hook and then immediately entering a configuration sequence of DTMF tones. The sequence signaled to the CMX208 will determine the configuration to be performed, as shown in the following table.

Configuration Sequence	Name	Description	Default
02#	Test watchdog	Puts the CMX208 into a permanent loop, not updating the external watchdog counter, so after 2s it should reset.	N/A
90#	Clear MSN	Clears any saved digits	N/A
*90*n#	Save Multiple Subscriber Number (MSN)	n = MSN (up to 23 digits)	Clear
93#	Clear country code	Country code is set to UK by default	N/A
*93*n#	Change country code	n = country code 0 = UK 1 = Belgium 2 = Rest of Europe	UK
94#	Clear channel mapping	Incoming calls on any channel are accepted (provided other parameters are valid e.g. MSN).	N/A
*94*n#	Enable channel mapping	Where n = 1 or 2 for the appropriate channel.	No channel map
95#	Disable Calling Party No. transmit	Outgoing call SETUP messages do not contain any Calling Party Number Information Elements.	N/A
*95*1#	Enable Calling Party No. transmit	Outgoing call SETUP messages contain Calling Party Number Information Element with number set to saved MSN (if a number is present).	Enabled
96#	Disable DDI transmit	Prevents digits being transmitted to the POTS port upon call connection.	N/A
*96*1#	Enable DDI transmit	Upon connection of a call on POTS port 1 only, if there was a Called Party Number Information Element present in the incoming call setup message, the digits are sent as DTMF tones to the POTS port.	Disabled
97#	Disable line failure detection	Once the CMX208 is de-activated it stays de-activated until the network re-activates it or an outgoing call needs to be made.	N/A
*97*1#	Enable line failure detection	The CMX208 checks to see if the ISDN line is activated and Layer 2 communications can be made. It then sets the ILFI pin accordingly.	Disabled
*9**1234567890#	Initialize all configurations.	Resets all of the configuration variables back to their default values.	N/A

Of the above configurations, the following are saved on a per port basis:

MSN
Channel mapping

The rest are saved on a system-wide basis, the last details entered at either port being the configuration saved.

Once the '*' has been recognized, each digit pressed is then checked for validity as a configuration sequence. If any digit pressed is not a valid configuration digit, all digits pressed so far will be transmitted to the network in INFORMATION messages as Keypad Information Elements, until a '#' is entered (with the exception of '*#' being entered, see Keypad Operation below). If the first four digits received are a valid configuration sequence then the configuration mode is entered. When a valid configuration has been completed the CMX208 will send a single DTMF tone to the POTS port. If a valid configuration sequence is received but subsequent digits are invalid, then subsequent digits entered will be ignored and two DTMF tones will be sent to the POTS port.

If the port goes on-hook part way through configuration, it will cause any digits received so far to be ignored. Configurations can be performed consecutively with the exception of the test function (where the attached handset must be replaced immediately after the configuration has been audibly signaled to the POTS port). All configurations entered will be retained after a power-down as they are stored in the external EEPROM.

4.5 POTS Operation

4.5.1 Keypad Operation

The CMX208 supports ISDN keypad messages for control of Network Supplementary services either before or during call establishment. When dialing a number (i.e. off-hook and dial tone audible on POTS port), or if a call has been disconnected by the network but the POTS port has not yet gone on-hook, any keypad string entered will be sent to the network as 'Keypad Information Elements' within INFORMATION messages.

Keypad strings are defined as the following sequences of digits, with the exception of the configuration strings defined in the previous section:

*...#

*#...#

#...#

When a call is connected, pressing the recall key results in all subsequent key presses being sent to the network as 'Keypad Information Elements' within INFORMATION messages, until the handset is replaced. The tones generated by the key presses are also passed down the B-channel, so the remote user will be able to hear them.

4.5.2 Incoming POTS Calls

An incoming POTS call is identified by the Bearer Capability Information Element of the SETUP message being set to 'Speech' or '3.1kHz Audio'. The call will be routed to either (or both) of the POTS ports which satisfy the following three conditions:

- The port is on-hook.
- The MSN saved for the port matches the Called Number in the incoming SETUP message, or no MSN is specified for the port, or there is no Called Number in the SETUP message. See Section 4.3.5 for details of POTS port MSN selection.
- The ISDN B-channel on which the call is placed (as indicated in the SETUP message) is compatible with the channel mapping configuration for the port. See Section 4.3.6 for details of POTS port channel mapping selection.

When the call is routed to a port, the ringing signal for that port will be applied by means of the RING1 and RING1 (or RING2 and RING2) pins.

The call is answered when either of the ports with ringing signal goes off-hook. The ringing signal is then stopped and the ISDN call is connected to that port.

4.5.3 Outgoing POTS Calls

Outgoing calls are initiated when a POTS port goes off-hook. An ISDN SETUP message is sent to the network with the Bearer Capability Information Element set to 'Speech'. The dial tone presented by the network on that ISDN B-channel which was selected by channel mapping (See Section 4.3.6), will be routed to the POTS port initiating the call.

When DTMF tones are received from the POTS port, they are sent to the network either as Called Party Number or Keypad Information Elements. Keypad Information Elements are discussed in Section 4.5.1.

Receipt of a valid DTMF tone will prompt its conversion to IA5 coded digits, as shown in the following table (IA5 hex digits are in brackets). If the first valid digit to be received is a '*' then the configuration mode is entered and subsequent digits will be monitored and saved as indicated in Section 4.4.1. If the first tone received is not a '*' or '#' (See Section 4.5.1) that digit and all subsequent digits will be passed to the network in an INFORMATION message as a Called Party Number Information Element. Digits received before the network has returned the SETUP ACK message are saved. Upon receipt of the SETUP ACK any saved digits will be transmitted.

The DTMF tone mapping is as shown below:

Low Group (Hz)	High Group (Hz)			
	1209	1336	1477	1633
697	1 (31)	2 (32)	3 (33)	A (not used)
770	4 (34)	5 (35)	6 (36)	B (not used)
852	7 (37)	8 (38)	9 (39)	C (not used)
941	* (2A)	0 (30)	# (23)	D (not used)

Once the network has indicated that the full number has been received, no further digits will be sent to the network. All tones and announcements from the network (e.g. ringing, NU, busy etc) and audio (if the call is connected) will be routed to the POTS port initiating the call, until that port goes on-hook.

4.5.4 Connected Calls

Once a call is connected to an analog port, whether it was incoming or outgoing, a port-specific LED indicator pin is set high to indicate that the call is connected. See Section 4.7.1 for details of the LED indicator pins. Once the call is disconnected, either by receipt of a DISCONNECT message from the network or an on-hook indication, the ports' LED indicator pin is set low.

During a call, if a Recall (i.e. a line break of appropriate length) is received from a POTS port, the CMX208 will start to look for DTMF tones received on that POTS port. Any tones received will then be sent to the network in ISDN INFORMATION messages, as Keypad Information Elements.

4.5.5 Call Clearing

The call is cleared either by the port going on-hook or by the ISDN network. Note that the ISDN B-channel, which was being used, is not released until the POTS port, which was in use, has gone on-hook.

4.6 Application Programmer's Interface

Details of this will be supplied to customers under a Non-Disclosure Agreement.

The following Memory Map indicates the main code areas used on the CMX208:

Function	Start Hex Address	End Hex Address
Code Space	000 000	01F FFF
External RAM	020 000	03F FFF
API area	0C0 000	0EF FFF
AMD79C30 ISDN Interface Chip	0F0 000	0F0 0FF
PSB21525 HDLC Driver Chip	0F0 100	0F0 1FF
Reserved	0F0 200	0FF FFF

4.7 Hardware Description

4.7.1 LED Status Indicators (LED1 to LED9, and ILFI)

LED1 (HK1)	is low when analog port 1 is off-hook, high when on-hook.
LED2 (HK2)	is low when analog port 2 is off-hook, high when on-hook.
LED4 (CN2)	is high when analog port 2 is connected to the ISDN network, low when not connected.
LED8 (AR)	is pulsed high and low until the ISDN line is activated, when it remains low constantly.
LED9 (CN1)	is high when analog port 1 is connected to the ISDN network, low when not connected.
ILFI	is high when an ISDN Link Failure is Indicated, low when the link is operational.

The functions of the LED and ILFI indicators are set out in the table below:

Pin No.	Designation	POTS port 1	POTS port 2
12	LED1	Off-Hook	~
13	LED2	~	Off-Hook
15	LED4	~	Call Connected
19	LED8	ISDN Line Activated	ISDN Line Activated
21	LED9	Call Connected	~
54	ILFI	ISDN Line Failure Indicator	ISDN Line Failure Indicator

5. Application Notes

5.1 General

The CMX208 is intended for use as part of an ISDN chipset. The MX-COM recommended hardware implementation contains the following elements (refer to Figure 3):

- 'S' bus interface via RJ45 socket.
- RJ11 analog telephone sockets and analog circuitry.
- ISDN line transformer.
- AMD79C30 S-interface controller.
- Auxiliary Motorola MC145480 PCM codec.
- 64K bytes external RAM.
- 16K Non-volatile memory.
- Six processor controlled LED indicator signals.
- HDLC drivers for the 2 ISDN B-channels, both channels can be used for data transfer.

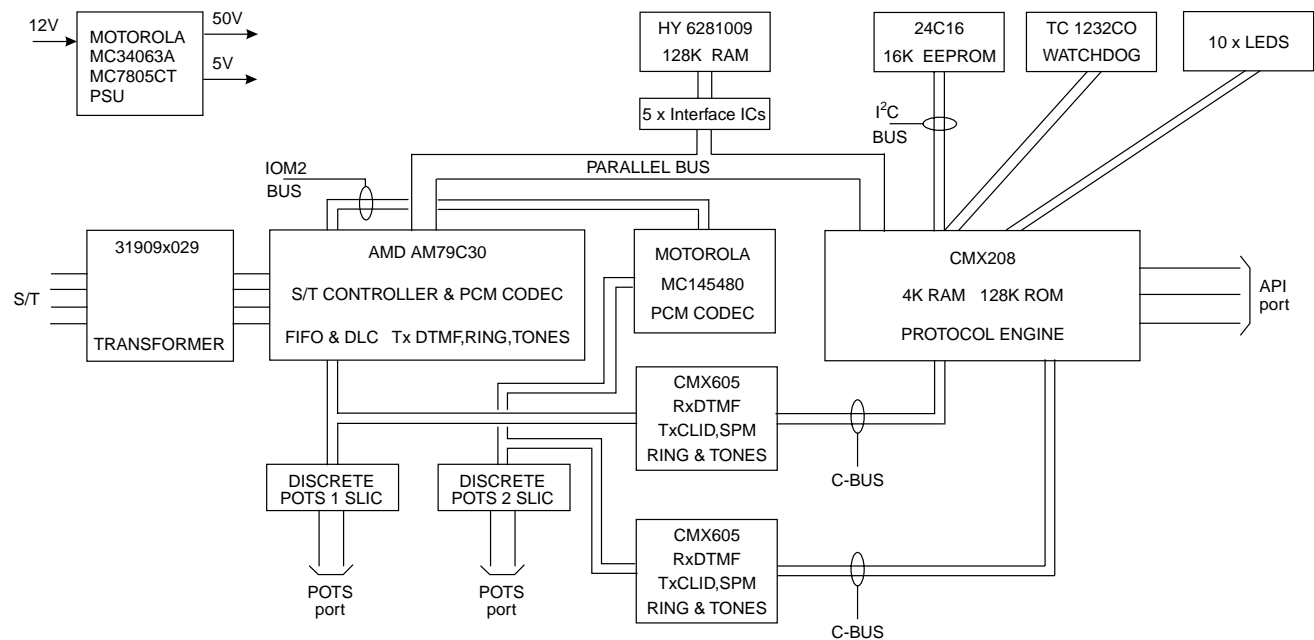


Figure 3: Application Block Diagram

5.2 Approvals

The firmware and finite state machine embedded in the CMX208 has been designed into products that have gained ETSI CTR3 approval.

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply ($AV_{DD} - AV_{SS}$), ($DV_{DD0} - DV_{SS0}$), ($DV_{DD1} - DV_{SS1}$)	-0.3	7.0	V
Voltage on any pin to AV_{SS} , DV_{SS0} or DV_{SS1}	-0.3	$V_{DD} + 0.3$	V
Current into or out of any V_{DD} or V_{SS} pin	-30	100	mA
Current into or out of any other pin	-20	10	mA
S1 Package (QFP)			
Total Allowable Power Dissipation at $T_{AMB} = 25^{\circ}\text{C}$		1300	mW
Derating above 25°C		17	mW/ $^{\circ}\text{C}$ above 25°C
Storage Temperature	-55	125	$^{\circ}\text{C}$
Operating Temperature	-40	85	$^{\circ}\text{C}$

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply: ($AV_{DD} - AV_{SS}$), ($DV_{DD0} - DV_{SS0}$), and ($DV_{DD1} - DV_{SS1}$)		2.7	5.5	V
Operating Temperature		-40	85	$^{\circ}\text{C}$
32 MHz Xtal Frequency Tolerance		-100	100	ppm

6.1.3 Operating Characteristics

Details in this section represent design target values and are not currently guaranteed.

For the following conditions unless otherwise specified:

Xtal Frequency = 32MHz \pm 100ppm, AV_{DD} = DV_{DD0} = DV_{DD1} = 3.0V to 5.0V, T_{AMB} = - 40°C to +85°C.

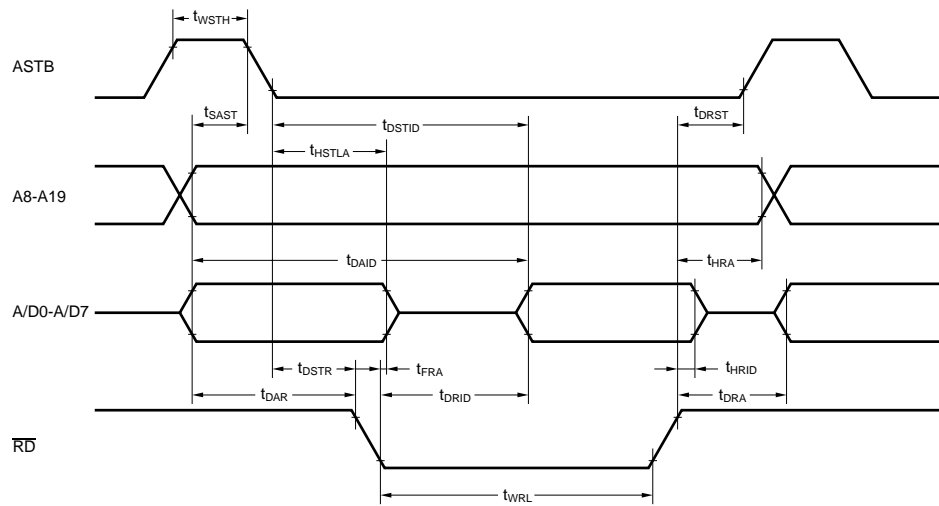
	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I _{DD} (total, operational)	1		25.0	45.0	mA
I _{DD} (total in HALT mode)	1		13.0	26.0	mA
I _{DD} (total in IDLE mode)	1			12.0	mA
Digital Interface					
Input logic "1" level		70%			V _{DD}
Input logic "0" level				30%	V _{DD}
Input leakage current (V _{IN} = 0 to DV _{DD})		-10.0		+10.0	μ A
Output logic "1" level (I _{OH} = 120 μ A)		V _{DD} -1.0		-	V
Output logic "0" level (I _{OL} = 360 μ A)				400	mV
Input or Output leakage current (V _{OUT} = V _{DD})				10	μ A
Xtal/Clock Input					
'High' pulse width (t _{WXH})	2	10		125	ns
'Low' pulse width (t _{WXL})	2	10		125	ns
Risetime (t _{XR})	2			10	ns
Falltime (t _{XF})	2			10	ns
Period (t _{CYK})	2, 3	31.2468		31.2531	ns

Notes:

1. Not including any current drawn by external circuitry.
2. Timing for an external input to the XTAL pin.
3. A fundamental cut crystal is recommended.

6.1.3.1 Timing Diagrams

(1) Read Operation



(2) Write Operation

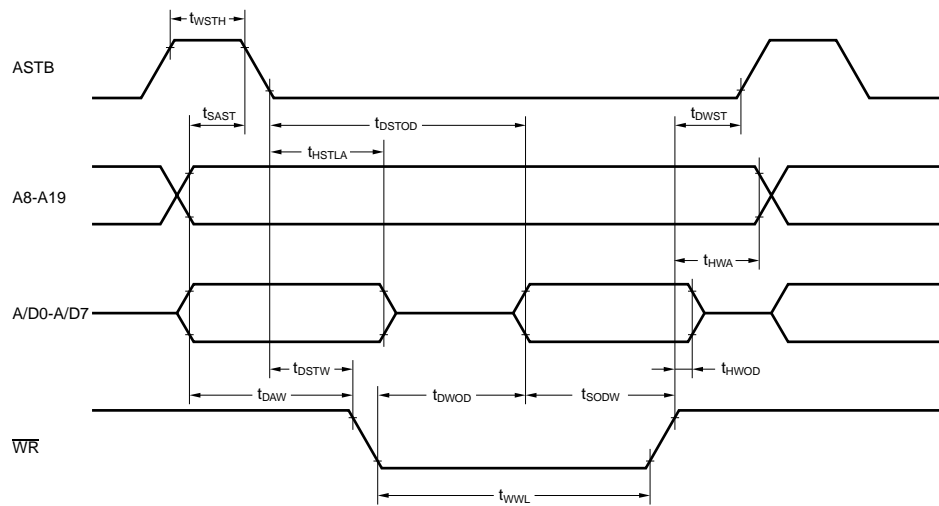
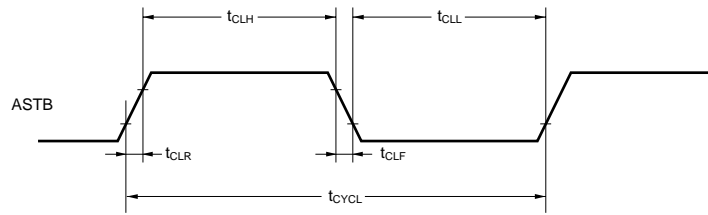
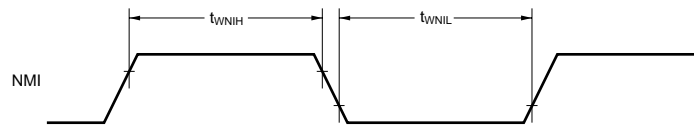


Figure 4: External Memory Access Timing

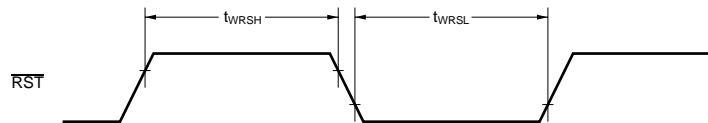
CLOCK OUTPUT TIMING



INTERRUPT INPUT TIMING



RESET INPUT TIMING



EXTERNAL CLOCK TIMING

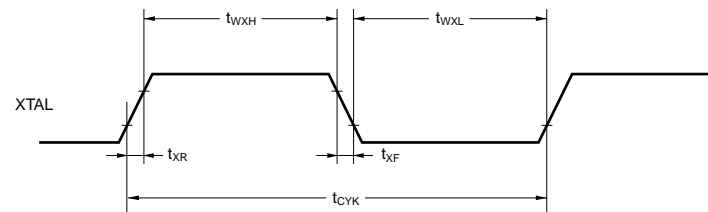


Figure 5: Miscellaneous Timing

6.1.3.2 AC Timing Parameters

For the following conditions unless otherwise specified:

Xtal Frequency = 32MHz, $V_{DD} = DV_{DD0} = DV_{DD1} = 3.0V$ to $5.0V$, $T_{AMB} = -40^{\circ}C$ to $+85^{\circ}C$.

6.1.3.2.1 Read/Write Operation

Where: $T = t_{CYK}$ (system clock cycle time)
 $a = 1$ (during address wait), otherwise, 0
 $n =$ Number of wait states ($n = 2$)

Parameter	Symbol	Conditions	Min.	Max.	Units
Address setup time	t_{SAST}	$V_{DD} = +5.0V \pm 10\%$	$(0.5 + a) T - 15$ $(0.5 + a) T - 31$		ns ns
ASTB high-level width	t_{WSTH}	$V_{DD} = +5.0 V \pm 10\%$	$(0.5 + a) T - 17$ $(0.5 + a) T - 40$		ns ns
Address hold time to (ASTB \downarrow)	t_{HSTLA}	$V_{DD} = +5.0 V \pm 10\%$	0.5T - 24 0.5T - 34		ns ns
Address hold time (to $\overline{RD} \uparrow$)	t_{HRA}		0.5T - 14		ns
Delay from address to $\overline{RD} \downarrow$	t_{DAR}	$V_{DD} = +5.0V \pm 10\%$	$(1 + a) T - 9$ $(1 + a) T - 15$		ns ns
Address float time (to $\overline{RD} \downarrow$)	t_{FRA}			0	ns
Delay from address to data input	t_{DAID}	$V_{DD} = +5.0V \pm 10\%$		$(2.5 + a + n) T - 37$ $(2.5 + a + n) T - 52$	ns ns
Delay from ASTB \downarrow to data input	t_{DSTID}	$V_{DD} = +5.0V \pm 10\%$		$(2 + n) T - 40$ $(2 + n) T - 60$	ns ns
Delay from $\overline{RD} \downarrow$ to data input	t_{DRID}	$V_{DD} = +5.0 V \pm 10\%$		$(1.5 + n) T - 50$ $(1.5 + n) T - 70$	ns ns
Delay from ASTB \downarrow to $\overline{RD} \downarrow$	t_{DSTR}		0.5T - 9		ns
Data hold time (to $\overline{RD} \uparrow$)	t_{HRID}		0		ns
Delay from $\overline{RD} \uparrow$ to address active	t_{DRA}	$V_{DD} = +5.0 V \pm 10\%$ After program is read After program is read $V_{DD} = +5.0 V \pm 10\%$ After data is read After data is read	0.5T - 8 0.5T - 12 1.5T - 8 1.5T - 12		ns ns ns ns
Delay from $\overline{RD} \uparrow$ to ASTB \uparrow	t_{DRST}		0.5T - 17		ns
\overline{RD} low-level width	t_{WRL}	$V_{DD} = 5.0 V \pm 10\%$	$(1.5 + n) T - 30$ $(1.5 + n) T - 40$		ns ns
Address hold time (to $\overline{WR} \uparrow$)	t_{HWA}		0.5T - 14		ns
Delay from address to $\overline{WR} \downarrow$	t_{DAW}	$V_{DD} = +5.0V \pm 10\%$	$(1 + a) T - 5$ $(1 + a) T - 15$		ns ns
Delay from ASTB \downarrow to data output	t_{DSTOD}	$V_{DD} = +5.0V \pm 10\%$		0.5T + 19 0.5T + 35	ns ns
Delay from $\overline{WR} \downarrow$ to data output	t_{DWOD}			0.5T - 11	ns
Delay from ASTB \downarrow to $\overline{WR} \downarrow$	t_{DSTW}		0.5T - 9		ns
Data setup time (to $\overline{WR} \uparrow$)	t_{SODW}	$V_{DD} = +5.0 V \pm 10\%$	$(1.5 + n) T - 30$ $(1.5 + n) T - 40$		ns ns
Data hold time (to $\overline{WR} \uparrow$) ^{Note 1}	t_{HWOD}	$V_{DD} = +5.0V \pm 10\%$	0.5T - 5 0.5T - 25		ns ns
Delay from $\overline{WR} \uparrow$ to ASTB \uparrow	t_{DWST}		0.5T - 12		ns
\overline{WR} low-level width	t_{WWL}	$V_{DD} = +5.0V \pm 10\%$	$(1.5 + n) T - 30$ $(1.5 + n) T - 40$		ns ns

Note 1: Hold time includes the time during which V_{OH1} and V_{OL1} are held under the load conditions of $C_L = 50$ pF and $R_L = 4.7$ k Ω .

6.1.3.2.2 Miscellaneous timing

Where: $T = t_{CYK}$ (system clock cycle time)
 $a = 1$ (during address wait), otherwise, 0.
 $n =$ Number of wait states ($n = 2$)

Parameter	Symbol	Conditions	Min.	Max.	Units
ASTB cycle time	t_{CYCL}		nT		ns
ASTB low-level width	t_{CLL}	$V_{DD} = +5.0 V \pm 10\%$	$0.5 t_{CYCL} - 10$ $0.5 t_{CYCL} - 20$		ns ns
ASTB high-level width	t_{CLH}	$V_{DD} = +5.0 V \pm 10\%$	$0.5 t_{CYCL} - 10$ $0.5 t_{CYCL} - 20$		ns ns
ASTB rise time	t_{CLR}	$V_{DD} = +5.0 V \pm 10\%$		10 20	ns ns
ASTB fall time	t_{CLF}	$V_{DD} = +5.0 V \pm 10\%$		10 20	ns ns
NMI low-level width	t_{WNIL}		10		μ s
NMI high-level width	t_{WNIH}		10		μ s
\overline{RST} low-level width	t_{WRSL}		10		μ s
\overline{RST} high-level width	t_{WRSH}		10		μ s

6.2 Packaging

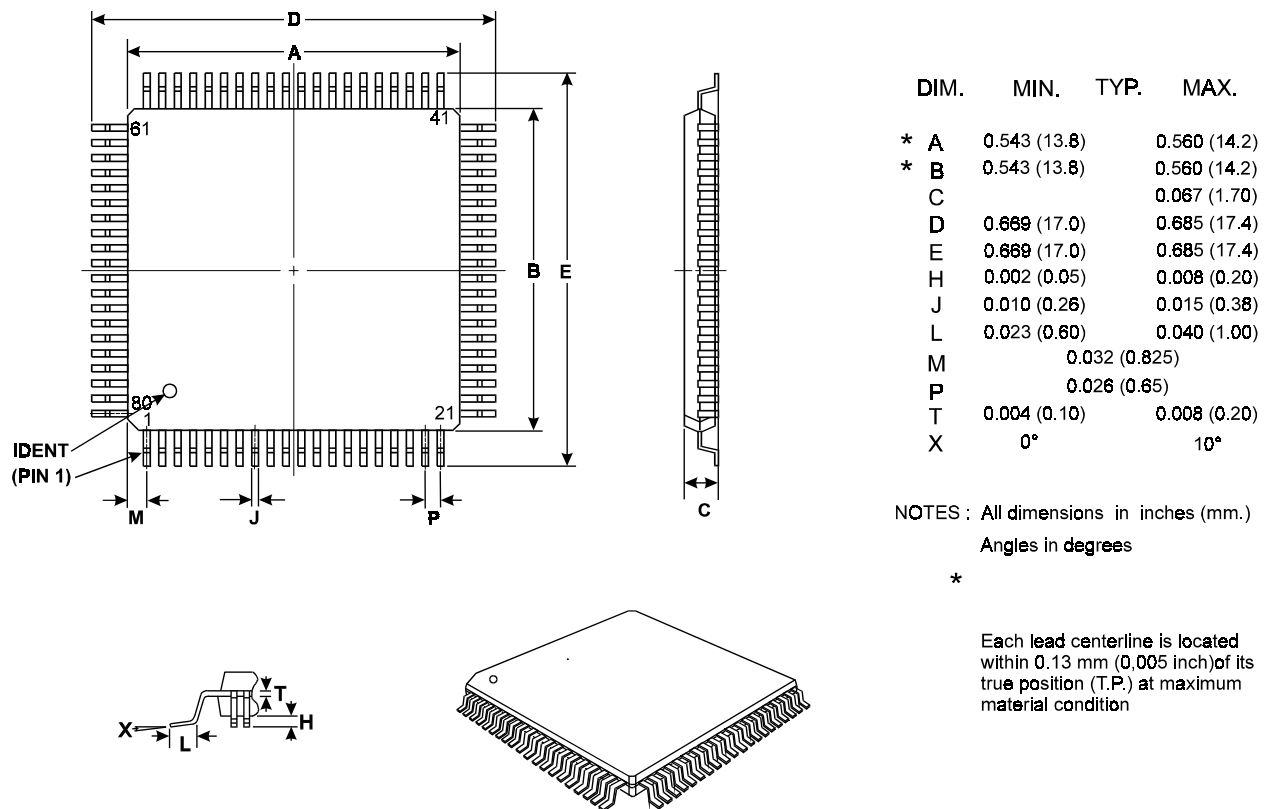


Figure 6: 80-pin QFP Mechanical Outline: Order as part no. CMX208S1