PROCESS CP188

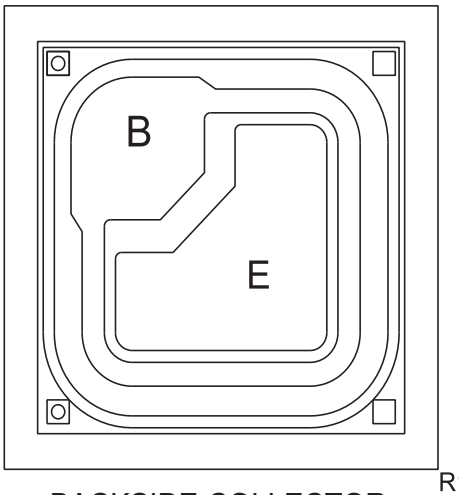
Small Signal Transistor

NPN - Low Noise Amplifier Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	14.6 x 14.6 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	3.9 x 3.9 MILS
Emitter Bonding Pad Area	5.5 x 5.5 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au-As - 18,000Å

GEOMETRY



R1

BACKSIDE COLLECTOR

GROSS DIE PER 4 INCH WAFER

54,599

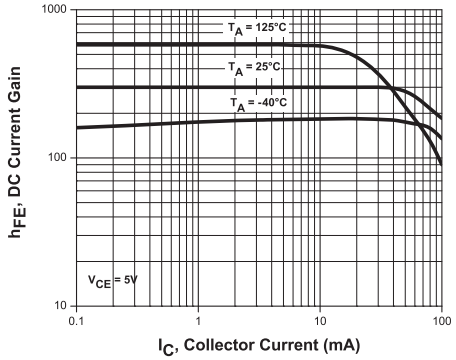
PRINCIPAL DEVICE TYPES

CMPT2484
CMPT5088
CMPT5089
CMPT6428
CMPT6429
2N2484

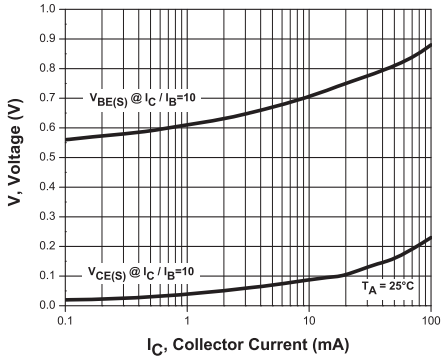
PROCESS CP188

Typical Electrical Characteristics

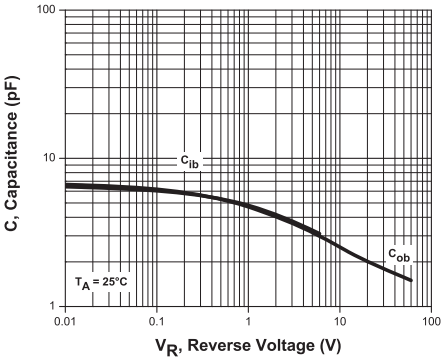
DC Current Gain



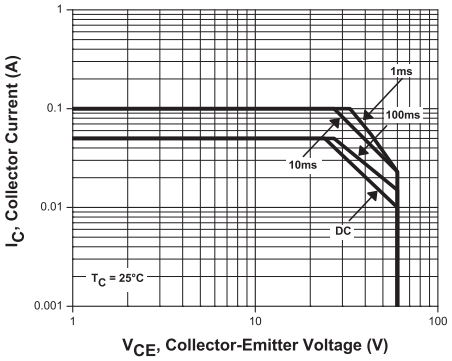
"ON" Voltage



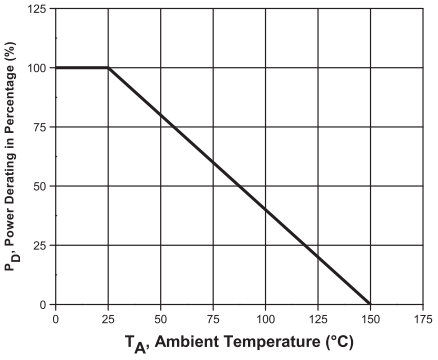
Capacitance



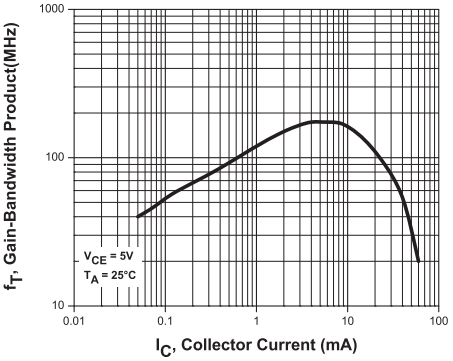
Safe Operating Area



Normalized Power Derating



Current Gain-Bandwidth Product



R5 (22-March 2010)