PROCESS CP309

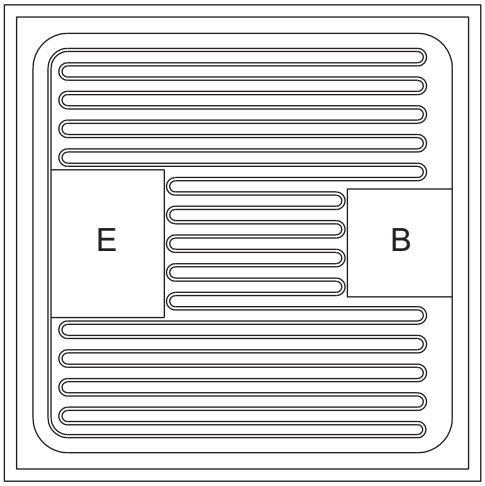
Power Transistor

NPN - Low Saturation Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	41.3 x 41.3 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	9.4 x 9.2 MILS
Emitter Bonding Pad Area	12.8 x 10.2 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Ag - 12,000Å

GEOMETRY



BACKSIDE COLLECTOR R1

GROSS DIE PER 4 INCH WAFER

6,285

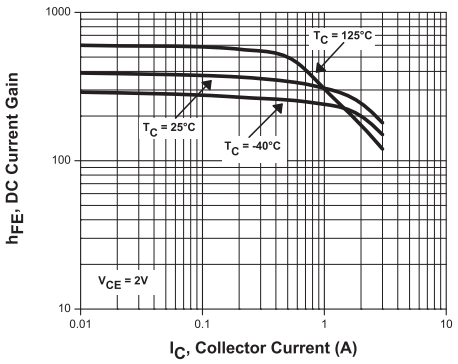
PRINCIPAL DEVICE TYPES

CMPT3090L
CXT3090L
CZT3090L
CMXT3090L

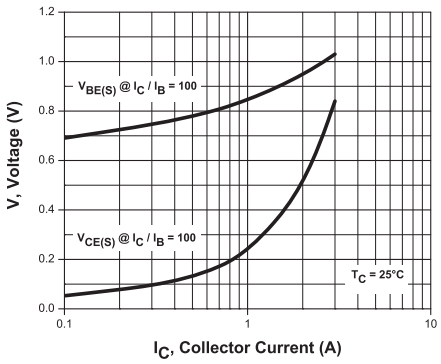
PROCESS CP309

Typical Electrical Characteristics

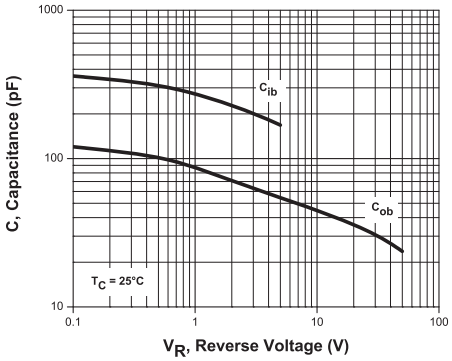
DC Current Gain



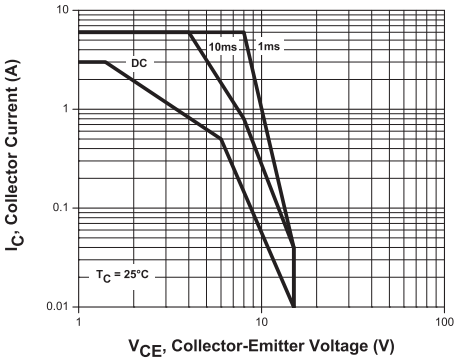
"ON" Voltage



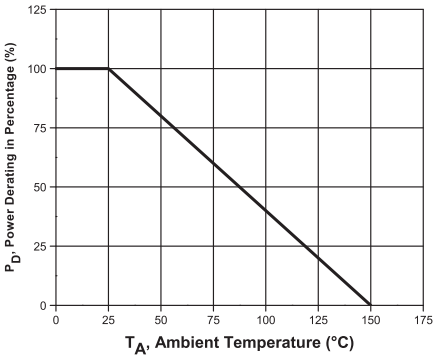
Capacitance



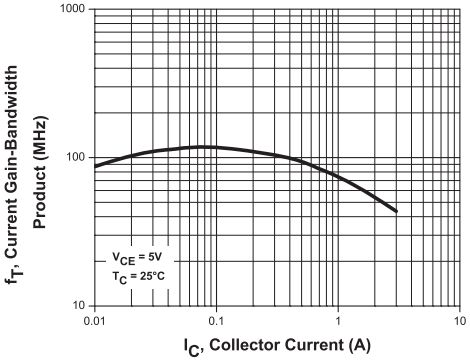
Safe Operating Area



Normalized Power Derating



Current Gain-Bandwidth Product



R4 (22-March 2010)