PROCESS CP318V

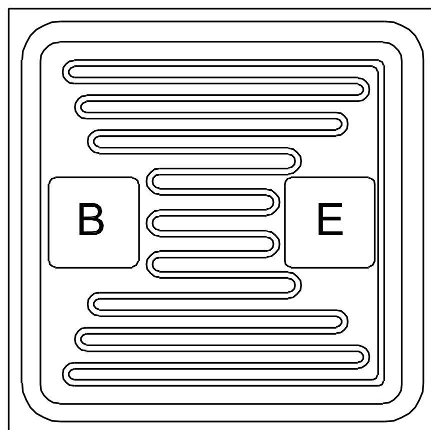
Small Signal Transistor

NPN - High Voltage Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	26 x 26 MILS
Die Thickness	7.1 MILS ± 0.6 MILS
Base Bonding Pad Area	5.5 x 5.5 MILS
Emitter Bonding Pad Area	5.5 x 5.5 MILS
Top Side Metalization	Al-Si - 17,000Å
Back Side Metalization	Au - 12,000Å

GEOMETRY



R0

BACKSIDE COLLECTOR

GROSS DIE PER 4 INCH WAFER

25,536

PRINCIPAL DEVICE TYPES

MPS455

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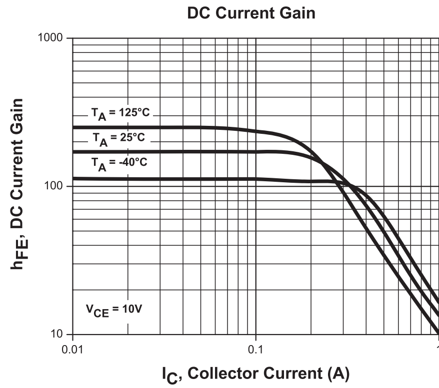
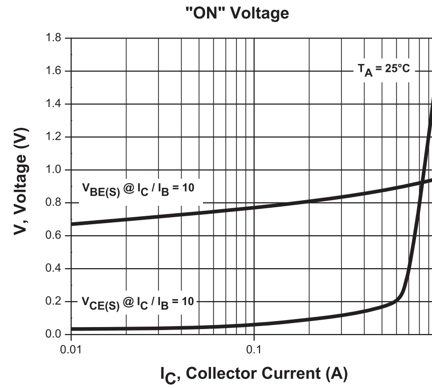
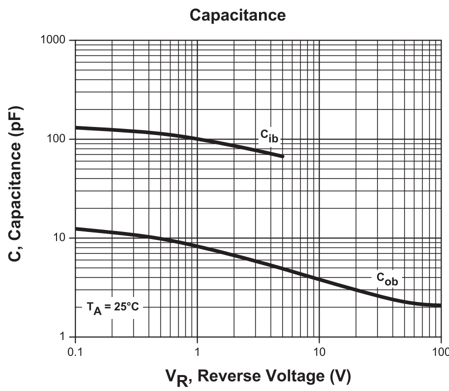
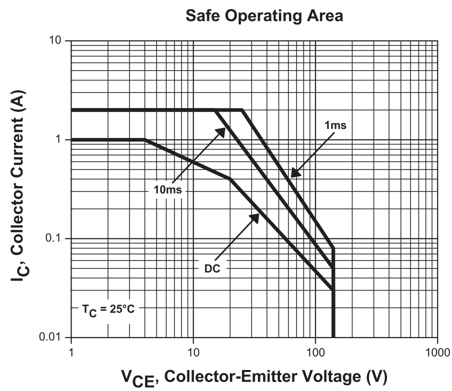
PROCESS CP318V

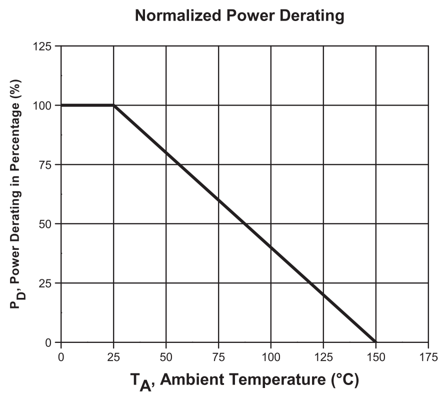
Typical Electrical Characteristics

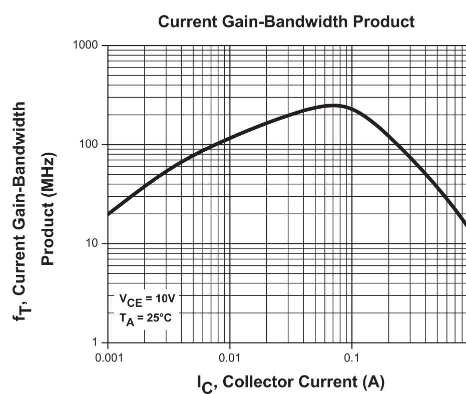












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