PROCESS CP319

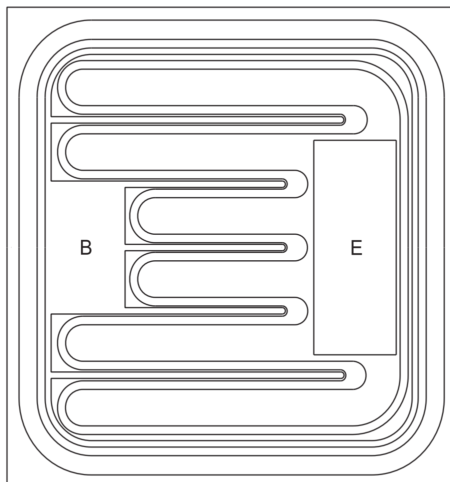
Power Transistor

NPN - Silicon Power Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	87 x 87 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	24 x 15 MILS
Emitter Bonding Pad Area	38 x 16 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Ti/Ni/Ag - 11,000Å

GEOMETRY



BACKSIDE COLLECTOR R0

GROSS DIE PER 4 INCH WAFER
1,462

PRINCIPAL DEVICE TYPES
CZTA44HC
TIP47
TIP48
TIP50

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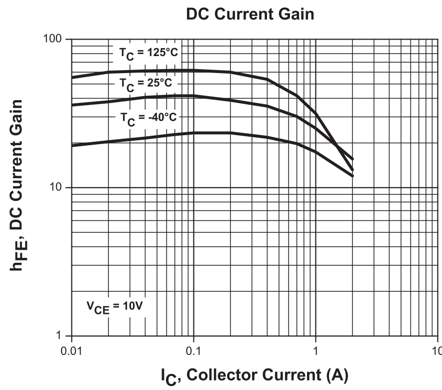
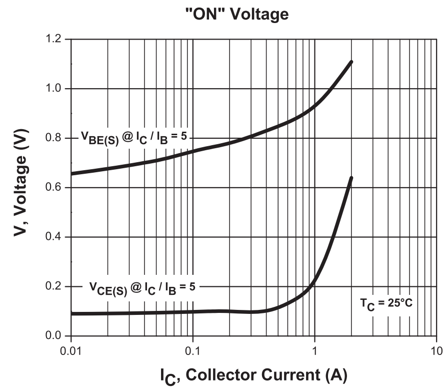
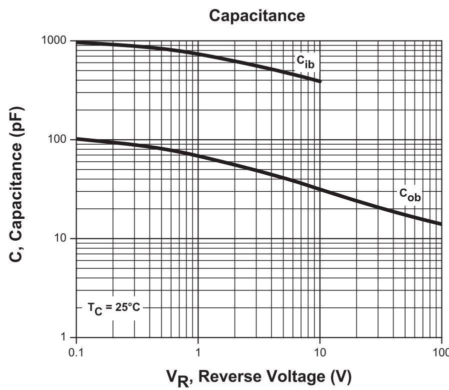
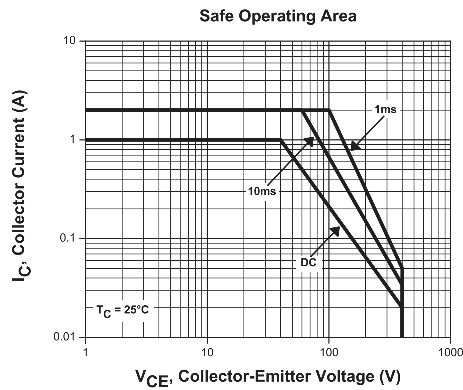
PROCESS CP319

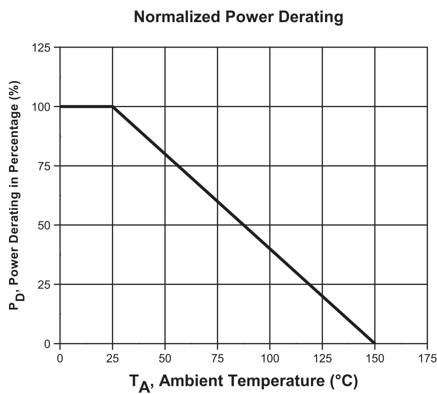
Typical Electrical Characteristics

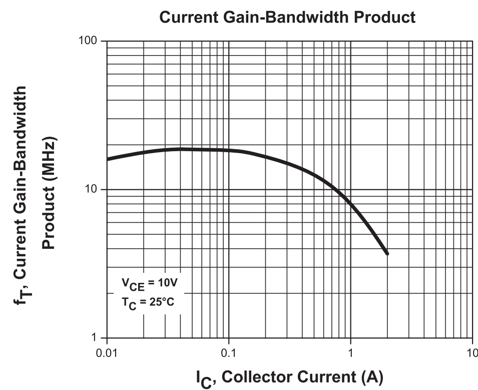












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