PROCESS CP348

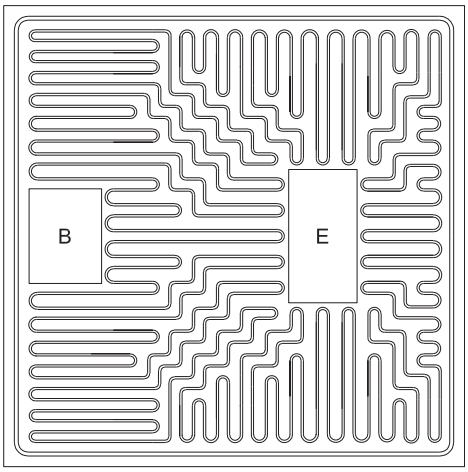
Power Transistor

NPN - High Current Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	82 x 82 MILS
Die Thickness	9.1 MILS
Base Bonding Pad Area	13 x 17 MILS
Emitter Bonding Pad Area	13 x 25 MILS
Top Side Metalization	Al-Si - 40,000Å
Back Side Metalization	Ti/Ni/Ag - 2,000Å/3,000Å/20,000Å

GEOMETRY



BACKSIDE COLLECTOR R0

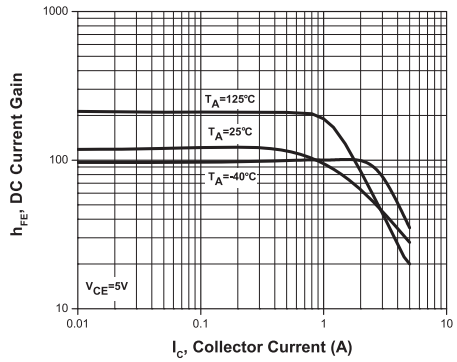
GROSS DIE PER 5 INCH WAFER
2,449

PRINCIPAL DEVICE TYPE
BUY48

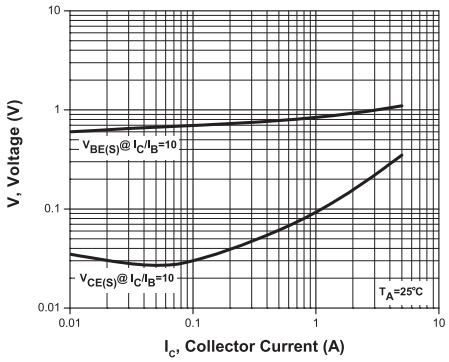
PROCESS CP348

Typical Electrical Characteristics

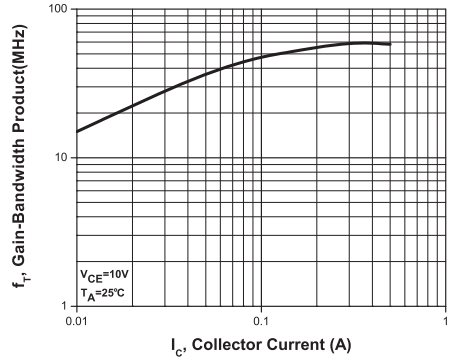
DC Current Gain



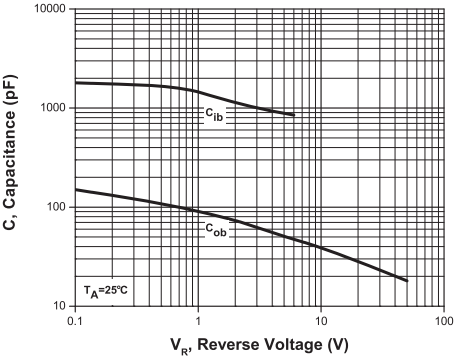
"ON" Voltage



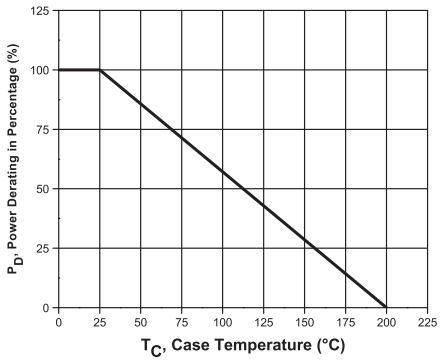
Current Gain-Bandwidth Product



Capacitance



Normalized Power Derating



R2 (1-June 2012)