PROCESS CP588

Small Signal Transistor

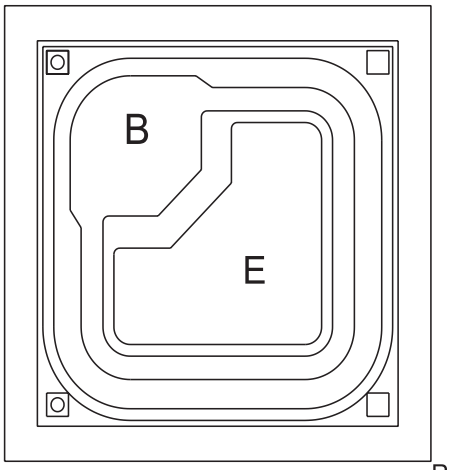
PNP - Low Noise Amplifier Transistor Chip

Central™ Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	15 x 15 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	4.0 x 4.0 MILS
Emitter Bonding Pad Area	5.5 x 5.5 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



BACKSIDE COLLECTOR

R1

GROSS DIE PER 4 INCH WAFER

53,730

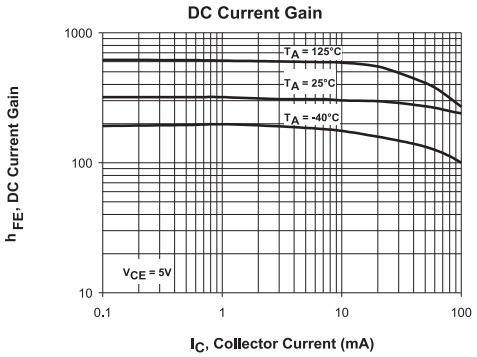
PRINCIPAL DEVICE TYPES

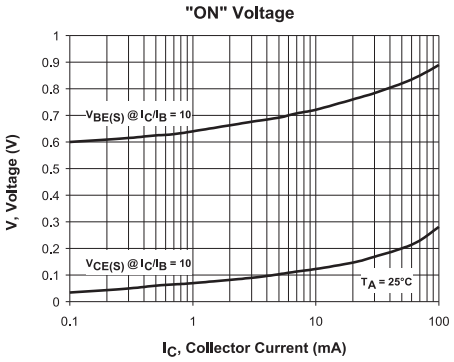
2N2605
2N3799
PN4250A
CMPT5086
CMPT5087

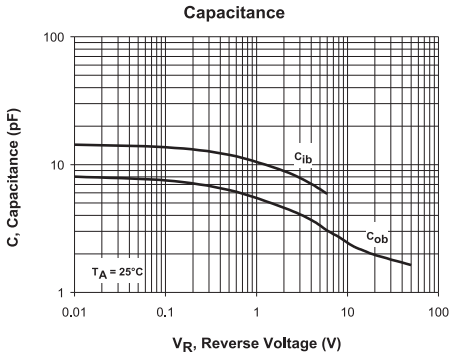
145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

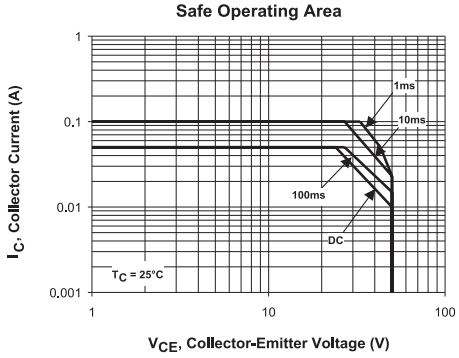
R2 (1-August 2002)

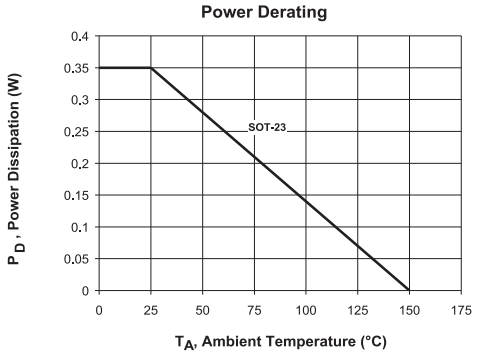
Typical Electrical Characteristics

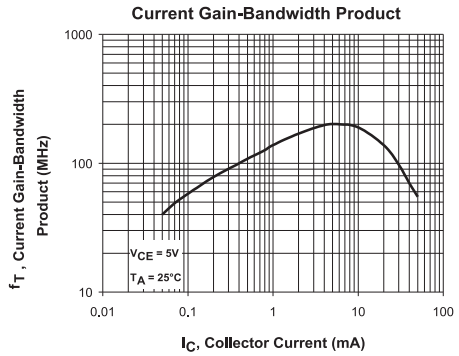












145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com