PROCESS CP588V

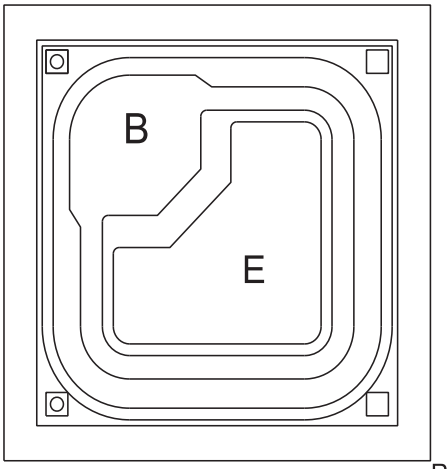
Small Signal Transistor

PNP - Low Noise Amplifier Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	14.6 x 14.6 MILS
Die Thickness	7.1 MILS
Base Bonding Pad Area	3.9 x 3.9 MILS
Emitter Bonding Pad Area	5.5 x 5.5 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



BACKSIDE COLLECTOR

R1

GROSS DIE PER 4 INCH WAFER

54,599

PRINCIPAL DEVICE TYPES

2N2605
2N3799
PN4250A
CMPT5086
CMPT5087

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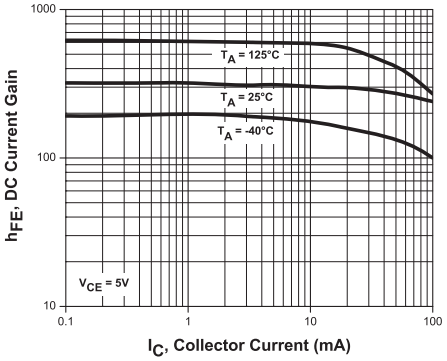
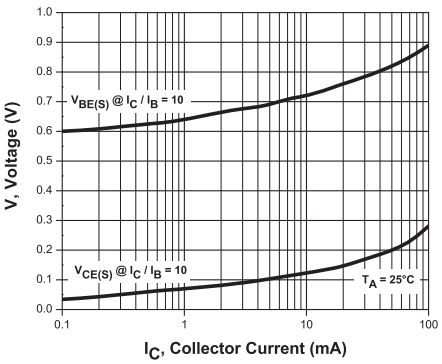
PROCESS CP588V

Typical Electrical Characteristics

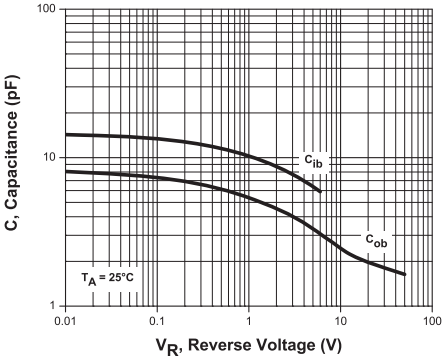
DC Current Gain



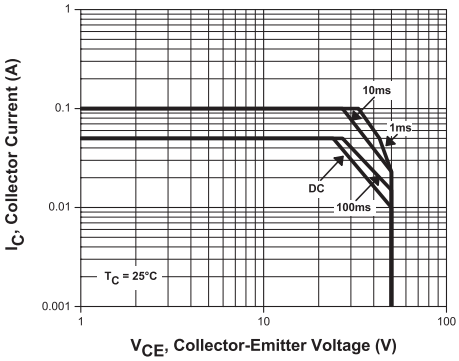
"ON" Voltage



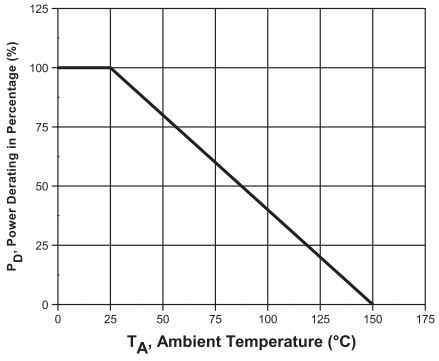
Capacitance



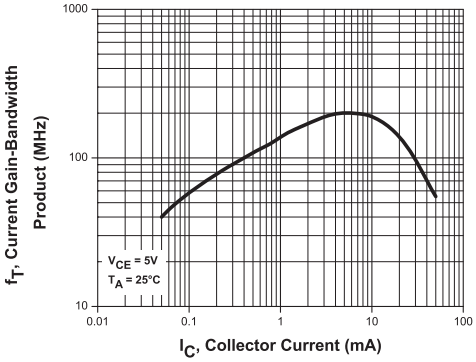
Safe Operating Area



Normalized Power Derating



Current Gain-Bandwidth Product



R2 (22-March 2010)