SONY

CXD3519TQ

Reference Voltage and Driver IC for LCD

Description

The CXD3519TQ is suitable IC for applying reference voltage for gamma correction which is necessary for TFT liquid crystal display. This IC has a built-in 9 channels of rail-to-rail buffer circuit which enables 2-input switch and a common driver circuit.

Features

- Built-in 9 channels of rail-to-rail buffer circuit
- Built-in common driver circuit
- Current consumption: 3.6mA (typ.)
- Package: 48-pin TQFP

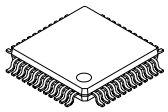
Structure

CMOS IC

Applications

Small liquid crystal monitor

48 pin TQFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

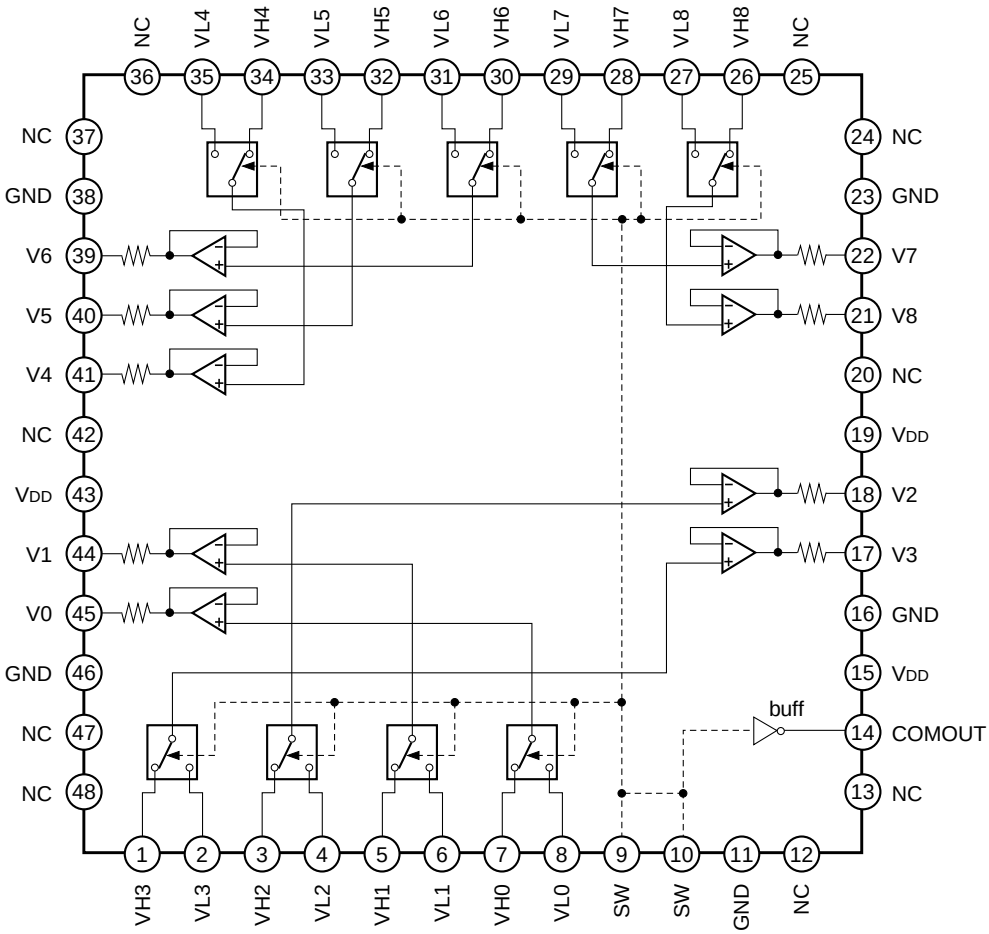
• Supply voltage	V_{DD}	V_{SS} – 0.3 to +6.0	V
• Input pin voltage	V_I	V_{SS} – 0.3 to V_{DD} + 0.3	V
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation (Ta ≤ 85°C)	P_D	220	mW

Operating Conditions

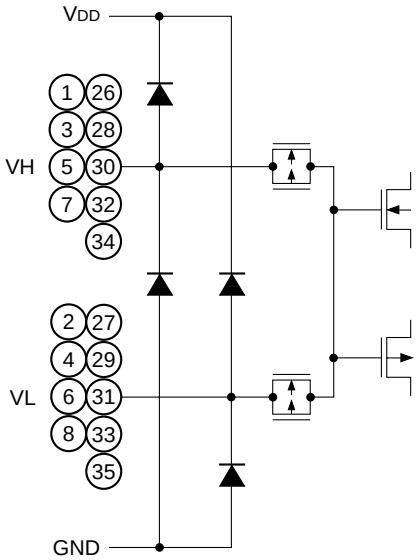
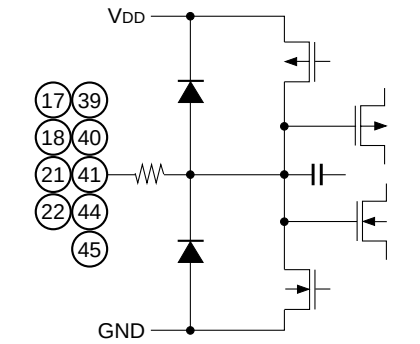
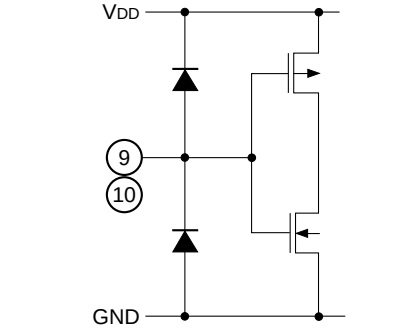
• Supply voltage	V_{DD}	4.5 to 5.5 (5.0 typ.)	V
• Operating temperature	Topr	–35 to +85	°C

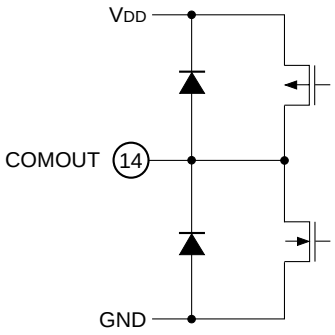
E00Y07-PS

Block Diagram



Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	VH3	0.5 to 4.0V (max.: 2.0Vp-p)		DC input when SW is high.
2	VL3			DC input when SW is low.
3	VH2	0.2 to 4.8V		DC input when SW is high.
4	VL2			DC input when SW is low.
5	VH1			DC input when SW is high.
6	VL1			DC input when SW is low.
7	VH0			DC input when SW is high.
8	VL0			DC input when SW is low.
26	VH8			DC input when SW is high.
27	VL8			DC input when SW is low.
28	VH7			DC input when SW is high.
29	VL7			DC input when SW is low.
30	VH6			DC input when SW is high.
31	VL6			DC input when SW is low.
32	VH5	0.5 to 4.0V (max.: 2.0Vp-p)		DC input when SW is high.
33	VL5			DC input when SW is low.
34	VH4			DC input when SW is high.
35	VL4			DC input when SW is low.
45	V0	0.2 to 4.8V		V0 output.
44	V1			V1 output.
18	V2			V2 output.
39	V6			V6 output.
22	V7			V7 output.
21	V8			V8 output.
17	V3	0.5 to 4.0V		V3 output.
41	V4			V4 output.
40	V5			V5 output.
9	SW			Input switch. For V0 to V8 output, VL is output for low; VH for high. For COMOUT output, VDD level is output for low; GND level for high. Also, Pins 9 and 10 are connected internally. Input the same signal, or input one signal and leave the other signal open.
10	SW			

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
14	COMOUT			COM output.
15	VDD	5.0V		5V power supply.
19	VDD	5.0V		5V power supply.
43	VDD	5.0V		5V power supply.
11	GND			GND.
16	GND			GND.
23	GND			GND.
38	GND			GND.
46	GND			GND.
12	NC			No connected.
13	NC			No connected.
20	NC			No connected.
24	NC			No connected.
25	NC			No connected.
36	NC			No connected.
37	NC			No connected.
42	NC			No connected.
47	NC			No connected.
48	NC			No connected.

Note)

- GND

  Make sure that Pins 11, 16, 23, 38 and 46 are connected to GND potential, and do not release them.
- Decoupling capacitor

  Locate decoupling capacitor connected between power supply and GND as near IC pin as possible.
- Design VH and VL input pins not to have capacity.

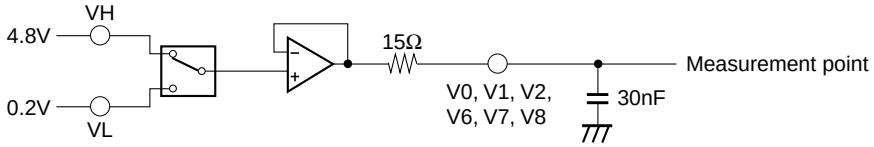
Electrical Characteristics

(Ta = 25°C, V_{DD} = 5V)

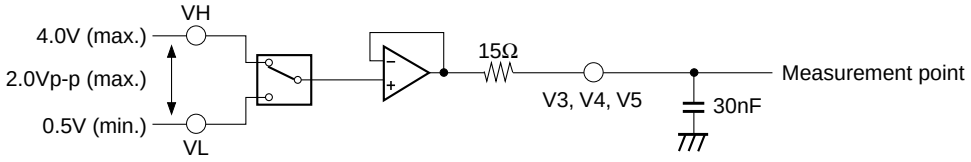
No.	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
1	Current consumption	I_{CC}	Input voltage = 2.5V, No load	—	3.6	6.0	mA
2	VH, VL input current high	I_{IH}	Input voltage = 4.8V	–0.1	—	0.1	µA
3	VH, VL input current low	I_{IL}	Input voltage = 0.2V	–0.1	—	0.1	µA
4	SW input current high	I_{ISH}	Input voltage = 5V	–10	—	10	µA
5	SW input current low	I_{ISL}	Input voltage = 0V	–10	—	10	µA
6	VREF voltage gain	AV	Input voltage = 0.2 to 4.8V	0.985	—	—	V/V
7	SW input voltage high	V_{IH}		2.0	—	—	V
8	SW input voltage low	V_{IL}		—	—	0.8	V
9	VREF output voltage high	V_{OH}	I_{SOURCE} = 10mA	V_{DD} – 1.0	—	—	V
10	VREF output voltage low	V_{OL}	I_{SINK} = 10mA	—	—	GND + 1.0	V
11	COMOUT output voltage high	V_{COH}	I_{SOURCE} = 10mA	V_{DD} – 0.1	—	—	V
12	COMOUT output voltage low	V_{COL}	I_{SINK} = 10mA	—	—	GND + 0.1	V
13	VREF offset voltage	V_{OFF}		—	—	20	mV
14	VREF (V0, 1, 2, 6, 7, 8) load regulation 1	ΔV_O1	Input voltage = 0.2 to 4.8V I_{SOURCE} = 10mA I_{SINK} = 10mA	—	±5	±10	mV
15	VREF (V3, 4, 5) load regulation 2	ΔV_O2	Input voltage = 0.5 to 4.0V I_{SOURCE} = 10mA I_{SINK} = 10mA	—	±7	±14	mV
16	Setting time 1	ts1 ts2	Measurement circuits 1, 2	—	—	10	µs
17	Setting time 2	ts3 ts4	Measurement circuit 3	—	—	6	µs
18	Output impedance	Rimp	V0 – V8	—	15	—	Ω

Measurement Circuits

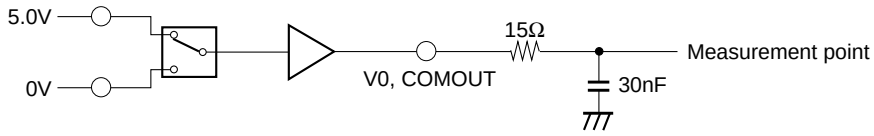
Measurement circuit 1

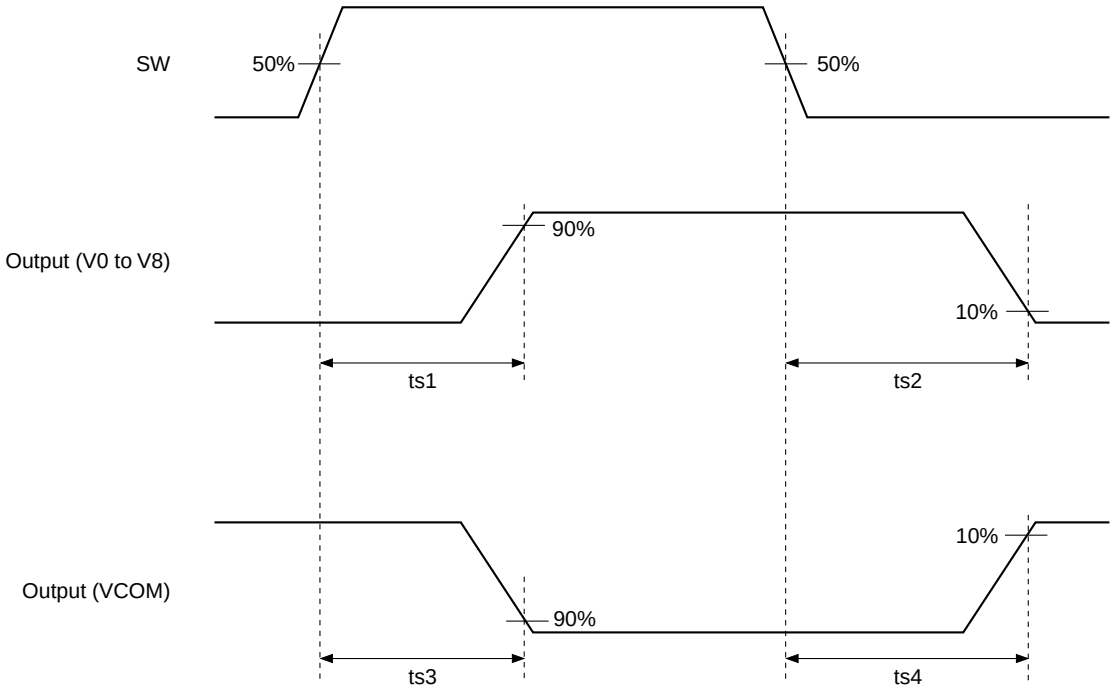


Measurement circuit 2

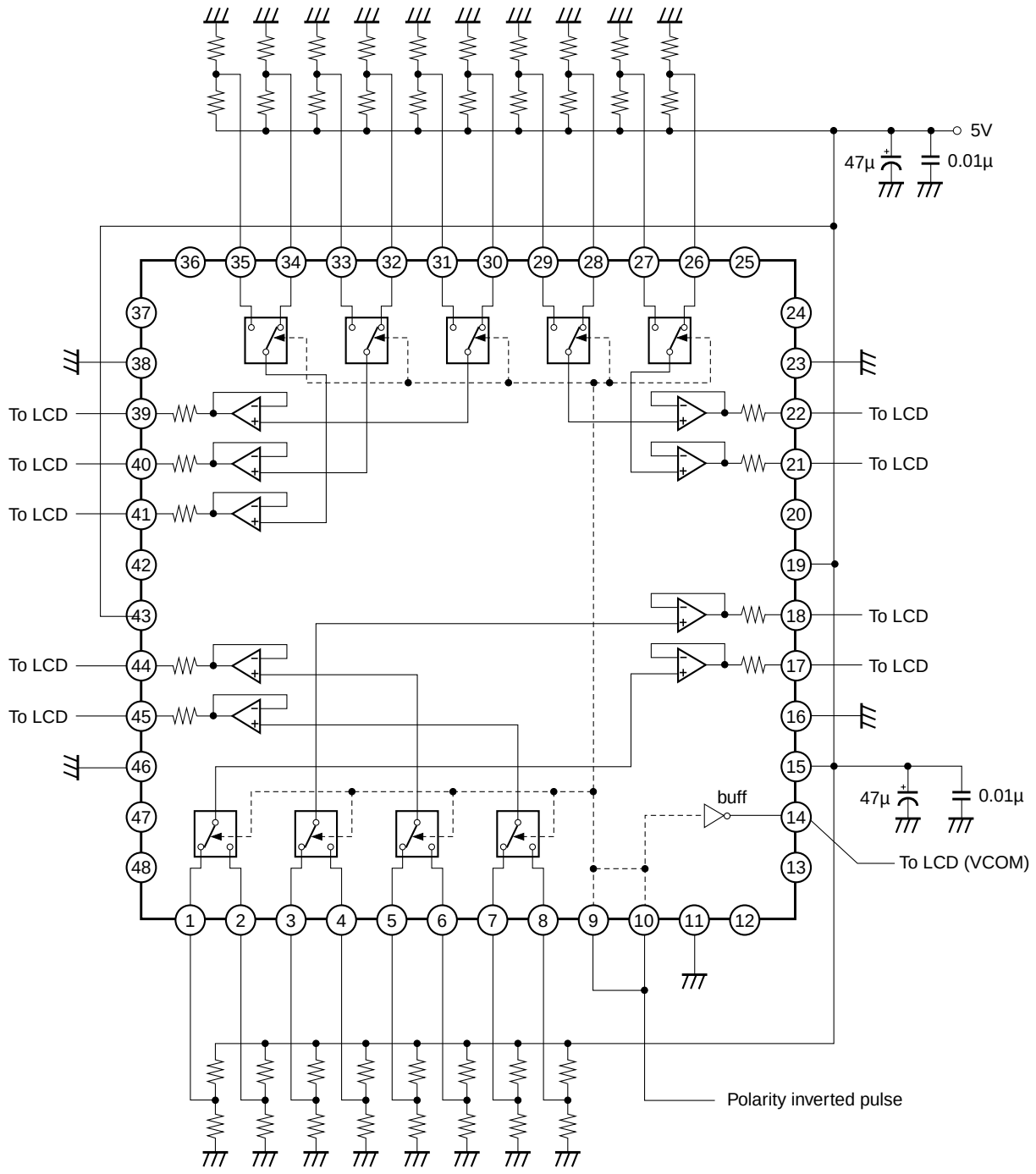


Measurement circuit 3





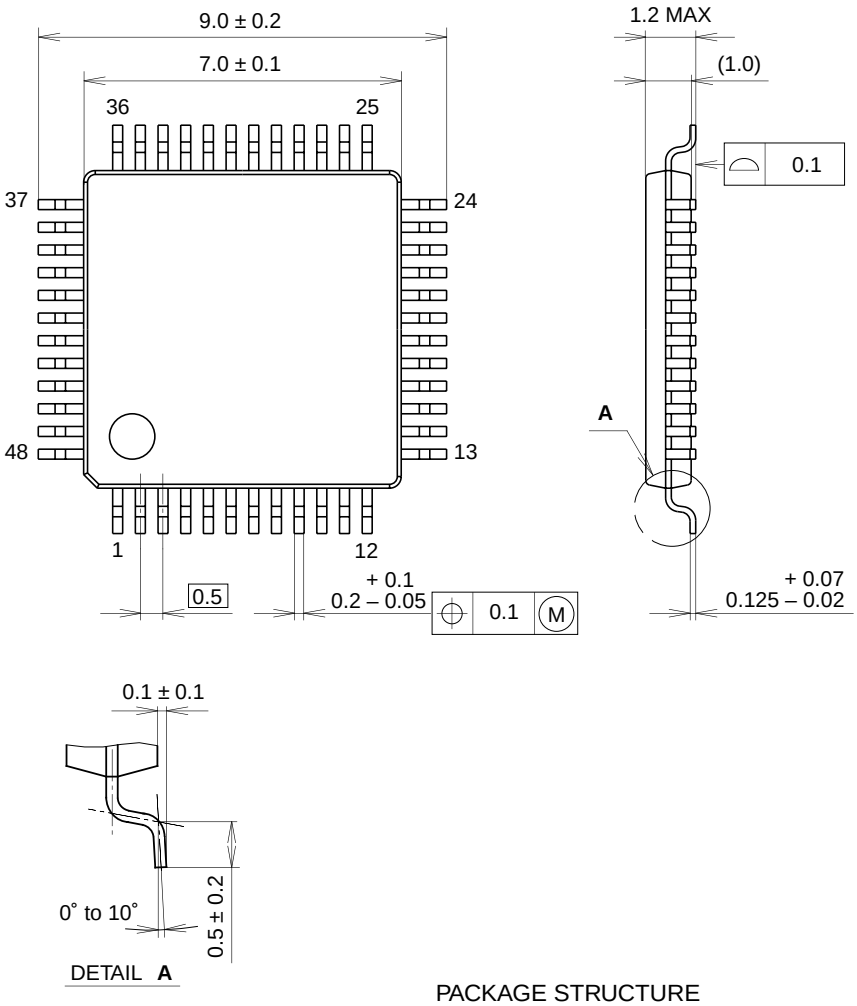
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

48PIN TQFP (PLASTIC)



SONY CODE	TQFP-48P-L061
EIAJ CODE	P-TQFP48-7X7-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	SOLDER PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.15g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
LEAD TREATMENT	Sn-Pb 10%
LEAD TREATMENT THICKNESS	5-18µm