

32K x 8 3.3V Static RAM

Features

- Single 3.3V power supply
- Ideal for low-voltage cache memory applications
- High speed
 - 10/12/15 ns
- Low active power
 - 216 mW (max.)
- Low-power alpha immune 6T cell
- Plastic SOJ and TSOP packaging

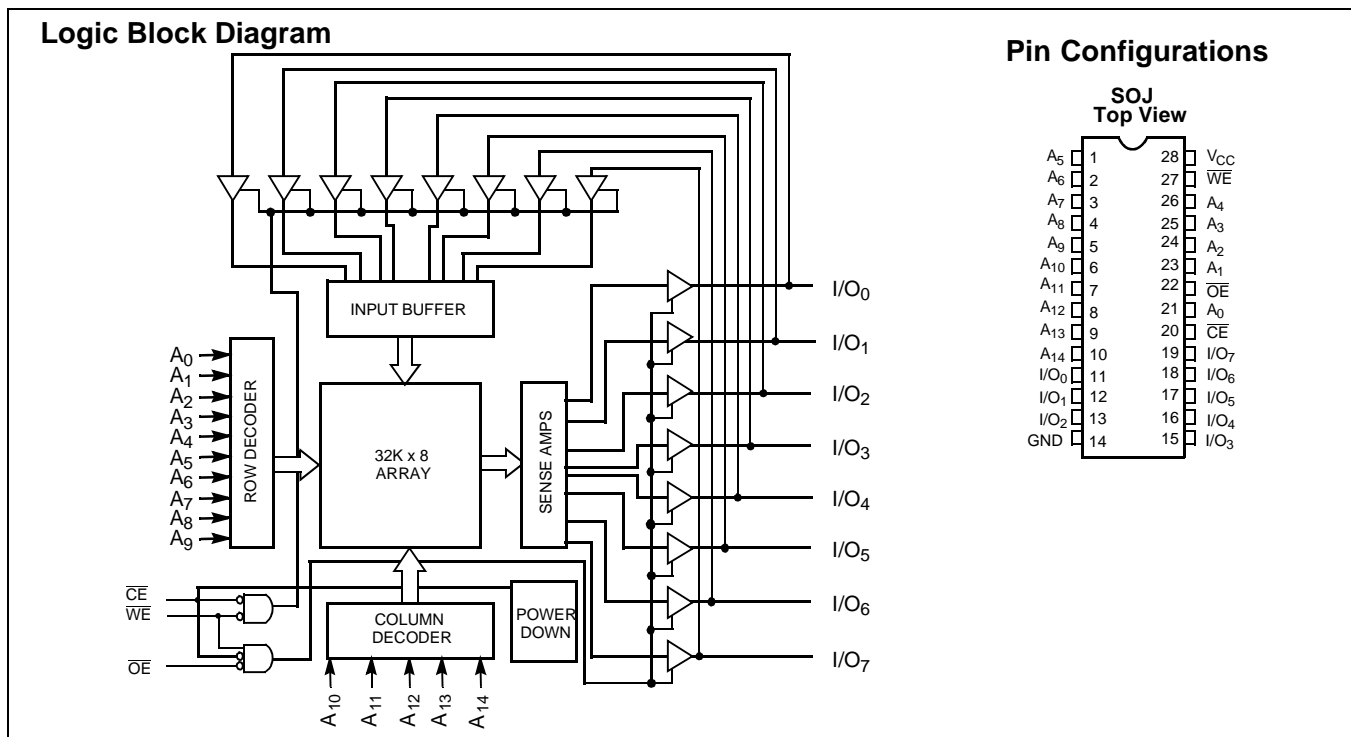
Functional Description^[1]

The CY7C1399B is a high-performance 3.3V CMOS Static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}) and

active LOW Output Enable (\overline{OE}) and three-state drivers. The device has an automatic power-down feature, reducing the power consumption by more than 95% when deselected.

An active LOW Write Enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE} and \overline{WE} inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE} and \overline{OE} active LOW, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and Write Enable (\overline{WE}) is HIGH. The CY7C1399B is available in 28-pin standard 300-mil-wide SOJ and TSOP Type I packages.



Selection Guide

| | 1399B-10 | 1399B-12 | 1399B-15 | 1399B-20 |
|---|----------|----------|----------|----------|
| Maximum Access Time (ns) | 10 | 12 | 15 | 20 |
| Maximum Operating Current (mA) | 60 | 55 | 50 | 45 |
| Maximum CMOS Standby Current (μ A) | | 500 | 500 | 500 |
| | L | 50 | 50 | 50 |

Note:

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

Pin Configuration
**TSOP
Top View**

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[2] -0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State^[2] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[2]..... -0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

| Range | Ambient Temperature | V_{CC} |
|------------|---------------------|--------------|
| Commercial | 0°C to +70°C | 3.3V ±300 mV |
| Industrial | -40°C to +85°C | 3.3V ±300 mV |

Electrical Characteristics Over the Operating Range^[1]

| Parameter | Description | Test Conditions | 7C1399B-10 | | 7C1399B-12 | | Unit |
|-----------|--|--|------------|-----------------|------------|-----------------|------|
| | | | Min. | Max. | Min. | Max. | |
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min.}, I_{OH} = -2.0 \text{ mA}$ | 2.4 | | 2.4 | | V |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min.}, I_{OL} = 4.0 \text{ mA}$ | | 0.4 | | 0.4 | V |
| V_{IH} | Input HIGH Voltage | | 2.2 | $V_{CC} + 0.3V$ | 2.2 | $V_{CC} + 0.3V$ | V |
| V_{IL} | Input LOW Voltage ^[2] | | -0.3 | 0.8 | -0.3 | 0.8 | V |
| I_{IX} | Input Load Current | | -1 | +1 | -1 | +1 | μA |
| I_{OZ} | Output Leakage Current | $GND \leq V_I \leq V_{CC}$, Output Disabled | -5 | +5 | -5 | +5 | μA |
| I_{OS} | Output Short Circuit Current ^[3] | $V_{CC} = \text{Max.}, V_{OUT} = GND$ | | -300 | | -300 | mA |
| I_{CC} | V_{CC} Operating Supply Current | $V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}$, $f = f_{MAX} = 1/t_{RC}$ | | 60 | | 55 | mA |
| I_{SB1} | Automatic CE Power-Down Current — TTL Inputs | Max. V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$, or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$ | | 5 | | 5 | mA |
| | | | L | 4 | | 4 | mA |
| I_{SB2} | Automatic CE Power-Down Current — CMOS Inputs ^[4] | Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, $WE \geq V_{CC} - 0.3V$ or $WE \leq 0.3V$, $f = f_{MAX}$ | | 500 | | 500 | μA |
| | | | L | 50 | | 50 | μA |

Notes:

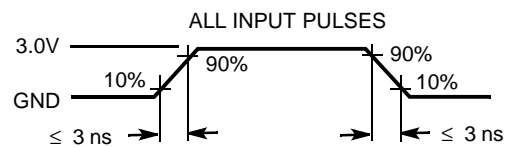
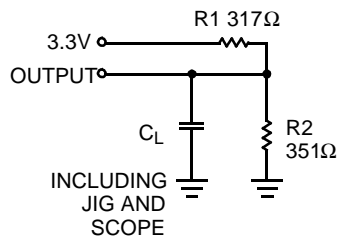
- Minimum voltage is equal to -2.0V for pulse durations of less than 20 ns.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Device draws low standby current regardless of switching on the addresses.

Electrical Characteristics Over the Operating Range (continued)

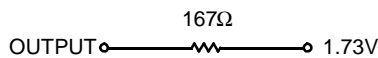
| Parameter | Description | Test Conditions | 1399B-15 | | 1399B-20 | | Unit |
|-----------|--|--|----------|-----------------|----------|-----------------|---------------|
| | | | Min. | Max. | Min. | Max. | |
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min.}, I_{OH} = -2.0 \text{ mA}$ | 2.4 | | 2.4 | | V |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min.}, I_{OL} = 4.0 \text{ mA}$ | | 0.4 | | 0.4 | V |
| V_{IH} | Input HIGH Voltage | | 2.2 | $V_{CC} + 0.3V$ | 2.2 | $V_{CC} + 0.3V$ | V |
| V_{IL} | Input LOW Voltage | | -0.3 | 0.8 | -0.3 | 0.8 | V |
| I_{IX} | Input Load Current | | -1 | +1 | -1 | +1 | μA |
| I_{OZ} | Output Leakage Current | $GND \leq V_I \leq V_{CC},$ Output Disabled | -5 | +5 | -5 | +5 | μA |
| I_{OS} | Output Short Circuit Current ^[3] | $V_{CC} = \text{Max.}, V_{OUT} = GND$ | | -300 | | -300 | mA |
| I_{CC} | V_{CC} Operating Supply Current | $V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA},$ $f = f_{MAX} = 1/t_{RC}$ | | 50 | | 45 | mA |
| I_{SB1} | Automatic CE Power-Down Current — TTL Inputs | Max. $V_{CC}, \overline{CE} \geq V_{IH},$ $V_{IN} \geq V_{IH},$ or $V_{IN} \leq V_{IL},$ $f = f_{MAX}$ | | 5 | | 5 | mA |
| | | | L | 4 | | 4 | mA |
| I_{SB2} | Automatic CE Power-Down Current — CMOS Inputs ^[4] | Max. $V_{CC}, \overline{CE} \geq V_{CC} - 0.3V, V_{IN} \geq$ $V_{CC} - 0.3V,$ or $V_{IN} \leq 0.3V,$ $WE \geq V_{CC} - 0.3V$ or $WE \leq 0.3V,$ $f = f_{MAX}$ | | 500 | | 500 | μA |
| | | | L | 50 | | 50 | μA |

Capacitance^[5]

| Parameter | Description | Test Conditions | Max. | Unit |
|----------------------|--------------------|--|------|------|
| C_{IN} : Addresses | Input Capacitance | $T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 3.3V$ | 5 | pF |
| C_{IN} : Controls | | | 6 | pF |
| C_{OUT} | Output Capacitance | | 6 | pF |

AC Test Loads and Waveforms


Equivalent to: THÉVENIN EQUIVALENT


Note:

- Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range^[6]

| Parameter | Description | 1399B-10 | | 1399B-12 | | Unit |
|--------------------------------------|--|----------|------|----------|------|------|
| | | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | |
| t_{RC} | Read Cycle Time | 10 | | 12 | | ns |
| t_{AA} | Address to Data Valid | | 10 | | 12 | ns |
| t_{OHA} | Data Hold from Address Change | 3 | | 3 | | ns |
| t_{ACE} | \overline{CE} LOW to Data Valid | | 10 | | 12 | ns |
| t_{DOE} | \overline{OE} LOW to Data Valid | | 5 | | 5 | ns |
| t_{LZOE} | \overline{OE} LOW to Low Z ^[7] | 0 | | 0 | | ns |
| t_{HZOE} | \overline{OE} HIGH to High Z ^[7, 8] | | 5 | | 5 | ns |
| t_{LZCE} | \overline{CE} LOW to Low Z ^[7] | 3 | | 3 | | ns |
| t_{HZCE} | \overline{CE} HIGH to High Z ^[7, 8] | | 5 | | 6 | ns |
| t_{PU} | \overline{CE} LOW to Power-Up | 0 | | 0 | | ns |
| t_{PD} | \overline{CE} HIGH to Power-Down | | 10 | | 12 | ns |
| Write Cycle^[9, 10] | | | | | | |
| t_{WC} | Write Cycle Time | 10 | | 12 | | ns |
| t_{SCE} | \overline{CE} LOW to Write End | 8 | | 8 | | ns |
| t_{AW} | Address Set-Up to Write End | 7 | | 8 | | ns |
| t_{HA} | Address Hold from Write End | 0 | | 0 | | ns |
| t_{SA} | Address Set-Up to Write Start | 0 | | 0 | | ns |
| t_{PWE} | \overline{WE} Pulse Width | 7 | | 8 | | ns |
| t_{SD} | Data Set-Up to Write End | 5 | | 7 | | ns |
| t_{HD} | Data Hold from Write End | 0 | | 0 | | ns |
| t_{HZWE} | \overline{WE} LOW to High Z ^[9] | | 7 | | 7 | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z ^[7] | 3 | | 3 | | ns |

Notes:

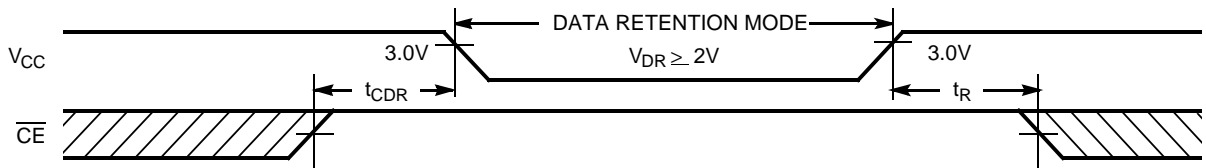
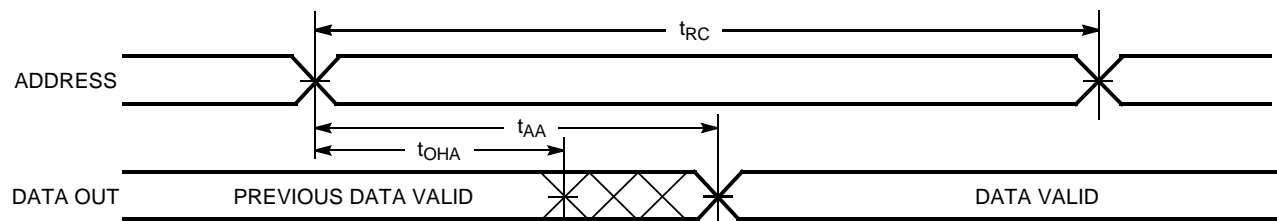
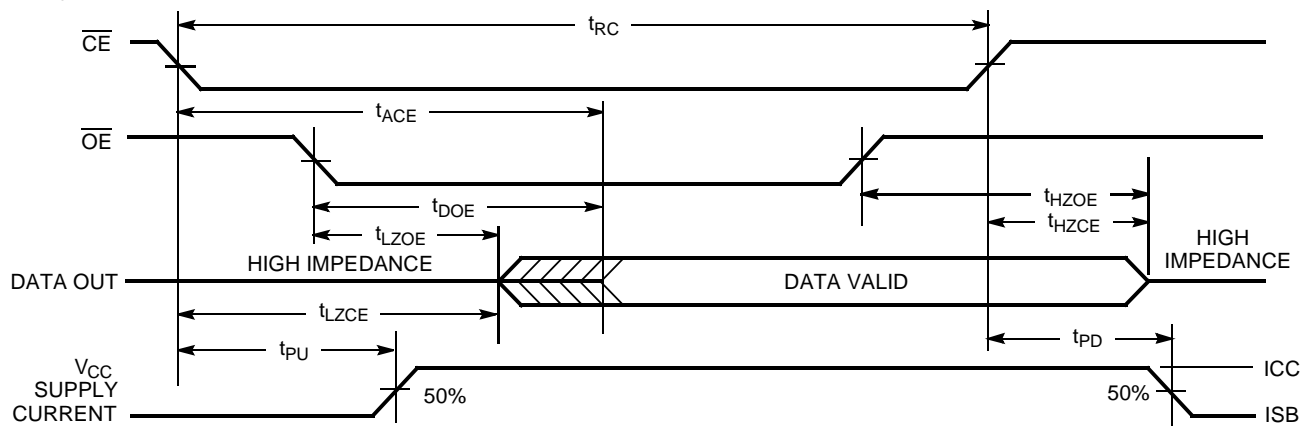
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and capacitance $C_L = 30$ pF.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZOE} , t_{HZCE} , t_{HZWE} are specified with $C_L = 5$ pF as in AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. The minimum write cycle time for write cycle #3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Characteristics Over the Operating Range^[6] (Continued)

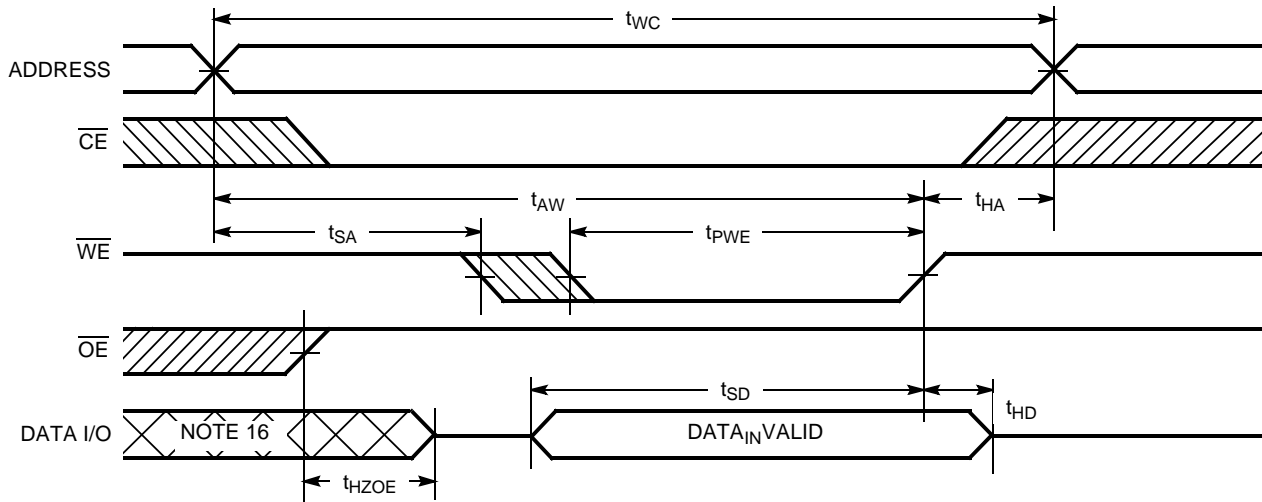
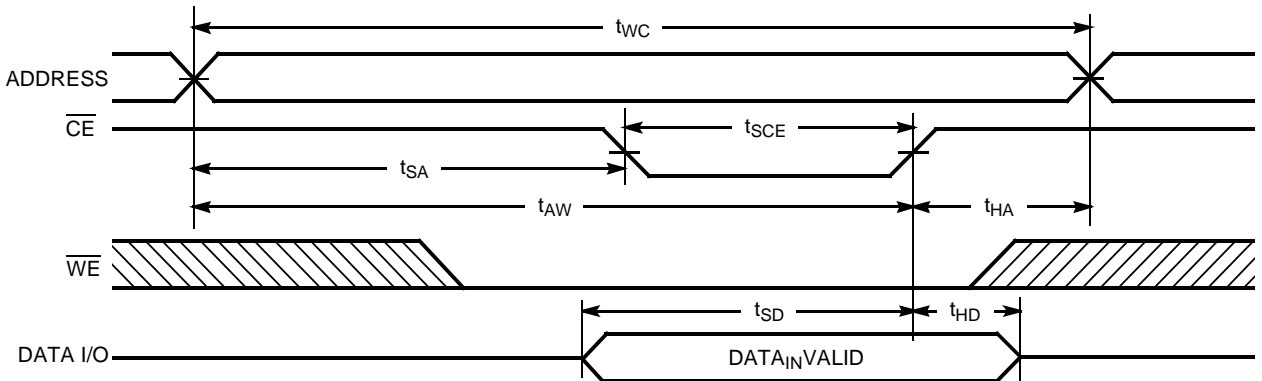
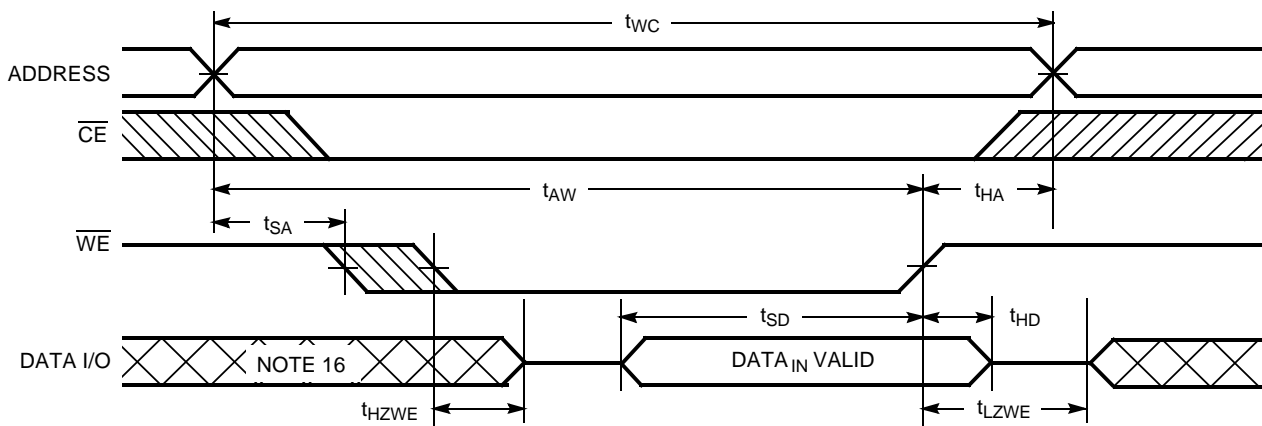
| Parameter | Description | 1399B-15 | | 1399B-20 | | Unit |
|--------------------------------------|--|----------|------|----------|------|------|
| | | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | |
| t_{RC} | Read Cycle Time | 15 | | 20 | | ns |
| t_{AA} | Address to Data Valid | | 15 | | 20 | ns |
| t_{OHA} | Data Hold from Address Change | 3 | | 3 | | ns |
| t_{ACE} | \overline{CE} LOW to Data Valid | | 15 | | 20 | ns |
| t_{DOE} | \overline{OE} LOW to Data Valid | | 6 | | 7 | ns |
| t_{LZOE} | \overline{OE} LOW to Low Z ^[7] | 0 | | 0 | | ns |
| t_{HZOE} | \overline{OE} HIGH to High Z ^[7, 8] | | 6 | | 6 | ns |
| t_{LZCE} | \overline{CE} LOW to Low Z ^[7] | 3 | | 3 | | ns |
| t_{HZCE} | \overline{CE} HIGH to High Z ^[7, 8] | | 7 | | 7 | ns |
| t_{PU} | \overline{CE} LOW to Power-Up | 0 | | 0 | | ns |
| t_{PD} | \overline{CE} HIGH to Power-Down | | 15 | | 20 | ns |
| Write Cycle^[9, 10] | | | | | | |
| t_{WC} | Write Cycle Time | 15 | | 20 | | ns |
| t_{SCE} | \overline{CE} LOW to Write End | 10 | | 12 | | ns |
| t_{AW} | Address Set-Up to Write End | 10 | | 12 | | ns |
| t_{HA} | Address Hold from Write End | 0 | | 0 | | ns |
| t_{SA} | Address Set-Up to Write Start | 0 | | 0 | | ns |
| t_{PWE} | \overline{WE} Pulse Width | 10 | | 12 | | ns |
| t_{SD} | Data Set-Up to Write End | 8 | | 10 | | ns |
| t_{HD} | Data Hold from Write End | 0 | | 0 | | ns |
| t_{HZWE} | \overline{WE} LOW to High Z ^[9] | | 7 | | 7 | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z ^[7] | 3 | | 3 | | ns |

Data Retention Characteristics (Over the Operating Range - L version only)

| Parameter | Description | | Conditions | Min. | Max. | Unit |
|------------|--------------------------------------|-------|---|----------|------|---------|
| V_{DR} | V_{CC} for Data Retention | | | 2.0 | | V |
| I_{CCDR} | Data Retention Current | Com'l | $V_{CC} = V_{DR} = 2.0V$, $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ | 0 | 20 | μA |
| t_{CDR} | Chip Deselect to Data Retention Time | | | 0 | | ns |
| t_R | Operation Recovery Time | | | t_{RC} | | ns |

Data Retention Waveform

Switching Waveforms
Read Cycle No. 1^[11, 12]

Read Cycle No. 2^[12, 13]

Notes:

11. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
12. WE is HIGH for read cycle.
13. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{WE} Controlled)^[9, 14, 15]

Write Cycle No. 2 (\overline{CE} Controlled)^[9, 14, 15]

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[10, 15]

Notes:

14. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
15. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
16. During this period, the I/Os are in the output state and input signals should not be applied.

Truth Table

| CE | WE | OE | Input/Output | Mode | Power |
|-----------|-----------|-----------|---------------------|---------------------------|----------------------|
| H | X | X | High Z | Deselect/Power-Down | Standby (I_{SB}) |
| L | H | L | Data Out | Read | Active (I_{CC}) |
| L | L | X | Data In | Write | Active (I_{CC}) |
| L | H | H | High Z | Deselect, Output Disabled | Active (I_{CC}) |

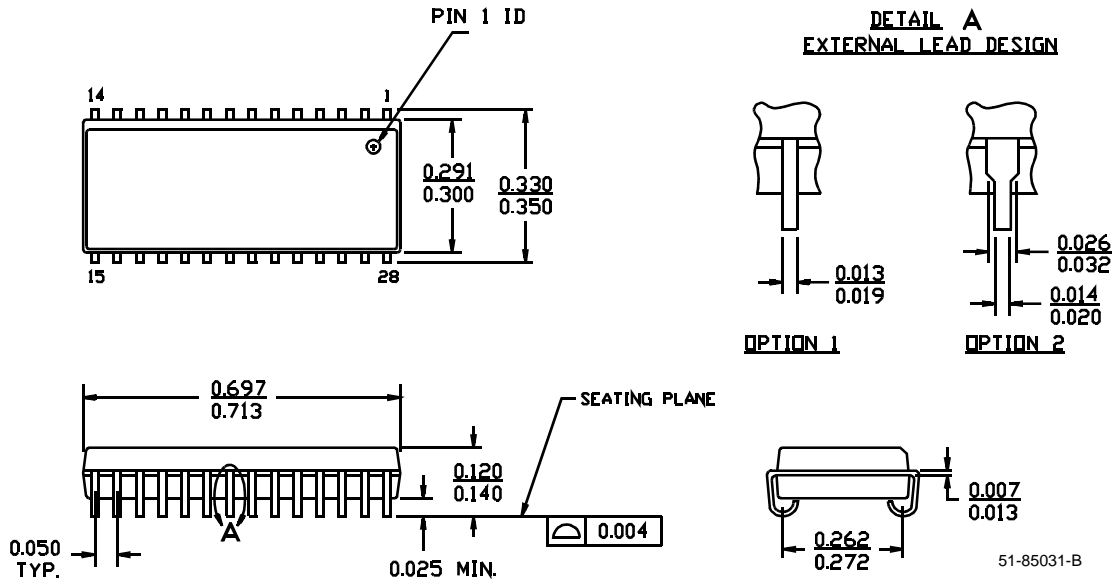
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Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range | |
|-------------------|----------------------|---------------------|------------------------------------|------------------------|------------|
| 10 | CY7C1399B-10VC | V21 | 28-Lead Molded SOJ | Commercial | |
| | CY7C1399B-10ZC | Z28 | 28-Lead Thin Small Outline Package | | |
| | CY7C1399BL-10VC | V21 | 28-Lead Molded SOJ | | |
| | CY7C1399BL-10ZC | Z28 | 28-Lead Thin Small Outline Package | | |
| 12 | CY7C1399B-12VC | V21 | 28-Lead Molded SOJ | Commercial | |
| | CY7C1399B-12ZC | Z28 | 28-Lead Thin Small Outline Package | | |
| | CY7C1399BL-12VC | V21 | 28-Lead Molded SOJ | | |
| | CY7C1399BL-12ZC | Z28 | 28-Lead Thin Small Outline Package | | |
| | CY7C1399B-12VI | V21 | 28-Lead Molded SOJ | | Industrial |
| | CY7C1399B-12ZI | Z28 | 28-Lead Thin Small Outline Package | | |
| 15 | CY7C1399B-15VC | V21 | 28-Lead Molded SOJ | Commercial | |
| | CY7C1399B-15ZC | Z28 | 28-Lead Thin Small Outline Package | | |
| | CY7C1399BL-15VC | V21 | 28-Lead Molded SOJ | | |
| | CY7C1399BL-15ZC | Z28 | 28-Lead Thin Small Outline Package | | |
| | CY7C1399B-15VI | V21 | 28-Lead Molded SOJ | | Industrial |
| | CY7C1399B-15ZI | Z28 | 28-Lead Thin Small Outline Package | | |
| 20 | CY7C1399B-20VC | V21 | 28-Lead Molded SOJ | Commercial | |
| | CY7C1399B-20ZC | Z28 | 28-Lead Thin Small Outline Package | | |
| | CY7C1399BL-20VC | V21 | 28-Lead Molded SOJ | | |
| | CY7C1399BL-20ZC | Z28 | 28-Lead Thin Small Outline Package | | |
| | CY7C1399B-20VI | V21 | 28-Lead Molded SOJ | | Industrial |
| | CY7C1399B-20ZI | Z28 | 28-Lead Thin Small Outline Package | | |

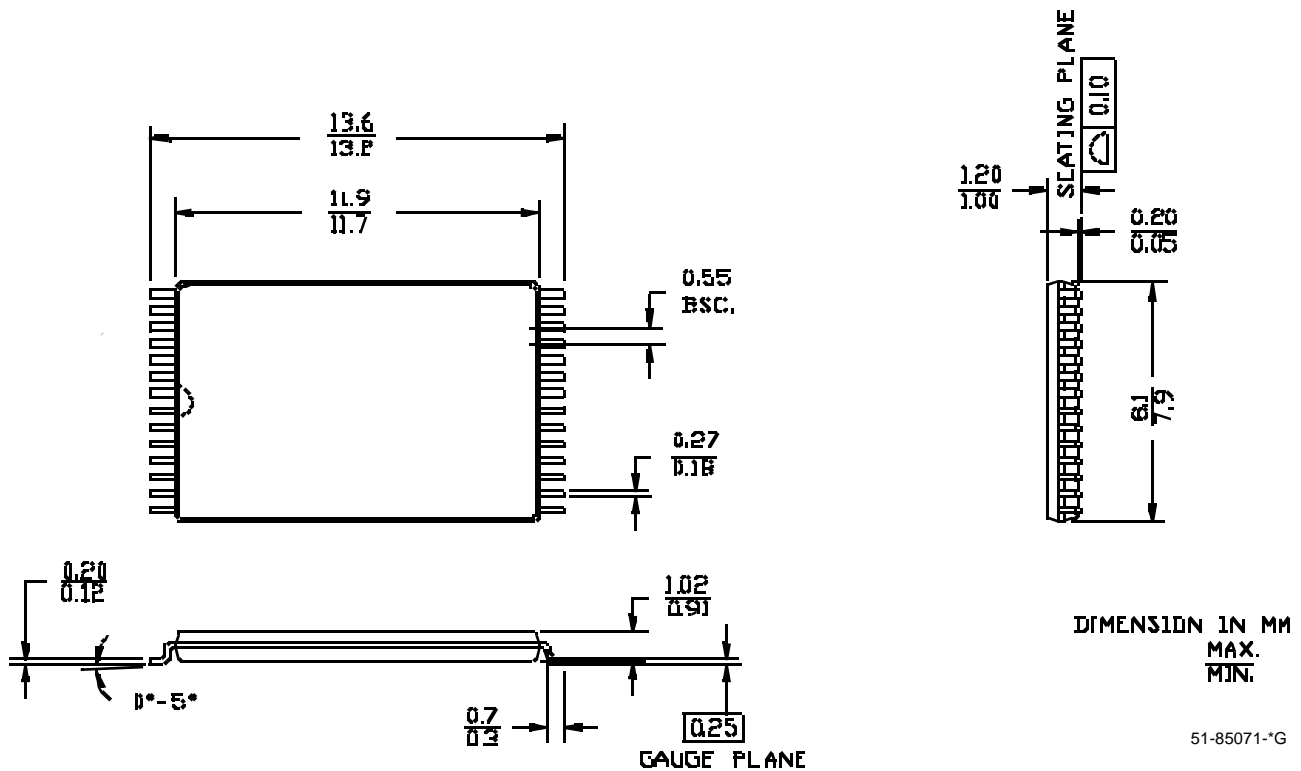
Package Diagrams

28-Lead (300-Mil) Molded SOJ V21

DIMENSIONS IN INCHES
MIN.
MAX.



28-Lead Thin Small Outline Package Type 1 (8x13.4 mm) Z28



Document History Page

| Document Title: CY7C1399B 32K x 8 3.3V Static RAM | | | | |
|--|----------------|-------------------|------------------------|--|
| Document Number: 38-05071 | | | | |
| REV. | ECN NO. | ISSUE DATE | ORIG. OF CHANGE | DESCRIPTION OF CHANGE |
| ** | 107264 | 05/25/01 | SZV | Change from Spec #: 38-01102 to 38-05071 |
| *A | 107533 | 06/28/01 | MAX | Add Low Power |
| *B | 116472 | 09/17/02 | CEA | Add applications foot note to data sheet, page 1. |
| *C | 224340 | See ECN | RKF | Option 1 of the Orientation ID on TSOP-I Package Diagram [Page #9] removed |