PRELIMINARY

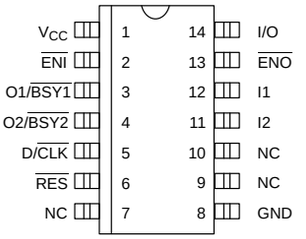
DALLAS SEMICONDUCTOR

DS1481
1–Wire Bus Master with Overdrive

FEATURES

- Provides a synchronous interface to Dallas Semiconductor 1–wire devices
- Compatible with low power parallel ports
- Can be cascaded with other DS1481's
- Allows print spooler and other processes to run during 1–wire I/O
- Provides high speed communcation with overdrive capable devices
- Space saving 14–pin (150 mil), SOIC package

PIN ASSIGNMENT



14–PIN SOIC (150 MIL)

PIN DESCRIPTION

V_{CC}	–	Supply
$\overline{ENI}$	–	Enable In
D/$\overline{CLK}$	–	Data/Clock
$\overline{RES}$	–	Reset
O1/$\overline{BSY1}$	–	Output 1/Busy 1
O2/$\overline{BSY2}$	–	Output 2/Busy 2
GND	–	Ground
I1	–	Input 1
I2	–	Input 2
I/O	–	1–wire I/O
$\overline{ENO}$	–	Enable Out
NC	–	No Connect

DESCRIPTION

The DS1481 is a dedicated 1–wire timing generator. The device is normally used in conjunction with a parallel port controller to provide the necessary interface to the host processor. Busy signals allow the host processor to perform other tasks while 1–wire "time–slots" are completed. The DS1481 also saves the state of D/$\overline{CLK}$ and $\overline{RES}$ allowing print spoolers to operate without affecting 1–wire communication.

DS1481 based devices can be cascaded. The first device's O1/$\overline{BSY1}$ and O2/$\overline{BSY2}$ connect to the PC printer port's BUSY and SELECT OUT signals (pins 11 and 13 respectively). The next DS1481 connects its O1/$\overline{BSY1}$ and O2/$\overline{BSY2}$ to the first device's I1 and I2 respectively. $\overline{ENO}$ of the first device connects to $\overline{ENI}$ of the second device. More DS1481's can be stacked in a similar manner. The last devices I1 and I2 connect to BUSY and SELECT of the attached printer.

The DS1481's 3–volt operation insures compatibility with most low power parallel ports (i.e., portable computers).

OPERATION

One wire communication is executed in “time slots”. The DS1481 generates either a read/write bit “time slot” or a reset on the I/O pin. The operation performed is determined by the states of the D/$\overline{CLK}$ and $\overline{RES}$ pins as follows:

TIME SLOT	D/$\overline{CLK}$	$\overline{RES}$
Read 0, Read 1, Write 1	logic high	logic high (see Figure 4)
Write 0	logic low	logic high (see Figure 5)
1–wire Reset	logic high	logic low (see Figure 6)

After D/$\overline{CLK}$ and $\overline{RES}$ have been set, the time slot begins when $\overline{ENI}$ is driven to its active state. A falling edge on $\overline{ENI}$ causes the DS1481 to save the state of D/$\overline{CLK}$ and $\overline{RES}$. If the time slot is a 1–wire reset the DS1481 will issue a busy signal by driving O1/$\overline{BSY1}$ low and O2/$\overline{BSY2}$ high. After 2 µs O2/$\overline{BSY2}$ is driven low. Both outputs will remain low until the communication on the I/O line is finished. A busy signal for a bit time slot differs from the reset busy signal only in that both O1/$\overline{BSY1}$ and O2/$\overline{BSY2}$ are driven low immediately.

While the busy signal is asserted, the host processor is free to perform other tasks (including running the print spooler). When the time slot is complete, the DS1481 restores both O1/$\overline{BSY1}$ and O2/$\overline{BSY2}$ to the states of I1 and I2 (see Figure 1).

When the host detects that one or both of the busy signals has returned high, it must query the result of the time slot. This is accomplished by driving D/$\overline{CLK}$ low. If the result of the time slot was low (Read 0, Write 0 or presence detect) the DS1481 drives both O1/$\overline{BSY1}$ and O2/$\overline{BSY2}$ low (this state is held until $\overline{ENI}$ returns high). Otherwise it propagates the states of I1 and I2.

After the host reads the result of the time slot it must drive $\overline{ENI}$ to its inactive state (high). The DS1481 will then set O1/$\overline{BSY1}$ and O2/$\overline{BSY2}$ to the states of I1 and I2.

1–WIRE TIMING GENERATION

For all time slots, the DS1481 samples the I/O pin at t_{SO} (see Figure 4). The DS1481 waits a minimun of 60 µs from the start of the time slot and de–asserts O1/$\overline{BSY1}$ and O2/$\overline{BSY2}$.

When a reset is requested, the DS1481 drives the I/O pin low for at least 480 µs and then releases it. During a normal reset the I/O pin immediately begins to return high.

If a 1–wire device is present on the I/O line it pulls I/O low after time T (15 µs ≤ T ≤ 60 µs) from the previous rising edge. The 1–wire device(s) holds the I/O line low for 4T and then releases it, allowing the I/O line to return high. This is the presence detect pulse. The I/O line must remain high (in its idle state) for at least 3T before the 1–wire device(s) is ready for further communication. To insure this idle high time is satisfied, the DS1481 does not release O1/$\overline{BSY1}$ and O2/$\overline{BSY2}$ for at least 960 µs (measured from the 1st falling edge on the I/O pin).

If after 480 µs of low time the I/O line did not return high, either the I/O line has been shorted to ground or there is at least one 1–wire device connected to the I/O line which is issuing an alarm interrupt (see Figure 6). In this case the DS1481 waits for I/O to return high for an additional 3840 µs (64 * 60). If time expires the I/O line is assumed to be shorted and the DS1481 releases O1/$\overline{BSY1}$ and O2/$\overline{BSY2}$. If the I/O line returns high, the DS1481 continues to monitor the presence detect portion of the reset (as described above) as for the non–interrupt case. Note that the 3T idle high time is still required after the presence detect ends.

OVERDRIVE

The DS1481 also supports overdrive communication with overdrive capable 1–wire devices. When the DS1481 powers up it is in normal mode (i.e., OD = 0, Figure 1). To toggle to overdrive mode the host sets D/$\overline{CLK}$ and $\overline{RES}$ low and drives $\overline{ENI}$ low. The DS1481 toggles the OD bit to a logic high and returns the states of I1 and I2 on O1/$\overline{BSY1}$ and O2/$\overline{BSY2}$. Overdrive mode is cleared in the same way. When overdrive is turned off (OD = 0). O1/$\overline{BSY1}$ and O2/$\overline{BSY2}$ are driven low to report the state of the OD bit.

When OD = 1, communication with the 1–wire device is exactly as described in the operation section above. The actual 1–wire timing for both modes of operation is described in Figures 4, 5 and 6.

Note that when toggling the OD bit there is no change on the I/O line.

PRINTER COEXISTENCE

In order to coexist with parallel port printers, the DS1481 utilizes two input pins (I1 and I2) and two output pins (O1/$\overline{BSY1}$ and O2/$\overline{BSY2}$). When $\overline{ENI}$ is low these pins are used for transmitting data received on the I/O pin or for issuing an unmistakable busy signal. When $\overline{ENI}$ is inactive (high) O1/$\overline{BSY1}$ and O2/$\overline{BSY2}$ propagate the states of I1 and I2.

If a printer is attached to a DS1481, I1 is connected to the printers BUSY signal (low only if printer is on line and busy), and I2 is connected to SELECT OUT (driven low if printer is off line), see Figure 2.

If the attached printer is “powered up” and on line, the DS1481 uses SELECT OUT for communication regardless of the state of the printers BUSY signal. If the printer is off line its BUSY signal is inactive (high) and this line is used by the DS1481 for host communication.

If the attached printer is powered off, both SELECT OUT and BUSY will be low. This prevents meaningful communication with the DS1481 because it is unable to de–assert its busy signal (O1/$\overline{BSY1}$ and O2/$\overline{BSY2}$ low) or return a high sample of the I/O pin.

To solve this problem, the DS1481 uses the busy signal issued during a reset to detect the presence of another DS1481 based device attached behind it on the parallel port. If this busy signal is not detected by the DS1481, it assumes that it is the last DS1481 based device on the port.

If the DS1481 determines that it is the last device on the port it ignores the states of its I1 and I2 pins while $\overline{ENI}$ is low. It also leaves the $\overline{ENO}$ pin high to prevent sending line feed signals to the printer. This gives the last device the ability to control O1/$\overline{BSY1}$ and O2/$\overline{BSY2}$ without affecting stackability.

EPP/ECP TRANSPARENT MODE

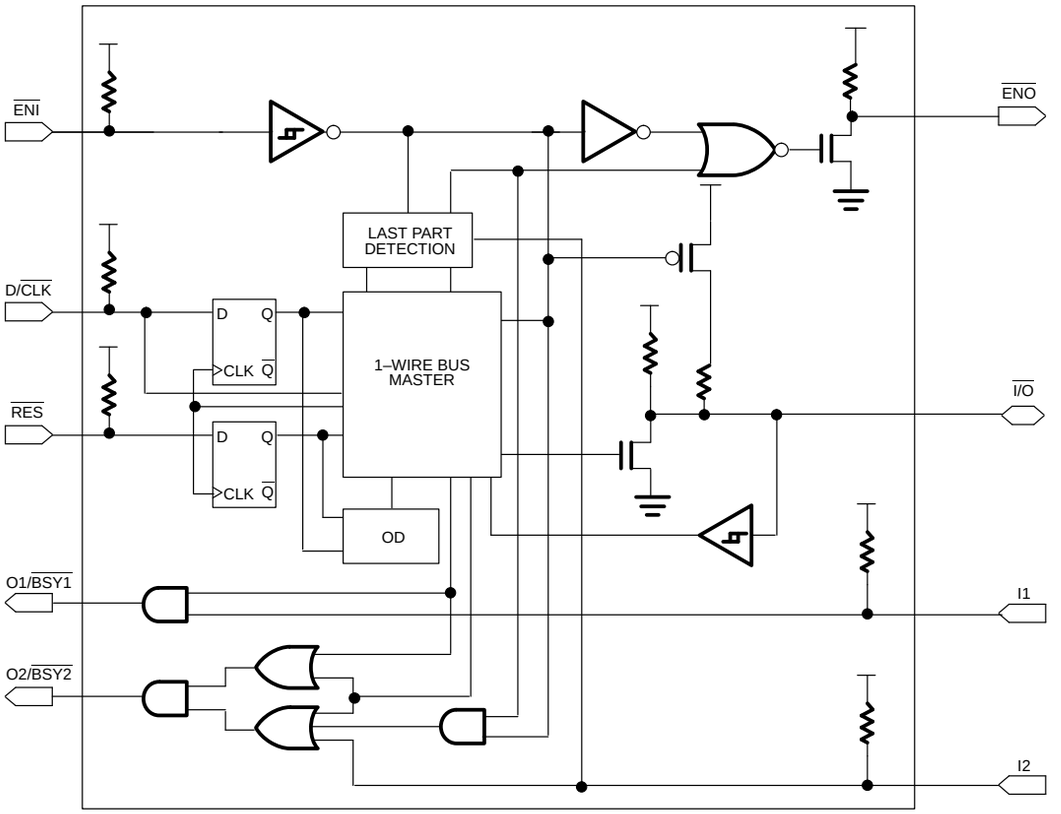
When the DS1481 first powers up it is in a transparent mode in which the three signal lines (auto line feed, busy and select) that pass through the part are directly connected by transmission gates. This allows bi–directional printers (or other parallel port peripherals) to communicate in either the EPP or ECP mode of the PC parallel port. The DS1481 pin sets connected are as follows:

$\overline{ENI}$	$\overline{ENO}$
O1/$\overline{BSY1}$	I1
O2/$\overline{BSY2}$	I2

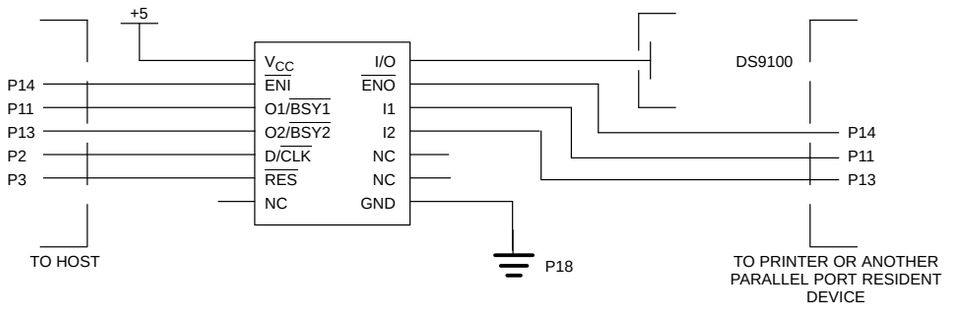
1–wire communication using the DS1481 is impossible in transparent mode. To toggle to normal mode four consecutive overdrive toggle commands must be issued. If this sequence has been issued and the $\overline{ENI}$ pin remains high for at least 10 ms the part will enter its normal mode of operation. Note that any other 1–wire time slot command issued during the sequence resets the sequence. The steps needed to return to transparent mode are as described above with the exception that no additional wait is required at the end of the four overdrive toggles to enter transparent mode.

While in transparent mode if the DS1481 detects that the $\overline{ENO}$ pin has been held low for more than 10 ms it turns off the transmission gate connecting $\overline{ENI}$ and $\overline{ENO}$. This guarantees the host will have the ability to take the DS1481 out of transparent mode and perform 1–wire I/O operations.

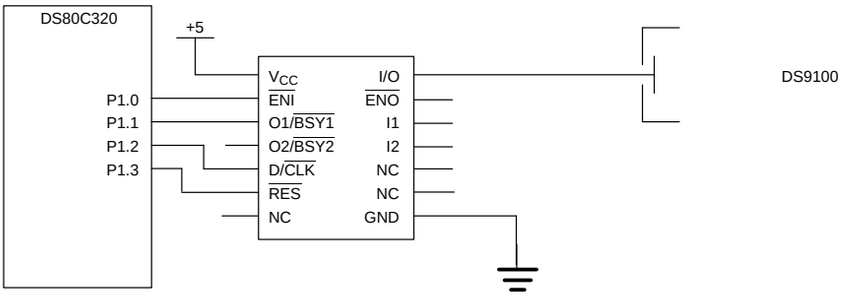
DS1481 FUNCTIONAL BLOCK DIAGRAM Figure 1



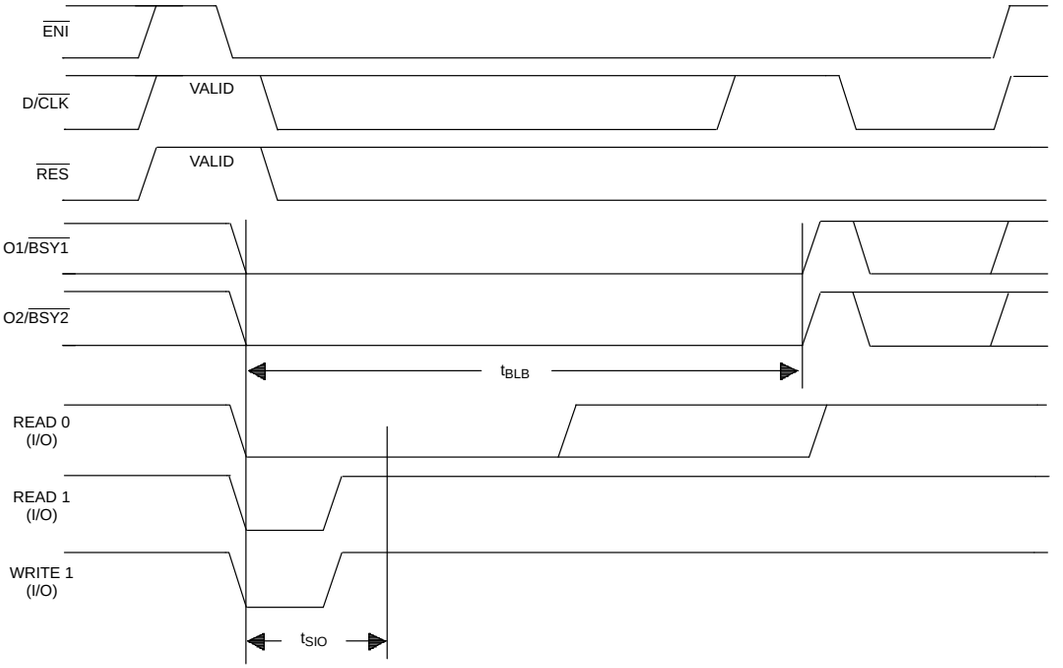
CONNECTION TO PC TYPE PARALLEL PORTS Figure 2



CONNECTION TO MICROCONTROLLERS Figure 3



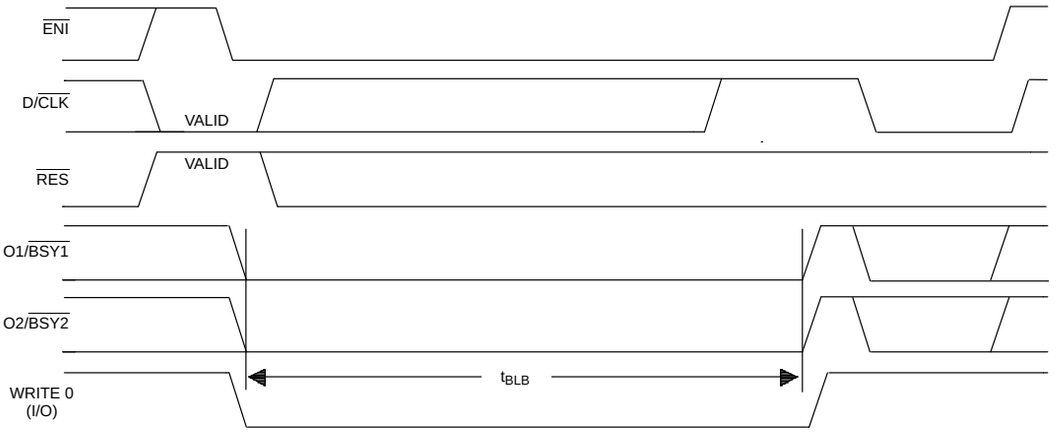
TIMING DIAGRAM: HOST INTERFACE Figure 4



t_{SIO} = 8 µs (TYPICAL), t_{BLB} = 60 µs (MINIMUM) (OD = 0)
t_{SIO} = 2 µs (MAXIMUM), t_{BLB} = 6 µs (MINIMUM) (OD = 1)

READ O, READ 1, WRITE 1 BIT TIME SLOTS

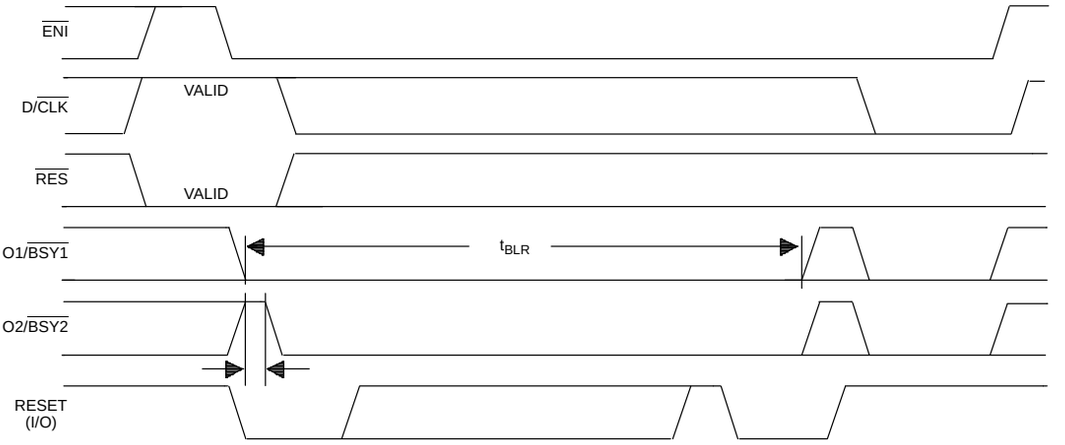
TIMING DIAGRAM: HOST INTERFACE Figure 5



t_{BLB} = 60 µs (MINIMUM) (OD = 0)
t_{BLB} = 6 µs (MINIMUM) (OD = 1)

WRITE 0 TIME SLOT

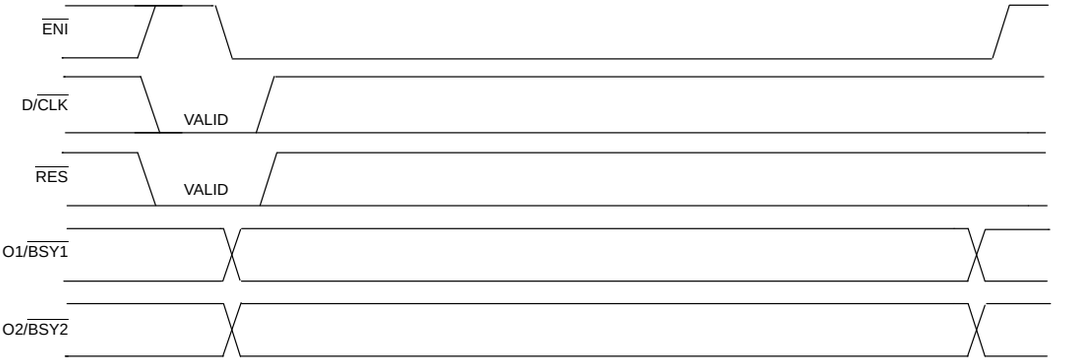
TIMING DIAGRAM: HOST INTERFACE Figure 6



t_{PDH} = 2 µs (TYPICAL)
t_{BLR} = 960 µs (MINIMUM) (OD = 0)
t_{BLB} = 96 µs (MINIMUM) (OD = 1)

1–WIRE RESET

TIMING DIAGRAM: HOST INTERFACE Figure 7



TOGGLE OVERDRIVE MODE

DETAILED PIN DESCRIPTION

PIN	TYPE	DESCRIPTION
Vcc		DC supply voltage.
$\overline{ENI}$	I	Chip enable, driven low to begin 1–wire I/O.
O1/$\overline{BSY1}$	O	Driven low during time slot (to indicate a DS1481 busy condition). Set to state of I1 after time slot has finished. O1/$\overline{BSY1}$ will go low after D/$\overline{CLK}$ goes low if sample of I/O communication was low. Returns to state of I1 when $\overline{ENI}$ goes back high (see Figure 1).
O2/$\overline{BSY2}$	O	Driven low during time slot (to indicate a DS1481 busy condition). Set to state of I2 after time slot has finished. O2/$\overline{BSY2}$ will go low after D/$\overline{CLK}$ goes low if sample of I/O communication was low. Returns to state of I2 when $\overline{ENI}$ goes back high (see Figure 1).
D/$\overline{CLK}$	I	Data/Clock pin. Used to specify type of time slot before communication begins. After the time slot has been completed this pin is driven low in order to solicit the result of the time slot.
$\overline{RES}$	I	Set low (before $\overline{ENI}$ is driven low) to specify that a reset pulse should be generated on the I/O pin.
GND		System ground.
I1	I	Can be connected to the O1/$\overline{BSY1}$ of another DS1481. May also be connected to parallel port printer's BUSY signal. Internally pulled high via a weak resistor.
I2	I	Can be connected to the O2/$\overline{BSY2}$ of another DS1481. Can also be connected to a parallel port printer SELECT OUT signal. Internally pulled high via a weak resistor.
$\overline{ENO}$	O	Set to $\overline{ENI}$ if not the last part on port. Open drain output with weak internal pull–up resistor.
I/O	I/O	1–wire I/O line. Bi–directional line with open drain output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to ground	–1.0V to +7.0V
Operating temperature	0°C to 70°C
Storage temperature	–55°C to +125°C
Soldering temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 40°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.4		V_{CC} + 0.3	V	1
Logic 0	V_{IL}	–0.3		+0.8	V	1
Supply	V_{CC}	2.7	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 40°C; 2.7 ≤ V_{CC}≤ 5.5)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	–1		+1	µA	5
Output Leakage	I_{LO}	–1		+1	µA	
V_{OL} @ I_{SINK} = –2 mA				0.4	V	
I1 pull–up resistance	Z_{I1}		50		KΩ	
I2 pull–up resistance	Z_{I2}		50		KΩ	
$\overline{ENI}$ pull–up resistance	Z_{ENI}		50		KΩ	
$\overline{ENO}$ pull–up resistance	Z_{ENO}		50		KΩ	
D/$\overline{CLK}$ Pull–Up resistance	Z_{DC}		50K			
$\overline{RES}$ Pull–Up resistance	Z_R		50K			
Active Current	I_{CC}			500	µA	2
Available I/O Current	$I_{I/O}$		40		mA	6

AC ELECTRICAL CHARACTERISTICS: HOST INTERFACE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Sample Time (for bit time slot, OD = 0) (for bit time slot, OD = 1)	t_{SIO}		8	 2	µs	
Recovery Time	t_{REC}	1			µs	
Data to Enable Hold	t_{DE}	40			µs	
Reset to Enable Hold	t_{RE}	40			ns	
Clock low time	t_{CL}	200			ns	
Clock low to O1, O2 valid	t_{COV}			200	ns	
BSY1, BSY2 low time (for bit time slot, OD = 0) (OD = 1)	t_{BLB}	60 6			µs	3
BSY1, BSY2 low time (for reset time slot, OD = 0) (OD = 1)	t_{BLR}	960 96			µs	4

NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open and I1, I2 high.
3. Minimum time required for 1–wire bit time slot.
4. Minimum time required for 1–wire reset time slot.
5. Only pins without pull–ups.
6. Overdrive mode only.