

## Dual Channel, Ultra-Low Resistance Load Switch

### General Description

The EM5208 is a small, ultra-low RON, dual channel load switch with controlled turn on. The device contains two N-channel MOSFETs that can operate over an input voltage range of 0.8V to 5.5V and can support a maximum continuous current of 4A per channel. Each switch is independently controlled by an on/off input (ON1 and ON2), which is capable of interfacing directly with low-voltage control signals. In EM5208, a 220-Ω on-chip load resistor is added for quick output discharge when switch is turned off.

The EM5208 is available in a small, space-saving DFN3X2 package with integrated thermal pad allowing for high power dissipation.

### Ordering Information

Part Number	Package	Remark
EM5208VF	DFN3X2-14L	

### Features

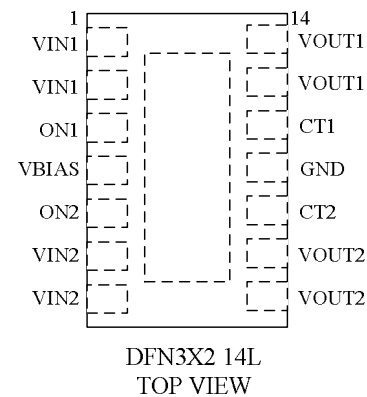
- Integrated dual channel load switch
- Input voltage range : 0.8V to 5.5V
- Ultra low R<sub>ON</sub> resistance 30mΩ per channel
- 4A maximum continuous switch current per channel
- Low quiescent current 45uA (dual channel), 40uA (single channel)
- Configurable rise time
- Quick Output Discharge (QOD)
- DFN3X2 14-pin package with Thermal Pad
- Bias voltage supports : 2.5V and 5V

### Applications

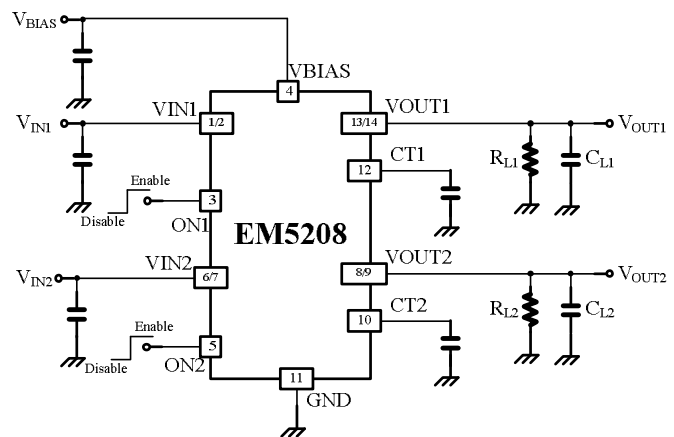
- Ultrabook
- Notebooks & Netbooks
- Tablet PC
- Consumer electronics
- Set-top boxes/Residential gateway
- Telecom systems
- Solid State Drives (SSD)



### Pin Configuration



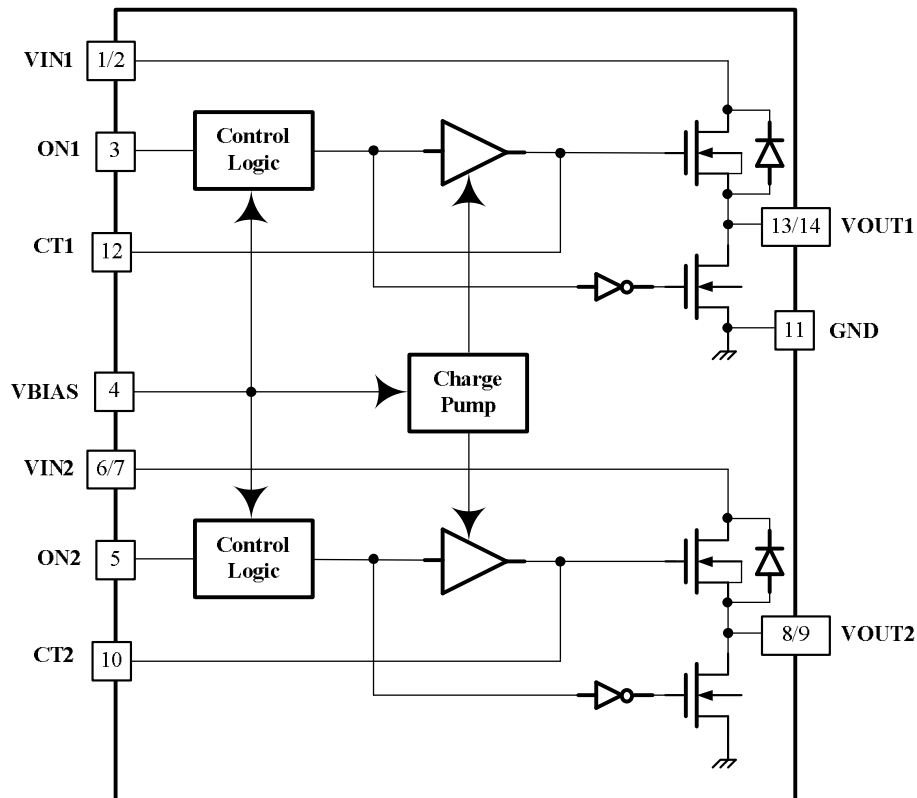
### Typical Application Circuit



**Pin Assignment**

Pin Name	Pin No.	Pin Function
VIN1	1 / 2	Switch #1 input. Bypass this input with a ceramic capacitor to GND. Recommended voltage range for this pin for optimal RON performance is 0.8V to VBIAS.
ON1	3	Active high switch #1 control input. Do not leave floating.
VBIAS	4	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5V to 5.5V.
ON2	5	Active high switch #2 control input. Do not leave floating.
VIN2	6 / 7	Switch #2 input. Bypass this input with a ceramic capacitor to GND. Recommended voltage range for this pin for optimal RON performance is 0.8V to VBIAS.
VOUT2	8 / 9	Switch #2 output.
CT2	10	Switch #2 slew rate control. Can be left floating.
GND	11	Ground
CT1	12	Switch #1 slew rate control. Can be left floating.
VOUT1	13 / 14	Switch #1 output.
Thermal PAD	15	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND.

**Function Block Diagram**



**Absolute Maximum Ratings (Note1)**

- $V_{IN1,2}$  ----- -0.3V to +6.0V
- $V_{OUT1,2}$  ----- -0.3V to +6.0V
- $V_{ON1,2}$  ----- -0.3V to +6.0V
- Power Dissipation,  $P_D @ T_A = 25^\circ\text{C}$ , DFN3X2 ----- 1.53W
- Package Thermal Resistance,  $\Theta_{JA}$ , DFN3X2 (Note 2)----- 65°C/W
- Junction Temperature----- 150°C
- Lead Temperature (Soldering, 10 sec.)----- 260°C
- Storage Temperature ----- -65°C to 150°C
- ESD susceptibility (Note3)
  - HBM (Human Body Mode)----- 2KV
  - MM (Machine Mode)----- 200V

**Recommended Operating Conditions (Note4)**

- Bias Voltage,  $V_{BIAS}$  ----- +2.5V to +5.5V
- Supply Input Voltage,  $V_{IN1,2}$  ----- +0.8V to  $V_{BIAS}$
- ON Voltage,  $V_{ON1,2}$  ----- +0V to  $V_{IN}$
- Junction Temperature ----- -40°C to 125°C
- Ambient Temperature ----- -40°C to 85°C

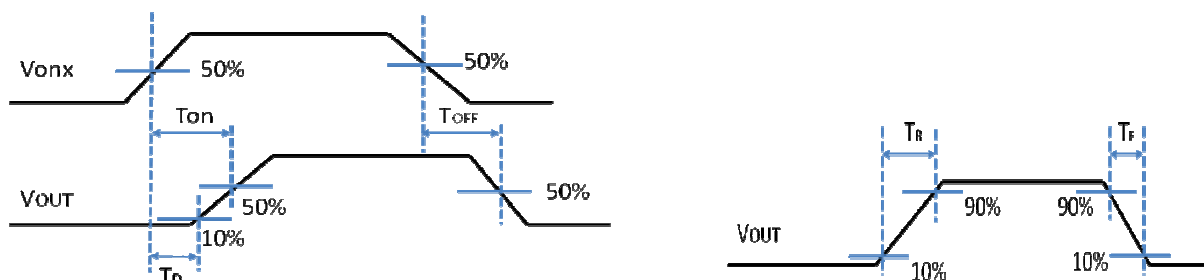
**Electrical Characteristics**
 $V_{BIAS} = 5V, T_A = 25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	
<b>Power Supplies and Currents Section</b>							
VBIAS Quiescent current (both channels)	$I_{BIAS-ON-both}$	$I_{OUT1} = I_{OUT2} = 0,$ $V_{IN1,2} = V_{ON1,2} = V_{BIAS} = 5V$		50	65	uA	
VBIAS Quiescent current (single channel)	$I_{BIAS-ON-single}$	$I_{OUT1} = I_{OUT2} = 0, V_{ON2} = 0V$ $V_{IN1,2} = V_{ON1} = V_{BIAS} = 5V$		40		uA	
VBIAS Shutdown current	$I_{BIAS-OFF}$	$V_{OUT1,2} = 0V, V_{ON1,2} = 0V$ $V_{IN1,2} = V_{BIAS} = 5V$			2	uA	
$V_{IN1,2}$ Off state supply current (per channel)	$I_{VIN-OFF}$	$V_{OUT1,2} = 0V,$ $V_{ON1,2} = 0V$	$V_{IN1,2} = 5.0V$			2	uA
			$V_{IN1,2} = 3.3V$			2	
			$V_{IN1,2} = 1.8V$			2	
			$V_{IN1,2} = 0.8V$			1	
ON pin leakage current	$I_{ON}$	$V_{ON} = 5.5V$			1	uA	
<b>Resistance Section</b>							
ON-state Resistance	$R_{ON}$	$I_{OUT} = 200mA,$ $V_{BIAS} = 5.0V$	$V_{IN} = 5.0V$		30	35	mΩ
			$V_{IN} = 3.3V$		30	35	
			$V_{IN} = 1.8V$		30	35	
			$V_{IN} = 1.5V$		30	35	
			$V_{IN} = 1.2V$		30	35	
Output Pull-down Resistance	$R_{PD}$	$V_{IN} = 5.0V, V_{ON} = 0V, I_{OUT} = 15mA$		220	300	Ω	

$V_{BIAS} = 2.5V, T_A = 25^\circ C$ , unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	
<b>Power Supplies and Currents Section</b>							
VBIAS Quiescent current (both channels)	$I_{BIAS-ON-both}$	$I_{OUT1} = I_{OUT2} = 0, V_{IN1,2} = V_{ON1,2} = V_{BIAS} = 2.5V$		50	65	$\mu A$	
VBIAS Quiescent current (single channel)	$I_{BIAS-ON-single}$	$I_{OUT1} = I_{OUT2} = 0, V_{ON2} = 0V, V_{IN1,2} = V_{ON1} = V_{BIAS} = 2.5V$		40		$\mu A$	
VBIAS Shutdown current	$I_{BIAS-OFF}$	$V_{OUT1,2} = 0V, V_{ON1,2} = 0V, V_{IN1,2} = V_{BIAS} = 2.5V$			2	$\mu A$	
$V_{IN1,2}$ Off state supply current (per channel)	$I_{VIN-OFF}$	$V_{OUT1,2} = 0V, V_{ON1,2} = 0V$	$V_{IN1,2} = 2.5V$			2	$\mu A$
			$V_{IN1,2} = 1.8V$			2	
			$V_{IN1,2} = 1.2V$			2	
			$V_{IN1,2} = 0.8V$			1	
ON pin leakage current	$I_{ON}$	$V_{ON} = 5.5V$			1	$\mu A$	
<b>Resistance Section</b>							
ON-state Resistance	$R_{ON}$	$I_{OUT} = 200mA, V_{BIAS} = 2.5V$	$V_{IN} = 2.5V$		32	37	$m\Omega$
			$V_{IN} = 1.8V$		32	37	
			$V_{IN} = 1.5V$		32	37	
			$V_{IN} = 1.2V$		32	37	
			$V_{IN} = 0.8V$		32	37	
Output Pull-down Resistance	$R_{PD}$	$V_{IN} = 2.5V, V_{ON} = 0V, I_{OUT} = 1mA$		260	320	$\Omega$	

Switching Timing Diagrams



Switching characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b><math>V_{IN} = V_{ON} = V_{BIAS} = 5V, T_A = 25^\circ C</math></b>						
Turn-on time	$T_{ON}$	$R_L = 10\Omega, C_L = 0.1\mu F, C_T = 1000pF$		1210		$\mu S$
Turn-off time	$T_{OFF}$	$R_L = 10\Omega, C_L = 0.1\mu F, C_T = 1000pF$		6		$\mu S$
Vout Rising time	$T_R$	$R_L = 10\Omega, C_L = 0.1\mu F, C_T = 1000pF$		1370		$\mu S$
Vout falling time	$T_F$	$R_L = 10\Omega, C_L = 0.1\mu F, C_T = 1000pF$		2		$\mu S$
ON Delay time	$T_D$	$R_L = 10\Omega, C_L = 0.1\mu F, C_T = 1000pF$		460		$\mu S$
<b><math>V_{IN} = 0.8V, V_{ON} = V_{BIAS} = 5V, T_A = 25^\circ C</math></b>						
Turn-on time	$T_{ON}$	$R_L = 10\Omega, C_L = 0.1\mu F, C_T = 1000pF$		550		$\mu S$
Turn-off time	$T_{OFF}$	$R_L = 10\Omega, C_L = 0.1\mu F, C_T = 1000pF$		170		$\mu S$
Vout Rising time	$T_R$	$R_L = 10\Omega, C_L = 0.1\mu F, C_T = 1000pF$		325		$\mu S$
Vout falling time	$T_F$	$R_L = 10\Omega, C_L = 0.1\mu F, C_T = 1000pF$		16		$\mu S$

ON Delay time	$T_D$	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	400		$\mu S$
<b><math>V_{IN}=2.5V, V_{ON}=5V, V_{BIAS}=2.5V, T_A=25^\circ C</math></b>					
Turn-on time	$T_{ON}$	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	2050		$\mu S$
Turn-off time	$T_{OFF}$	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	5		$\mu S$
Vout Rising time	$T_R$	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	2275		$\mu S$
Vout falling time	$T_F$	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	2.5		$\mu S$
ON Delay time	$T_D$	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	990		$\mu S$
<b><math>V_{IN}=0.8V, V_{ON}=5V, V_{BIAS}=2.5V, T_A=25^\circ C</math></b>					
Turn-on time	$T_{ON}$	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	1300		$\mu S$
Turn-off time	$T_{OFF}$	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	130		$\mu S$
Vout Rising time	$T_R$	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	875		$\mu S$
Vout falling time	$T_F$	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	16		$\mu S$
ON Delay time	$T_D$	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	870		$\mu S$

**Note 1.** Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2.**  $\theta_{JA}$  is measured in the natural convection at  $T_A=25^\circ C$  on a 4-layers high effective thermal conductivity test board with minimum copper area of JEDEC 51-7 thermal measurement standard.

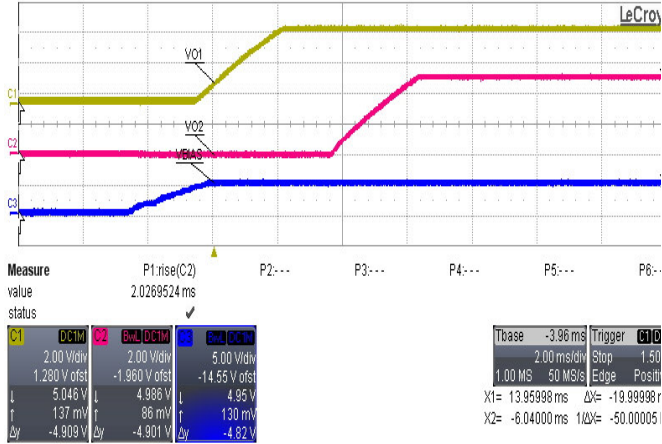
**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

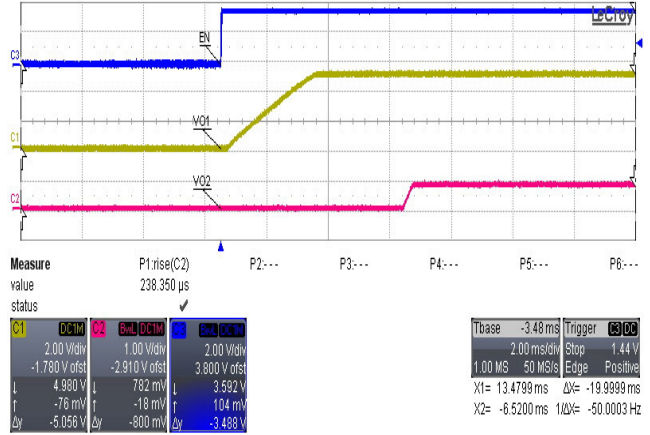
**Typical Operating Characteristics**

$V_{CNTL} = 5V$  ;  $T_A = 25^\circ C$

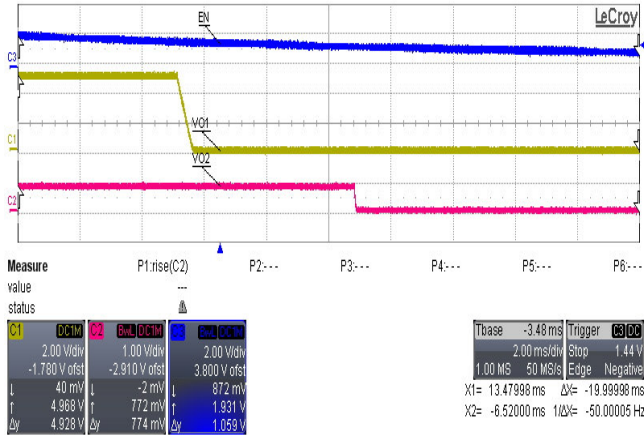
**Turn-on from  $V_{CNTL}$   
 (BOTH Channel)**



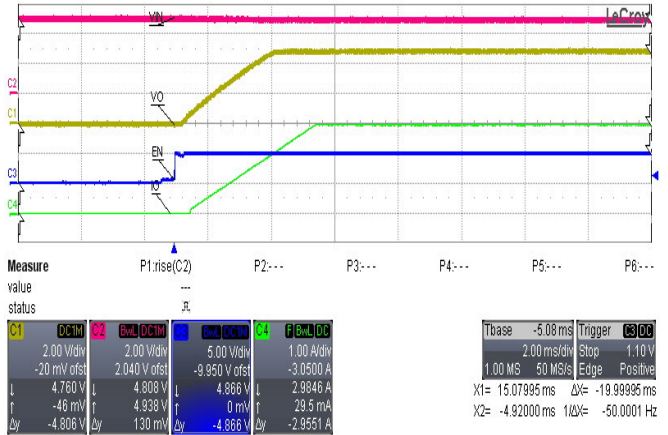
**Turn-on from Von1&Von2  
 (BOTH Channel)**



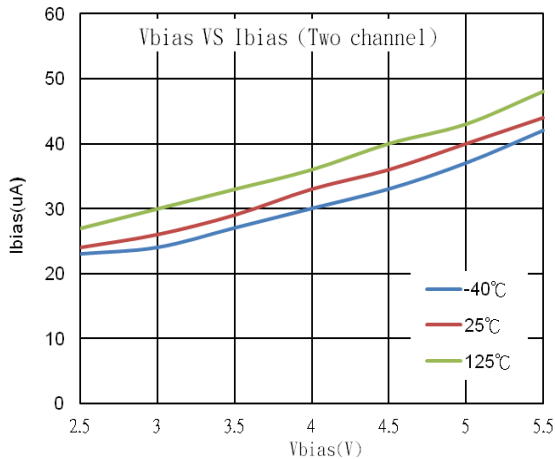
**Turn-off from Von1&Von2  
 (BOTH Channel)**



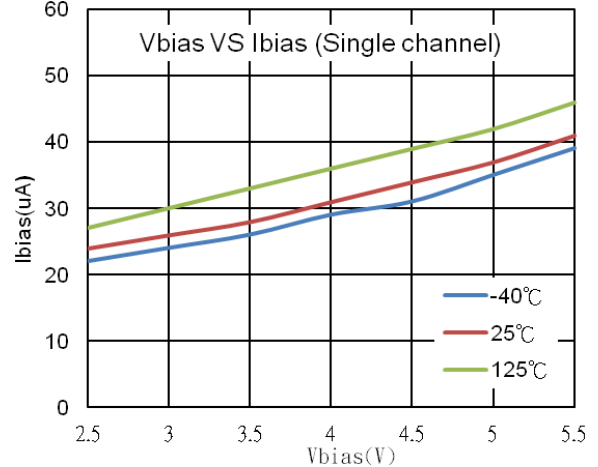
**Turn-on when Heavy load (3A)  
 (Single Channel)**



**VBIAS vs. Quiescent Current  
 (Both Channel)**

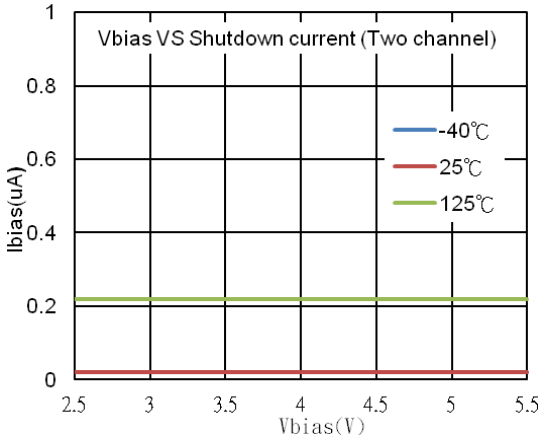


**VBIAS vs. Quiescent Current  
 (Single Channel)**

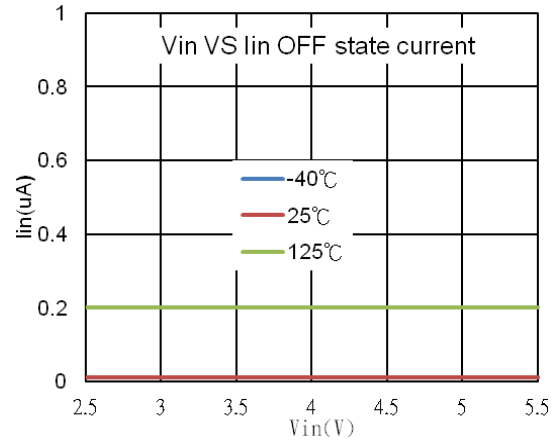




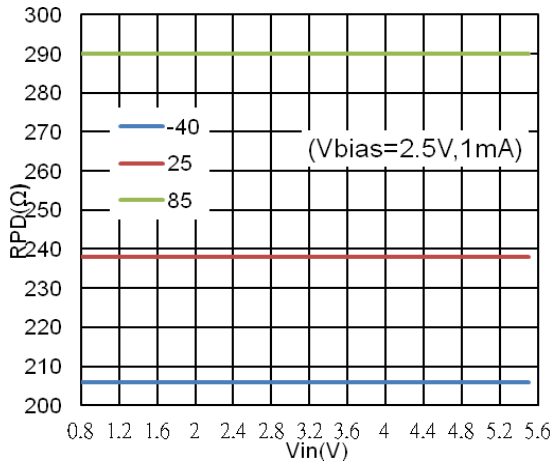
VBIAS vs. Shutdown Current  
(Both Channel)



VIN vs. OFF-State Supply Current



VIN vs. RPD  
(VBIAS=2.5V)



## Functional Description

### On-Resistance

The MOSFET gate voltage in the EM5208 is driven by an internal charge pump. The output voltage of the charge pump is dependent on the voltage on VBIAS pin. Care must be taken to ensure a sufficient VBIAS is used to keep the desired Ron when given the anticipated input voltage.

### ON/OFF Control

EM5208 is enabled if the voltage of the Von pin is greater than logic high level and the VBIAS voltage has an adequate applied. If the voltage of the EN pin is less than logic low level, the device will be disabled.

### Input Capacitor

The EM5208 do not require an input capacitor. In order to limit the voltage drop on the input supply caused by transient inrush current, an input bypass capacitor is recommended. A 1uF ceramic capacitor should be placed as closed as possible to the VIN pin. Higher values capacitor can help to further reduce the voltage drop.

### Output Capacitor

Due to the integrated body diode in the NMOS switch, the CIN greater than Co is highly recommended. A CIN to Co ratio of 10 to 1 is recommended for minimizing VIN drop caused by inrush during startup. It also helps to prevent parasitic inductance forces Vo below GND when switching off. Output capacitor has minimal affect on device's turn on slew rate time.

### Slew Rate Control

The slew rate of each channel output voltage can be controlled by the capacitor on the CT pin to GND which provides soft start functionality. This limits the inrush current caused by capacitor charging.

## Thermal and Layout Consideration

EM5208 is designed to maintain a constant output load current. Due to physical limitations of the chip layout and assembly of the device the maximum switch current is 4A for each channel, the figure below show an example of typical PCB layout. All copper traces for the VIN and Vo pin should be widely and short to carry the maximum continuous current and obtain the best effect. The input and output capacitor (option) should be close to the device as possible to minimize the parasitic trace inductances and prevents the voltage drop when load transient.

The maximum IC junction temperature should be restricted to 125 °C under normal operating conditions. To calculate the maximum allowable dissipation, PD(MAX) for a given output current and ambient temperature, used the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

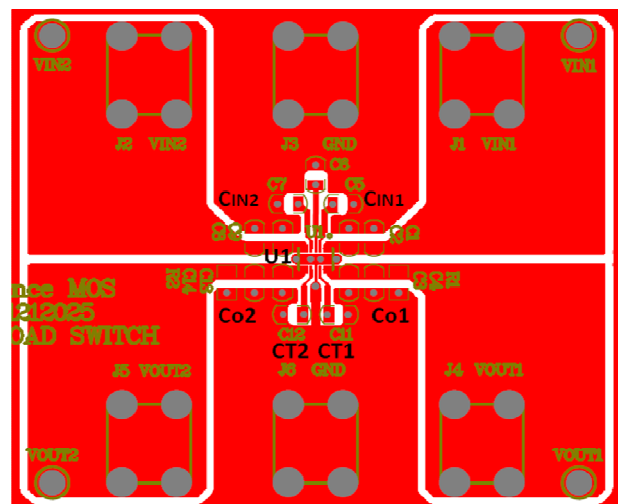
Where:

PD(MAX)=Maximum allowable power dissipation

TJ(MAX)=Maximum allowable junction temperature (125 °C for the EM5208)

TA=Ambient Temperature of the device

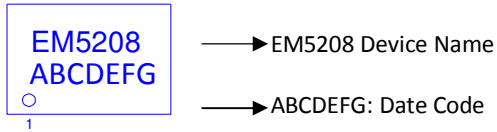
θJA= Junction to air thermal impedance. This parameter is also dependent upon PCB layout.



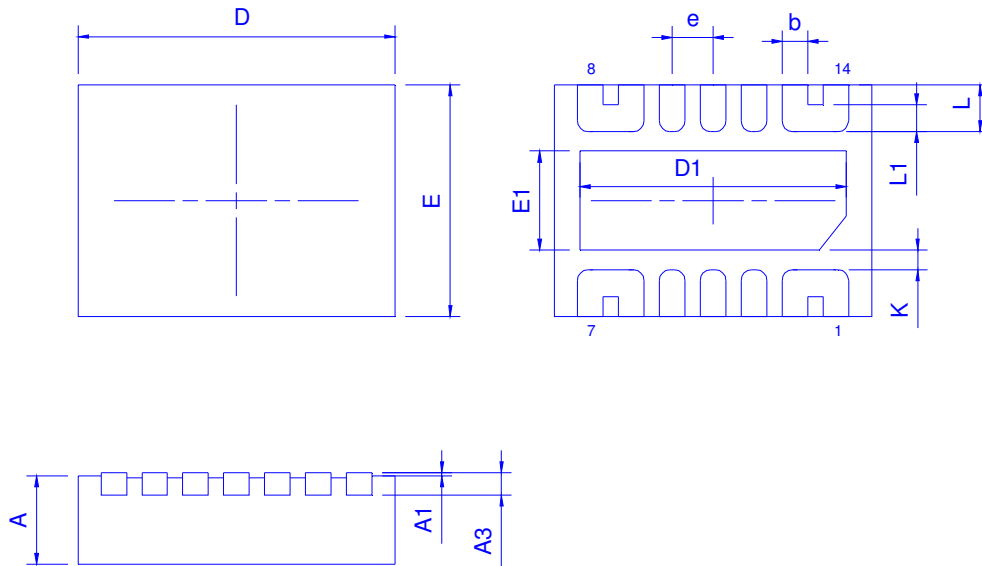


**Marking Information**

Device Name: EM5208VF for DFN3X2-14L



**Outline Drawing**



Dimension in mm

Dimension	A	A1	A3	b	D	E	D1	E1	e	L	K
Min.	0.7	0.00		0.13	2.9	1.9	2.4	0.7	0.3	0.200	0.15
Typ.			0.203		3.0	2.0					
Max.	0.8	0.05		0.25	3.1	2.1	2.6	1.0	0.5	0.426	0.35