

# FDD3570

# 80V N-Channel PowerTrench® MOSFET

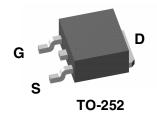
## **General Description**

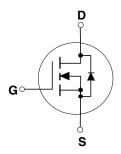
This N-Channel Logic level MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

This MOSFET features faster switching and lower gate change than other MOSFETs with comparable  $R_{\rm DS(ON)}$  specifications resulting in DC/DC power supply designs with higher overall efficiency.

#### **Features**

- 10 A, 80 V.  $R_{DS(ON)} = 0.019 \Omega @ V_{GS} = 10 V$  $R_{DS(ON)} = 0.022 \Omega @ V_{GS} = 6 V.$
- Fast switching speed.
- High performance trench technology for extremely low  $R_{\mbox{\scriptsize DS(ON)}}$  .
- High power and current handling capability.





# **Absolute Maximum Ratings**

T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage	80	V
V <sub>GSS</sub>	Gate-Source Voltage	± 20	V
I <sub>D</sub>	Maximum Drain Current-Continuous (Note 1)	43	A
	(Note 1a)	10	
	Maximum Drain Current – Pulsed	110	
P <sub>D</sub>	Maximum Power Dissipation @T <sub>C</sub> = 25°C (Note 1)	69	W
	$T_A = 25^{\circ}C$ (Note 1a)	3.4	
	$T_A = 25^{\circ}C$ (Note 1b)	1.3	
T <sub>J</sub> , T <sub>stg</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C

# **Thermal Characteristics**

R <sub>eJC</sub>	Thermal Resistance, Junction-to- Case	(Note 1)	1.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to- Ambient	(Note 1a)	37	°C/W
		(Note 1b)	96	°C/W

**Package Marking and Ordering Information** 

Device Marking	Device	Reel Size	Tape width	Quantity
FDD3570	FDD3570	13"	16mm	2500

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics		I	I		
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	80			V
ΔBV <sub>DSS</sub> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^{\circ}\text{C}$		78		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 64 \text{ V}, \qquad V_{GS} = 0 \text{ V}$			1	μΑ
I <sub>GSSF</sub>	Gate–Body Leakage Current, Forward	$V_{GS} = 20 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			100	nA
I <sub>GSSR</sub>	Gate–Body Leakage Current, Reverse	$V_{GS} = -20 \text{ V}$ $V_{DS} = 0 \text{ V}$			-100	nA
On Chara	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	2	2.4	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}, \text{Referenced to } 25^{\circ}\text{C}$		-7		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	$V_{GS} = 10 \text{ V},  I_D = 10 \text{ A}$ $V_{GS} = 10 \text{ V},  I_D = 10 \text{ A}, T_J = 125^{\circ}\text{C}$ $V_{GS} = 6 \text{ V},  I_D = 9 \text{ A}$		0.015 0.027 0.016	0.019 0.038 0.022	Ω
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = 6 \text{ V}, I_D = 9 \text{ A}$ $V_{GS} = 10 \text{ V}, V_{DS} = 5 \text{ V}$	25			Α
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 5 \text{ V}, \qquad I_{D} = 14 \text{ A}$		40		S
Dvnamic	Characteristics		•	•	•	
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 40 \text{ V}, \qquad V_{GS} = 0 \text{ V},$		2800		pF
Coss	Output Capacitance	f = 1.0 MHz		230		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			117		pF
Switchine	g Characteristics (Note 2)			•	•	
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 40 \text{ V}, \qquad I_D = 1 \text{ A},$		20	32	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, \qquad R_{GEN} = 6 \Omega$		12	24	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			60	95	ns
t <sub>f</sub>	Turn-Off Fall Time			24	38	ns
Qg	Total Gate Charge	$V_{DS} = 40V$ , $I_{D} = 9 A$ ,		54	76	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V		9.6		nC
Q <sub>gd</sub>	Gate-Drain Charge			14		nC
Drain-So	urce Diode Characteristics a	nd Maximum Ratings	•	•	•	
I <sub>s</sub>	Maximum Continuous Drain-Source	<del>_</del>			2.8	Α
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V},  I_{S} = 2.8 \text{ A}$ (Note 2)		0.72	1.2	V

#### Notes

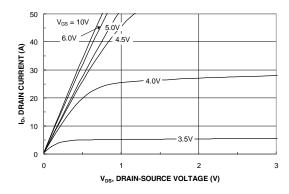
 R<sub>8JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>8JC</sub> is guaranteed by design while R<sub>9CA</sub> is determined by the user's board design.



Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width <  $300\mu s,$  Duty Cycle < 2.0%

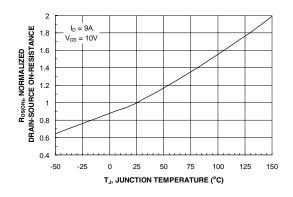
# **Typical Characteristics**



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Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.



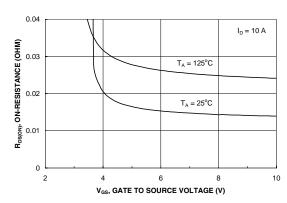
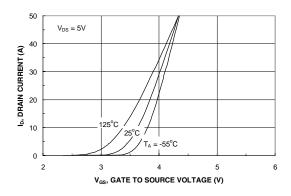


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.



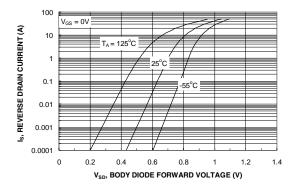
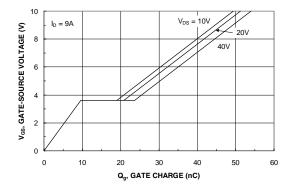


Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

# **Typical Characteristics**



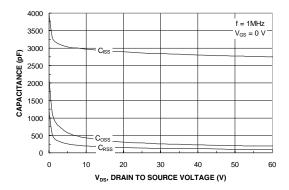
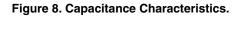
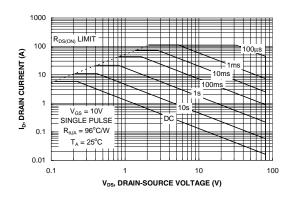


Figure 7. Gate Charge Characteristics.





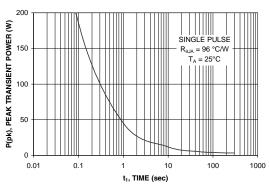


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

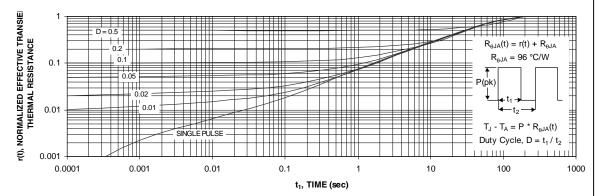
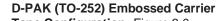


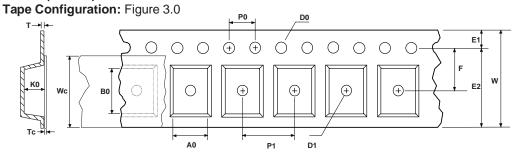
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

## TO-252 Tape and Reel Data and Package Dimensions FAIRCHILD SEMICONDUCTOR TM D-PAK (TO-252) Packaging Configuration: Figure 1.0 Packaging Description: Packaging Description: TO-252 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2500 units per 13' or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). This and some other options are further described in the Packaging Information table. Antistatic Cover Tape ESD Label These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped. Static Dissipative **Embossed Carrier Tape** F63TNR Label D-PAK (TO-252) Packaging Information Packaging Option D-PAK (TO-252) Unit Orientation Packaging type TNR Qty per Reel/Tube/Bag 2.500 Reel Size 13" Dia Box Dimension (mm) 359x359x57 5,000 Max qty per Box 359mm x 359mm x 57mm Weight per unit (gm) 0.300 Standard Intermediate box Weight per Reel(kg) 1.200 **ESD Label** F63TNR Label sample F63TNR Label D/C1: Z9942 D/C2: SPEC REV: CPN: QTY1: QTY2: TO-252 (D-PAK) Tape Leader and **Trailer Configuration:** Figure 2.0 $\bigcirc$ $\bigcirc$ $\bigcirc$ $\bigcirc$ $\bigcirc$ 0 0 0 0 Components Trailer Tape 640mm minimum or 1680mm minimum or 80 empty pockets 210 empty pockets







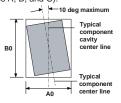
# **User Direction of Feed**

	Dimensions are in millimeter													
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	т	Wc	Тс
<b>TO252</b> (24mm)	6.90 +/-0.10	10.50 +/-0.10	16.0 +/-0.3	1.55 +/-0.05	1.5 +/-0.10	1.75 +/-0.10	14.25 min	7.50 +/-0.10	8.0 +/-0.1	4.0 +/-0.1	2.65 +/-0.10	0.30 +/-0.05	13.0 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation



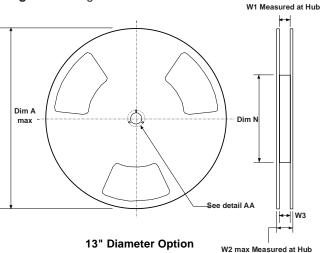
Sketch B (Top View)

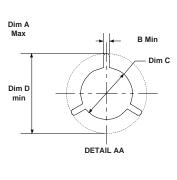
Component Rotation



Sketch C (Top View)
Component lateral movement

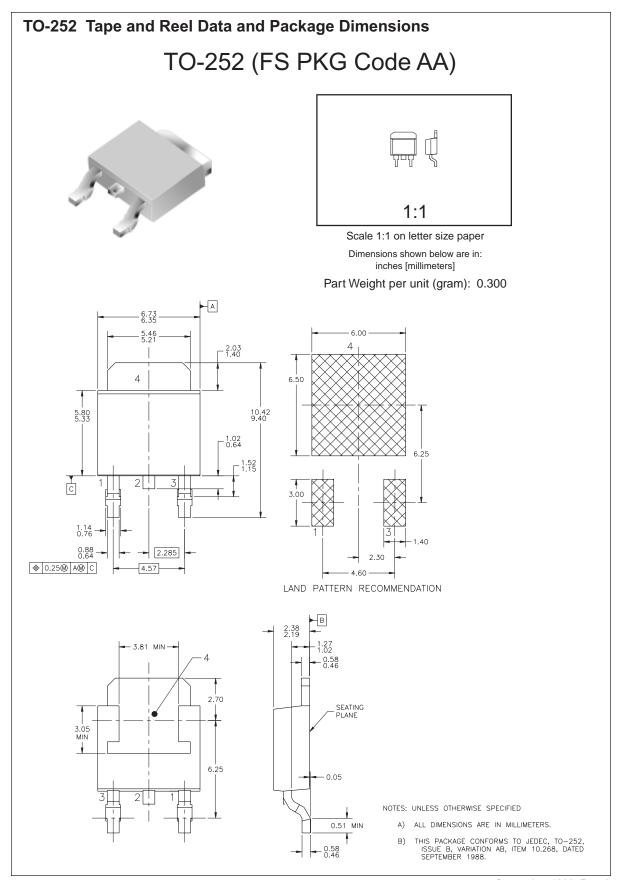
## D-PAK (TO-252) Reel Configuration: Figure 4.0





3"	Diameter Option	W2 max Measured at Hu

Dimensions are in inches and millimeters									
Tape Size Reel Option Dim A Dim B Dim C Dim D Dim N Dim W1 Dim W2 Dim W3						Dim W3 (LSL-USL)			
164mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.646 +0.078/-0.000 16.4 +2/0	0.882 22.4	0.626 - 0.764 15.9 - 19.4



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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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