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1.0   Features

- Generates one bank of ten differential 2.5V HSTL clock outputs (YP0/YN0 to YP9/YN9) from one differential HSTL reference clock input

- Meets the JEDEC Standard PLL Clock Driver for DDR Applications

- External feedback input (FBINP/FBINN) to synchronize all clock outputs to the reference input

- Operating frequency 60MHz to 170MHz

- Tight tracking skew (spread-spectrum tolerant)

- Integrated 25Ω series damping resistors for driving point-to-point loads

- Serial programming interface provides tristate control over one or more output driver pairs

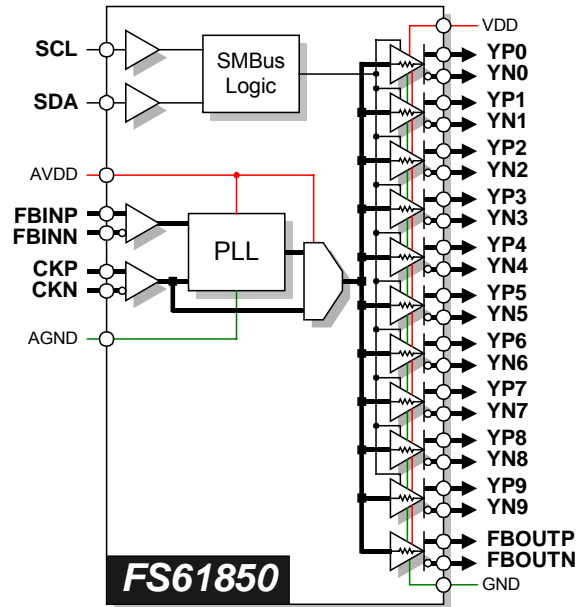- Packaged in a 48-pin TSSOP

2.0   Description

The FS61850 is a low skew, low jitter CMOS zero-delay phase-lock loop (PLL) clock buffer IC. Ten differential buffered clock outputs are derived from an onboard open-loop PLL. The PLL aligns the frequency and phase of all output clock pairs to the differential reference input clock CLKP/CLKN, including a feedback output clock pair that feeds back to FBINP/FBINN to close the loop.

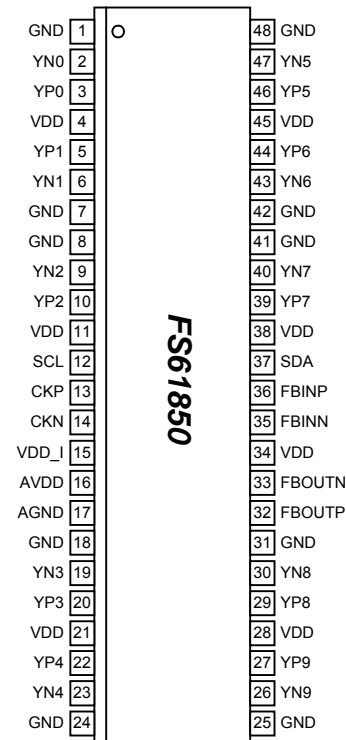The PLL can be bypassed for test purposes by pulling AVDD to ground.

Figure 1: Block Diagram

Figure 2: Pin Configuration

Table 1: Function Table

PLL	INPUT			OUTPUT			
	AVDD	**CKP**	**CKN**	**YP0-YP9**	**YN0-YN9**	**FBOUTP**	**FBOUTN**
OFF	2.5V	L	H	Z	Z	Z	Z
	2.5V	H	L	Z	Z	Z	Z
Zero-Delay	2.5V	L	H	L	H	L	H
	2.5V	H	L	H	L	H	L
OFF	GND	L	H	Z	Z	Z	Z
	GND	H	L	Z	Z	Z	Z
PLL Bypass	GND	L	H	L	H	L	H
	GND	H	L	H	L	H	L
OFF	-	<20MHz		Z	Z	Z	Z

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1:10 HSTL SMBus Zero-Delay Clock Buffer IC

Table 2: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI$_D$ = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

PIN	TYPE	NAME	DESCRIPTION
16	P	AVDD	2.5V PLL power supply / Test mode enable. This pin provides the power supply to the internal PLL. When pulled low, the PLL is by-passed and the output clocks directly follow the input clock
17	P	AGND	PLL ground
13 / 14	DI	CKP / CKN	Reference clock input (true / complementary)
36 / 35	DI	FBINP / FBINN	Feedback input (true / complementary)
32 / 33	DO	FBOUTP / FBOUTN	Feedback output (true / complementary)
12	DI	SCL	Serial interface clock
37	DIO	SDA	Serial interface data input/output
3 / 2	DO	YP0 / YN0	Clock outputs (true / complementary)
5 / 6		YP1 / YN1	
10 / 9		YP2 / YN2	
20 / 19		YP3 / YN3	
22 / 23		YP4 / YN4	
46 / 47		YP5 / YN5	
44 / 43		YP6 / YN6	
39 / 40		YP7 / YN7	
29 / 30		YP8 / YN8	
27 / 26		YP9 / YN9	
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	P	GND	Ground for all clock outputs
15	P	VDD_I	2.5V power supply for SMBus logic
4, 11, 21, 28, 34, 38, 45	P	VDD	2.5V power supply for all clock outputs

3.0   Device Operation

The FS61850 precisely aligns the frequency and phase of the differential HSTL output clocks to the differential reference input CKP/CKN by use of an on-chip phase-lock loop (PLL). The PLL generates 10 low-skew, low-jitter copies of the reference, with the outputs adjusted for 50% duty cycle.

The differential FBOUT clock must be hardwired to the FBINP/FBINN pins to complete the loop. The PLL actively adjusts the output clocks so that there is no phase error between the reference clock and the feedback input.

Since the device uses a PLL to lock the output clocks to the input clock, there is a power-up stabilization time that is required for the PLL to achieve phase lock.

Note that all inputs and outputs use 2.5V HSTL signal levels.

3.1   PLL Bypass

When the AVDD pin is pulled low, the reference clock signal bypasses the PLL and is muxed directly through to the outputs. The PLL is powered down, and device acts a fanout buffer. Note that if AVDD is re-established, the PLL requires a power-up and stabilization time to lock to the input clock.

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4.0   Programming Interface

This device supports both Block Write and Block Read commands. The device address is:

Table 3: Device Address

A6	A5	A4	A3	A2	A1	A0
1	1	0	1	0	0	1

4.1   Block Write

The Block Write command allows the Bus Host to write several bytes of data to sequential registers, starting with the Byte 0 Register. As shown in Figure 3, a Block Write starts with the seven-bit device address followed by a logic-low R/W bit.

According to SMBus protocol, a command code containing all zeroes (0000 0000) and a byte count describing the number of data bytes to be written should be issued by the Bus Host after the acknowledge handshake.

This device, however, ignores both the byte count and the command code.

After a device acknowledge of the byte count, data bytes are written sequentially, starting with the Byte 0 Register and incrementing in order. An acknowledge between each byte of data must occur before the next data byte is sent.

After the last byte is written, any additional byte information sent to the device wraps around and starts rewriting information contained in Byte 0.
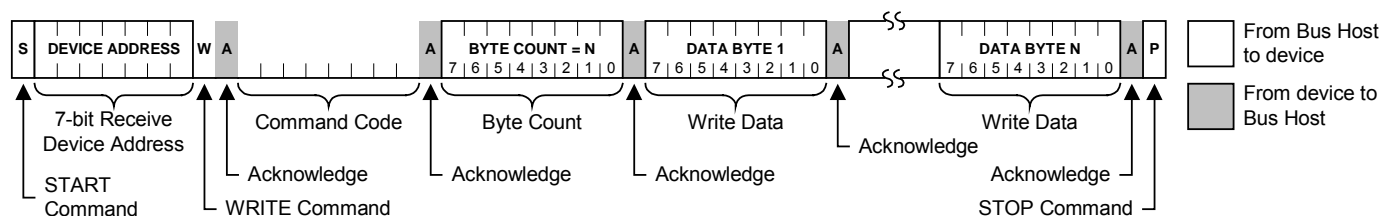
4.2   Block Read

The Block Read command, shown in Figure 4, permits the Bus Host to read several bytes of data from sequential registers, starting by default at the Byte 0 Register. To begin a Block Read, the seven-bit device address is sent from the Host, followed by a logic-high R/W bit.

Note that a repeated START command is not required to initiate a Block Read.

After an acknowledgement of the byte count this device takes command of the bus and transmits all the data beginning the Byte 0 Register. After the last byte of data, the Bus Host should generate a "not-acknowledge," followed by a STOP command.

Without a STOP command, any additional read requests after reading the last byte wrap around and begin re-reading information contained in Byte 0. If the host does not want to receive all the data contained in the device, the host should not-acknowledge the last desired data byte and issue a STOP command on the next clock.

Figure 3: Block Write

Figure 4: Block Read
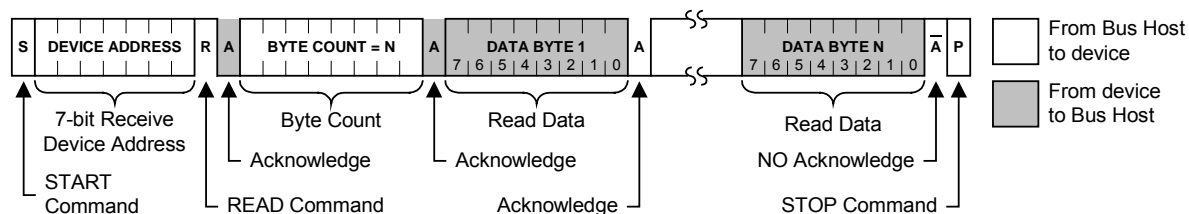
4.3   Register Programming

A logic-one written to a valid bit location enables (turns on) the assigned output clock. Likewise, a logic-zero written to a valid bit location disables (turns off) the assigned output clock.

Any unused or reserved register bits should be cleared to zero. Serial bits are written to this device starting with Byte 0 and proceeding higher. Bit 7 of each byte is written first, and bits are written to in descending order down to Bit 0.

Table 4: Byte 0 Register

BIT	DESCRIPTION		PIN	RW
7	**YP0 / YN0 Control**		3, 2	RW
	0 = Outputs Tristated	1 = Outputs Enabled		
6	**YP1 / YN1 Control**		5, 6	RW
	0 = Outputs Tristated	1 = Outputs Enabled		
5	**YP2 / YN2 Control**		10, 9	RW
	0 = Outputs Tristated	1 = Outputs Enabled		
4	**YP3 / YN3 Control**		20, 19	RW
	0 = Outputs Tristated	1 = Outputs Enabled		
3	**YP4 / YN4 Control**		22, 23	RW
	0 = Outputs Tristated	1 = Outputs Enabled		
2	**YP5 / YN5 Control**		46, 47	RW
	0 = Outputs Tristated	1 = Outputs Enabled		
1	**YP6 / YN6 Control**		44, 43	RW
	0 = Outputs Tristated	1 = Outputs Enabled		
0	**YP7 / YN7 Control**		39, 40	RW
	0 = Outputs Tristated	1 = Outputs Enabled		

Shaded areas indicate default settings

Table 5: Byte 1 Register

BIT	DESCRIPTION		PIN	RW
7	**YP8 / YN8 Control**		29, 30	RW
	0 = Outputs Tristated	1 = Outputs Enabled		
6	**YP9 / YN9 Control**		27, 26	RW
	0 = Outputs Tristated	1 = Outputs Enabled		
5	**Reserved**: Always write this bit to 0		-	R
	0 = Default			
4	**Reserved**: Always write this bit to 0		-	R
	0 = Default			
3	**Reserved**: Always write this bit to 0		-	R
	0 = Default			
2	**Reserved**: Always write this bit to 0		-	R
	0 = Default			
1	**Reserved**: Always write this bit to 0		-	R
	0 = Default			
0	**Reserved**: Always write this bit to 0		-	R
	0 = Default			

Shaded areas indicate default settings

5.0 Electrical Specifications

Table 6: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage, dc, Clock Buffers (GND = ground)	AV_{DD}	GND-0.5	4	V
Supply Voltage, dc, Core	V_{DD}	GND-0.5	4	V
Input Voltage, dc	V_I	GND-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	GND-0.5	V_{DD}+0.5	V
Input Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{IK}	-50	50	mA
Output Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV

CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 7: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	AV_{DD}	Core	2.3	2.5	2.7	V
	V_{DD}	Outputs	2.3	2.5	2.7	
Ambient Operating Temperature Range	T_A		0		70	°C
Input Frequency (CKP / CKN)	f_{CLK}	Frequency range over which PLL acquires lock	60		170	MHz
		Frequency range where all timing parameter specification are met	90		170	
Input Duty Cycle		CKP / CKN	40		60	%
Input Rise/Fall Time	t_r, t_f	CKP / CKN (over 20% to 80%)	0.375		1.5	ns
Spread-Spectrum Modulation Frequency	f_m		30		50	MHz
Spread-Spectrum Modulation Index	δ_m		0		-0.5	%
Output Load Capacitance	C_L				15	pF
Serial Data Transfer Rate			10		100	kb/s

ISO9001
QS9000

Table 8: DC Electrical Specifications

Unless otherwise stated, all power supplies = 2.5V, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are $\pm 3\sigma$ from typical. Negative currents indicate current flows out of the device.

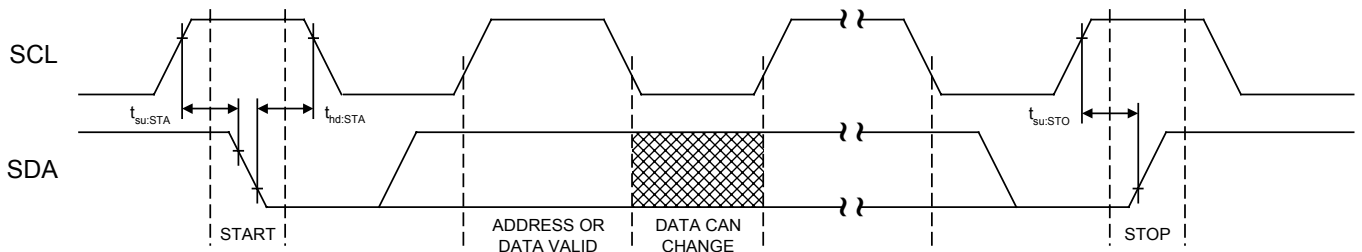| PARAMETER	SYMBOL		CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall							
Supply Current, Dynamic, with Loaded Outputs	I_{DD}		V_{DD} = 2.7V, f_{CLK} = 170MHz		200	300	mA
Supply Current, Static	I_{DDL}		V_{DD} = 2.7V, PWRDWN# low or f_{CLK} < 20MHz			100	µA
SCL, SDA Serial Interface I/O							
High-Level Input Voltage	V_{IH}	Input		1.67		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}			GND-0.3		0.833	V
Hysteresis Voltage	V_{hys}				0.833		V
Input Leakage Current	I_I			-10		10	µA
Low-Level Output Sink Current (SDA)	I_{OL}		V_{OH} = 0.4V, V_{DD} = 2.7V				mA
Differential Clock Inputs (CKP, CKN, FBINP, FBINN)							
Input Voltage Level	V_{IN}			GND-0.3		V_{DD}+0.3	V
Crossover Voltage	V_{IX}			V_{DD}/2 -0.2		V_{DD}/2 +0.2	V
Differential Voltage	V_{ID}		Magnitude of the difference between the input level on CKP and the input level on CKN	0.36		V_{DD}+0.6	
Input Leakage Current	I_I		V_{DD} = 2.7V	-10		10	µA
Input Loading Capacitance *	$C_{L(in)}$		V_I = 0V, as seen by an external clock driver	2.5		3.5	pF
Differential Clock Outputs (YP0:9, YN0:9, FBOUTP, FBOUTN)							
High-Level Output Source Current	I_{OH}		V_{DD} = 2.3V, V_O = 1.7V			-12	mA
			V_{DD} = 2.3V, V_O = 2.2V	-100			µA
Low-Level Output Sink Current	I_{OL}		V_{DD} = 2.3V, V_O = 0.6V			12	mA
			V_{DD} = 2.3V, V_O = 0.1V	100			µA
Crossover Voltage	V_{OX}			V_{DD}/2 -0.2		V_{DD}/2 +0.2	
Differential Voltage	V_{OD}		Magnitude of the difference between the output levels on YP0:9, FBOUTP and the output levels on YN0:9, FBOUTN	0.70		V_{DD}+0.6	
Output Impedance	z_O		Measured at 1.25V, output driving low				Ω
	z_{OL}		Measured at 1.25V, output driving high				
Tristate Output Current	I_{OZ}			-5		5	µA
Short Circuit Source Current *	I_{OSH}		V_O = 0V; shorted for 30s, max.				mA
Short Circuit Sink Current *	I_{OSL}		V_O = 2.5V; shorted for 30s, max.				mA

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Table 9: AC Timing Specifications
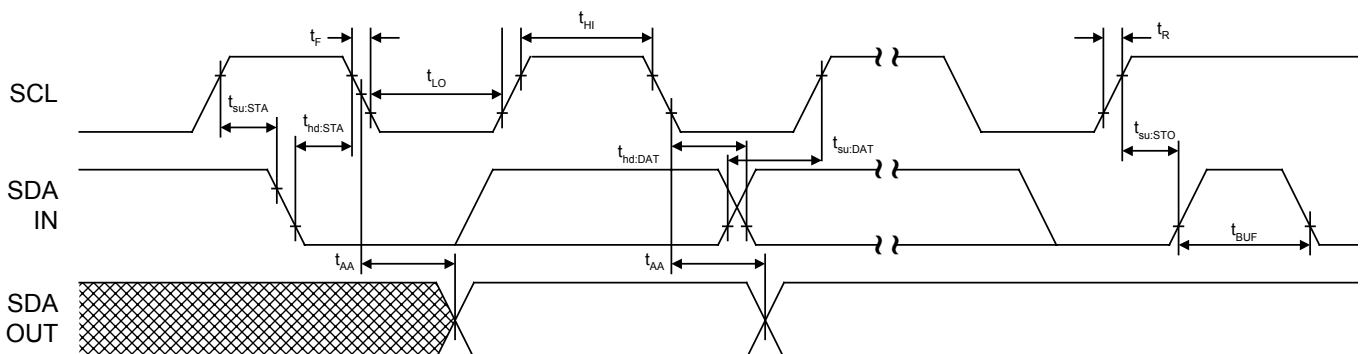
Unless otherwise stated, all power supplies = 2.5V, no load on any output, and ambient temperature T_A = 25°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are $\pm 3\sigma$ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Clock Skew, Output to Output *	$t_{sk(o)}$	Measured V_X between two output pairs C_L = 15pF				ps
Dynamic Phase Offset	$t_{d\Phi}$	Spread modulation ON				ps
		Spread modulation ON				
Static Phase Offset	t_{Φ}	Does not include jitter	-120		120	ps
Clock Stabilization Time *		Time required for the PLL to achieve phase lock				ms
Phase-Lock Loop						
Loop Bandwidth *		For calculation of Tracking Skew	2.0			MHz
Phase Angle *		For calculation of Tracking Skew			-0.031	°
Phase Error *		From rising edge on CLK to rising edge on FBIN				ps
Clock Outputs (1Y0:9, FBOUT)						
Duty Cycle *	d_t		45		55	%
Jitter, Cycle-cycle * (peak-peak)	$t_{j(CC)}$		-75		75	ps
Jitter, Period * (peak-peak)	$t_{j(\Delta P)}$		-75		75	ps
Jitter, Half-Period * (peak-peak)	$t_{j(\Delta \frac{1}{2}P)}$		-100		100	ps
Rise Time *	t_r	V_O = 0.5V to 2.0V; C_L = 15pF	0.75		1.5	ns
Fall Time *	t_f	V_O = 2.0V to 0.5V; C_L = 15pF	0.75		1.5	ns
Enable Delay *	t_{DLH}	via PWRDWN#				ns
Disable Delay *	t_{DHL}	via PWRDWN#				ns

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Table 10: Serial Interface Timing Specifications

Unless otherwise stated, all power supplies = 2.5V, no load on any output, and ambient temperature T_A = 25°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are $\pm 3\sigma$ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	STANDARD MODE		UNITS
			MIN.	MAX.	
Clock frequency	f_{SCL}	SCL	0	100	kHz
Bus free time between STOP and START	t_{BUF}		4.7		µs
Set up time, START (repeated)	$t_{su:STA}$		4.7		µs
Hold time, START	$t_{hd:STA}$		4.0		µs
Set up time, data input	$t_{su:DAT}$	SDA	250		ns
Hold time, data input	$t_{hd:DAT}$	SDA	0		µs
Output data valid from clock	t_{AA}	Minimum delay to bridge undefined region of the fall-ing edge of SCL to avoid unintended START or STOP		3.5	µs
Rise time, data and clock	t_r	SDA, SCL		1000	ns
Fall time, data and clock	t_f	SDA, SCL		300	ns
High time, clock	t_{HI}	SCL	4.0		µs
Low time, clock	t_{LO}	SCL	4.7		µs
Set up time, STOP	$t_{su:STO}$		4.0		µs

Figure 5: Bus Timing Data

Figure 6: Data Transfer Sequence

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1:10 HSTL SMBus Zero-Delay Clock Buffer IC

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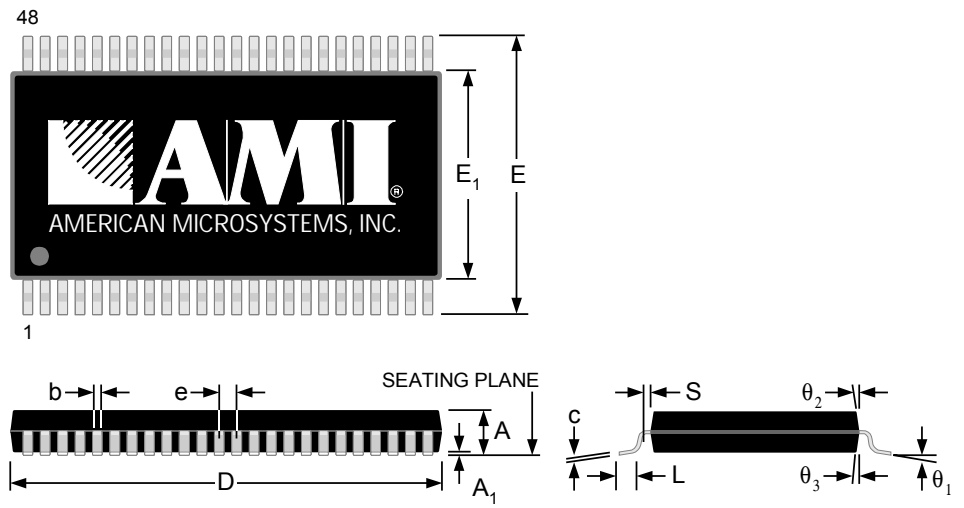
6.0   Package Information

Table 11: 48-pin TSSOP (6.1mm) Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	-	0.047	-	1.20
A_1	0.002	0.006	0.05	0.15
b	0.0067	0.011	0.17	0.27
c	0.0035	0.008	0.09	0.20
D	0.488	0.496	12.40	12.60
E	0.318 BSC		8.10 BSC	
E_1	0.236	0.244	6.00	6.20
e	0.019 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
S	0.008	-	0.20	-
θ_1	0°	8°	0°	8°
θ_2	12° REF		12° REF	
θ_3	12° REF		12° REF	

Table 12: 48-pin TSSOP (6.1mm) Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{JA}	Air flow = 0 m/s	89	°C/W
Lead Inductance, Self	L_{11}	Longest lead	3.50	nH
Lead Inductance, Mutual	L_{12}	Longest lead to any 1st adjacent lead	1.82	nH
	L_{13}	Longest lead to any 2nd adjacent lead	1.17	
Lead Capacitance, Bulk	C_{11}	Longest lead to V_{SS}	0.63	pF
Lead Capacitance, Mutual	C_{12}	Longest lead to any 1st adjacent lead	0.30	pF
	C_{13}	Longest lead to any 2nd adjacent lead	0.03	

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7.0   Ordering Information

Table 13: Device Ordering Codes

DEVICE NUMBER	ORDERING CODE	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
FS61850-01	**13810-802**	48-pin TSSOP (Thin Shrink Small Outline Package)	0° C to 70° C (Commercial)	Tape and Reel

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