HL15203

LCD Driver IC

Preliminary

2Q. 1999

Hyundai Electronics Industries

System IC Division

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1. General Description

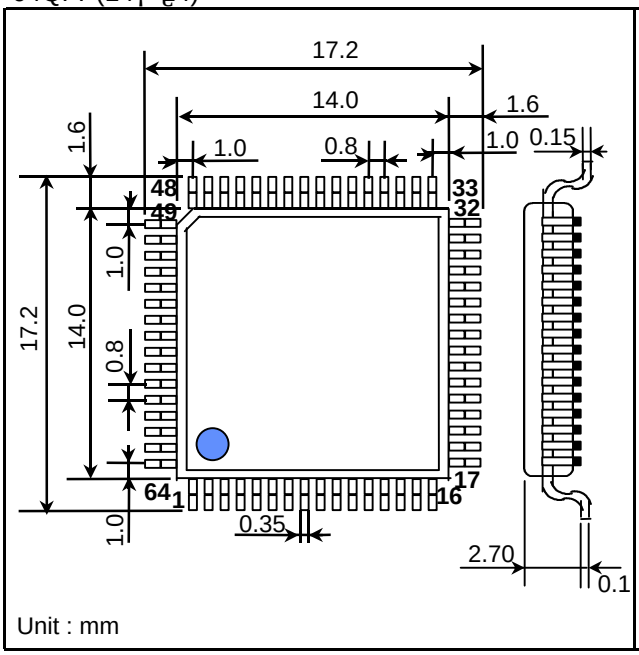
The HL15203 is 1/3 duty LCD display driver. It can drive directly maximum 156 segments.

2. Features

- LCD display ..... 52 segments x 3 commons
  1/3 duty - 1/2 bias
  1/3 duty - 1/3 bias
- Power down mode ..... Sleep mode and all segments off mode
- Serial I/O ..... Data transfer and receive
- RC oscillator
- Package 64QFP

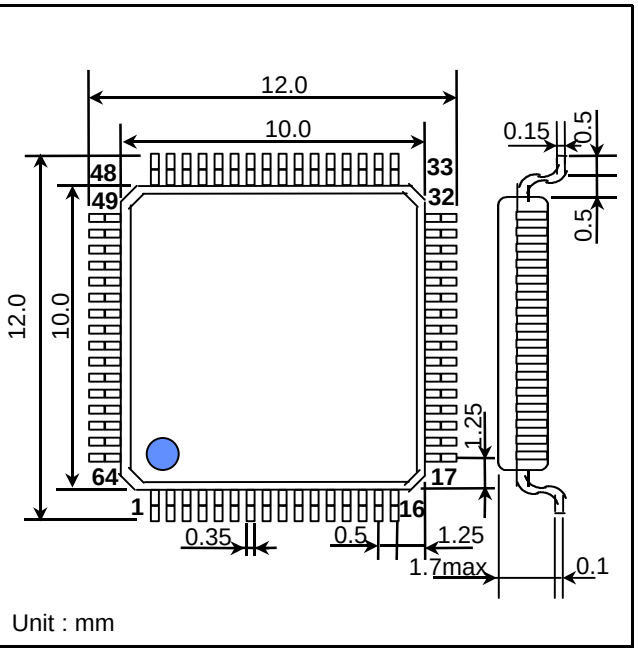
Package Dimensions

64QFP(14¡ ¿14)



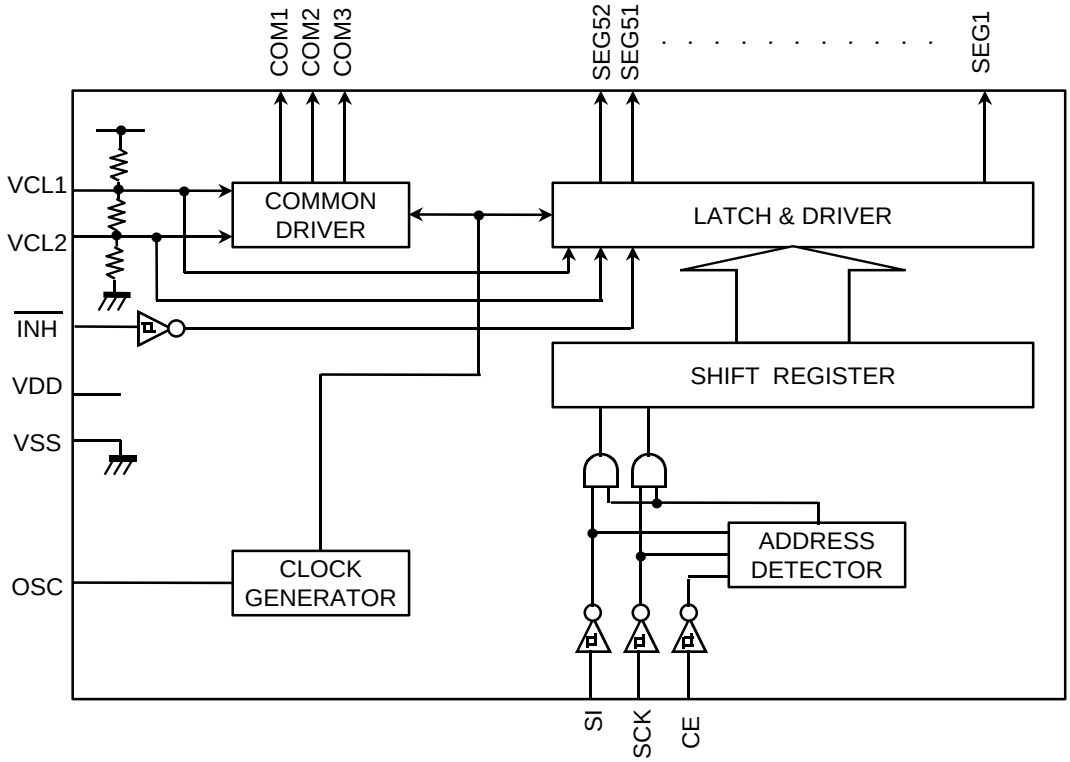
Unit : mm

64QFP(12¡ ¿12)

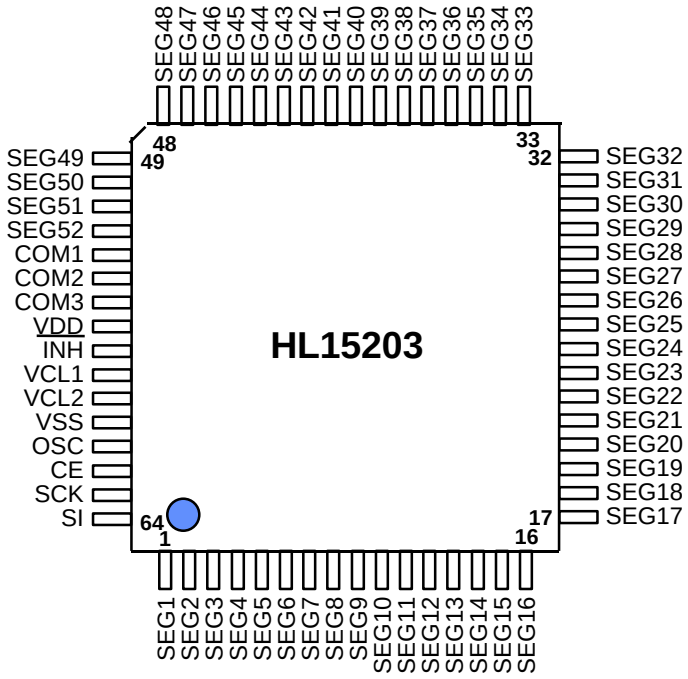


Unit : mm

3. Block Diagram



4. Pin Diagram

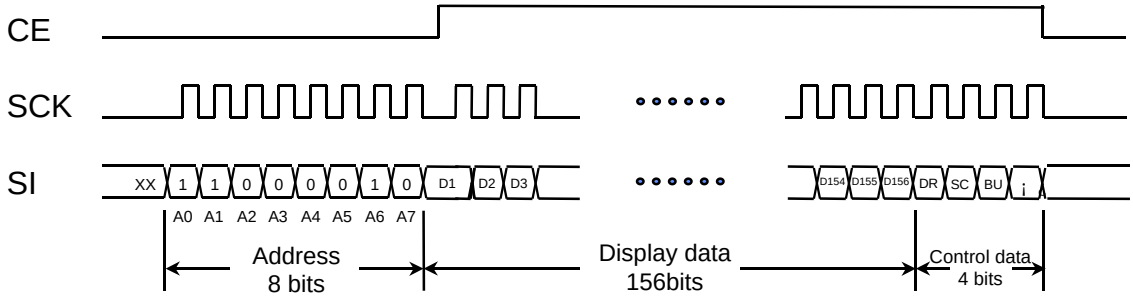


5. Pin Description

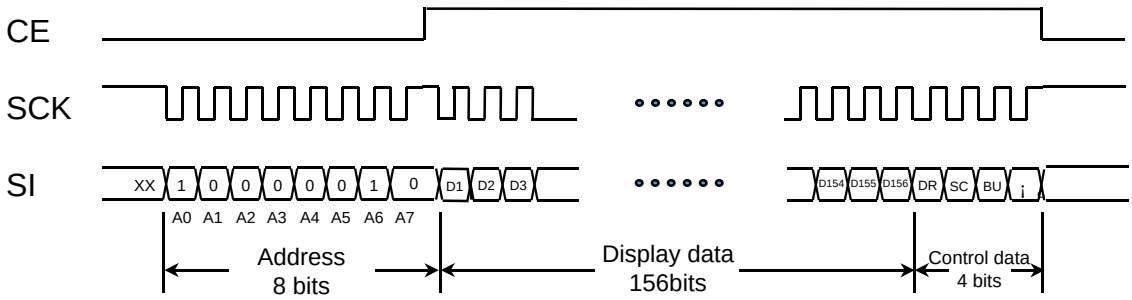
PIN Name	I/O	Pin Number	Contents
SEG[52:1]	O	52	LCD SEG Pins
COM [3:1]	O	3	LCD Common Pins
VCL[2:1]	I	2	LCD Bias Pins
OSC	I	1	Oscillator Input Pin
CE	I	1	Serial I/O Control Pin
SCK	I	1	Serial I/O Clock Pin
SI	I	1	Serial I/O Data Input Pin
$\overline{\text{INH}}$	I	1	Display off control pin
VDD	I	1	Power Supply Pin
VSS	I	1	Ground Pin

DATA Writing

i) SCK is stopped at the low level



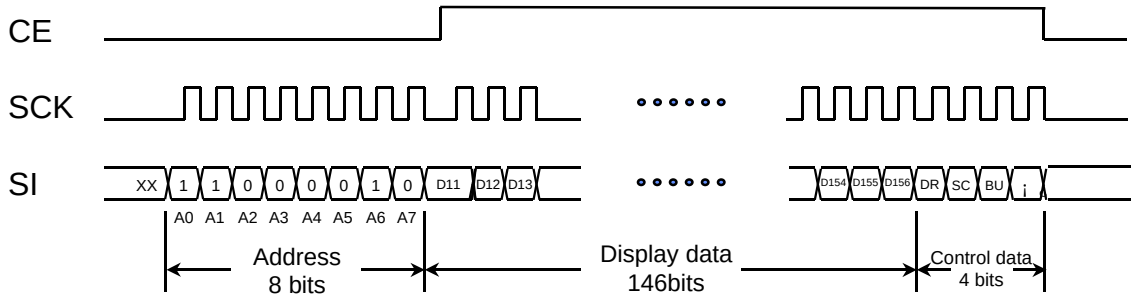
ii) SCK is stopped at the high level



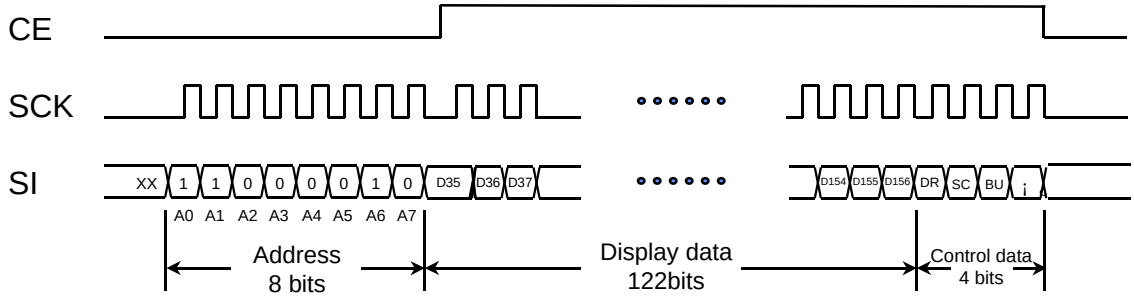
ADDRESS : 41H
D1 ~ D156 : Display data
Dn(n=1~156)=1 … … … Display on
Dn(n=1~156)=0 … … … Display off
DR : 1/2-bias drive or 1/3-bias drive switching control data
SC : Segments on/off control data
BU : Normal mode/power-saving mode control data

DATA Writing Examples

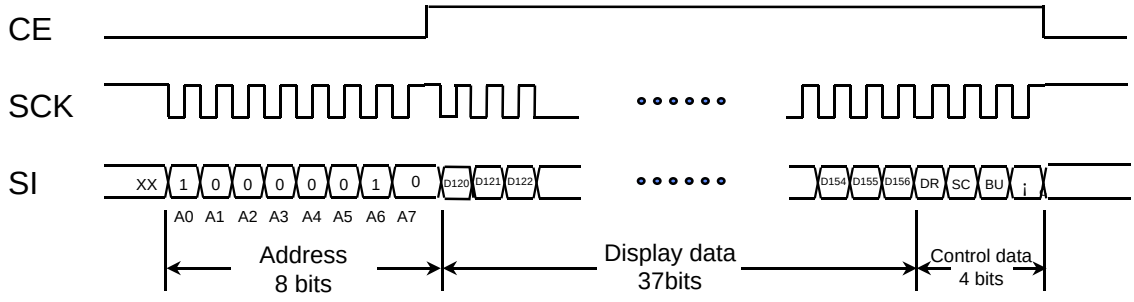
i) When 146 segments are used 146bits of display data (D11 to D156) must be sent.



ii) When 122 segments are used 122bits of display data (D35 to D156) must be sent.



iii) When 37 segments are used 37bits of display data (D120 to D156) must be sent.



7. Registers

1) Display Registers

Output Pin	COM3	COM2	COM1
SEG1	D1	D2	D3
SEG2	D4	D5	D6
SEG3	D7	D8	D9
SEG4	D10	D11	D12
SEG5	D13	D14	D15
SEG6	D16	D17	D18
SEG7	D19	D20	D21
SEG8	D22	D23	D24
SEG9	D25	D26	D27
SEG10	D28	D29	D30
SEG11	D31	D32	D33
SEG12	D34	D35	D36
SEG13	D37	D38	D39
SEG14	D40	D41	D42
SEG15	D43	D44	D45
SEG16	D46	D47	D48
SEG17	D49	D50	D51
SEG18	D52	D53	D54
SEG19	D55	D56	D57
SEG20	D58	D59	D60
SEG21	D61	D62	D63
SEG22	D64	D65	D66
SEG23	D67	D68	D69
SEG24	D70	D71	D72
SEG25	D73	D74	D75
SEG26	D76	D77	D78
SEG27	D79	D80	D81
SEG28	D82	D83	D84
SEG29	D85	D86	D87
SEG30	D88	D89	D90
SEG31	D91	D92	D93
SEG32	D94	D95	D96
SEG33	D97	D98	D99
SEG34	D100	D101	D102
SEG35	D103	D104	D105
SEG36	D106	D107	D108
SEG37	D109	D110	D111
SEG38	D112	D113	D114
SEG39	D115	D116	D117
SEG40	D118	D119	D120
SEG41	D121	D122	D123
SEG42	D124	D125	D126

Output Pin	COM3	COM2	COM1
SEG43	D127	D128	D129
SEG44	D130	D131	D132
SEG45	D133	D134	D135
SEG46	D136	D137	D138
SEG47	D139	D140	D141
SEG48	D142	D143	D144
SEG49	D145	D146	D147
SEG50	D148	D149	D150
SEG51	D151	D152	D153
SEG52	D154	D155	D156

2) Control Registers

i) 1/2-bias drive or 1/3-bias drive switching control data

DR	Bias Selection
0	1/3 Bias
1	1/2 Bias

ii) Segments on/off control data

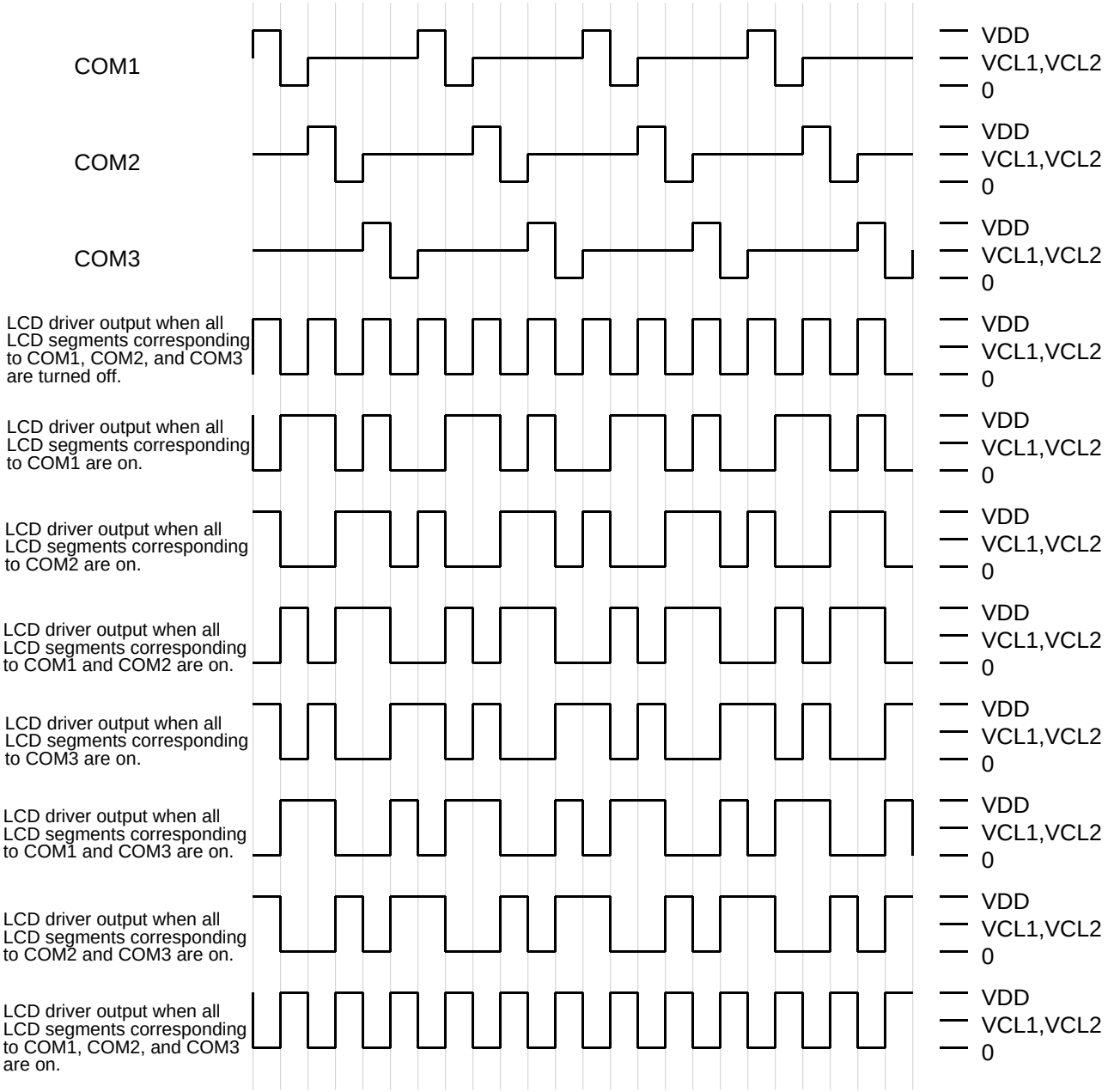
Control Data	Display Status
SC	SEG1 ~ SEG52
0	On
1	Off

iii) Normal mode/power-saving mode control data

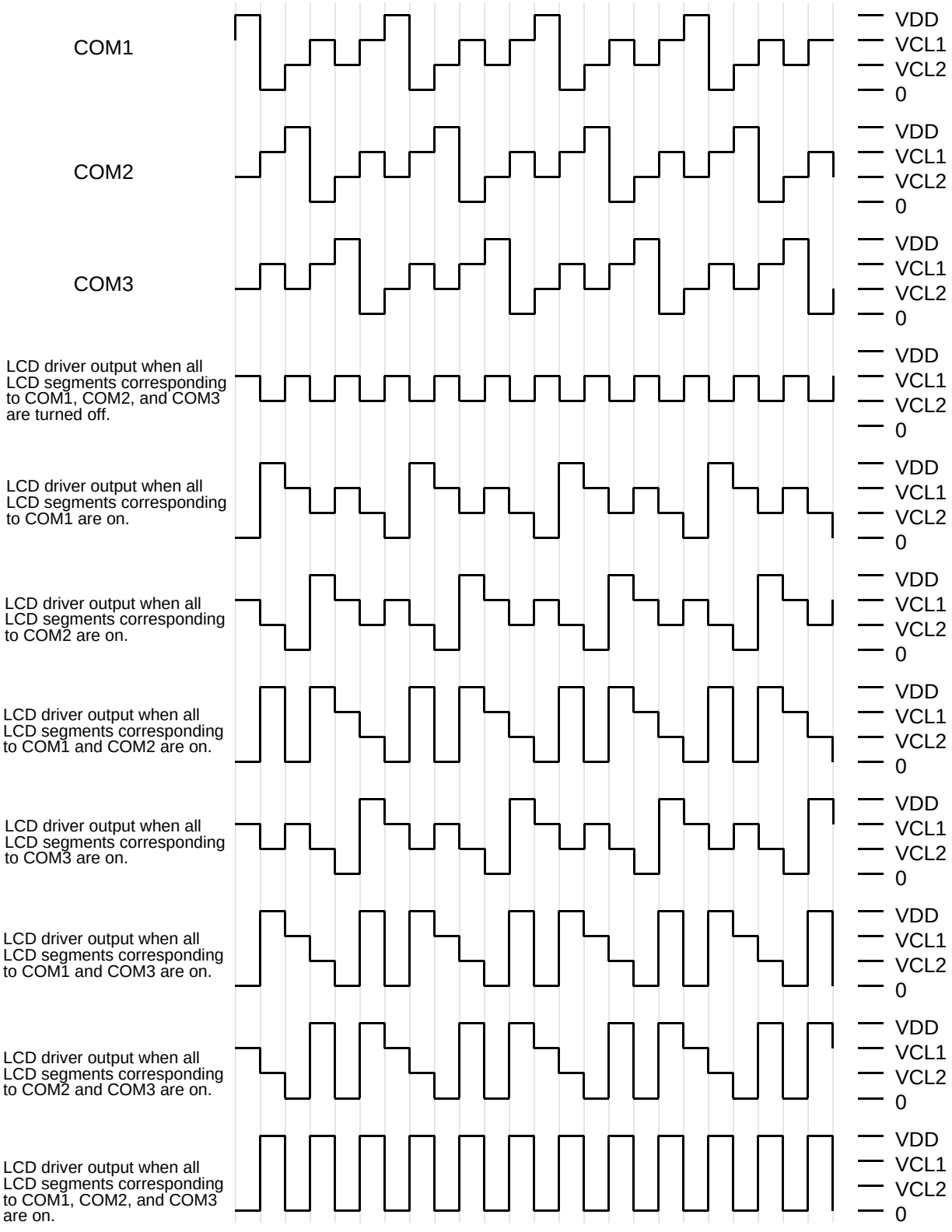
BU	Mode
0	Normal Mode
1	Power-saving mode. In this mode the OSC pin oscillator is stopped and the common and segment pins output Vss levels.

9. LCD Display Function

1) 1/2 Bias, 1/3 Duty Waveforms

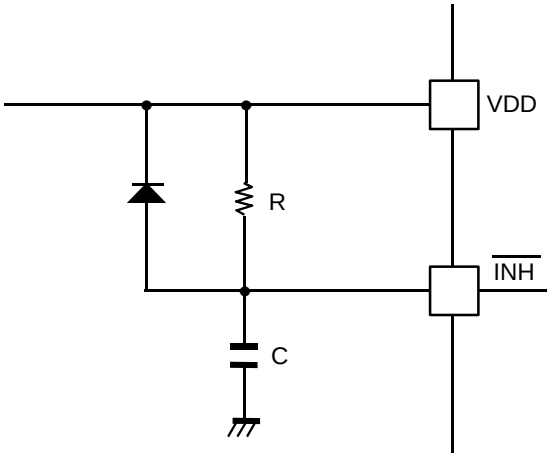


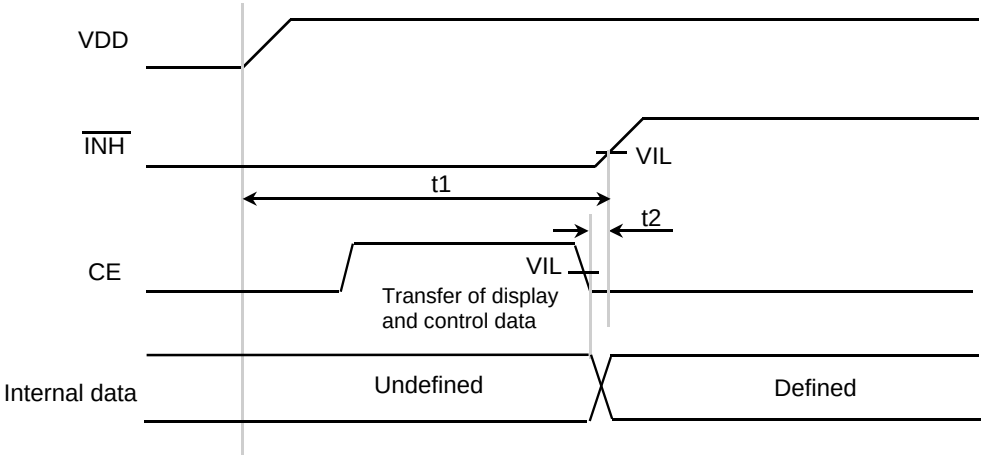
2) 1/3 Duty 1/3 Bias Waveforms



10. $\overline{\text{INH}}$ and Display Control

Since the LSI internal data (D1 to D156, DR, SC, and BU) is undefined when power is first applied, then display is off(SEG1 to SEG52,COM1 to COM3=low) by setting the $\overline{\text{INH}}$ pin low at the same time as power is applied.Then meaningless display at the power-on can be prevented by transferring serial data from the controller while the display is off and setting $\overline{\text{INH}}$ pin high after the transfer completes.





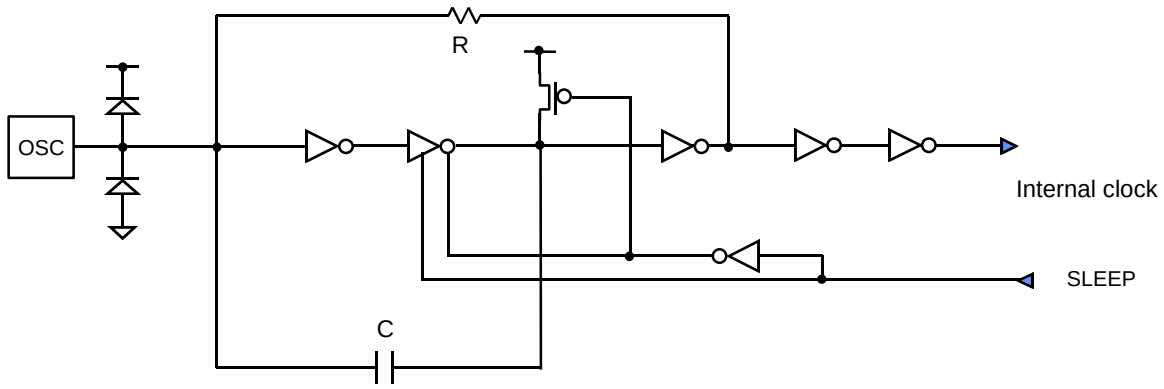
t1 : Determined by the value of C and R
t2 : 10μs(minimum)

11. Power Down Mode

Sleep mode is set up by setting S0 or S1 in the control data to 1. The segment outputs will all go low and the common outputs will also go low, and the oscillator on the OSC pin will stop (it will be started by a key press). This reduces power dissipation. This mode is cleared by sending control data with both S0 and S1 set to 0. Note that the SEG1 to SEG4 outputs can be used as general purpose output ports according to the state of the P0 and P1 control data bits, even in sleep mode.

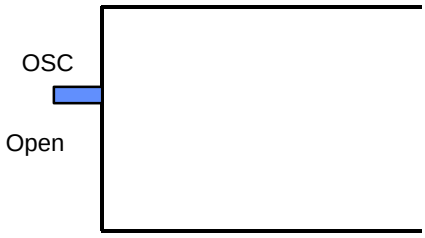
12. Oscillator Port

OSC Pin Diagram

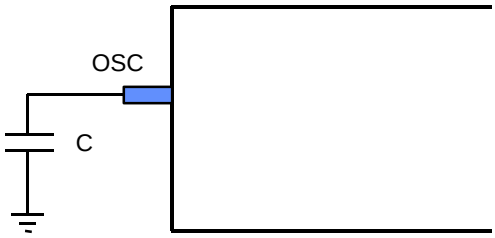


Oscillator circuit consists of internal R and C.

No Capacitor



Using Capacitor



HL15203 has internal resistor and capacitor, so it can be oscillation without external capacitor.
If you want to adjust the clock period then you can adjust it using external capacitor.

13. Electrical Characteristics

Absolute Maximum Rating at Ta=25¡ ÉVss = 0V

Parameter	Symbol	Condition	Rating	unit
Maximum supply voltage	VDD max	VDD	-0.3 to +6.5	V
Input voltage	Vin1	CE,SCK,SI,$\overline{INH}$	-0.3 to +6.5	V
	Vin2	OSC	-0.3 to VDD+0.3	V
Output voltage	Vout	OSC	-0.3 to VDD+0.3	V
Output current	Iout1	SEG1 to SEG52	300	uA
	Iout2	COM1 to COM3	3	mA
Allowable power dissipation	Pd max	Ta = 85¡ É	200	mW
Operating temperature	Topr		-40 to +85	¡ É
Storage temperature	Tstg		-55 to +125	¡ É

Recommend operating ranges at Ta= -40¡ Ëto +85¡ ÉVss = 0V

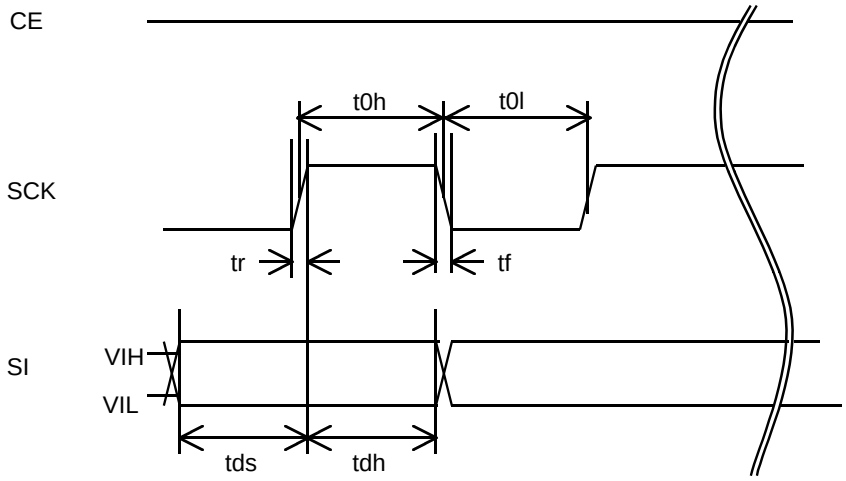
Parameter	Symbol	Condition	min	typ	max	unit
Supply voltage	VDD	VDD	4.5		6.0	V
Input voltage	VCL1	VCL1		2/3VDD	6.0	V
	VCL2	VCL2		1/3VDD	6.0	V
Input high level voltage	VIH	CE,SCK,SI,$\overline{INH}$	4.0		6.0	V
Input low level voltage	VIL	CE,SCK,SI,$\overline{INH}$	0		0.7	V
Recommended external capacitance	COSC	OSC		TBD		pF
Guaranteed oscillation range	f_{OSC}	OSC	19	38	76	KHz
Data setup time	tds	SCK,SI	100			ns
Data hold time	tdh	SCK,SI	100			ns
CE wait time	tcp	CE,SCK	100			ns
CE setup time	tcs	CE,SCK	100			ns
CE hold time	tch	CE,SCK	100			ns
High level clock pulse width	t0h	SCK	100			ns
Low level clock pulse width	tol	SCK	100			ns
Rise time	tr	CE,SCK,SI		100		ns
Fall time	tf	CE,SCK,SI		100		ns
$\overline{INH}$ switching time	t2	$\overline{INH}$,CE	10			µs

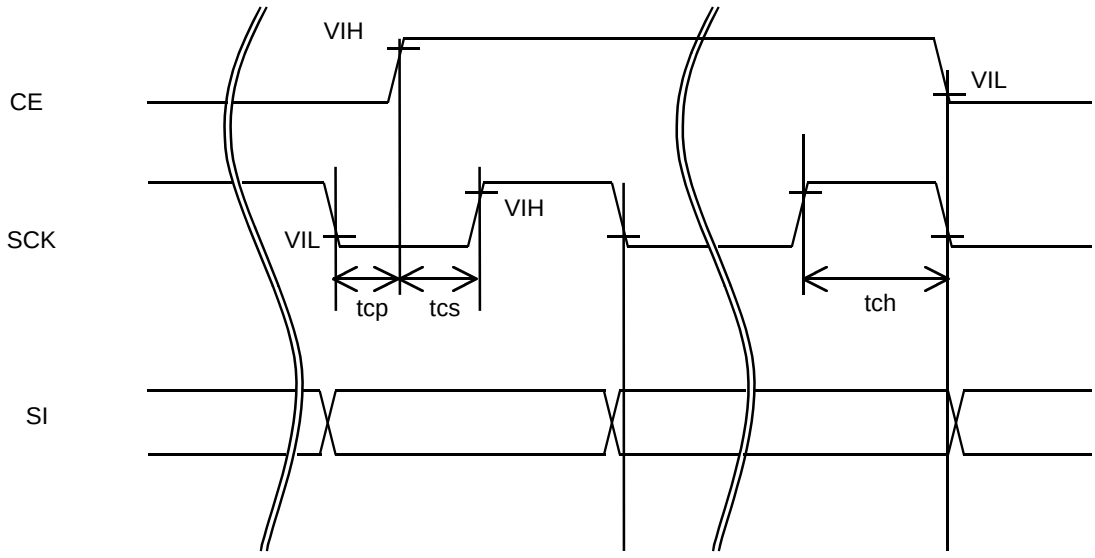
Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Condition	min	typ	max	unit
Input high level current	I_{IH}	CE,SCK,SI,$\overline{INH}$: V1 = 6.0V			5.0	µA
Input low level current	I_{IL}	CE,SCK,SI $\overline{INH}$: V1 = 0V	-5.0			µA
Oscillator frequency	f_{OSC}	OSC : C = TBD		38		kHz
Hysteresis width	VH	CE,SCK,SI,$\overline{INH}$,VDD=5V	0.3			V
Output high level voltage	VOH1	SEG1 to SEG52 : IO = -20 µA	VDD -1.0			V
	VOH2	COM1 to COM3 : IO = -100 µA	VDD -1.0			V
Output low level voltage	VOL1	SEG1 to SEG52 : IO = 20 µA			1.0	V
	VOL2	COM1 to COM3 : IO = 100 µA			1.0	V
Intermediate level voltage*	VMID1	1/2 bias, COM1 to COM3: Io = ¡ ¾100µA	1/2 VDD ±1.0			V
	VMID2	1/3 bias, COM1 to COM3: Io = ¡ ¾100µA	2/3VDD ± 1.0			V
	VMID3	1/2 bias, COM1 to COM3: Io = ¡ ¾100µA	1/3VDD ± 1.0			V
	VMID4	1/3 bias ,SEG1 to SEG52 : Io = ¡ ¾20µA	2/3VDD ± 1.0			V
	VMID5	1/3 bias ,SEG1 to SEG52 : Io = ¡ ¾20µA	1/3VDD ± 1.0			V
Supply Current	IDD1	Power saving mode			5	µA
	IDD2	f_{OSC} = 38 kHz,1/2bias,VDD = 5V		400	800	µA
	IDD3	f_{OSC} = 38 kHz,1/3bias,VDD = 5V		300	600	µA
	IDD2	f_{OSC} = 38 kHz,1/2bias,VDD = 6V		650	1300	µA
	IDD3	f_{OSC} = 38 kHz,1/3bias,VDD = 6V		580	1200	µA

Note : *2. Except the bias voltage generation divider resistor that are built into VCL1 and VCL2

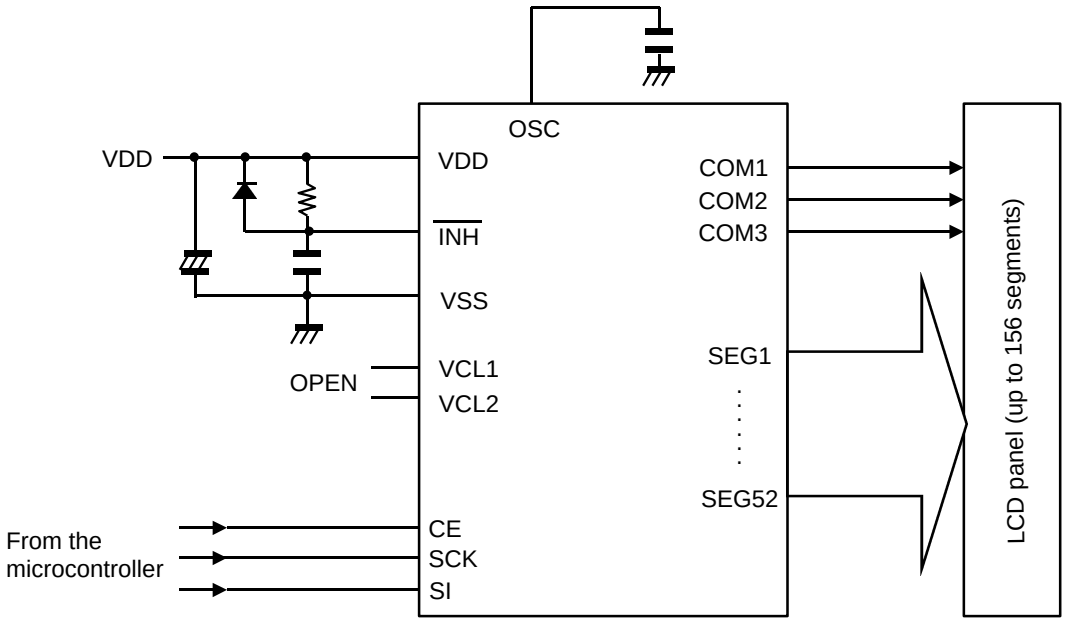
Timing diagram of SIO



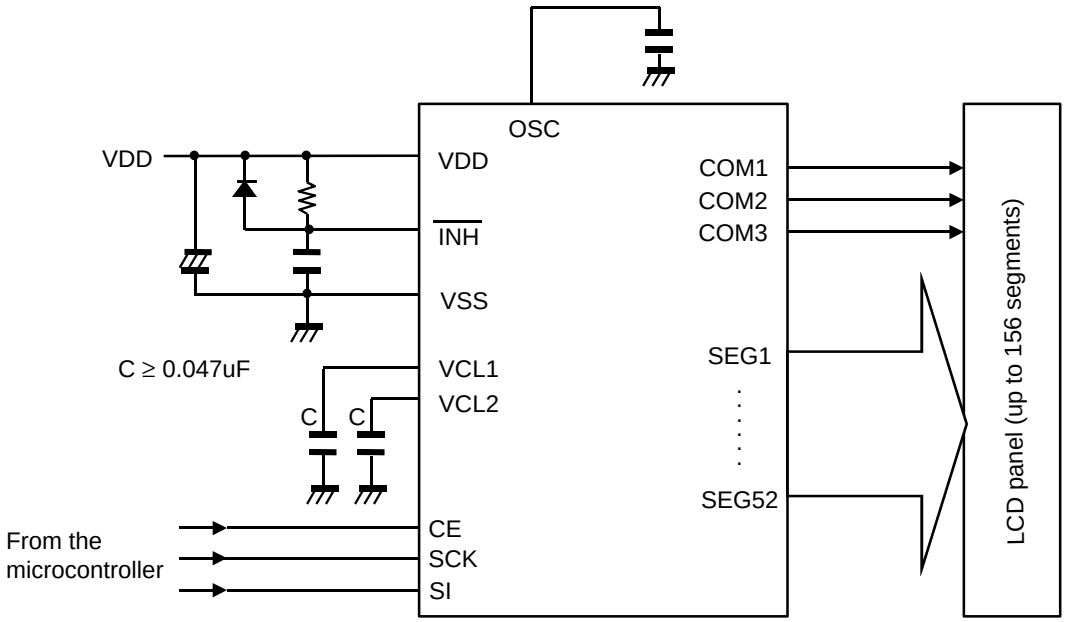


14. Application

1/3 bias (for use with small panels)



1/3 bias (for use with normal panels)



1/3 bias (for use with large panels)