Preliminary Specification(0.3)

128XRGBX82 OUTPUT LCD DRIVER IC with built-in RAM

■ INSTRUCTION

HM17CM256 is a dot-Matrix LCD drive IC with 82 commons (80 + 2 icons) and 384 segments (128 X RGB) drive ports for 256 colors driving.

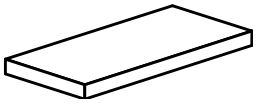
This IC stores the serial or parallel BIT data transferred by the microcomputer on the built-in RAM (81,920 bits for graphic + 2048 bits for icons) and generates the signals to drive LCD panel.

Color graphic display is achieved by selecting 8 gray (256 color) levels out of 32 gray palettes independently.

This IC is suitable for battery-operated system, hand-carrying information equipment by ensuring low power consumption, low power supply (1.7V ~) and a wide range of operating voltage.

And 164 x 128 display (maximum) is possible with master and slave application.

- **EXTERNAL SHAPE**



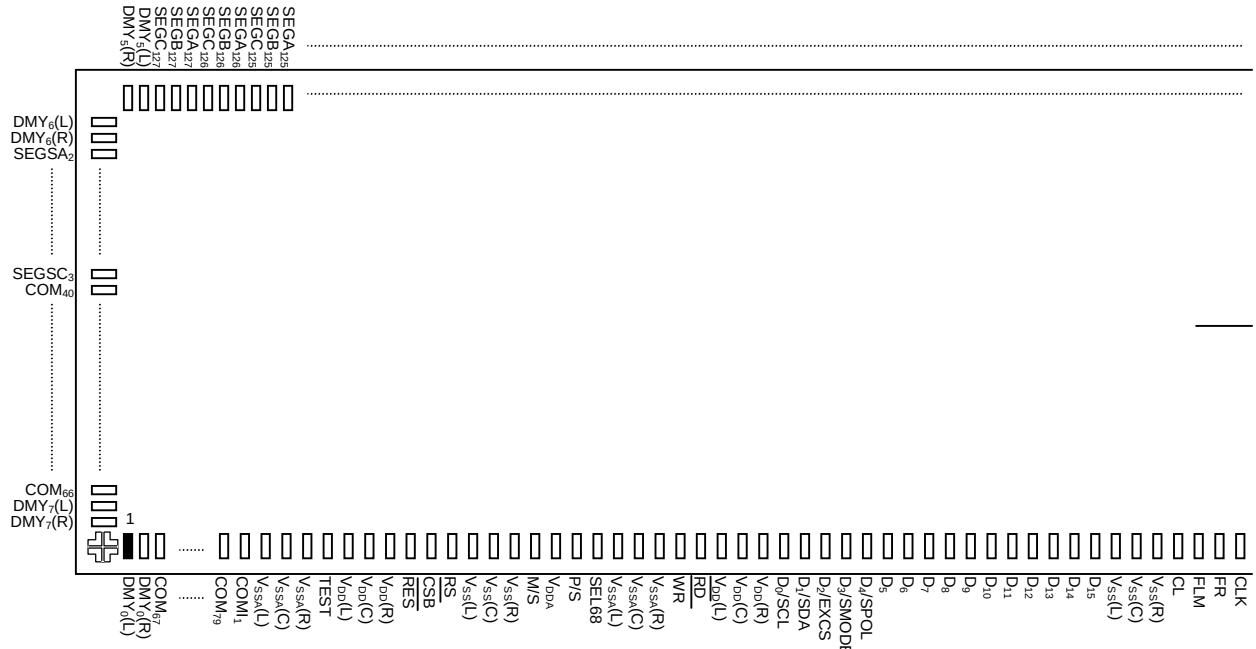
HM17CM256

■ FEATURES

- 256 color bitmap LCD driver
- LCD drive outputs 128×RGB segments, 80 commons for graphic and 2 commons for icons
- Display RAM capacity 81,920bits (for graphic usage)
  2,048bits (for icon usage)
- Gradation display 8 gradations can be selected from 32 gradations by PWM control
- Black/White display 82 × (128 × 3) bits display is possible
- 8 bit BUS interface directly connectable with 68 / 80 series CPU
- RAM data length 8 BIT / 16 BIT selectable
- Serial interface available
- Programmable duty / bias ratio with command
- Various instruction set
  display data read/write, display ON/OFF, positive/negative display, page address set
  display start line address set, partial display, bias select,
  column address set, all display ON/OFF, boosting selection, n line inversion mode
  read modified write, power save …
- Built-in voltage booster (programmable) : 7 × boosting
- Built-in voltage regulator
- Controllable contrast with built-in electric volume (128 steps)
- Low current consumption
- Logic supply 1.7V ~ 3.3V
- LCD drive supply 5.0V ~ 18.0V
- C-MOS silicon process
- Package bumped chip / bare chip

01/02/09

PAD LAYOUT

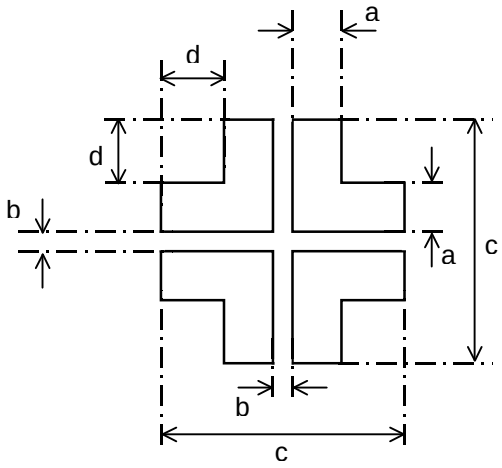


note 1) The (L) (R) (C) mark after port name is internally shorted.
note 2) DMYport is opened electrically.

chip center	**:**	**X= 0μm, Y= 0μm**
chip size	**:**	**with scribe lane : 19.84mm x 2.48mm ,**
		main chip : 19.74mm x 2.38mm
chip thickness	**:**	**625μm ± 25μm**
bump size	**:**	**100μm x 32μm, 100μm x 80μm**
bump pitch	**:**	**50μm(Min)**
bump height	**:**	**18 ± 3μm**
bump material	**:**	**Au**

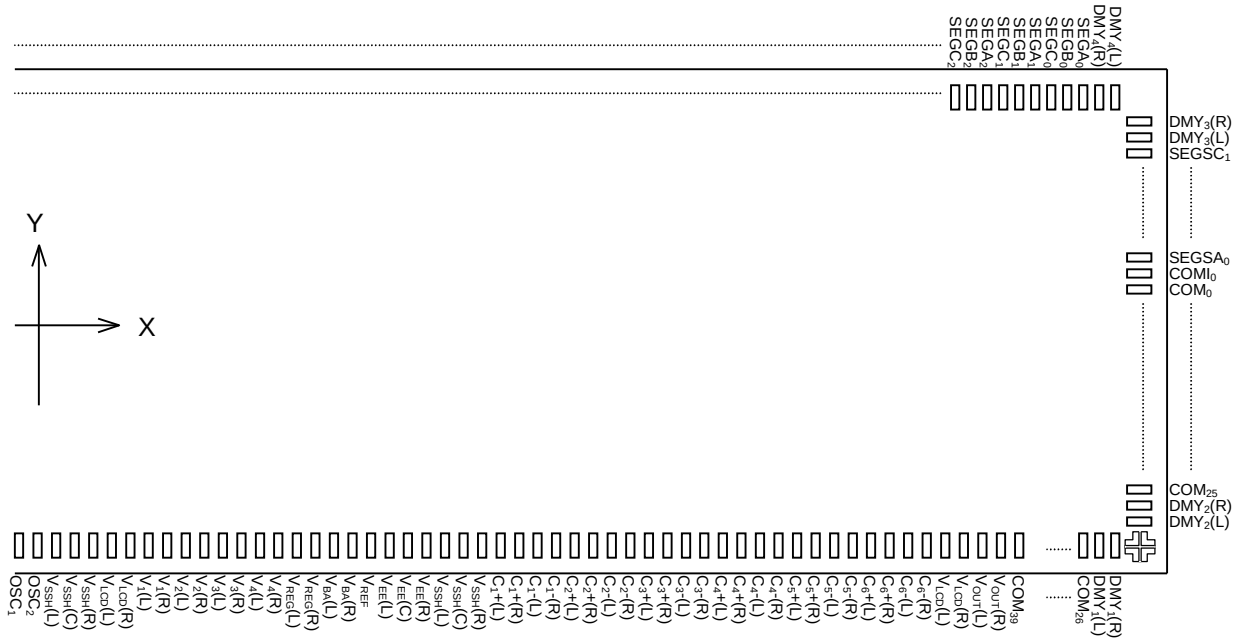
align mark appearance and size

a : 30μm
b : 6μm
c : 120μm
d : 27μm



coordinates of align marks

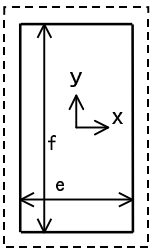
(X= - 9732μm, Y= -1052μm)
(X= 9732μm, Y= -1052μm)



All sorts of PAD open

1. open size (e, f)=(66, 86)
17~118

2. open size (e, f)=(18, 86)
1~16, 119~596



unit（μm）

Original point mark of left picture is presented at the table of pad coordinates.

■ PAD coordinates 1

chip size 19840μm x 2480μm (chip center : 0μm x 0μm)

PAD No.	Pin name	X(μm)	Y(μm)	PAD No.	Pin name	X (μm)	Y (μm)	PAD No.	Pin name	X (μm)	Y (μm)
1	DMY_0(L)	-9625	-1068	52	D_{10}	-2550	-1068	103	C_4+(L)	6120	-1068
2	DMY_0(R)	-9575	-1068	53	D_{11}	-2380	-1068	104	C_4+(R)	6290	-1068
3	COM_{67}	-9525	-1068	54	D_{12}	-2210	-1068	105	C_4-(L)	6460	-1068
4	COM_{68}	-9475	-1068	55	D_{13}	-2040	-1068	106	C_4-(R)	6630	-1068
5	COM_{69}	-9425	-1068	56	D_{14}	-1870	-1068	107	C_5+(L)	6800	-1068
6	COM_{70}	-9375	-1068	57	D_{15}	-1700	-1068	108	C_5+(R)	6970	-1068
7	COM_{71}	-9325	-1068	58	V_{SS}(L)	-1472	-1068	109	C_5-(L)	7140	-1068
8	COM_{72}	-9275	-1068	59	V_{SS}(C)	-1340	-1068	110	C_5-(R)	7310	-1068
9	COM_{73}	-9225	-1068	60	V_{SS}(R)	-1190	-1068	111	C_6+(L)	7480	-1068
10	COM_{74}	-9175	-1068	61	CL	-1020	-1068	112	C_6+(R)	7650	-1068
11	COM_{75}	-9125	-1068	62	FLM	-850	-1068	113	C_6-(L)	7820	-1068
12	COM_{76}	-9075	-1068	63	FR	-680	-1068	114	C_6-(R)	7990	-1068
13	COM_{77}	-9025	-1068	64	CLK	-510	-1068	115	V_{LCD}(L)	8160	-1068
14	COM_{78}	-8975	-1068	65	OSC_1	-340	-1068	116	V_{LCD}(R)	8330	-1068
15	COM_{79}	-8925	-1068	66	OSC_2	-107	-1068	117	V_{OUT}(L)	8500	-1068
16	$COMI_1$	-8875	-1068	67	V_{SSH}(L)	74	-1068	118	V_{OUT}(R)	8670	-1068
17	V_{SSA}(L)	-8670	-1068	68	V_{SSH}(C)	196	-1068	119	COM_{39}	8875	-1068
18	V_{SSA}(C)	-8500	-1068	69	V_{SSH}(R)	318	-1068	120	COM_{38}	8925	-1068
19	V_{SSA}(R)	-8330	-1068	70	V_{LCD}(L)	510	-1068	121	COM_{37}	8975	-1068
20	TEST	-8171	-1068	71	V_{LCD}(R)	680	-1068	122	COM_{36}	9025	-1068
21	V_{DD}(L)	-7990	-1068	72	V_1(L)	850	-1068	123	COM_{35}	9075	-1068
22	V_{DD}(C)	-7820	-1068	73	V_1(R)	1020	-1068	124	COM_{34}	9125	-1068
23	V_{DD}(R)	-7650	-1068	74	V_2(L)	1190	-1068	125	COM_{33}	9175	-1068
24	$\overline{RES}$	-7480	-1068	75	V_2(R)	1360	-1068	126	COM_{32}	9225	-1068
25	$\overline{CS}$	-7310	-1068	76	V_3(L)	1530	-1068	127	COM_{31}	9275	-1068
26	RS	-7140	-1068	77	V_3(R)	1700	-1068	128	COM_{30}	9325	-1068
27	V_{SS}(L)	-6970	-1068	78	V_4(L)	1870	-1068	129	COM_{29}	9375	-1068
28	V_{SS}(C)	-6800	-1068	79	V_4(R)	2040	-1068	130	COM_{28}	9425	-1068
29	V_{SS}(R)	-6630	-1068	80	V_{REG}(L)	2210	-1068	131	COM_{27}	9475	-1068
30	M/S	-6448	-1068	81	V_{REG}(R)	2380	-1068	132	COM_{26}	9525	-1068
31	V_{DDA}	-6290	-1068	82	V_{BA}(L)	2550	-1068	133	DMY_1(L)	9575	-1068
32	P/S	-6120	-1068	83	V_{BA}(R)	2693	-1068	134	DMY_1(R)	9625	-1068
33	SEL68	-5950	-1068	84	V_{REF}	2879	-1068	135	DMY_2(L)	9726	-900
34	V_{SSA}(L)	-5780	-1068	85	V_{EE}(L)	3060	-1068	136	DMY_2(R)	9726	-850
35	V_{SSA}(C)	-5610	-1068	86	V_{EE}(C)	3230	-1068	137	COM_{25}	9726	-800
36	V_{SSA}(R)	-5440	-1068	87	V_{EE}(R)	3400	-1068	138	COM_{24}	9726	-750
37	$\overline{WR}$	-5270	-1068	88	V_{SSH}(L)	3570	-1068	139	COM_{23}	9726	-700
38	$\overline{RD}$	-5111	-1068	89	V_{SSH}(C)	3740	-1068	140	COM_{22}	9726	-650
39	V_{DD}(L)	-4930	-1068	90	V_{SSH}(R)	3910	-1068	141	COM_{21}	9726	-600
40	V_{DD}(C)	-4760	-1068	91	C_1+(L)	4102	-1068	142	COM_{20}	9726	-550
41	V_{DD}(R)	-4590	-1068	92	C_1+(R)	4250	-1068	143	COM_{19}	9726	-500
42	D_0/SCL	-4420	-1068	93	C_1-(L)	4420	-1068	144	COM_{18}	9726	-450
43	D_1/SDA	-4250	-1068	94	C_1-(R)	4590	-1068	145	COM_{17}	9726	-400
44	D_2/EXCS	-3995	-1068	95	C_2+(L)	4760	-1068	146	COM_{16}	9726	-350
45	D_3/SMODE	-3740	-1068	96	C_2+(R)	4930	-1068	147	COM_{15}	9726	-300
46	D_4/SPOL	-3570	-1068	97	C_2-(L)	5100	-1068	148	COM_{14}	9726	-250
47	D_5	-3400	-1068	98	C_2-(R)	5270	-1068	149	COM_{13}	9726	-200
48	D_6	-3230	-1068	99	C_3+(L)	5440	-1068	150	COM_{12}	9726	-150
49	D_7	-3060	-1068	100	C_3+(R)	5610	-1068	151	COM_{11}	9726	-100
50	D_8	-2890	-1068	101	C_3-(L)	5780	-1068	152	COM_{10}	9726	-50
51	D_9	-2720	-1068	102	C_3-(R)	5950	-1068	153	COM_9	9726	0

■ PAD coordiantes 2

chip size 19840μm x 2480μm (chip center : 0μm x 0μm)

PAD No.	Pin name	X(μm)	Y(μm)	PAD No.	Pin name	X (μm)	Y (μm)	PAD No.	Pin name	X (μm)	Y (μm)
154	COM_8	9726	50	205	$SEGB_{10}$	8025	1068	256	$SEGB_{27}$	5475	1068
155	COM_7	9726	100	206	$SEGC_{10}$	7975	1068	257	$SEGC_{27}$	5425	1068
156	COM_6	9726	150	207	$SEGA_{11}$	7925	1068	258	$SEGA_{28}$	5375	1068
157	COM_5	9726	200	208	$SEGB_{11}$	7875	1068	259	$SEGB_{28}$	5325	1068
158	COM_4	9726	250	209	$SEGC_{11}$	7825	1068	260	$SEGC_{28}$	5275	1068
159	COM_3	9726	300	210	$SEGA_{12}$	7775	1068	261	$SEGA_{29}$	5225	1068
160	COM_2	9726	350	211	$SEGB_{12}$	7725	1068	262	$SEGB_{29}$	5175	1068
161	COM_1	9726	400	212	$SEGC_{12}$	7675	1068	263	$SEGC_{29}$	5125	1068
162	COM_0	9726	450	213	$SEGA_{13}$	7625	1068	264	$SEGA_{30}$	5075	1068
163	$COMI_0$	9726	500	214	$SEGB_{13}$	7575	1068	265	$SEGB_{30}$	5025	1068
164	$SEGSA_0$	9726	550	215	$SEGC_{13}$	7525	1068	266	$SEGC_{30}$	4975	1068
165	$SEGSB_0$	9726	600	216	$SEGA_{14}$	7475	1068	267	$SEGA_{31}$	4925	1068
166	$SEGSC_0$	9726	650	217	$SEGB_{14}$	7425	1068	268	$SEGB_{31}$	4875	1068
167	$SEGSA_1$	9726	700	218	$SEGC_{14}$	7375	1068	269	$SEGC_{31}$	4825	1068
168	$SEGSB_1$	9726	750	219	$SEGA_{15}$	7325	1068	270	$SEGA_{32}$	4775	1068
169	$SEGSC_1$	9726	800	220	$SEGB_{15}$	7275	1068	271	$SEGB_{32}$	4725	1068
170	DMY_3(L)	9726	850	221	$SEGC_{15}$	7225	1068	272	$SEGC_{32}$	4675	1068
171	DMY_3(R)	9726	900	222	$SEGA_{16}$	7175	1068	273	$SEGA_{33}$	4625	1068
172	DMY_4(L)	9675	1068	223	$SEGB_{16}$	7125	1068	274	$SEGB_{33}$	4575	1068
173	DMY_4(R)	9625	1068	224	$SEGC_{16}$	7075	1068	275	$SEGC_{33}$	4525	1068
174	$SEGA_0$	9575	1068	225	$SEGA_{17}$	7025	1068	276	$SEGA_{34}$	4475	1068
175	$SEGB_0$	9525	1068	226	$SEGB_{17}$	6975	1068	277	$SEGB_{34}$	4425	1068
176	$SEGC_0$	9475	1068	227	$SEGC_{17}$	6925	1068	278	$SEGC_{34}$	4375	1068
177	$SEGA_1$	9425	1068	228	$SEGA_{18}$	6875	1068	279	$SEGA_{35}$	4325	1068
178	$SEGB_1$	9375	1068	229	$SEGB_{18}$	6825	1068	280	$SEGB_{35}$	4275	1068
179	$SEGC_1$	9325	1068	230	$SEGC_{18}$	6775	1068	281	$SEGC_{35}$	4225	1068
180	$SEGA_2$	9275	1068	231	$SEGA_{19}$	6725	1068	282	$SEGA_{36}$	4175	1068
181	$SEGB_2$	9225	1068	232	$SEGB_{19}$	6675	1068	283	$SEGB_{36}$	4125	1068
182	$SEGC_2$	9175	1068	233	$SEGC_{19}$	6625	1068	284	$SEGC_{36}$	4075	1068
183	$SEGA_3$	9125	1068	234	$SEGA_{20}$	6575	1068	285	$SEGA_{37}$	4025	1068
184	$SEGB_3$	9075	1068	235	$SEGB_{20}$	6525	1068	286	$SEGB_{37}$	3975	1068
185	$SEGC_3$	9025	1068	236	$SEGC_{20}$	6475	1068	287	$SEGC_{37}$	3925	1068
186	$SEGA_4$	8975	1068	237	$SEGA_{21}$	6425	1068	288	$SEGA_{38}$	3875	1068
187	$SEGB_4$	8925	1068	238	$SEGB_{21}$	6375	1068	289	$SEGB_{38}$	3825	1068
188	$SEGC_4$	8875	1068	239	$SEGC_{21}$	6325	1068	290	$SEGC_{38}$	3775	1068
189	$SEGA_5$	8825	1068	240	$SEGA_{22}$	6275	1068	291	$SEGA_{39}$	3725	1068
190	$SEGB_5$	8775	1068	241	$SEGB_{22}$	6225	1068	292	$SEGB_{39}$	3675	1068
191	$SEGC_5$	8725	1068	242	$SEGC_{22}$	6175	1068	293	$SEGC_{39}$	3625	1068
192	$SEGA_6$	8675	1068	243	$SEGA_{23}$	6125	1068	294	$SEGA_{40}$	3575	1068
193	$SEGB_6$	8625	1068	244	$SEGB_{23}$	6075	1068	295	$SEGB_{40}$	3525	1068
194	$SEGC_6$	8575	1068	245	$SEGC_{23}$	6025	1068	296	$SEGC_{40}$	3475	1068
195	$SEGA_7$	8525	1068	246	$SEGA_{24}$	5975	1068	297	$SEGA_{41}$	3425	1068
196	$SEGB_7$	8475	1068	247	$SEGB_{24}$	5925	1068	298	$SEGB_{41}$	3375	1068
197	$SEGC_7$	8425	1068	248	$SEGC_{24}$	5875	1068	299	$SEGC_{41}$	3325	1068
198	$SEGA_8$	8375	1068	249	$SEGA_{25}$	5825	1068	300	$SEGA_{42}$	3275	1068
199	$SEGB_8$	8325	1068	250	$SEGB_{25}$	5775	1068	301	$SEGB_{42}$	3225	1068
200	$SEGC_8$	8275	1068	251	$SEGC_{25}$	5725	1068	302	$SEGC_{42}$	3175	1068
201	$SEGA_9$	8225	1068	252	$SEGA_{26}$	5675	1068	303	$SEGA_{43}$	3125	1068
202	$SEGB_9$	8175	1068	253	$SEGB_{26}$	5625	1068	304	$SEGB_{43}$	3075	1068
203	$SEGC_9$	8125	1068	254	$SEGC_{26}$	5575	1068	305	$SEGC_{43}$	3025	1068
204	$SEGA_{10}$	8075	1068	255	$SEGA_{27}$	5525	1068	306	$SEGA_{44}$	2975	1068

PAD coordinates 3

chip size 19840μm x 2480μm (chip center : 0μm x 0μm)

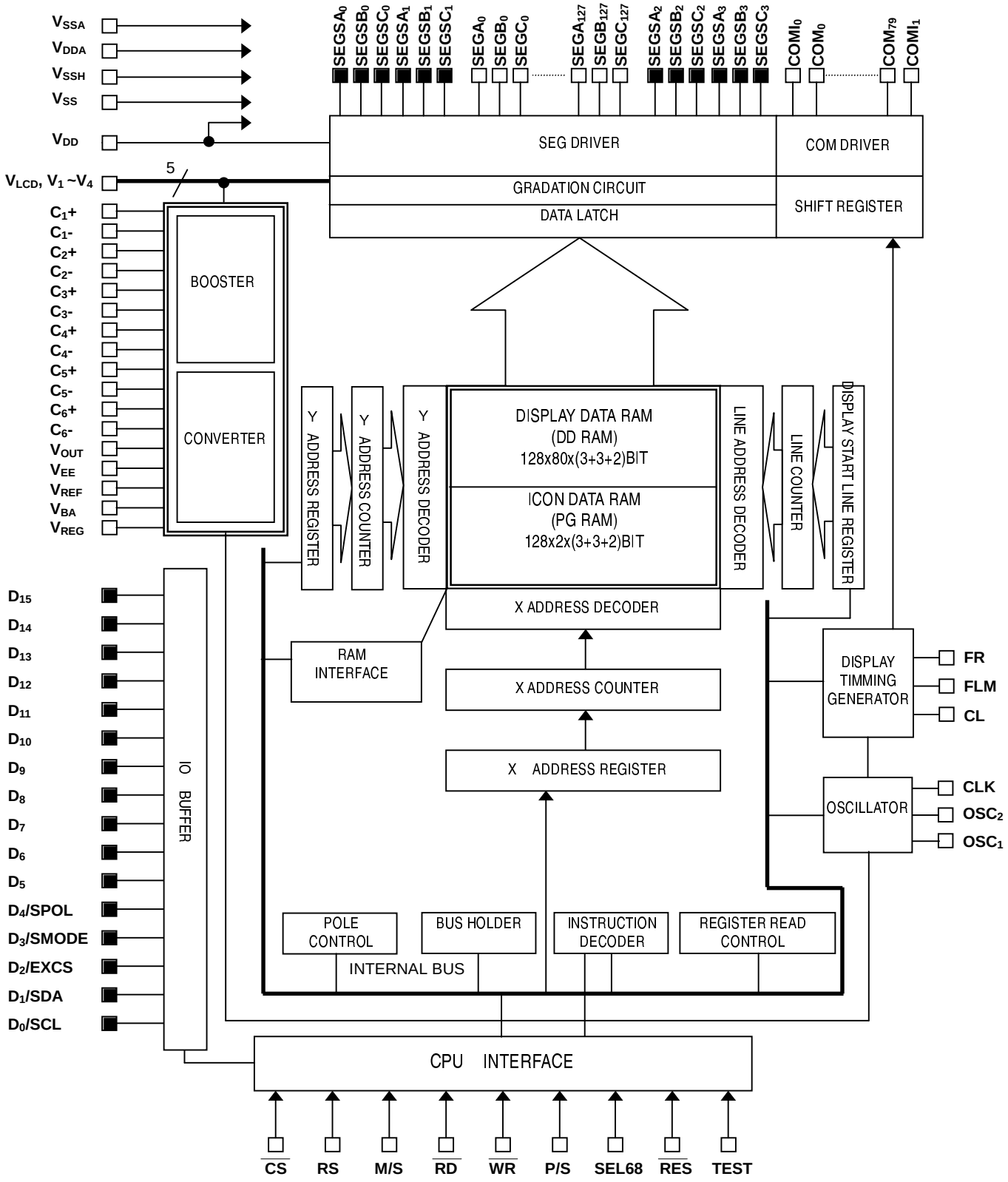
PAD No.	Pin name	X(μm)	Y(μm)	PAD No.	Pin name	X (μm)	Y (μm)	PAD No.	Pin name	X (μm)	Y (μm)
307	$SEGB_{44}$	2925	1068	358	$SEGB_{61}$	375	1068	409	$SEGB_{78}$	-2175	1068
308	$SEGC_{44}$	2875	1068	359	$SEGC_{61}$	325	1068	410	$SEGC_{78}$	-2225	1068
309	$SEGA_{45}$	2825	1068	360	$SEGA_{62}$	275	1068	411	$SEGA_{79}$	-2275	1068
310	$SEGB_{45}$	2775	1068	361	$SEGB_{62}$	225	1068	412	$SEGB_{79}$	-2325	1068
311	$SEGC_{45}$	2725	1068	362	$SEGC_{62}$	175	1068	413	$SEGC_{79}$	-2375	1068
312	$SEGA_{46}$	2675	1068	363	$SEGA_{63}$	125	1068	414	$SEGA_{80}$	-2425	1068
313	$SEGB_{46}$	2625	1068	364	$SEGB_{63}$	75	1068	415	$SEGB_{80}$	-2475	1068
314	$SEGC_{46}$	2575	1068	365	$SEGC_{63}$	25	1068	416	$SEGC_{80}$	-2525	1068
315	$SEGA_{47}$	2525	1068	366	$SEGA_{64}$	-25	1068	417	$SEGA_{81}$	-2575	1068
316	$SEGB_{47}$	2475	1068	367	$SEGB_{64}$	-75	1068	418	$SEGB_{81}$	-2625	1068
317	$SEGC_{47}$	2425	1068	368	$SEGC_{64}$	-125	1068	419	$SEGC_{81}$	-2675	1068
318	$SEGA_{48}$	2375	1068	369	$SEGA_{65}$	-175	1068	420	$SEGA_{82}$	-2725	1068
319	$SEGB_{48}$	2325	1068	370	$SEGB_{65}$	-225	1068	421	$SEGB_{82}$	-2775	1068
320	$SEGC_{48}$	2275	1068	371	$SEGC_{65}$	-275	1068	422	$SEGC_{82}$	-2825	1068
321	$SEGA_{49}$	2225	1068	372	$SEGA_{66}$	-325	1068	423	$SEGA_{83}$	-2875	1068
322	$SEGB_{49}$	2175	1068	373	$SEGB_{66}$	-375	1068	424	$SEGB_{83}$	-2925	1068
323	$SEGC_{49}$	2125	1068	374	$SEGC_{66}$	-425	1068	425	$SEGC_{83}$	-2975	1068
324	$SEGA_{50}$	2075	1068	375	$SEGA_{67}$	-475	1068	426	$SEGA_{84}$	-3025	1068
325	$SEGB_{50}$	2025	1068	376	$SEGB_{67}$	-525	1068	427	$SEGB_{84}$	-3075	1068
326	$SEGC_{50}$	1975	1068	377	$SEGC_{67}$	-575	1068	428	$SEGC_{84}$	-3125	1068
327	$SEGA_{51}$	1925	1068	378	$SEGA_{68}$	-625	1068	429	$SEGA_{85}$	-3175	1068
328	$SEGB_{51}$	1875	1068	379	$SEGB_{68}$	-675	1068	430	$SEGB_{85}$	-3225	1068
329	$SEGC_{51}$	1825	1068	380	$SEGC_{68}$	-725	1068	431	$SEGC_{85}$	-3275	1068
330	$SEGA_{52}$	1775	1068	381	$SEGA_{69}$	-775	1068	432	$SEGA_{86}$	-3325	1068
331	$SEGB_{52}$	1725	1068	382	$SEGB_{69}$	-825	1068	433	$SEGB_{86}$	-3375	1068
332	$SEGC_{52}$	1675	1068	383	$SEGC_{69}$	-875	1068	434	$SEGC_{86}$	-3425	1068
333	$SEGA_{53}$	1625	1068	384	$SEGA_{70}$	-925	1068	435	$SEGA_{87}$	-3475	1068
334	$SEGB_{53}$	1575	1068	385	$SEGB_{70}$	-975	1068	436	$SEGB_{87}$	-3525	1068
335	$SEGC_{53}$	1525	1068	386	$SEGC_{70}$	-1025	1068	437	$SEGC_{87}$	-3575	1068
336	$SEGA_{54}$	1475	1068	387	$SEGA_{71}$	-1075	1068	438	$SEGA_{88}$	-3625	1068
337	$SEGB_{54}$	1425	1068	388	$SEGB_{71}$	-1125	1068	439	$SEGB_{88}$	-3675	1068
338	$SEGC_{54}$	1375	1068	389	$SEGC_{71}$	-1175	1068	440	$SEGC_{88}$	-3725	1068
339	$SEGA_{55}$	1325	1068	390	$SEGA_{72}$	-1225	1068	441	$SEGA_{89}$	-3775	1068
340	$SEGB_{55}$	1275	1068	391	$SEGB_{72}$	-1275	1068	442	$SEGB_{89}$	-3825	1068
341	$SEGC_{55}$	1225	1068	392	$SEGC_{72}$	-1325	1068	443	$SEGC_{89}$	-3875	1068
342	$SEGA_{56}$	1175	1068	393	$SEGA_{73}$	-1375	1068	444	$SEGA_{90}$	-3925	1068
343	$SEGB_{56}$	1125	1068	394	$SEGB_{73}$	-1425	1068	445	$SEGB_{90}$	-3975	1068
344	$SEGC_{56}$	1075	1068	395	$SEGC_{73}$	-1475	1068	446	$SEGC_{90}$	-4025	1068
345	$SEGA_{57}$	1025	1068	396	$SEGA_{74}$	-1525	1068	447	$SEGA_{91}$	-4075	1068
346	$SEGB_{57}$	975	1068	397	$SEGB_{74}$	-1575	1068	448	$SEGB_{91}$	-4125	1068
347	$SEGC_{57}$	925	1068	398	$SEGC_{74}$	-1625	1068	449	$SEGC_{91}$	-4175	1068
348	$SEGA_{58}$	875	1068	399	$SEGA_{75}$	-1675	1068	450	$SEGA_{92}$	-4225	1068
349	$SEGB_{58}$	825	1068	400	$SEGB_{75}$	-1725	1068	451	$SEGB_{92}$	-4275	1068
350	$SEGC_{58}$	775	1068	401	$SEGC_{75}$	-1775	1068	452	$SEGC_{92}$	-4325	1068
351	$SEGA_{59}$	725	1068	402	$SEGA_{76}$	-1825	1068	453	$SEGA_{93}$	-4375	1068
352	$SEGB_{59}$	675	1068	403	$SEGB_{76}$	-1875	1068	454	$SEGB_{93}$	-4425	1068
353	$SEGC_{59}$	625	1068	404	$SEGC_{76}$	-1925	1068	455	$SEGC_{93}$	-4475	1068
354	$SEGA_{60}$	575	1068	405	$SEGA_{77}$	-1975	1068	456	$SEGA_{94}$	-4525	1068
355	$SEGB_{60}$	525	1068	406	$SEGB_{77}$	-2025	1068	457	$SEGB_{94}$	-4575	1068
356	$SEGC_{60}$	475	1068	407	$SEGC_{77}$	-2075	1068	458	$SEGC_{94}$	-4625	1068
357	$SEGA_{61}$	425	1068	408	$SEGA_{78}$	-2125	1068	459	$SEGA_{95}$	-4675	1068

■ PAD coordinates 4

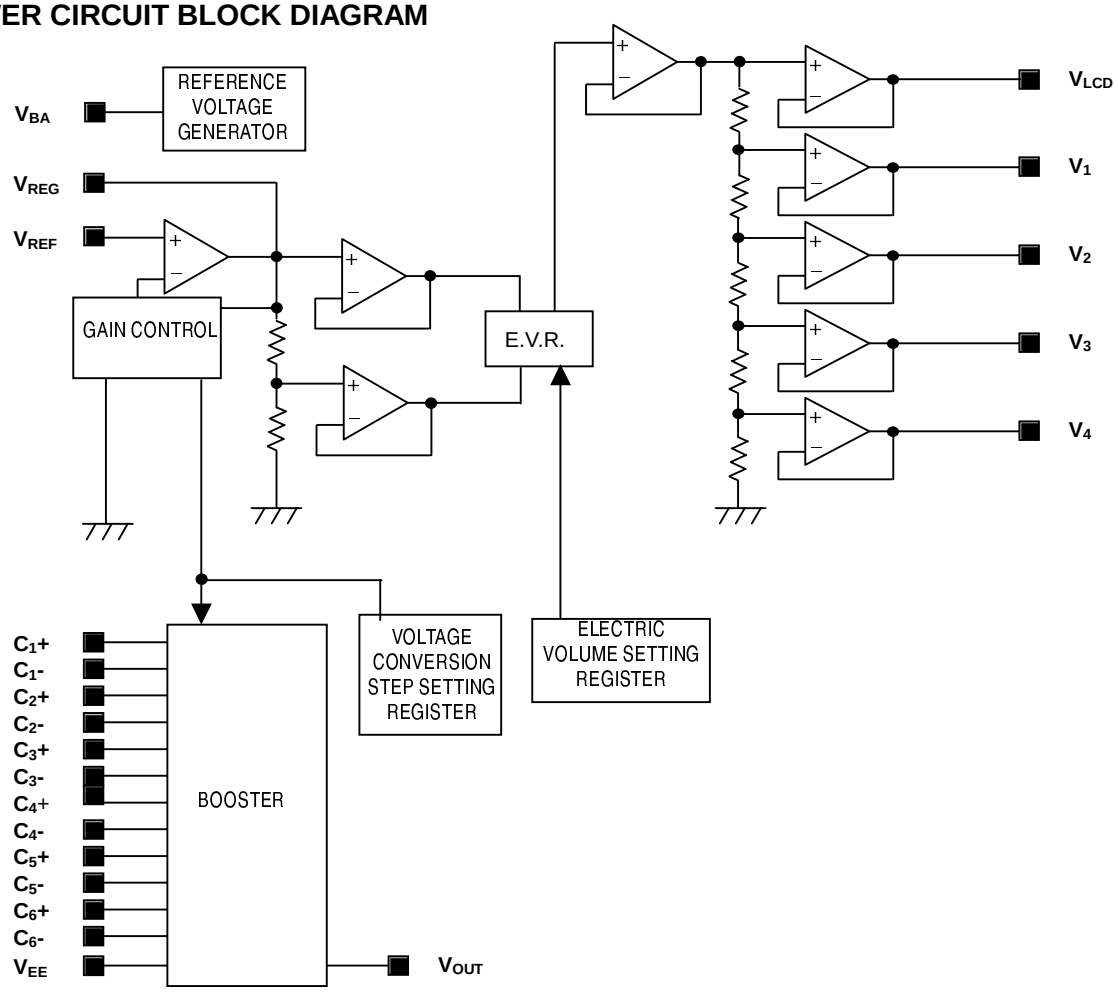
chip size 19840μm x 2480μm (chip center : 0μm x 0μm)

PAD No.	Pin name	X(μm)	Y(μm)	PAD No.	Pin name	X (μm)	Y (μm)	PAD No.	Pin name	X (μm)	Y (μm)
460	$SEGB_{95}$	-4725	1068	511	$SEGB_{112}$	-7275	1068	562	$SEGSA_{2}$	-9726	800
461	$SEGC_{95}$	-4775	1068	512	$SEGC_{112}$	-7325	1068	563	$SEGSB_{2}$	-9726	750
462	$SEGA_{96}$	-4825	1068	513	$SEGA_{113}$	-7375	1068	564	$SEGSC_{2}$	-9726	700
463	$SEGB_{96}$	-4875	1068	514	$SEGB_{113}$	-7425	1068	565	$SEGSA_{3}$	-9726	650
464	$SEGC_{96}$	-4925	1068	515	$SEGC_{113}$	-7475	1068	566	$SEGSB_{3}$	-9726	600
465	$SEGA_{97}$	-4975	1068	516	$SEGA_{114}$	-7525	1068	567	$SEGSC_{3}$	-9726	550
466	$SEGB_{97}$	-5025	1068	517	$SEGB_{114}$	-7575	1068	568	COM_{40}	-9726	500
467	$SEGC_{97}$	-5075	1068	518	$SEGC_{114}$	-7625	1068	569	COM_{41}	-9726	450
468	$SEGA_{98}$	-5125	1068	519	$SEGA_{115}$	-7675	1068	570	COM_{42}	-9726	400
469	$SEGB_{98}$	-5175	1068	520	$SEGB_{115}$	-7725	1068	571	COM_{43}	-9726	350
470	$SEGC_{98}$	-5225	1068	521	$SEGC_{115}$	-7775	1068	572	COM_{44}	-9726	300
471	$SEGA_{99}$	-5275	1068	522	$SEGA_{116}$	-7825	1068	573	COM_{45}	-9726	250
472	$SEGB_{99}$	-5325	1068	523	$SEGB_{116}$	-7875	1068	574	COM_{46}	-9726	200
473	$SEGC_{99}$	-5375	1068	524	$SEGC_{116}$	-7925	1068	575	COM_{47}	-9726	150
474	$SEGA_{100}$	-5425	1068	525	$SEGA_{117}$	-7975	1068	576	COM_{48}	-9726	100
475	$SEGB_{100}$	-5475	1068	526	$SEGB_{117}$	-8025	1068	577	COM_{49}	-9726	50
476	$SEGC_{100}$	-5525	1068	527	$SEGC_{117}$	-8075	1068	578	COM_{50}	-9726	0
477	$SEGA_{101}$	-5575	1068	528	$SEGA_{118}$	-8125	1068	579	COM_{51}	-9726	-50
478	$SEGB_{101}$	-5625	1068	529	$SEGB_{118}$	-8175	1068	580	COM_{52}	-9726	-100
479	$SEGC_{101}$	-5675	1068	530	$SEGC_{118}$	-8225	1068	581	COM_{53}	-9726	-150
480	$SEGA_{102}$	-5725	1068	531	$SEGA_{119}$	-8275	1068	582	COM_{54}	-9726	-200
481	$SEGB_{102}$	-5775	1068	532	$SEGB_{119}$	-8325	1068	583	COM_{55}	-9726	-250
482	$SEGC_{102}$	-5825	1068	533	$SEGC_{119}$	-8375	1068	584	COM_{56}	-9726	-300
483	$SEGA_{103}$	-5875	1068	534	$SEGA_{120}$	-8425	1068	585	COM_{57}	-9726	-350
484	$SEGB_{103}$	-5925	1068	535	$SEGB_{120}$	-8475	1068	586	COM_{58}	-9726	-400
485	$SEGC_{103}$	-5975	1068	536	$SEGC_{120}$	-8525	1068	587	COM_{59}	-9726	-450
486	$SEGA_{104}$	-6025	1068	537	$SEGA_{121}$	-8575	1068	588	COM_{60}	-9726	-500
487	$SEGB_{104}$	-6075	1068	538	$SEGB_{121}$	-8625	1068	589	COM_{61}	-9726	-550
488	$SEGC_{104}$	-6125	1068	539	$SEGC_{121}$	-8675	1068	590	COM_{62}	-9726	-600
489	$SEGA_{105}$	-6175	1068	540	$SEGA_{122}$	-8725	1068	591	COM_{63}	-9726	-650
490	$SEGB_{105}$	-6225	1068	541	$SEGB_{122}$	-8775	1068	592	COM_{64}	-9726	-700
491	$SEGC_{105}$	-6275	1068	542	$SEGC_{122}$	-8825	1068	593	COM_{65}	-9726	-750
492	$SEGA_{106}$	-6325	1068	543	$SEGA_{123}$	-8875	1068	594	COM_{66}	-9726	-800
493	$SEGB_{106}$	-6375	1068	544	$SEGB_{123}$	-8925	1068	595	$DMY_{7}(L)$	-9726	-850
494	$SEGC_{106}$	-6425	1068	545	$SEGC_{123}$	-8975	1068	596	$DMY_{7}(R)$	-9726	-900
495	$SEGA_{107}$	-6475	1068	546	$SEGA_{124}$	-9025	1068				
496	$SEGB_{107}$	-6525	1068	547	$SEGB_{124}$	-9075	1068				
497	$SEGC_{107}$	-6575	1068	548	$SEGC_{124}$	-9125	1068				
498	$SEGA_{108}$	-6625	1068	549	$SEGA_{125}$	-9175	1068				
499	$SEGB_{108}$	-6675	1068	550	$SEGB_{125}$	-9225	1068				
500	$SEGC_{108}$	-6725	1068	551	$SEGC_{125}$	-9275	1068				
501	$SEGA_{109}$	-6775	1068	552	$SEGA_{126}$	-9325	1068				
502	$SEGB_{109}$	-6825	1068	553	$SEGB_{126}$	-9375	1068				
503	$SEGC_{109}$	-6875	1068	554	$SEGC_{126}$	-9425	1068				
504	$SEGA_{110}$	-6925	1068	555	$SEGA_{127}$	-9475	1068				
505	$SEGB_{110}$	-6975	1068	556	$SEGB_{127}$	-9525	1068				
506	$SEGC_{110}$	-7025	1068	557	$SEGC_{127}$	-9575	1068				
507	$SEGA_{111}$	-7075	1068	558	$DMY_{5}(L)$	-9625	1068				
508	$SEGB_{111}$	-7125	1068	559	$DMY_{5}(R)$	-9675	1068				
509	$SEGC_{111}$	-7175	1068	560	$DMY_{6}(L)$	-9726	900				
510	$SEGA_{112}$	-7225	1068	561	$DMY_{6}(R)$	-9726	850				

BLOCK DIAGRAM



■ POWER CIRCUIT BLOCK DIAGRAM



■ PIN DESCRIPTION 1

No.	NAME	I/O	FUNCTION
21,22,23, 39,40,41	V_{DD}	supply	Power pin for logic
27,28,29, 58,59,60	V_{SS}	supply	GND pin for logic
67,68,69, 88,89,90	V_{SSH}	supply	High voltage GND pin
31	V_{DDA}	supply	This pin is internally connected to V_{DD} pin. This pin is used when the voltage of each input pin is fixed to V_{DD} level. *caution) Do not use to main power pin.*
17,18,19, 34,35,36	V_{SSA}	supply	This pin is internally connected to V_{SS} pin. This pin is used when the voltage of each input pin is fixed to V_{SS} level. *caution) Do not use to main power pin.*
70,71,115,116 72,73 74,75 76,77 78,79	V_{LCD} V_1 V_2 V_3 V_4	supply/O	LCD driver supply voltage • LCD driver power supply port when external power supply is used. When external power is used, voltages should have following relations. $V_{SS}<V_4<V_3<V_2<V_1<V_{LCD}$ • V_{LCD}, V_1~V_4 voltages are generated by voltage booster at master mode operation under power circuit ON. • When internal power supply is used, capacitors must be connected between V_{LCD}, V_1~V_4 and V_{SS}.
91,92 93,94	C_1+ C_1-	O	Capacitor connection pin for voltage converter
95,96 97,98	C_2+ C_2-	O	Capacitor connection pin for voltage converter
99,100 101,102	C_3+ C_3-	O	Capacitor connection pin for voltage converter
103,104 105,106	C_4+ C_4-	O	Capacitor connection pin for voltage converter
107,108 109,110	C_5+ C_5-	O	Capacitor connection pin for voltage converter
111,112 113,114	C_6+ C_6-	O	Capacitor connection pin for voltage converter
82,83	V_{BA}	O	Reference voltage output pin for voltage regulating.
84	V_{REF}	I	Reference voltage input pin for voltage regulating.
85,86,87	V_{EE}	supply	Voltage supply pin for boosted voltage generation. V_{DD} level at normal status.
117,118	V_{OUT}	supply/O	Internal DC/DC converter output pin.
80,81	V_{REG}	O	Voltage regulator output pin.
24	$\overline{RES}$	I	Reset pin Reset when $\overline{RES}$= “L”

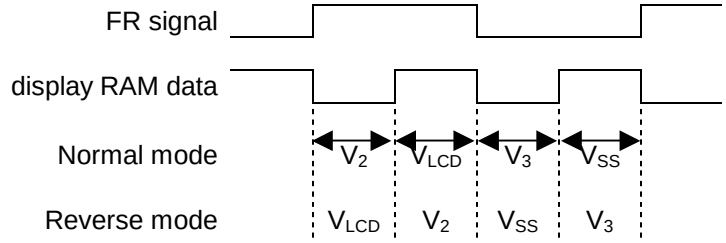
■ PIN DESCRIPTION 2

<table>
<tr><th>No.</th><th>NAME</th><th>I/O</th><th>FUNCTION</th></tr>
<tr><td>42</td><td>D_0/SCL</td><td>I/O</td><td rowspan="6">• When parallel interface is selected (P/S="H"), data line is connected to MPU data bus with 8bit bi-directional bus
• When serial interface is selected (P/S="L"),
D_0 and D_1(SCL, SDA) are used as serial interface pins and various sets are taken by serial interface use mode of D_2, D_3, D_4.
SDA : serial data input pin
SCL : data transfer clock
EXCS : extension chip selection I/O pin
SMODE : serial transfer mode setting input pin
SPOL : RS polarity selection pin when 3 line serial interface is selected.
SDA data is shifted at the rising edge of SCL
Internal serial/parallel conversion into 8-bit data occurs at the rising edge of 8th clock of SCL.
Set to "L" after data transfer or during non-access time</td></tr>
<tr><td>43</td><td>D_1/SDA</td><td>I/O</td></tr>
<tr><td>44</td><td>D_2/EXCS</td><td>I/O</td></tr>
<tr><td>45</td><td>D_3/SMODE</td><td>I/O</td></tr>
<tr><td>46</td><td>D_4/SPOL</td><td>I/O</td></tr>
<tr><td>47,48,49</td><td>D_5,D_6,D_7</td><td>I/O</td></tr>
<tr><td>50,51,52,53
54,55,56,57</td><td>D_8,D_9,D_{10},D_{11},
D_{12},D_{13},D_{14},D_{15}</td><td>I/O</td><td>Connect to data bus to MPU with 8bit bi-directional bus.
Used as MSB 8bit data bus in the 16bit data RAM transfer mode
Set to "L" or "H" when not used.</td></tr>
<tr><td>25</td><td>$\overline{CS}$</td><td>I</td><td>Chip selection pin.
Data in-out is possible when CS = "L".</td></tr>
<tr><td>26</td><td>RS</td><td>I</td><td>Input data selection pin.
Distinguish bus data from CPU whether instruction or display data.
<table>
<tr><td>RS</td><td>H</td><td>L</td></tr>
<tr><td>class</td><td>instruction</td><td>display data</td></tr>
</table></td></tr>
<tr><td>38</td><td>$\overline{RD}$ (E)</td><td>I</td><td><80 series CPU interface (P/S="H",SEL68="L")>
RD signal connection port of 80 series CPU.
Data bus goes to output state at $\overline{RD}$ = "L".
<68 series CPU interface (P/S="H",SEL68="H")>
Enable signal connection port of 68 series CPU.
Active status when this signal is at "H".</td></tr>
<tr><td>37</td><td>$\overline{WR}$ (R/W)</td><td>I</td><td><80 series CPU interface (P/S="H",SEL68="L")>
WR signal connection port of 80 series CPU.
Active at "L" and data bus signal is taken at the rising edge of WR.
<68 series CPU interface (P/S="H",SEL68="H")>
Read write control signal , R/W connection port of 68-series MPU.
<table>
<tr><td>R/W</td><td>H</td><td>L</td></tr>
<tr><td>status</td><td>read</td><td>write</td></tr>
</table></td></tr>
</table>

■ PIN DESCRIPTION 3

<table>
<tr><th>No.</th><th>NAME</th><th>I/O</th><th>FUNCTION</th></tr>
<tr><td>33</td><td>SEL68</td><td>I</td><td>CPU interface selection port
<table>
<tr><td>SEL68</td><td>H</td><td>L</td></tr>
<tr><td>status</td><td>68 series</td><td>80 series</td></tr>
</table></td></tr>
<tr><td>32</td><td>P/S</td><td>I</td><td>Serial / parallel interface selection port
<table>
<tr><td>P/S</td><td>chip select</td><td>data/ command</td><td>data</td><td>read/ write</td><td>serial clock</td></tr>
<tr><td>H</td><td>$\overline{CS}$</td><td>RS</td><td>D_0~D_7</td><td>$\overline{RD}$, $\overline{WR}$</td><td>-</td></tr>
<tr><td>L</td><td>$\overline{CS}$</td><td>RS</td><td>SDA(D_1)</td><td>write only</td><td>SCL (D_0)</td></tr>
</table>
※ P/S = “L” :serial interface selection ,D15~D5 goes to Hi-Z state. Fix $\overline{RD}$, $\overline{WR}$ to “H” or “L”.</td></tr>
<tr><td>20</td><td>TEST</td><td>I</td><td>Test port.
Fix to ”L”.</td></tr>
<tr><td>61</td><td>CL</td><td>I/O</td><td>Latching signal pin of display data.
Display line counter is counted up at the rising edge and LCD driving signal is generated at the falling edge
<table>
<tr><td>M/S</td><td>status</td><td>CL</td></tr>
<tr><td>H</td><td>master</td><td>output</td></tr>
<tr><td>L</td><td>slave</td><td>input</td></tr>
</table></td></tr>
<tr><td>62</td><td>FLM</td><td>I/O</td><td>LCD synchronous signal (first line marker) I/O pin.
Display start address is loaded in the display line counter at FLM = “H”.
<table>
<tr><td>M/S</td><td>status</td><td>FLM</td></tr>
<tr><td>H</td><td>master</td><td>output</td></tr>
<tr><td>L</td><td>slave</td><td>input</td></tr>
</table></td></tr>
<tr><td>63</td><td>FR</td><td>I/O</td><td>Alternated display signal of LCD driver output I/O pin.
<table>
<tr><td>M/S</td><td>status</td><td>FR</td></tr>
<tr><td>H</td><td>master</td><td>output</td></tr>
<tr><td>L</td><td>slave</td><td>input</td></tr>
</table></td></tr>
<tr><td>30</td><td>M/S</td><td>I</td><td>Master / slave mode selection pin
<table>
<tr><td>M/S</td><td>mode</td><td>oscillator</td><td>Power supply</td></tr>
<tr><td>H</td><td>master</td><td>enable</td><td>enable</td></tr>
<tr><td>L</td><td>slave</td><td>disable</td><td>disable</td></tr>
</table>
Fix to “H” or “L” according to operating mode.</td></tr>
</table>

PIN DESCRIPTION 4

<table>
<tr><th>No.</th><th>NAME</th><th>I/O</th><th>FUNCTION</th></tr>
<tr><td>174~557</td><td>$SEGA_0$~$SEGA_{127}$,
$SEGB_0$~$SEGB_{127}$,
$SEGC_0$~$SEGC_{127}$</td><td>O</td><td>Segment drive port
Segment output from display RAM data
<table>
<tr><td>mode</td><td>Non-lighted</td><td>lighted</td></tr>
<tr><td>Normal</td><td>0</td><td>1</td></tr>
<tr><td>Reverse</td><td>1</td><td>0</td></tr>
</table>
The output level is selected among V_{LCD}, V_2, V_3, V_{SS} by the combination of FR signal and RAM data
(B/W mode)
 
</td></tr>
<tr><td>164~169,
562~567</td><td>$SEGSA_0$~$SEGSA_3$,
$SEGSB_0$~$SEGSB_3$,
$SEGSC_0$~$SEGSC_3$</td><td>O</td><td>Dummy segment driver output
Located at both side of segment drivers, used for edge display.</td></tr>
<tr><td>162~137,
132~119,
568~594,
3~15</td><td>COM_0~COM_{79}</td><td>O</td><td>Common driver output
The output level is selected among V_{LCD}, V_1, V_4 and V_{SS} by the combination of FR and scan data.
<table>
<tr><td>data</td><td>FR</td><td>Output level</td></tr>
<tr><td>H</td><td>H</td><td>V_{SS}</td></tr>
<tr><td>L</td><td>H</td><td>V_1</td></tr>
<tr><td>H</td><td>L</td><td>V_{LCD}</td></tr>
<tr><td>L</td><td>L</td><td>V_4</td></tr>
</table></td></tr>
<tr><td>163</td><td>$COMI_0$</td><td>O</td><td>Common drive output for icon display</td></tr>
<tr><td>16</td><td>$COMI_1$</td><td>O</td><td>Common drive output for icon display</td></tr>
<tr><td>65,
66</td><td>OSC_1,
OSC_2</td><td>I
O</td><td>External reference clock input pin
Open when using internal oscillator clock or used as slave device.
In this case, OSC_1 goes to V_{SS} level.
Connect external oscillating source to OSC_1 port or connect resistor between OSC_1 and OSC_2 when using external oscillator.</td></tr>
<tr><td>64</td><td>CLK</td><td>I/O</td><td>Input / output pin for display timing clock
Output clock from master device is applied to slave chip through CLK pin when used as master / slave mode.
<table>
<tr><td>M/S</td><td>mode</td><td>CLK</td></tr>
<tr><td>H</td><td>master</td><td>output</td></tr>
<tr><td>L</td><td>slave</td><td>input*</td></tr>
</table>
*input from master chip’s CLK output</td></tr>
</table>

(port No. 1,2,133,134,135,136,170,171,172,173,558,559,560,561,595,596 is dummy port.)

■ FUNCTION DESCRIPTION

(1) CPU interface

(1-1) Selection of interface type

HM17CM256 receives data through 8 bit parallel I/O(D_0~D_7)、16 bit parallel I/O(D_0~D_{15}) or divided into serial data input (SDA, SCL). Parallel or serial selection is decided by P/S pin setting.
Parallel or serial selection is possible as following table.
Reading out from internal register or RAM is not possible at serial interface mode.

TABLE

P/S	Type	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	SEL68	SDA	SCL	data
H	Parallel input	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	SEL68			D_0~D_7 (D_0~D_{15})
L	Serial input	$\overline{CS}$	RS	-	-	-	SDA	SCL	-

caution 1) "-" mark item : Fix to "H" or "L"

(1-2) Parallel input

In the parallel interface mode selected by P/S port, parallel data is transferred from the 8bit/16bit MPU through data bus. SEL68 port setting makes 80-series or 68-series interface selection

TABLE

SEL68	CPU type	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	data
H	68 series CPU	$\overline{CS}$	RS	E	R/W	D_0~D_7 (D_0~D_{15})
L	80 series CPU	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	D_0~D_7 (D_0~D_{15})

(1-3) Data identification

Combinations of RS, $\overline{RD}$, and $\overline{WR}$ signals identify contents of 8bit data bus.

TABLE

RS	68 series	80 series		FUNCTION
	R/W	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read out from internal register
1	0	1	0	Write in to internal register
0	1	0	1	Read display data
0	0	1	0	Write display data

(1-4) Serial interface

2 types of serial interface (3 line type mode, 4 line type mode) are available by selecting SMODE pin.

TABEL

SMODE	Serial interface mode
H	3 line type
L	4 line type

(1-5) 4 line type serial interface

4 line serial interface by SDA and SCL is possible at chip selection state ($\overline{CS}$="L")

When chip is not selected, internal shift register and counter are reset to initial value.

Serial input data from SDA are latched at the rising edge of serial clock (SCL) in the sequence of D_7, ⋯, D_1, D_0 and converted into 8-bit parallel data at the rising edge of 8th serial clock.

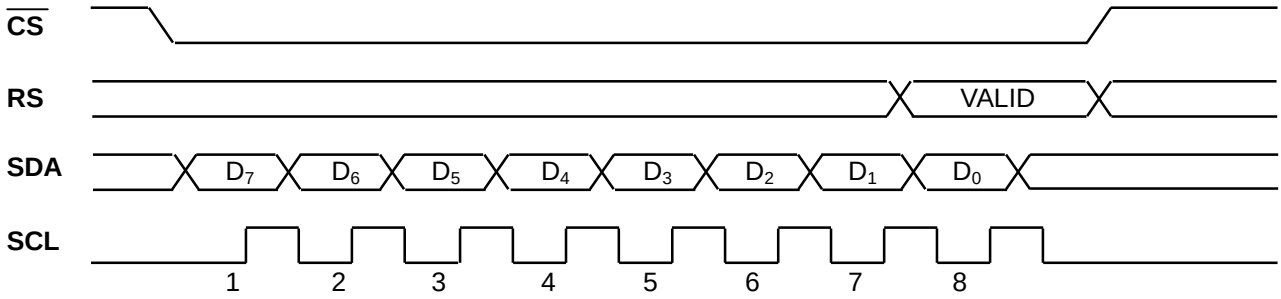
Serial data (SDA) are identified to display data or command by RS input.

TABLE

RS	Data contents
H	command
L	Display data

Make serial clock (SCL) "L" at the non-access period and after 8bit data transfer.

SDA and SCL signals are sensitive to external noise. To prevent mal-function, chip selector state should be released ($\overline{CS}$ = "H") after 8bit data transfer as shown in the following figure.



4 line serial interface

(1-6) 3 line type serial interface

3-line serial interface by SDA and SCL is possible at chip selection state ($\overline{CS}$="L")

When chip is not selected, internal shift register and counter are reset to initial value.

Input data from SDA are latched at the rising edge of serial clock (SCL) in the sequence of RS, D_7⋯, ,D_1, D_0, and converted to 8bit parallel data and handled at the rising edge of 9th serial clock.

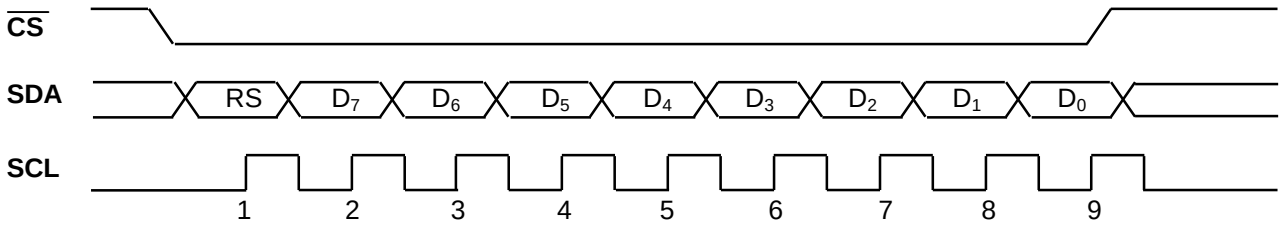
Serial data (SDA) are identified to display data or command by RS bit data at the rising of first serial clock (SCL) and state of command data bit polarity shift pin (SPOL).

TABLE

SPOL=L		SPOL=H	
RS	Data identify	RS	Data identify
L	Display data	L	command
H	command	H	Display data

Serial clock (SCL) should go to “L” at the non-access period and after 9bit data transfer.

SDA and SCL signals are sensitive to external noise. To prevent miss operation chip selector state should be released ($\overline{CS}$ = “H”) after 9bit data transfer as shown in the following figure**.**



3line serial interface

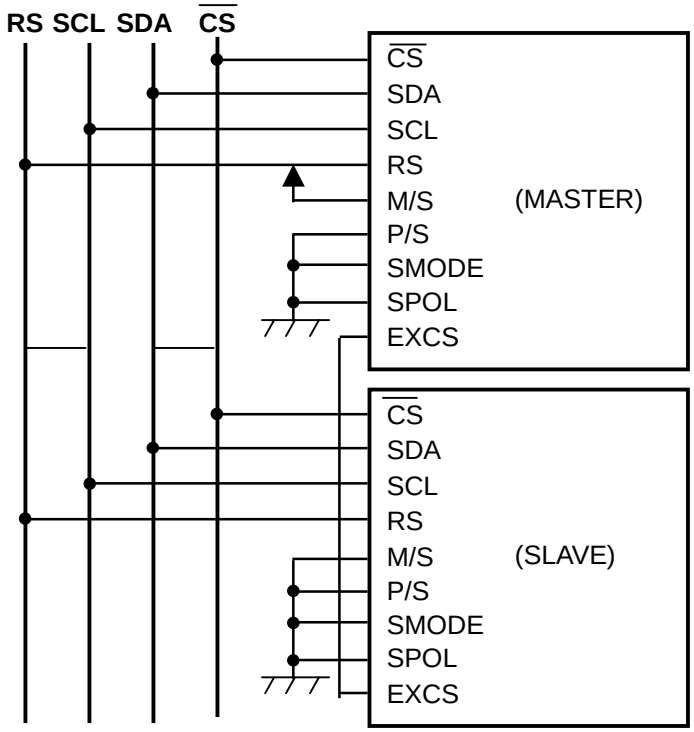
(1-7) One systematization of $\overline{CS}$ when serial interface is selected

In the multi-chip operation (master/slave) mode with serial I/F connection, one $\overline{CS}$ signal controls two chips to reduce control signal.

Connect extended chip selection port (EXCS) of master chip to EXCS port (input at slave device and output at master device mode) of slave chip.

When EXCS is “L”, master chip cannot accept command except for EXCS control; at this point, only slave chip can be controlled.

Slave device control is possible when $\overline{CS}$ = “L” period within EXCS = “L” state.



EXCS: expand $\overline{CS}$ signal (input port)
Master device : output port
Slave device : input port

P/S: parallel . serial selection port
(input port)
P/S=0: serial I/F
P/S=1: parallel I/F

M/S: master . slave selection port
(input port)
M/S=0: slave operation
M/S=1: master operation

SMODE: serial I/Fmode selection port
(input port)
SMODE=0: 4 line serial I/F
SMODE=1: 3 line serial I/F

SPOL:command data bit polarity selection port
(input port)
At 3 line serial I/F mode
Access display RAM at SPOL=0:RS=0
Access display RAM at SPOL=1:RS=1

(2) DDRAM and internal register access

DDRAM and internal register are accessed by data bus D_0~D_7(D_0~D_{15}), chip select pin ($\overline{CS}$), DDRAM / register select pin (RS), read / write control pin ($\overline{RD}$) or $\overline{WR}$ pin.

When $\overline{CS}$="H", it is in non-selective state and DDRAM and internal register access is impossible.

During access, Set $\overline{CS}$="L".

Access selection to DDRAM or internal register is controlled by RS input.

TABLE

RS	Data contents
L	Display RAM data
H	Internal command register

Write process starts after address setting and then the data on the 8bit data bus D_0~D_7 or 16bit data bus D_0~D_{15} will be written in by CPU. The data is written at the rising edge of $\overline{WR}$ (80 series) or falling edge of E (68 series).

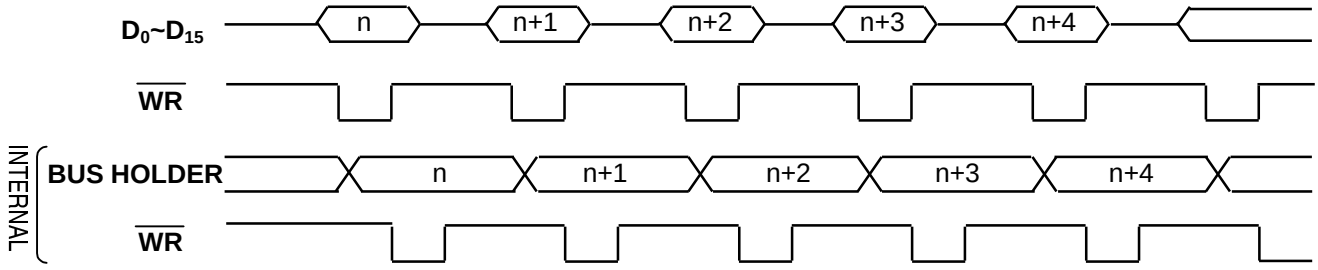
Internally, bus holder data is processed to data bus and data are written to bus holder from CPU until next cycle.

After address setting, data of assigned address are read at the 1st and 3rd clock, which means it needs dummy read at the 2nd clock.

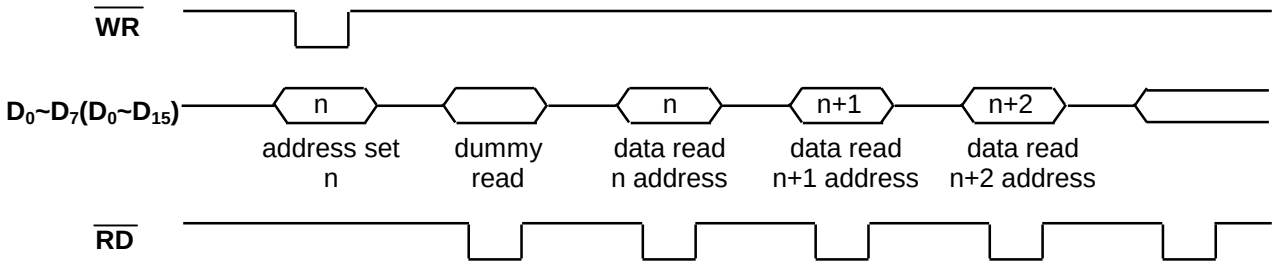
There are rules at reading data out of display RAM, after address setting, the data of assigned address is shown directly after the end of the read command, so pay attention that assigned data is available at 2nd timing step.

In other words, 1 cycle dummy read is needed after address setting and write cycle.

DATA WRITE IN OPERATION



DATA READ OUT OPERATION

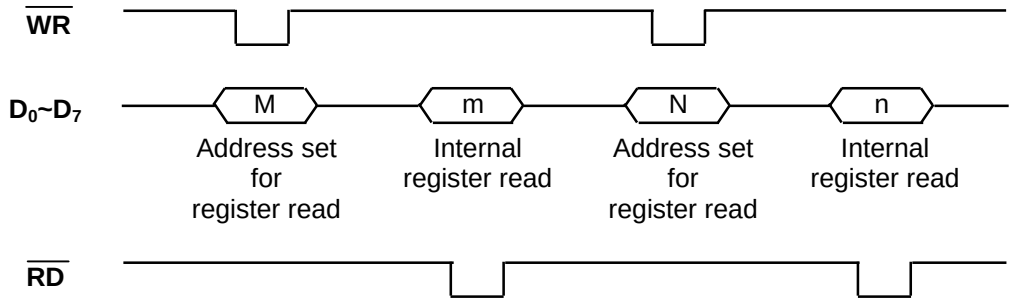


caution) When 16 bit mode, do write in and read out by 16 bit not only RAM access but also command setting.

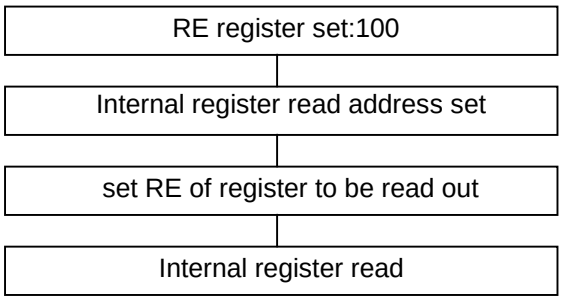
(3) Read out of internal register

Read out is possible not only from DDRAM, but also from the internal register. Addresses for read (0~F_H) are allocated in each register.

Read out is executed after writing read-out register address to internal register.



Internal register read out sequence



When register is read out, upper 4 bit data are “1111”.

Non-used bits of active registers are “0”.

When non-used registers are read out, upper 4 bits are “1111” and lower 4 bits are “0000”.

(4) 16 bit data access to DDRAM

It is possible to write in DDRAM by 16-bits access with the data of 16 bits data bus D_0~D_{15}.

16 bits data access mode is possible by setting the value of WLS register to “1”.

TABEL

WLS	Acess mode
L	8 bit
H	16 bit

Each command should be set to 8-bits(D_0~D_7) as well as to 16-bit access mode.

16-bit access is available at display RAM access.

(5) Display start line register

When displaying the DDRAM data, it is the contents of Y address register that is corresponding to display start line.

The data of Y address is displayed on the display start line depending on the value of the shift command register and the display start line register.

The data of this register are preset to the display line counter per FLM signal transition.

Line counter is counted up in synchronization with CL input and generates line address that read out 384bit data from DDRAM to LCD driver circuit.

(6) DDRAM addressing

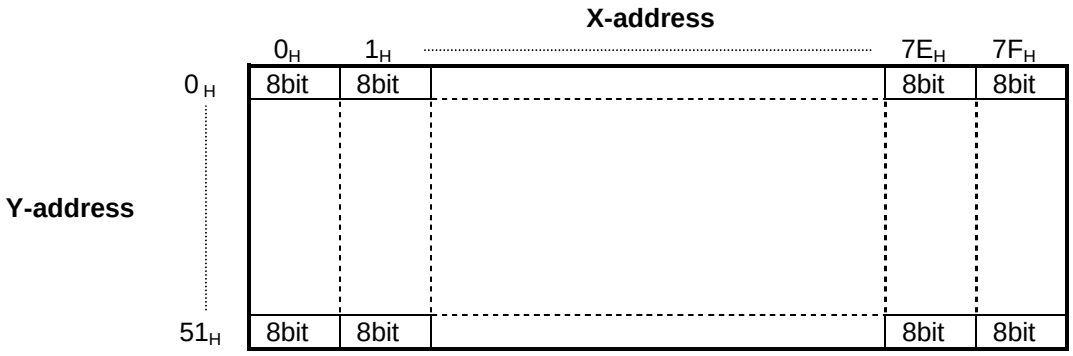
This IC includes display memory Bit mapped that is composed of 1024 bit of X direction (8bit×128) and 82bit of Y direction.

In gray mode, neighboring 3-bit data or 2-bit data are displayed by segment driver with 8 grays or 4 grays, respectively.

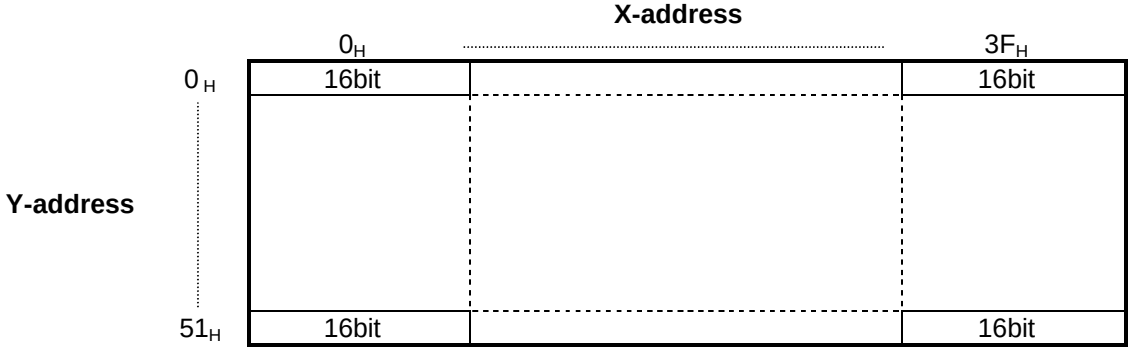
3 outputs of segment driver compose 1 pixel of RGB and 128×82 pixels are displayed with 256 color (8gray×8gray×4gray).

Address area of X direction is varied according to accessed data length. The area of X direction is 0_H~$7F_H$ at 8bit access mode and 0_H~$3F_H$ at 16bit access mode.

- **8BIT access**



- **16 BIT access**



In the Black & white mode, the MSBs of 3 bit and 2 bit corresponding with RGB are used to display data. And so, 128x82 dot gray display or 384 x 82 B/W mode display is possible.

Display RAM is accessed with X address and Y address from CPU by 8 bit or 16 bit unit.

X address and Y address can be increased automatically by setting status of control register.

The address is increased per every read and write of display RAM by CPU. (Please see detail description at command function.)

X direction is selected by X address and Y direction is selected by Y address. Please do not set the address on non-effective area and it is forbidden to set address on outside area in each case.

384bit display data of Y direction are read out to display latch at rising edge of CL signal per 1 line cycle and this data comes out from display latch at falling edge of CL signal.

Display start line address register is preset to line counter at “H” state of FLM signal which changes per one frame cycle and the address is counted up with synchronized CL input.

Display line address counter is synchronized by timing signals of LCD driver, and it operates independently with X, Y address counters.

(7) Window address assign of display RAM

This IC can be accessed to display RAM by window area designation in addition to access to display RAM designated by X and Y address.

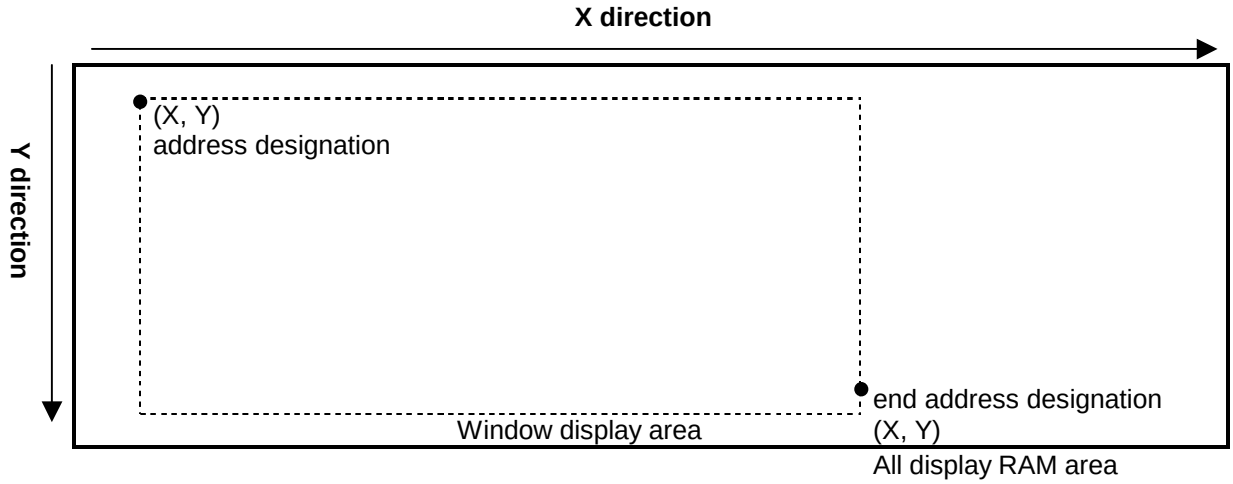
Through address space of all display address, specific area of RAM can be accessed by designated two points.

The start point of two point addresses is assigned by normal X address and Y address register and the end point of them is done by X end address and Y end address register value. Designated inner addresses depend on WLS bit.

Read modified write action can be taken by AIM="1".

In case of using window area accessing mode, you must set start point X address, Y address in sequence and end point X address, Y address in sequence after executing Win command (WIN="1", auto increase mode AXI="1", AYI="1") and then access to Display RAM.

And set start point and end point not to be designated to access the outside of available address area. Address set value should be taken to set AX ≤ EX (end point of X address) and AY≤EY (end point of Y address).



(8) display RAM data and LCD

Display RAM data related with one dot of LCD is dependent on REV register. Normal display and reverse display by REV register are set up as follows.

TABLE

REV	Display	RAM data
L	normal	0
		1
H	reverse	0
		1

(9) Segment display output order/reverse set up

The order of display outputs, $SEGA_0$, $SEGB_0$, $SEGC_0$ to $SEGA_{127}$, $SEGB_{127}$, and can be reversed by reversing access to display RAM from MPU by using REF register, lessen the limitation in placing IC when assembling an LCD panel module.

(10) Relation between Display RAM and address

- RAM address and bitmap

COLOR / 16 BIT MODE

REF	SWAP	X address / bit / segment assign																																
0	0	X=00$_H$																......	X=3F$_H$															
1	1	X=3F$_H$																......	X=00$_H$															
		D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	......	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}
		palette A		palette B			palette C			palette A		palette B			palette C			......	palette A		palette B			palette C			palette A		palette B			palette C		
		SEGA0		SEGB0			SEGC0			SEGA1		SEGB1			SEGC1			......	SEGA126		SEGB126			SEGC126			SEGA127		SEGB127			SEGC127		

REF	SWAP	X address / bit / segment assign																																
0	1	X=00$_H$																......	X=3F$_H$															
1	0	X=3F$_H$																......	X=00$_H$															
		D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	......	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		palette C			palette B			palette A		palette C			palette B			palette A		......	palette C			palette B			palette A		palette C			palette B			palette A	
		$SEGA_0$			$SEGB_0$			$SEGC_0$		$SEGA_1$			$SEGB_1$			$SEGC_1$		......	$SEGA_{126}$			$SEGB_{126}$			$SEGC_{126}$		$SEGA_{127}$			$SEGB_{127}$			$SEGC_{127}$	

COLOR / 8 BIT MODE

REF	SWAP	X address / bit / segment assign																																
0	0	X=00$_H$								X=01$_H$								......	X=7E$_H$								X=7F$_H$							
1	1	X=7F$_H$								X=7E$_H$								......	X=01$_H$								X=00$_H$							
		D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	......	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
		palette A		palette B			palette C			palette A		palette B			palette C			......	palette A		palette B			palette C			palette A		palette B			palette C		
		$SEGA_0$		$SEGB_0$			$SEGC_0$			$SEGA_1$		$SEGB_1$			$SEGC_1$			......	$SEGA_{126}$		$SEGB_{126}$			$SEGC_{126}$			$SEGA_{127}$		$SEGB_{127}$			$SEGC_{127}$		

REF	SWAP	X address / bit / segment assign																																
0	1	X=00$_H$								X=01$_H$								......	X=7E$_H$								X=7F$_H$							
1	0	X=7F$_H$								X=7E$_H$								......	X=01$_H$								X=00$_H$							
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	......	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		palette C			palette B			palette A		palette C			palette B			palette A		......	palette C			palette B			palette A		palette C			palette B			palette A	
		$SEGA_0$			$SEGB_0$			$SEGC_0$		$SEGA_1$			$SEGB_1$			$SEGC_1$		......	$SEGA_{126}$			$SEGB_{126}$			$SEGC_{126}$		$SEGA_{127}$			$SEGB_{127}$			$SEGC_{127}$	

BLACK & WHITE / 16 BIT MODE

REF	SWAP	X address / bit / segment assign		
0	0	$X=00_H$	·····	$X=3F_H$
1	1	$X=3F_H$	·····	$X=00_H$

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	·····	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}
	$SEGA_0$			$SEGB_0$			$SEGC_0$		$SEGA_1$			$SEGB_1$			$SEGC_1$		·····	$SEGA_{126}$			$SEGB_{126}$			$SEGC_{126}$		$SEGA_{127}$			$SEGB_{127}$			$SEGC_{127}$		

REF	SWAP	X address / bit / segment assign		
0	1	$X=00_H$	·····	$X=3F_H$
1	0	$X=3F_H$	·····	$X=00_H$

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	·····	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	$SEGA_0$			$SEGB_0$			$SEGC_0$		$SEGA_1$			$SEGB_1$			$SEGC_1$		·····	$SEGA_{126}$			$SEGB_{126}$			$SEGC_{126}$		$SEGA_{127}$			$SEGB_{127}$			$SEGC_{127}$		

BLACK & WHITE / 8 BIT MODE

REF	SWAP	X address / bit / segment assign				
0	0	$X=00_H$	$X=01_H$	·····	$X=7E_H$	$X=7F_H$
1	1	$X=7F_H$	$X=7E_H$	·····	$X=01_H$	$X=00_H$

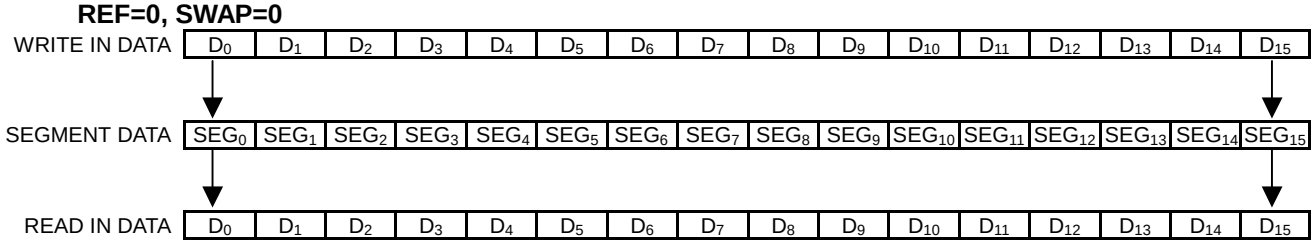
	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	·····	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
	$SEGA_0$			$SEGB_0$			$SEGC_0$		$SEGA_1$			$SEGB_1$			$SEGC_1$		·····	$SEGA_{126}$			$SEGB_{126}$			$SEGC_{126}$		$SEGA_{127}$			$SEGB_{127}$			$SEGC_{127}$		

REF	SWAP	X address / bit / segment assign				
0	1	$X=00_H$	$X=01_H$	·····	$X=7E_H$	$X=7F_H$
1	0	$X=7F_H$	$X=7E_H$	·····	$X=01_H$	$X=00_H$

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	·····	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	$SEGA_0$			$SEGB_0$			$SEGC_0$		$SEGA_1$			$SEGB_1$			$SEGC_1$		·····	$SEGA_{126}$			$SEGB_{126}$			$SEGC_{126}$		$SEGA_{127}$			$SEGB_{127}$			$SEGC_{127}$		

• WRITE IN / READ IN BITMAP (16 BIT MODE)

REF=0, SWAP=0



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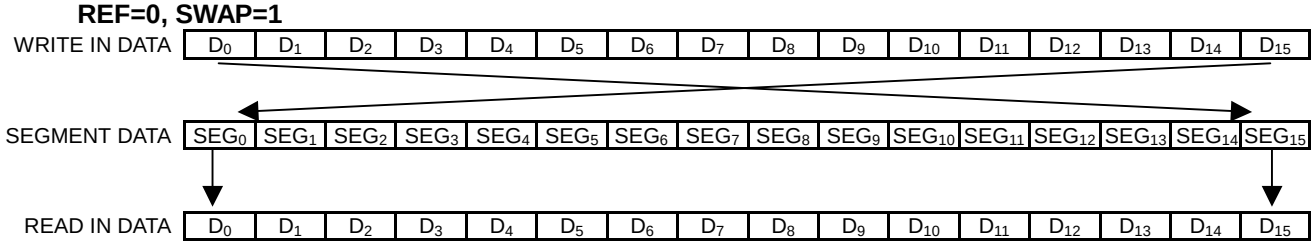
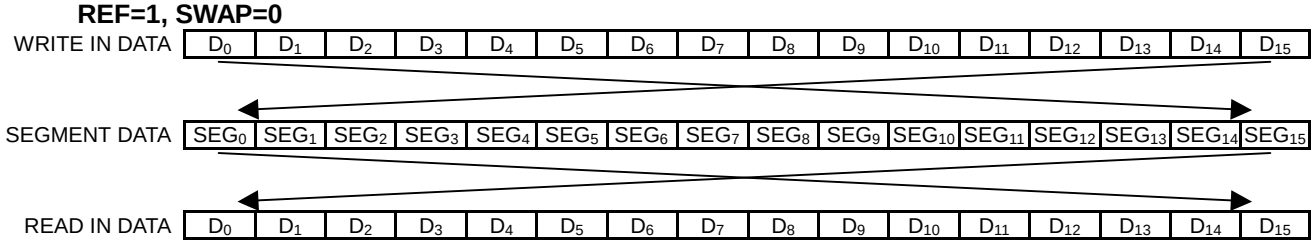
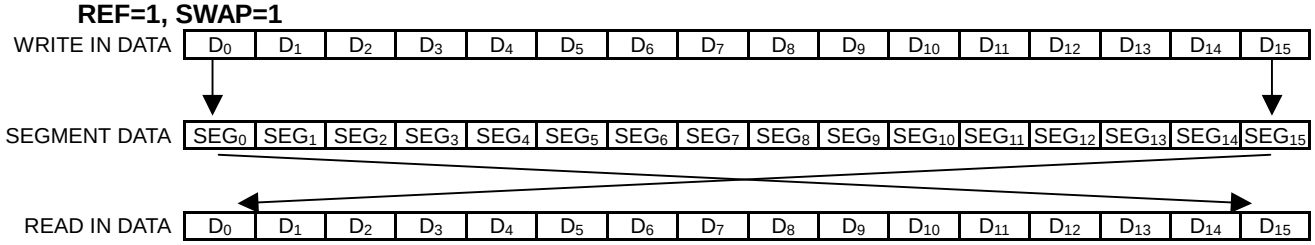


REF=1, SWAP=0



REF=1, SWAP=1



- READ OUT AFTER WROTE IN DATA (16 BIT MODE)

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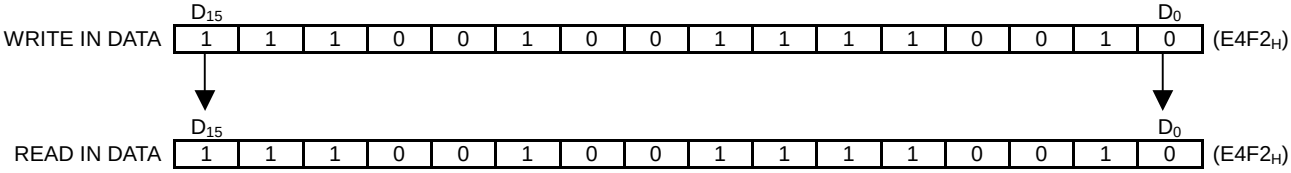
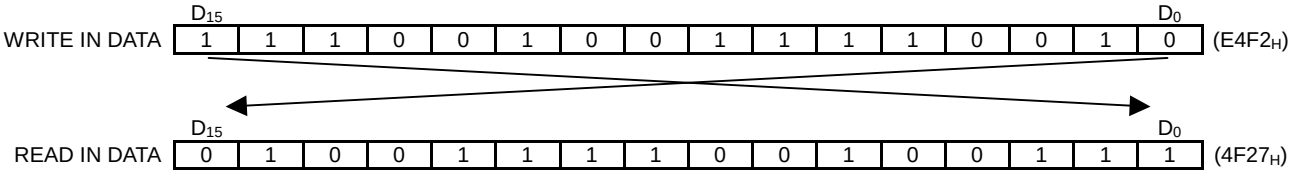
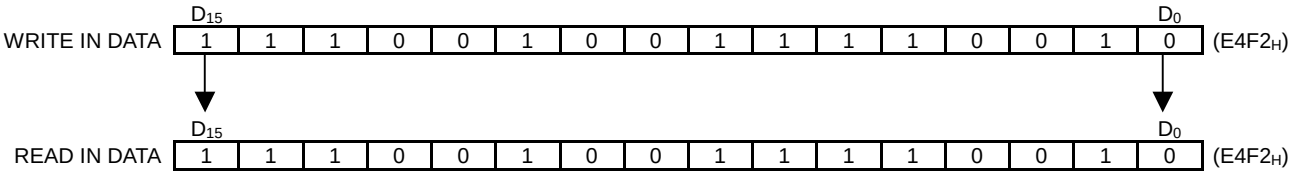


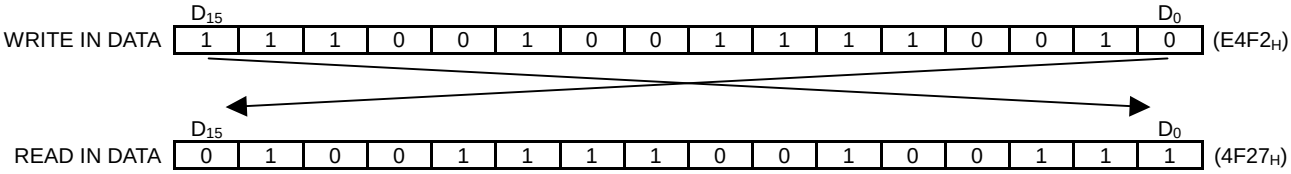
REF=0, SWAP=1



REF=1, SWAP=0

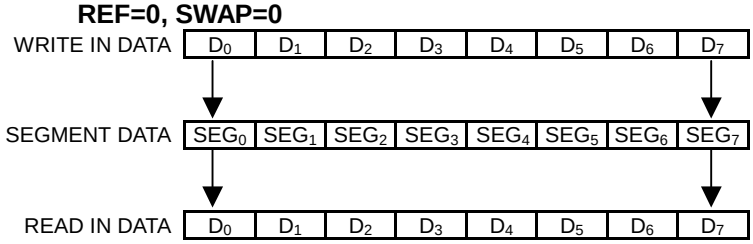


REF=1, SWAP=1

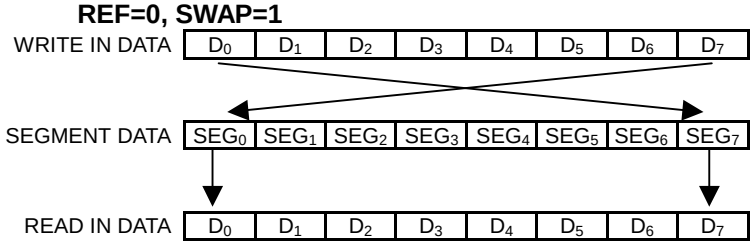


• WRITE IN / READ IN BITMAP (8 BIT MODE)

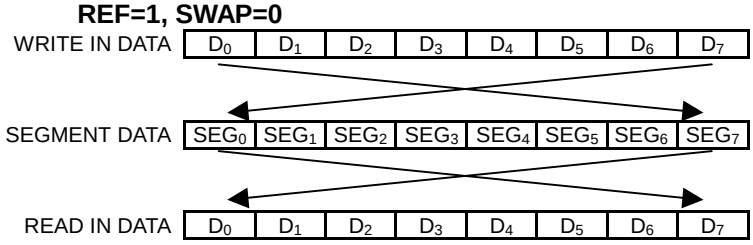
REF=0, SWAP=0



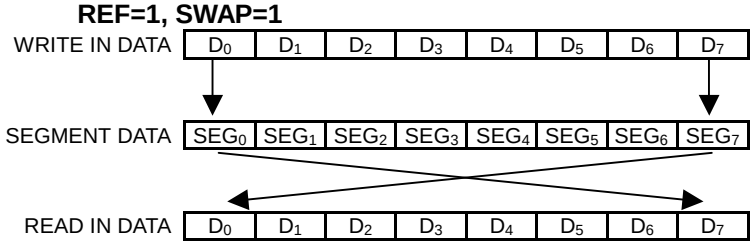
REF=0, SWAP=1



REF=1, SWAP=0

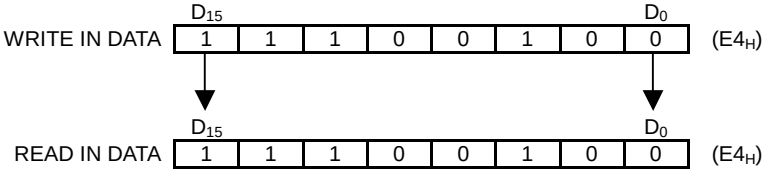


REF=1, SWAP=1

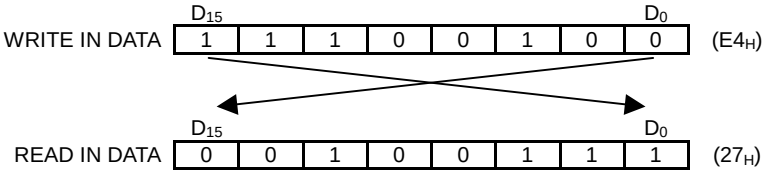


- READ OUT AFTER WROTE IN DATA (8 BIT MODE)

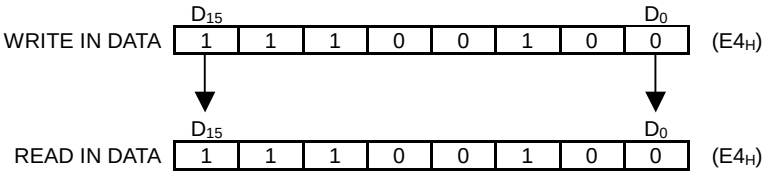
REF=0, SWAP=0



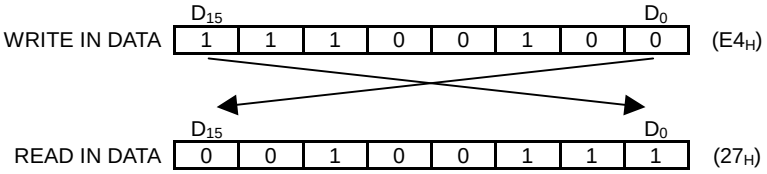
REF=0, SWAP=1



REF=1, SWAP=0



REF=1, SWAP=1



- DUMMY SEGMENT REGISTER ADDRESS AND BITMAP

COLOR / 16 BIT MODE

REF	SWAP	X address / bit segment assign																											
0	0	$X=00_H$														$X=01_H$													
1	1	$X=01_H$														$X=00_H$													
		D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}
		Palette A		Palette B		Palette C		Palette A		Palette B		Palette C		Palette A		Palette B		Palette C		Palette A		Palette B		Palette C		Palette A		Palette B		Palette C	
		$SEGSA_0$		$SEGSB_0$		$SEGSC_0$		$SEGSA_1$		$SEGSB_1$		$SEGSC_1$		$SEGSA_2$		$SEGSB_2$		$SEGSC_2$		$SEGSA_3$		$SEGSB_3$		$SEGSC_3$					

REF	SWAP	X address / bit segment assign																											
0	1	$X=00_H$														$X=01_H$													
1	0	$X=01_H$														$X=00_H$													
		D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D1	D_0	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		Palette C		Palette B		Palette A		Palette C		Palette B		Palette A		Palette C		Palette B		Palette A		Palette C		Palette B		Palette A		Palette C		Palette B		Palette A	
		$SEGSA_0$		$SEGSB_0$		$SEGSC_0$		$SEGSA_1$		$SEGSB_1$		$SEGSC_1$		$SEGSA_2$		$SEGSB_2$		$SEGSC_2$		$SEGSA_3$		$SEGSB_3$		$SEGSC_3$					

COLOR / 8 BIT MODE

REF	SWAP	X address / bit segment assign																											
0	0	$X=00_H$								$X=01_H$								$X=02_H$								$X=03_H$			
1	1	$X=03_H$								$X=02_H$								$X=01_H$								$X=00_H$			
		D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
		Palette A		Palette B		Palette C		Palette A		Palette B		Palette C		Palette A		Palette B		Palette C		Palette A		Palette B		Palette C					
		$SEGSA_0$		$SEGSB_0$		$SEGSC_0$		$SEGSA_1$		$SEGSB_1$		$SEGSC_1$		$SEGSA_2$		$SEGSB_2$		$SEGSC_2$		$SEGSA_3$		$SEGSB_3$		$SEGSC_3$					

REF	SWAP	X address / bit segment assign																											
0	1	$X=00_H$								$X=01_H$								$X=02_H$								$X=03_H$			
1	0	$X=03_H$								$X=02_H$								$X=01_H$								$X=00_H$			
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		Palette C		Palette B		Palette A		Palette C		Palette B		Palette A		Palette C		Palette B		Palette A		Palette C		Palette B		Palette A					
		$SEGSA_0$		$SEGSB_0$		$SEGSC_0$		$SEGSA_1$		$SEGSB_1$		$SEGSC_1$		$SEGSA_2$		$SEGSB_2$		$SEGSC_2$		$SEGSA_3$		$SEGSB_3$		$SEGSC_3$					

• BLACK 7 WHITE / 16 BIT MODE

REF	SWAP	X address / bit segment assign
0	0	$X=00_H$ / $X=01_H$
1	1	$X=01_H$ / $X=00_H$

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}
		$SEGSA_0$			$SEGSB_0$			$SEGSC_0$		$SEGSA_1$			$SEGSB_1$			$SEGSC_1$		$SEGSA_2$			$SEGSB_2$			$SEGSC_2$		$SEGSA_3$			$SEGSB_3$			$SEGSC_3$

REF	SWAP	X address / bit segment assign
0	1	$X=00_H$ / $X=01_H$
1	0	$X=01_H$ / $X=00_H$

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	$SEGSA_0$			$SEGSB_0$			$SEGSC_0$		$SEGSA_1$			$SEGSB_1$			$SEGSC_1$		$SEGSA_2$			$SEGSB_2$			$SEGSC_2$		$SEGSA_3$			$SEGSB_3$			$SEGSC_3$	

• BLACK & WHITE / 8 BIT MODE

REF	SWAP	X address / bit segment assign
0	0	$X=00_H$ / $X=01_H$ / $X=02_H$ / $X=03_H$
1	1	$X=03_H$ / $X=02_H$ / $X=01_H$ / $X=00_H$

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
		$SEGSA_0$			$SEGSB_0$			$SEGSC_0$		$SEGSA_1$			$SEGSB_1$			$SEGSC_1$		$SEGSA_2$			$SEGSB_2$			$SEGSC_2$		$SEGSA_3$			$SEGSB_3$			$SEGSC_3$

REF	SWAP	X address / bit segment assign
0	1	$X=00_H$ / $X=01_H$ / $X=02_H$ / $X=03_H$
1	0	$X=03_H$ / $X=02_H$ / $X=01_H$ / $X=00_H$

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	$SEGSA_0$			$SEGSB_0$			$SEGSC_0$		$SEGSA_1$			$SEGSB_1$			$SEGSC_1$		$SEGSA_2$			$SEGSB_2$			$SEGSC_2$		$SEGSA_3$			$SEGSB_3$			$SEGSC_3$	

(11) display data structure and gradation control

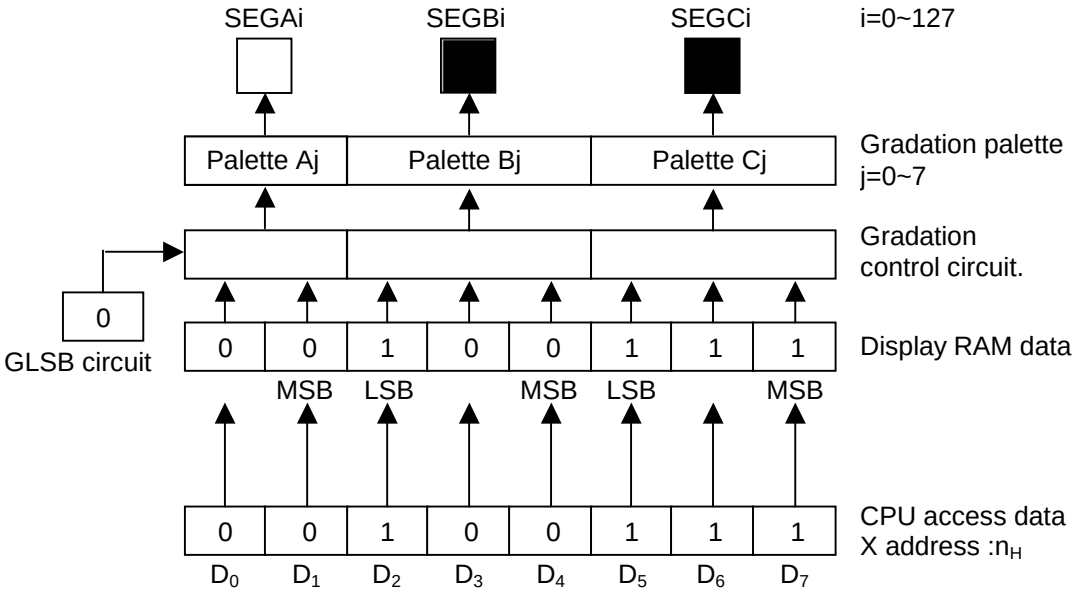
For the purpose of gradation control, information per pixel requires multiple bits. This IC has 3 bit or 2 bit data per output to achieve the gradation display.

This IC is connected to an STN color LCD panel by three segment port units and one pixel consists of three outputs of segment driver, and so 256 color (3 bits x 3 bits x 2 bits) display on 128 x 82 pixels is realized.

Since one pixel data can be processed by one time access to memory, the data can be rewritten fast and naturally.

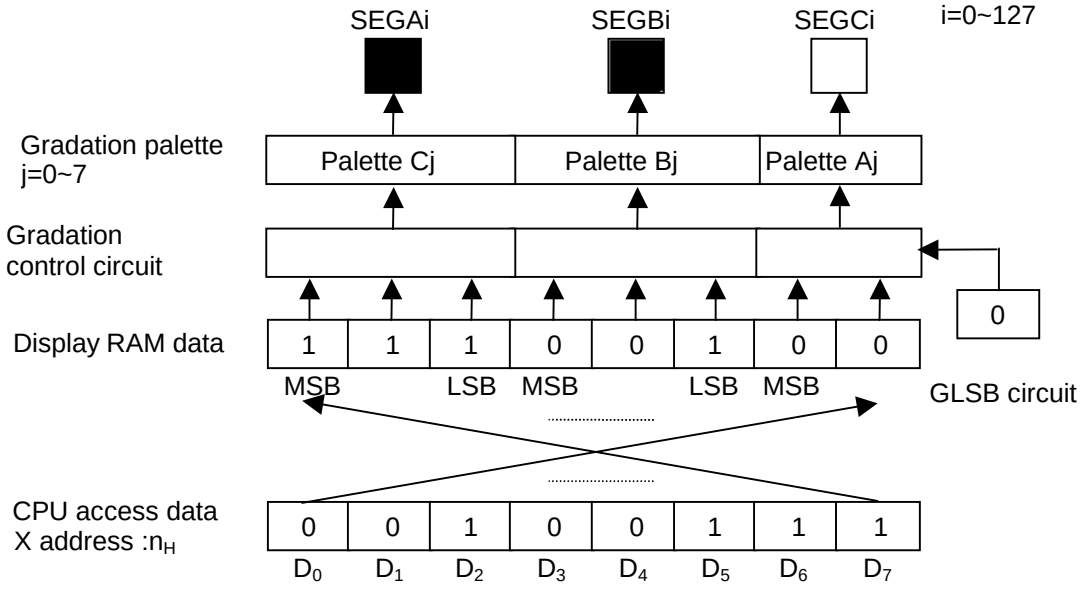
The weight of each data bit is dependent on the status of SWAP register bit and REF register when data is written to the display RAM.

- **ACCESS when (REF, SWAP)=(0, 0) or (1, 1)**



notice) internal access X address :n_H~$7F_H$ (access when REF="0")
:$7F_H$~n_H (access when REF="1")

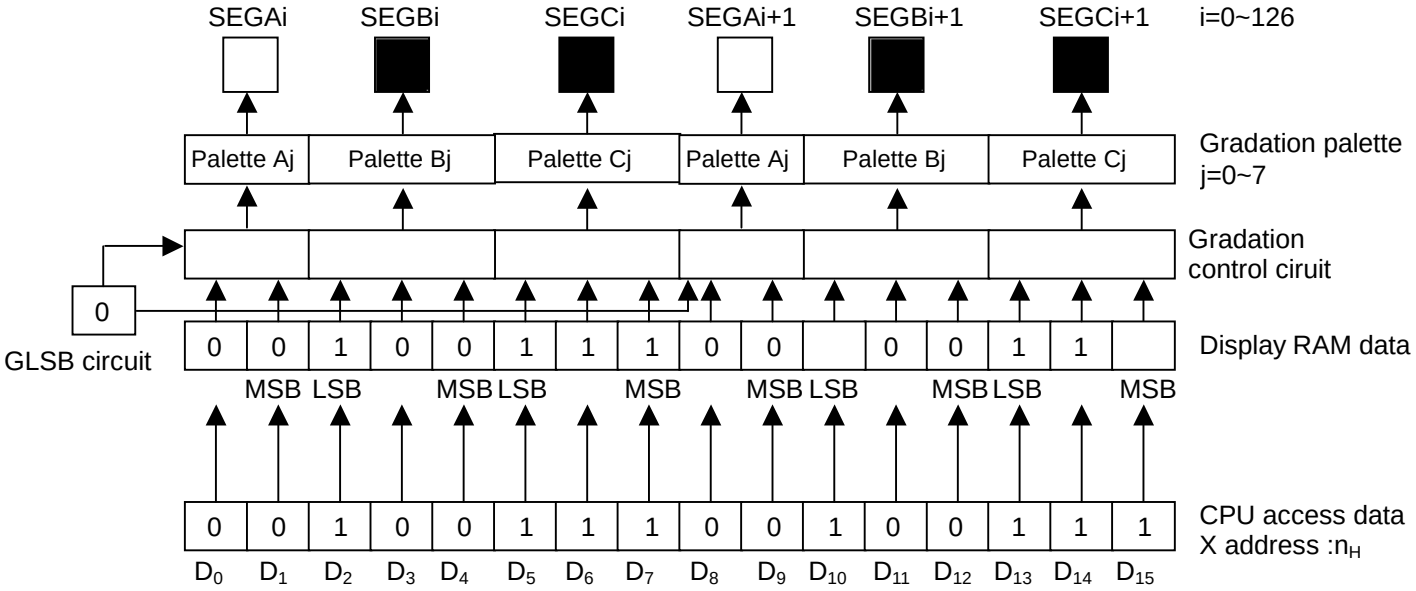
- **ACCESS when (REF, SWAP)=(0, 1) or (1, 0)**



notice) internal access X address :n_H~$7F_H$ (access when REF="0")
:$7F_H$~n_H (access when REF="1")

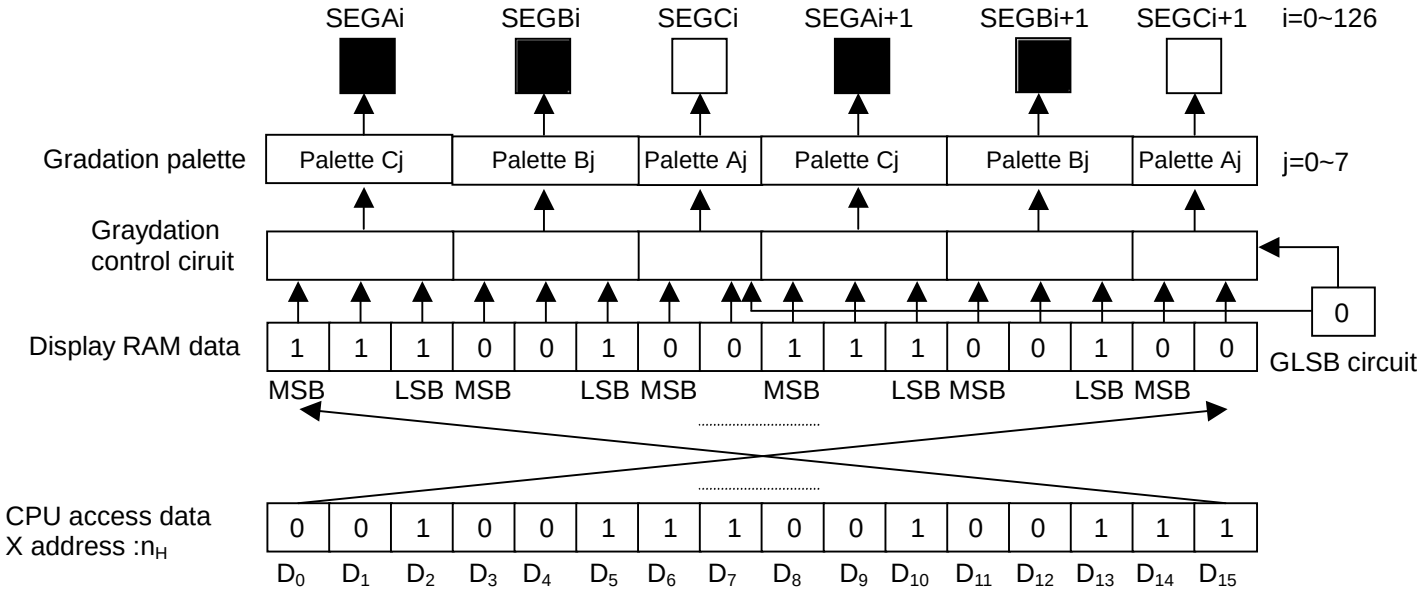
When display RAM is accessed by 16 bit data width, the weight of each data bit is dependent on the status of SWAP register and REF register, the same method as 8 bit access

- ACCESS when (REF, SWAP)=(0, 0) or (1, 1)



notice) internal access X address :n_H~$3F_H$ (access when REF="0")
:$3F_H$~n_H (access when REF="1")

- ACCESS when (REF, SWAP)=(0, 1) or (1, 0)

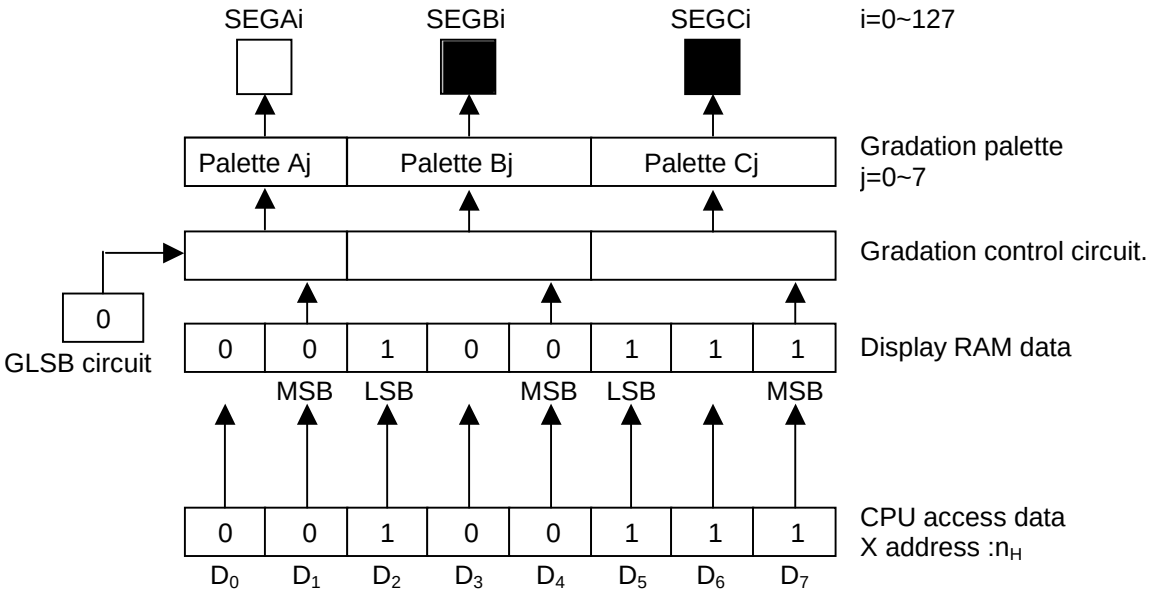


notice) internal access X address :n_H~$3F_H$ (access when REF="0")
:$3F_H$~n_H (access when REF="1")

- DISPLAY RAM BITMAP AT BLACK & WHITE MODE (MON="1")
  The MSBs of display RAM data (3 bit, 2 bit) is used as display data at black and white mode.

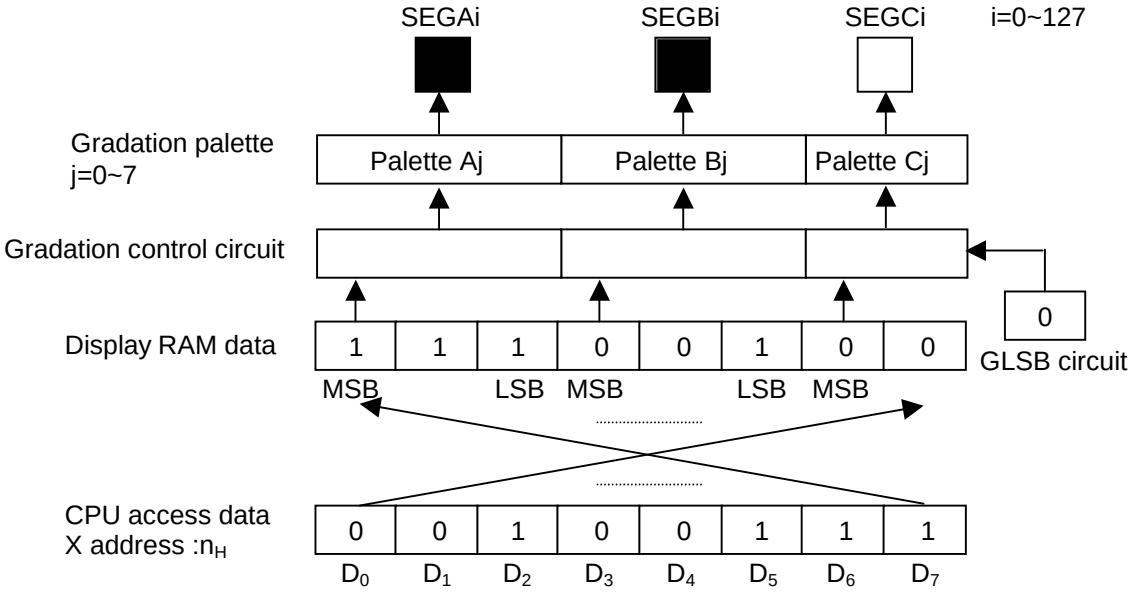
example) **8 bit width access (the same method as 16 bit width access)**

- ACCESS when (REF, SWAP)=(0, 0) or (1, 1)



notice) internal access X address :n_H (access when REF="0")
:7Fn_H~n_H (access when REF="1")

- ACCESS when (REF, SWAP)=(0, 1) or (1, 0)



notice) internal access X address :n_H (access when REF="0")
:7Fn_H~n_H (access when REF="1")

gradation level table (MON="1", Black & white mode)

(MSB)RAM data (LSB)			Gradation level
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

RAM data		GLSB	Gradation level
0	0	*	0
0	1	*	0
1	0	*	1
1	1	*	1

** : Don't Care*

(12) GRADATION LSB CONTROL

At 256 colors input mode, this IC provides segment driver output for 8-gradation display using successive 3 bits of data and that for 4-gradation display using successive 2 bits of data.

The segment driver output for the 4-gradation display uses 2 bits written to the corresponding RAM area and 1 bit supplemented by the gradation LSB circuit, and then selects 4 gradations from 8-gradations.

At fixed gradation mode, the segment driver output for the 4-gradation display result in a gradation level of 0 regardless of gradation LSB register, when 2 bits of data on the display RAM are "00". When 2 bits of data on the display RAM is "11", a gradation level of 7/7 is selected regardless of gradation LSB register. The other gradation levels are selected depending on 2 bits of data on the display RAM and the gradation LSB register.

One bit of data is supplemented by setting the gradation LSB register (GLSB).

For this register, the bit information specified for only one time setting is used as the LSB of the RAM for all the 4-gradation segment drivers.

Gradation LSB = "0": Set 0 as the LSB of the RAM for 4-gradation segment drivers.
Gradation LSB = "1": Set 1 as the LSB of the RAM for 4-gradation segment drivers.

(13) GRADATION PALETTE

This IC has two gradation display modes, the fixed gradation display mode and the variable gradation display mode.

Select mode by setting the gradation display mode register (PWM command) to the purpose.

PWM="0" : variable gradation mode among 32-level gradations.
PWM="1" : fixed 8 gradation mode

To select the best gradation level suited to LCD panel at variable gradation display mode, use the gradation palette register among 32-level gradation palettes. Segment driver outputs are set by selected 8-level gradation palette.

The gradation palette register provides three registers (palette Aj, Bj, and Cj : j=0~7) for the segment driver outputs, SEGAi(0~127), SEGBi(0~127), and SEGCi(0~127) . Each register consists of a 5-bit register, selecting 8 gradations from the 32 gradation pattern.

Segment driver selects 4 gradations among 8 gradation by 2 bits wrote-in RAM and 1bit calibrated by GLSB.

GRADATION PALETTE INITIAL VALUE

(palette Aj, palette Bj, palette Cj (j=0~7))

(MSB)RAM data (LSB)			Register name	Initial value
0	0	0	Gradation palette 0	0 0 0 0 0
0	0	1	Gradation palette 1	0 0 1 0 1
0	1	0	Gradation palette 2	0 1 0 1 0
0	1	1	Gradation palette 3	0 1 1 1 0
1	0	0	Gradation palette 4	1 0 0 0 1
1	0	1	Gradation palette 5	1 0 1 0 1
1	1	0	Gradation palette 6	1 1 0 1 0
1	1	1	Gradation palette 7	1 1 1 1 1

GRADATION PALETTE TABLE (PWM="0", variable mode)

(palette Aj, palette Bj, palette Cj (j=0~7))

Palette	Gradation	remark	Palette	gradation	remark
0 0 0 0 0	0	Palette 0 initial value	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Palette 4 initial value
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31		1 0 0 1 1	19/31	
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Palette 1 initial value	1 0 1 0 1	21/31	Palette 5 initial value
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31		1 0 1 1 1	23/31	
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31	Palette 2 initial value	1 1 0 1 0	26/31	Palette 6 initial value
0 1 0 1 1	11/31		1 1 0 1 1	27/31	
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31	Palette 3 initial value	1 1 1 1 0	30/31	
0 1 1 1 1	15/31		1 1 1 1 1	31/31	Palette 7 initial value

GRADATION PALETTE TABLE (PWM="1", fixed mode)

(MSB)RAM data(LSB)			gradation
0	0	0	0
0	0	1	1/7
0	1	0	2/7
0	1	1	3/7
1	0	0	4/7
1	0	1	5/7
1	1	0	6/7
1	1	1	7/7

RAM data		GLSB	gradation
0	0	0	0
0	0	1	
0	1	0	2/7
0	1	1	3/7
1	0	0	4/7
1	0	1	5/7
1	1	0	7/7
1	1	1	

(14) DISPLAY TIMMING GENERATOR

The display-timing generator makes a timing clock and timing pulses (CL, FLM, FR and CLK) for internal operation by inputting the original oscillating clock CK or by the oscillating circuit.

By setting up Master / Slave mode (M/S), the state of timing pulse pins and the timing generator changes.

Display timing pulse pins and generator status

M/S port	mode	CL port	FR port	FLM port	CLK port	Timing generator status
L	Slave	Input	Input	Input	Input	CL, FLM, FR signal generator stop
H	Master	Output	Output	Output	Output	Operating status

(15) SIGNAL GENERATION OF DISPLAY LINE COUNTER, DISPLAY DATA LATCH CIRCUIT.

The latch signal from line counter clock to display data latch circuit is generated from display clock (CL). Synchronized with the display clock, the line addresses of Display RAM are generated and 384-bit display data are latched to display-data latching circuit and then output to the LCD drive circuit (SEG output port).

Read-out of the display data to the LCD drive circuit is completely independent of MPU side and so MPU can access it with no relationship with the read-out operation of the display data.

(16) GENERATION OF THE ALTERNATED SIGNAL(FR), SYNCHRONOUS SIGNAL(FLM).

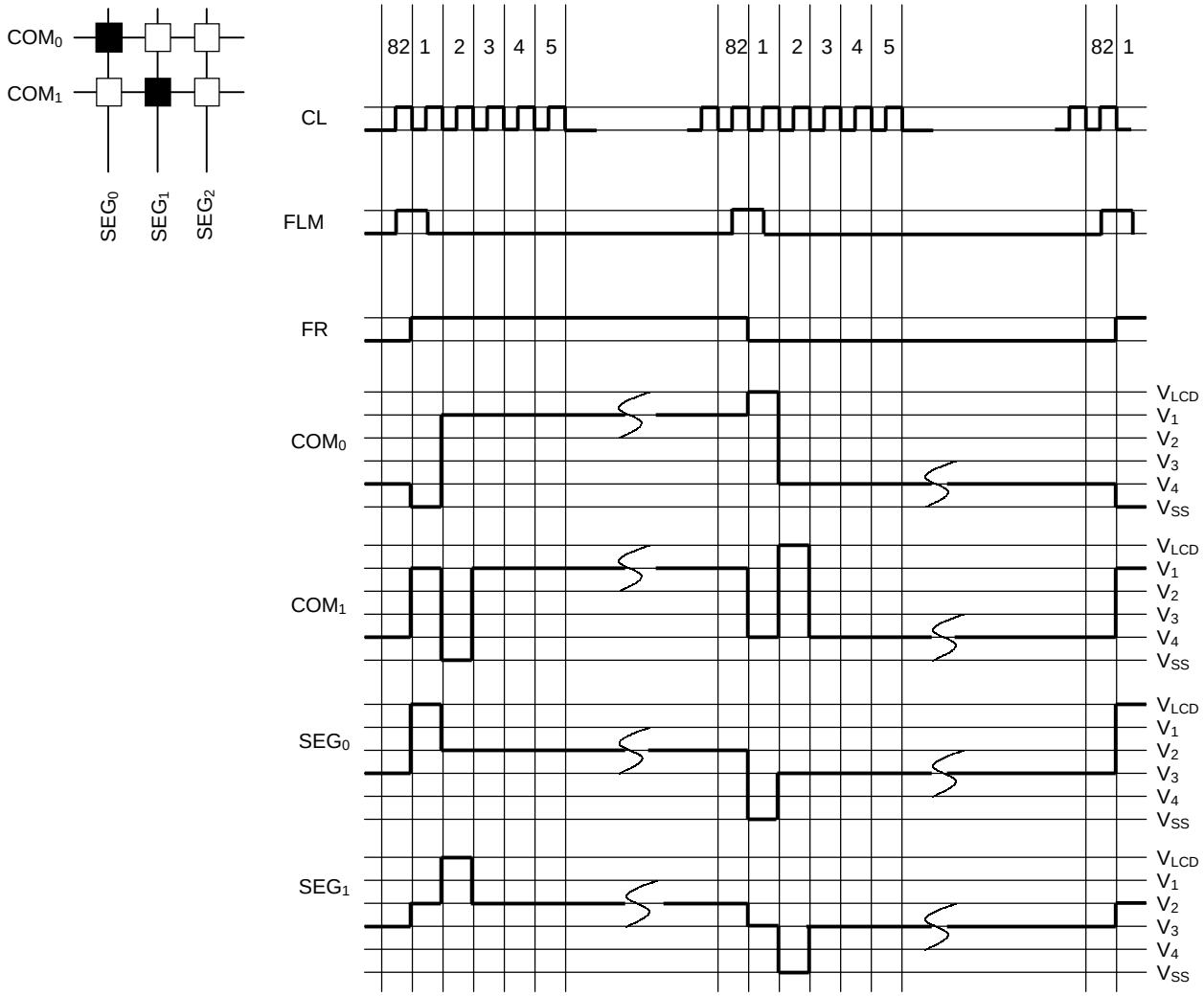
The alternated signal (FR) and synchronous signal (FLM) are generated from the display clock (CL). The FLM generates alternated drive waveform to the LCD drive circuit per frame at normal state (inverse FR signal level per 1 frame). But by setting up data (n-1) on n-line inversion register and “1” on n-line alternated command (NLIN), n-line inverse waveform can be generated.

When this **HM17CM256** is used in multi-chip application, the signals of CL, FLM, FR and CLK must be sent from master side to slave side.

(17) DISPLAY DATA LATCH CIRCUIT

This circuit latches the display data from display RAM to LCD driver circuit temporarily per every common period. Normal / reverse display, display ON/OFF, and display all on command are done by controlling data in this latch. And no data within display RAM changes.

(18) EXAMPLE OF LCD DRIVING (NORMAL MODE, 1/82 DUTY, BLACK & WHITE DISPLAY MODE)



(19) LCD DRIVER CIRCUIT

This drive circuit generates four levels of LCD drive voltage. The circuit has 384 segment outputs and 82 common outputs and outputs combined display data and FR signal.

Two of common outputs($COMI_0$,$COMI_1$) are for pictograph marker display only. The common drive circuit that has shift register and outputs common scan signals sequentially.

(20) DUMMY SEGMENT DRIVER CIRCUIT

Segment driver circuit has 6 dummy output ($SEGSA_0$ ~ $SEGSA_3$, $SEGSB_0$ ~ $SEGSB_3$, $SEGSC_0$ ~ $SEGSC_3$) at each edge side. Normally, the segment driver output is generated by memorized RAM data but there are no RAMs but registers for dummy segment driver. There are 8 bit registers correspond to $SEGSA_0$, $SEGSB_0$, $SEGSC_0$ and drive LCD with same level to Y direction. ($SEGSA_1$ ~ $SEGSA_3$, $SEGSB_1$ ~ $SEGSB_3$, $SEGSC_1$ ~ $SEGSC_3$ are the same function.)

$SEGSA_0$ ~ $SEGSA_3$ port is used same gradation palette with $SEGA_0$ ~ $SEGA_{127}$, $SEGSB_0$ ~ $SEGSB_3$ with $SEGB_0$ ~ $SEGB_{127}$, and $SEGSC_0$ ~ $SEGSC_3$ with $SEGC_0$ ~ $SEGC_{127}$

This circuit is effective at display of boundary or background display. The dummy segment drivers do not depend on LREV polarity but ALLON and REV command for display

There are 4-byte registers for dummy segment driver, $SEGSA_0$ ~ $SEGSA_3$, $SEGSB_0$ ~ $SEGSB_3$, $SEGSC_0$ ~ $SEGSC_3$, If you want to access this register, please use DMY =”1” command.

RS	DMY	68 series	80 series		Function
		$\overline{R/W}$	$\overline{RD}$	$\overline{WR}$	
0	0	1	0	1	Read out display data
0	0	0	1	0	Write in display data
0	1	1	0	1	Read out dummy segment register
0	1	0	1	0	Write in dummy segment register

There are the same rules at read out of dummy segment register as display RAM data read out sequence. After address setting, the data of assigned address is shown directly after the end of the read command, so pay attention that assigned data is available at 2nd timing step. In other words, there needs 1 cycle dummy read after address set and write cycle.

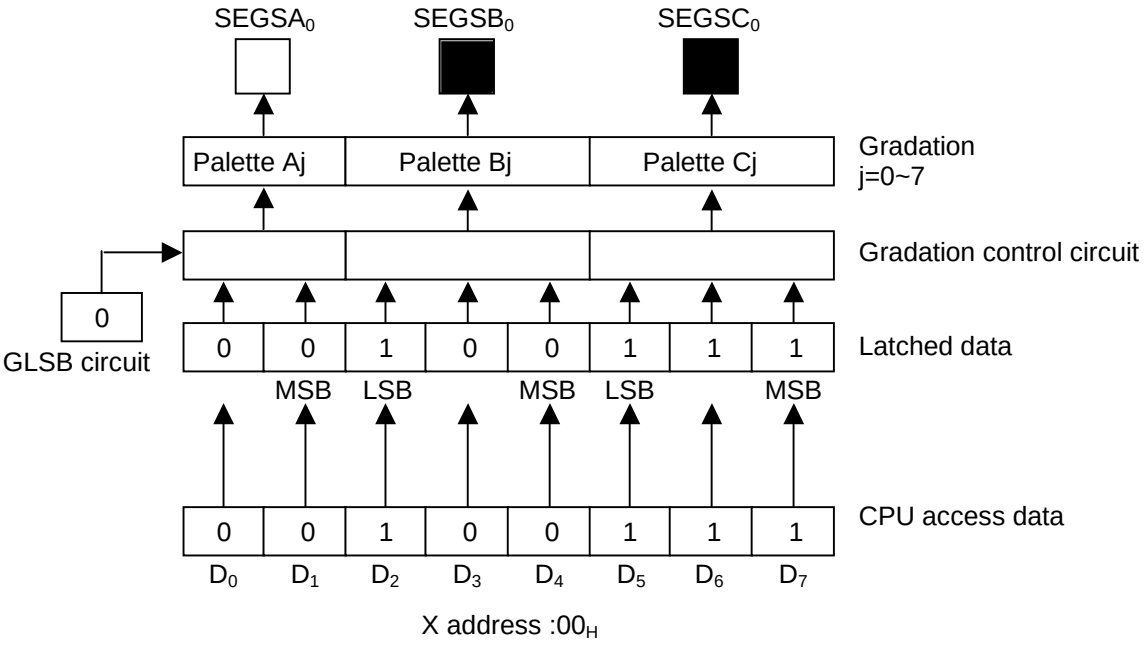
1 cycle dummy read is necessary for after address setting and write cycle.

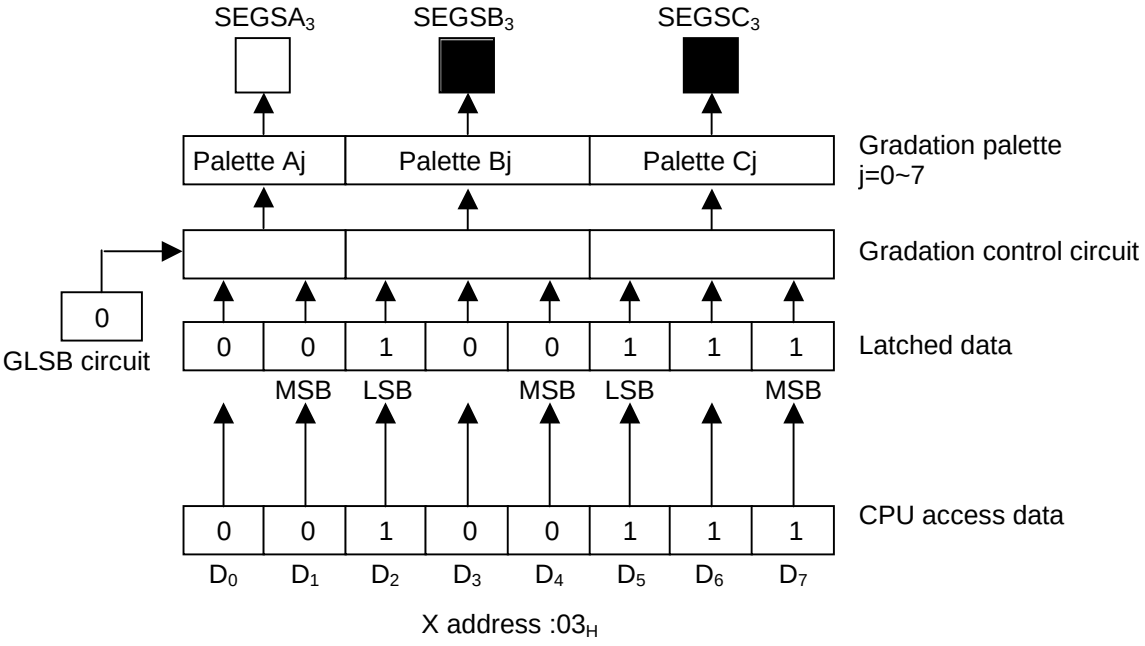
When access with DMY=”1”, X address is an effective value at address setting. There are 4-byte and so 00_H, 01_H, 02_H, 03_H are effective at 8-bit mode and 00_H, 01_H are effective at 16-bit mode. The access bears no relation to Y address setting.

When access with DMY=”1”, it is possible that the data is written into register by increment operation.

notice) more detail information at 「DUMMY SEGMENT REGISTER ADDRESS AND BITMAP」 in 「(10) Relation between Display RAM and address」

ACCESS WITH 8 BIT BUS EXAMPLE : GRAY MODE , ACCESS UNDER (REF, SWAP)=(0, 0)





(21) OSCILLATOR CIRCUIT

HM17CM256 has the CR oscillator. The output of oscillator is used as the timing signal source of display and boosting clock to the booster. This is valid only in the master operation mode.

When in the master operation mode and if external clock is used, feed the clock to OSC_1 pin or connect resistor between OSC_1 and OSC_2.

And feedback resistance with command can set the inner oscillator circuit of HM17CM256.

The frame frequency can be altered by changed oscillator frequency according to feedback resistance length set value. To get optimum frame frequency, please check LCD and then set the frequency of oscillator.

(22) POWER SUPPLY CIRCUIT

This block generates the voltages necessary for driving LCD panel. The power supply circuit consists of voltage boosting circuit and voltage converting circuit and generates the voltages (V_{LCD}, V_1, V_2, V_3, V_4.) for LCD driving.

For large panel driving, it's preferable to use external voltage source rather than to use built-in power supply circuit for good image quality.

When using external voltage source, disable the built-in power supply circuit(AMPON, DCON='00'), supply the V_{LCD}, V_1, V_2, V_3, V_4 and V_{OUT} externally and open the C_1+, C_1-, C_2+, C_2-, C_3+, C_3-, C_4+, C_4-, C_5+, C_5-, C_6+, C_6-, V_{REF}, V_{REG}, V_{EE} terminals.

According to power supply circuit control command input, the power supply circuit can be enabled partially. External power supply and partial inner power circuit can be used together. Refer to the next table.

DCON	AMPON	Boosting circuit	Converting circuit	External voltage input	remark
0	0	Disable	disable	V_{OUT}, V_{LCD}, V_1, V_2, V_3, V_4 common	※1,3
0	1	Disable	enable	V_{OUT} common	※2,3
1	1	Enable	enable	–	–

※1. All the built-in boosting circuit, converting circuit is not used. Open the ,C_1+, C_1-, C_2+, C_2-, C_3+, C_3-, C_4+, C_4-, C_5+, C_5-, C_6+, C_6-, V_{REF}, V_{REG}, V_{EE} terminals, LCD driving voltage should be applied externally.

※2.Only the Boosting circuit is not used. Open the C_1+,C_1-,C_2+,C_2-,C_3+,C_3-,C_4+,C_4-,C_5+,C_5-,C_6+,C_6-, V_{OUT} terminals, The power for converting circuit must be supplied through V_{OUT} terminal and the reference voltage must be supplied by V_{REF} terminal.

※3.The conditions between V_{OUT}, V_{LCD}, V_1, V_2, V_3, and V_4 are $V_{OUT} \geq V_{LCD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$.

(23) VOLTAGE BOOSTING CIRCUIT

By connecting capacitor CA_1 between C_1+ and C_1-, C_2+ and C_2-, C_3+ and C_3-, C_4+ and C_4-, C_5+ and C_5- , C_6+ and C_6-, V_{OUT} and V_{SS} , n-time boosted voltage of V_{EE} - V_{SS} can be generated through V_{OUT} port. The boosting coefficient can be set by command and 2-times/ 3-times / 4-times/ 5-times/ 6-times/ 7-times boosted voltage is output through V_{OUT} port.

At application, specific boosting coefficient is used, refer to the following description.

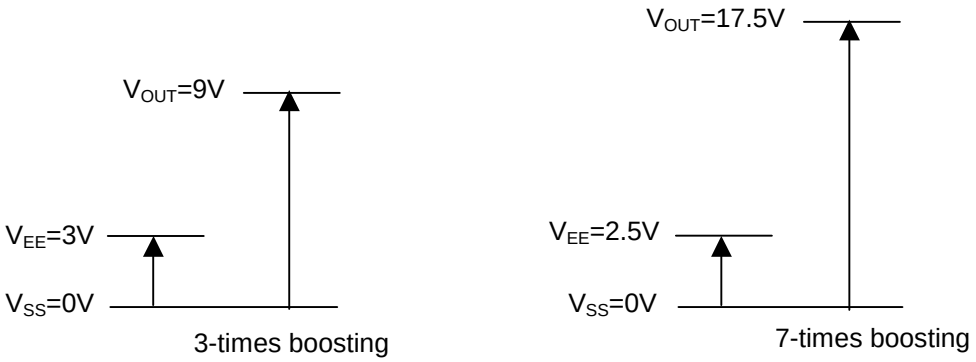
① At 2-times boosting is designed, connect boosting capacitor CA_1 between C_1+ and C_1- , and open C_2+, C_2-, C_3+, C_3-, C_4+, C_4-, C_5+, C_5-, C_6+, C_6- terminals.

② At 3-times boosting is designed, connect boosting capacitor CA_1 between C_1+ and C_1- , C_2+ and C_2- , and open C_3+,C_3-, C_4+, C_4-, C_5+, C_5-, C_6+, C_6- terminals.

③ At 4-times boosting is designed, connect boosting capacitor CA_1 between C_1+ and C_1- , C_2+ and C_2- , C_3+ and C_3- , and open C_4+, C_4-, C_5+, C_5-, C_6+, C_6- terminals

④ At 5-times/ 6-times/ 7-times boosting are same structures with upper case.

Special care should be taken so that the voltage of VOUT would not exceed 18V MAX.
VOUT voltage exceeding 18V can cause malfunction and reliability problem.



(24) ELECTRIC VOLUME

The electric volume is within voltage converting circuit and the brightness of LCD can be controlled by adjusting V_{LCD} level with command.

The LCD driving voltage V_{LCD} is generated by selecting 1 level within 128 step electric volume controlled levels by setting 7 bit electric volume register.

(25) VOLTAGE REGULATOR CIRCUIT

The voltage regulator circuit is within voltage converting circuit and generates regulated voltage using V_{REF} input with magnification by adjusting internal resistor. The generated voltage by voltage regulator is output at V_{REG} terminal. Even though boosted voltage variation, generated regulator voltage is stable because boosting voltage level is higher than the amplified regulator voltage V_{REG} . And so, stable voltage level can be generated even if there is load variation.

V_{REG} is used as input voltage of electric volume circuit to generate LCD driving voltage.

(26) REFERENCE VOLTAGE GENERATION CIRCUIT

The reference voltage generation circuit is within voltage converting circuit.

This circuit generates reference voltage V_{BA} terminal for using at regulator circuit through. The output voltage level from V_{BA} terminal is as following description.

$$V_{BA} = V_{EE} \times 0.9$$

The LCD driving voltages can be made by applying reference voltage to reference voltage input terminal V_{REF} .

(27) LCD DRIVING VOLTAGE GENERATION CIRCUIT

The generation circuit of LCD driving voltage is within voltage converting circuit and generates voltages V_{LCD}, V_1, V_2, V_3, V_4 by resistively dividing V_{LCD} into 4 levels.

The bias ratio of LCD driving voltages can be one of 1/5, 1/6, 1/7, 1/8, 1/9, 1/10.

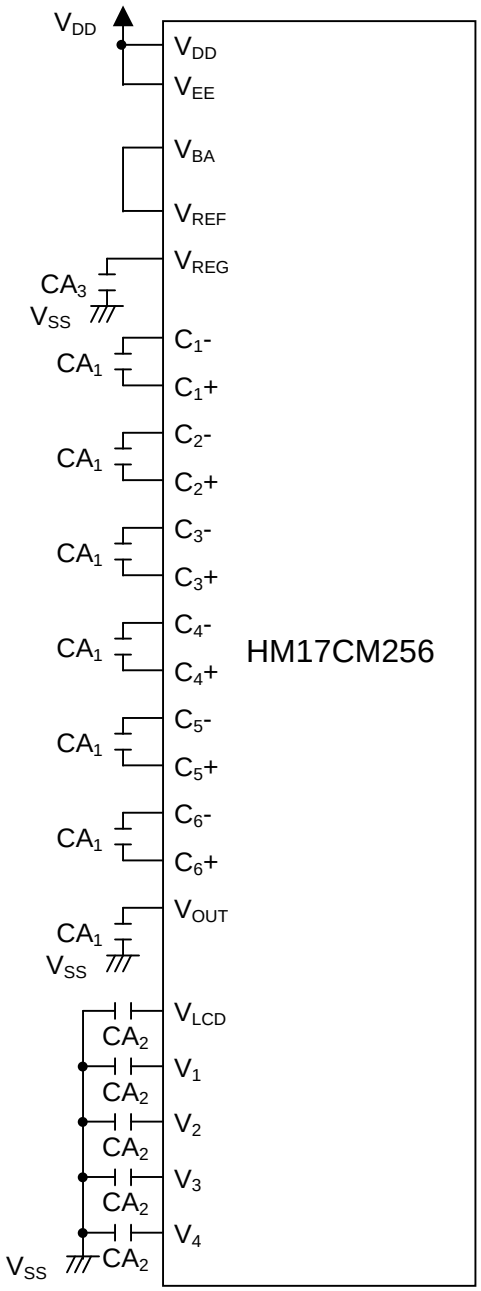
When using built-in power supply circuit, you should connect voltage stabilization capacitor CA_2 at each of LCD power terminals. There is need for selecting the coefficient of capacitor CA_2 after display the LCD.

When using external voltage supply, disable the built-in power supply circuit(AMPON, DCON='00'), supply the V_{OUT}, V_{LCD}, V_1, V_2, V_3, V_4 voltages externally and open the C_1+ , C_1- , C_2+ , C_2- , C_3+ , C_3- , C_4+ , C_4- , C_5+ , C_5- , C_6+ , C_6- , V_{EE} , V_{REF} , V_{REG} terminals.

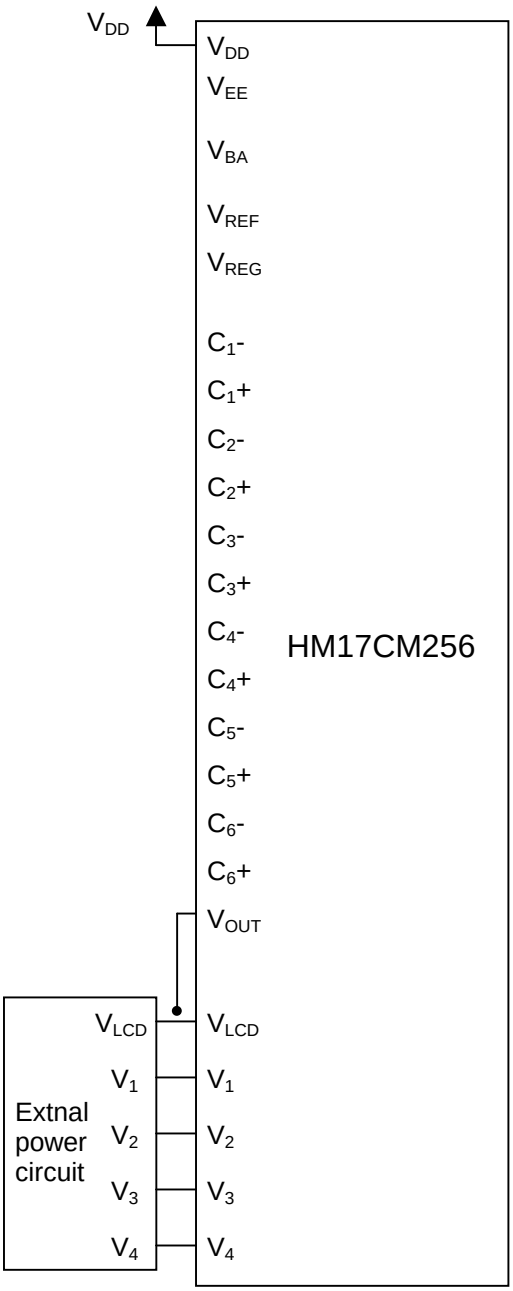
When using external voltage source and parts of built-in voltage converting circuit, the terminals of C_1+ , C_1- , C_2+ , C_2- , C_3+ , C_3- , C_4+ , C_4- , C_5+ , C_5- , C_6+ , C_6- should be open because boosting circuit is not activated, you should supply reference voltage through V_{REF} terminal and the voltage for voltage converting circuit at V_{OUT} .

Connecting stabilization capacitor CA_3 at V_{REG} terminal is recommended.

internal power circuit / internal reference voltage generating circuit are activated case.(7 times boosting)



internal power circuit is not used case

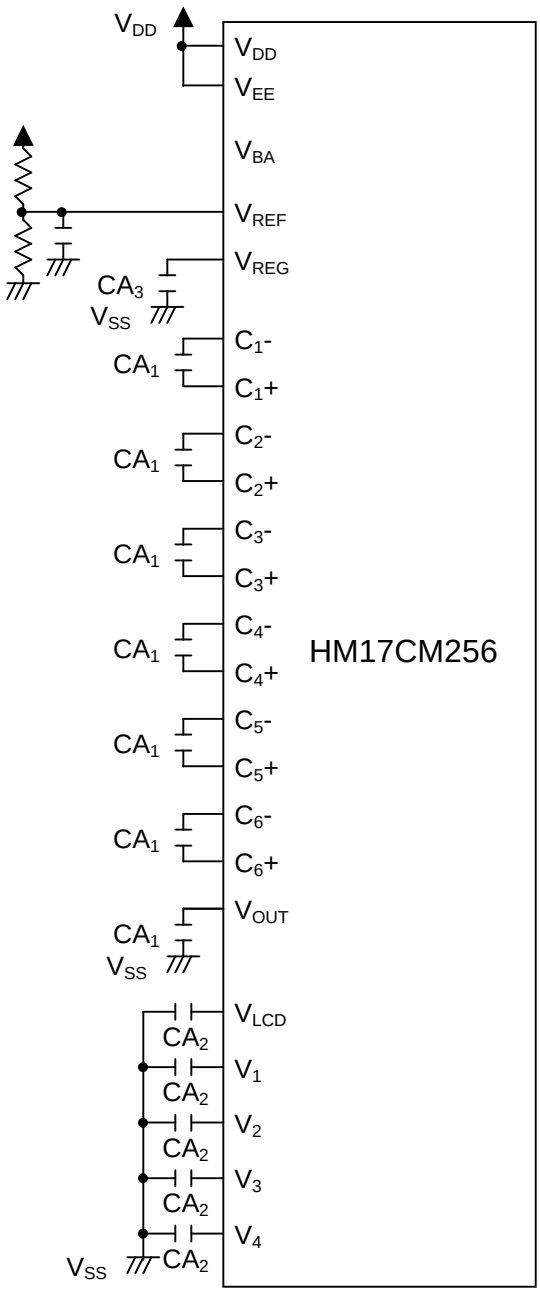


value

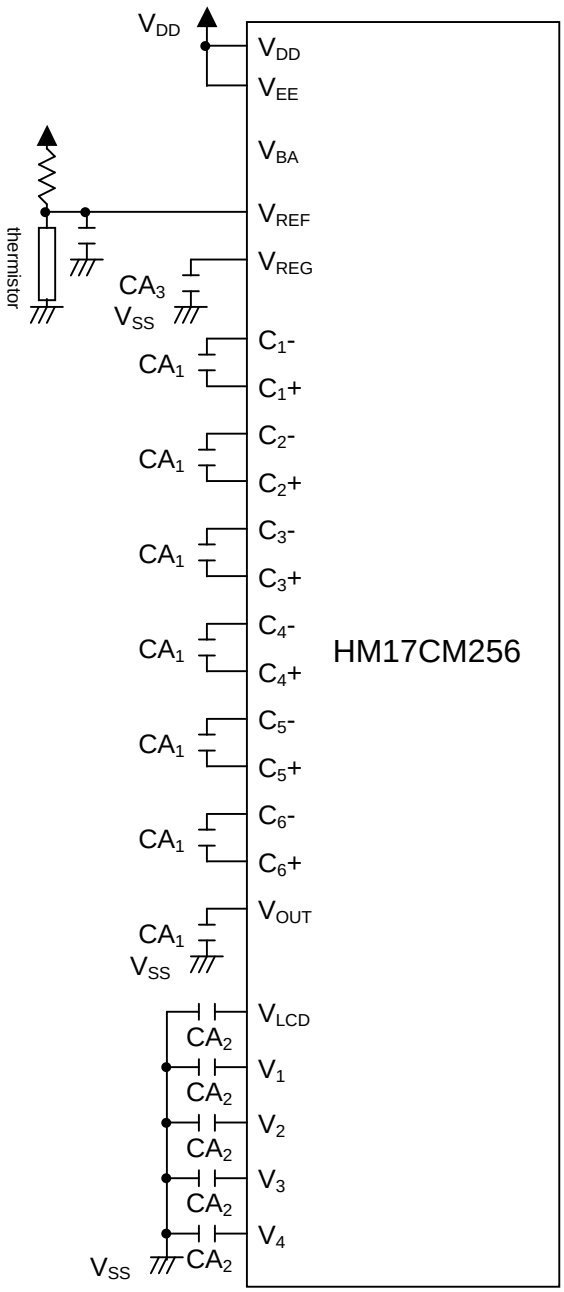
CA_1	1.0 ~ 4.7μF
CA_2	1.0 ~ 2.2μF
CA_3	0.1μF

caution） Please use B grade capacitor.

Internal power circuit is used case. Reference voltage input from outside . (7 times boosting)



Internal power circuit is used case. Temperature compensation by external thermistor . (7 times boosting)

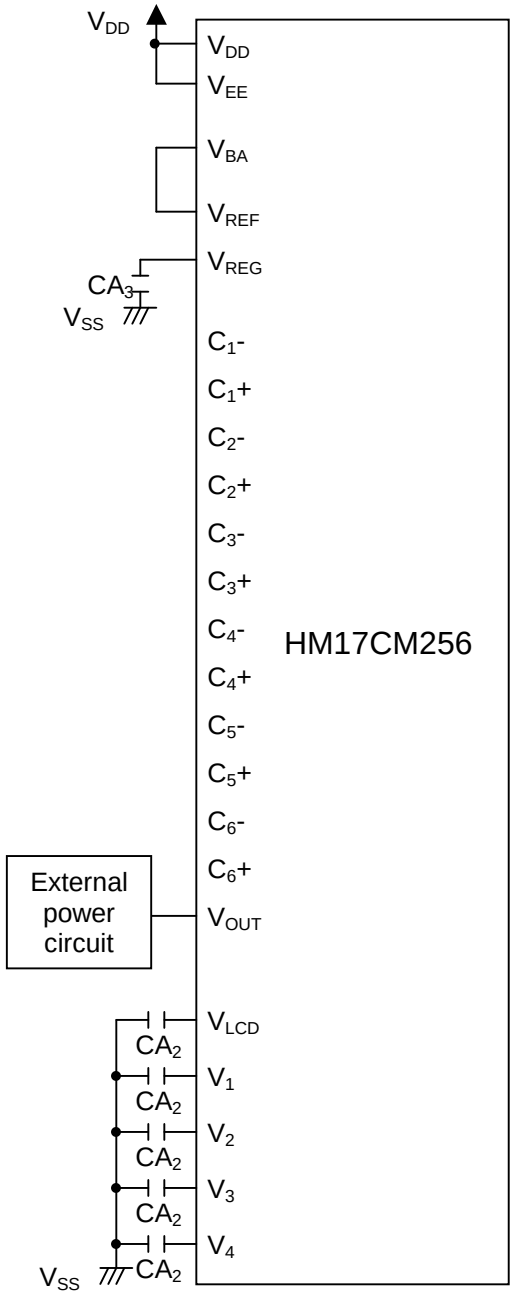


value

CA_1	1.0 ~ 4.7μF
CA_2	1.0 ~ 2.2μF
CA_3	0.1μF

caution） Please use B grade capacitor.

Internal power circuit is used case. (boosting circuit is not used, V_{OUT} is supplied from outside)



value

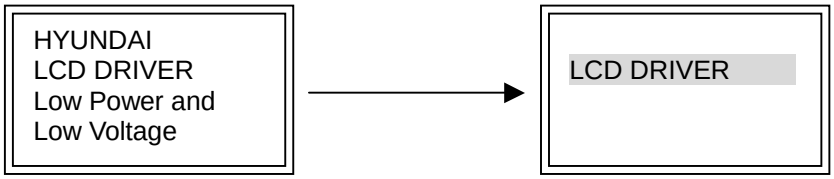
CA_1	1.0 ~ 4.7μF
CA_2	1.0 ~ 2.2μF
CA_3	0.1μF

caution） Please use B grade capacitor.

(28) PARTIAL DISPLAY FUNCTION

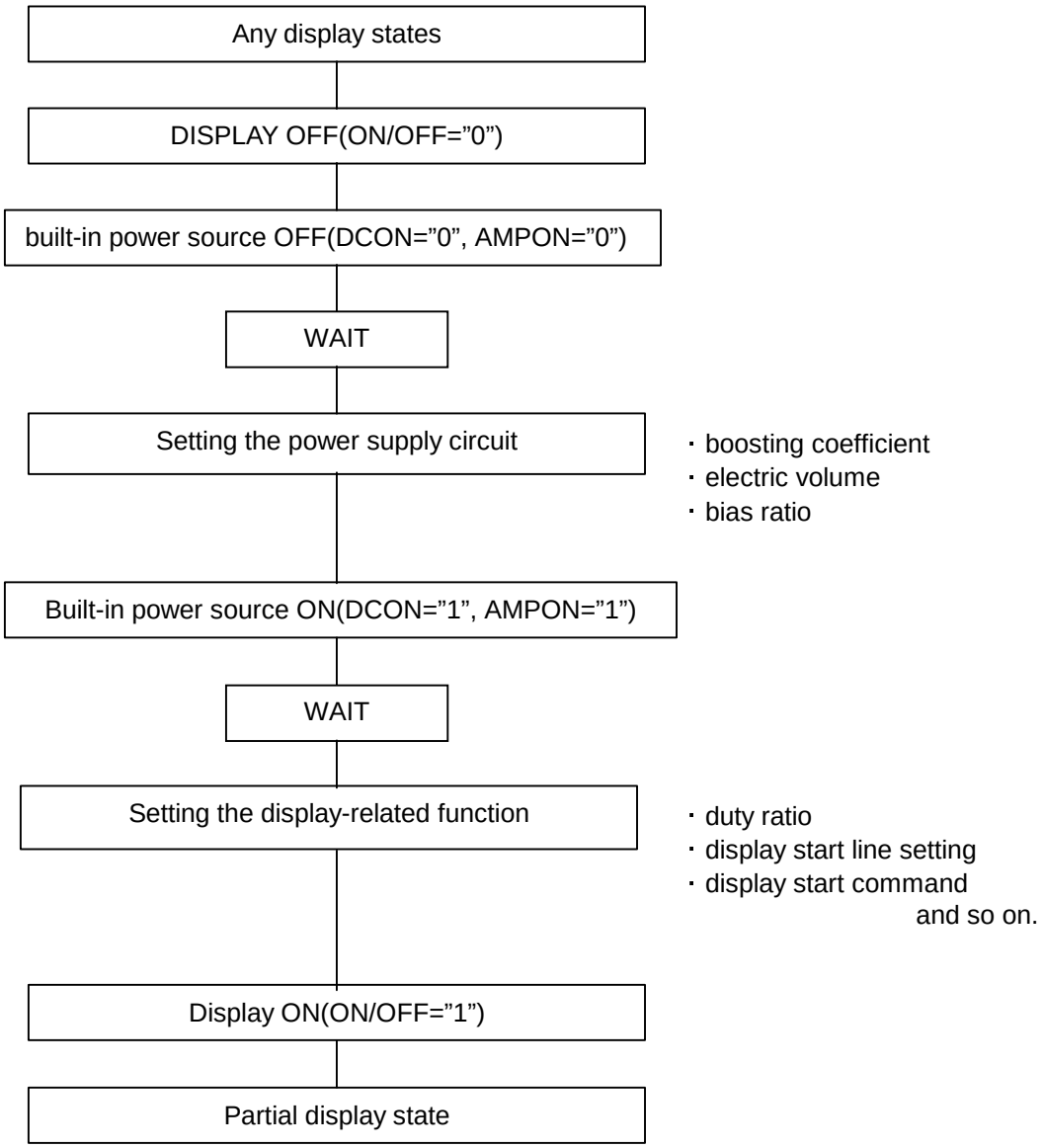
HM17CM256 can realize the partial display at graphic display area on LCD panel.
Partial display is used with lower duty than normal state at driving.
And so, HM17CM256 can drive the LCD panel with lower bias ratio, lower boosting times and lower LCD driving voltages, and that can drive the LCD panel with lower power consumption.
This function is suitable for calendar or clock display at mobile information apparatus.

PARTIAL DISPLAY IMAGE



Normal display　　partial display

The next sequence should be followed carefully to realize partial display function.



When using partial display function, the display duty can be selected among 1/17, 1/26, 1/32, 1/38, 1/47, 1/66, 1/77 by setting the LCD duty set command.

The display states such as LCD driving bias ratio, LCD Driving voltage, electric volume setting value, boosting coefficient should be optimized to the selected LCD and display duty.

(29) DISCHARGE CIRCUIT

The discharge circuit of voltage(V_{LCD}, V_1~V_4) stabilization capacitor is built in the HM17CM256.

To discharge the capacitors, set the DIS register to “1” or set the $\overline{RES}$ terminal to “0”. When built-in power supply circuit is used, built-in power supply circuit should be disabled before discharging of the capacitor is executed. When external power supply(V_{LCD}, V_1~V_4, V_{OUT}) is used, external power supply should be turned off before discharging of the capacitor is executed. Do not turn on the internal power supply and external power supply (V_{LCD}, V_1~V_4, V_{OUT}) during discharging is executed.

(30) RESET CIRCUIT

HM17CM256 is initialized as following description when $\overline{RES}$ terminal is set to “L”.

INITIAL SETTING CONDITION (default setting)

1. display RAM :unknown
2. X address :00_H set
3. Y address :00_H set
4. display start line :1 line value 0_H
5. display ON/OFF :display OFF
6. positive/negative :positive
7. display duty ratio :1/82
8. n line inversion :n inversion disable
9. COM shift direction :$COM_0 \rightarrow COM_{79}$, $COMI_0$, $COMI_1$
10. increment mode :increment OFF
11. REF mode :positive
12. data SWAP mode :OFF
13. electric volume :(0, 0, 0, 0, 0, 0, 0)
14. power circuit :OFF
15. display mode :gradation display mode
16. bias ratio :1/10 bias
17. gradation palette 0 :(0, 0, 0, 0, 0)
18. gradation palette 1 :(0, 0, 1, 0, 1)
19. gradation palette 2 :(0, 1, 0, 1, 0)
20. gradation palette 3 :(0, 1, 1, 1, 0)
21. gradation palette 4 :(1, 0, 0, 0, 1)
22. gradation palette 5 :(1, 0, 1, 0, 1)
23. gradation palette 6 :(1, 1, 0, 1, 0)
24. gradation palette 7 :(1, 1, 1, 1, 1)
25. gradation mode :variable mode
26. GLSB :"0"
27. RAM data length :8 bit mode
28. discharge register :"0"

Usually $\overline{RES}$ terminal is connected reset terminal of CPU, so that the chip can be initialized simultaneously with CPU. HM17CM256 should be initialized when the power is on.

(31) SUPPLYING POWER AND ON/OFF SEQUENCE

Special care should be taken to the next notice. Supplying the power at LCD driving voltage terminal when the logic VDD is floating can cause over-current and damage the IC

(31-1) WHEN USING EXTERNAL POWER SUPPLY

- power ON sequence

Reset the IC after supplying the logic power at V_{DD} terminal, and then turn on the LCD driving voltage at the terminals (V_{LCD}, V_1, V_2, V_3, V_4).

And when internal voltage converter is used, reset the IC after supplying the logic power at V_{DD} terminal, and then supply power to V_{LCD} terminal.

- power OFF sequence

Execute HALT command or reset the IC to turn off the outputs of LCD driving output port, and then turn off the LCD driving voltage after logic power OFF.

Inserting series resistor of 50 ~100Ω or fuse at V_{LCD} or V_{OUT} terminal (when only internal voltage converting circuit is used) is recommended to prevent over-current.

This series resistor should be selected carefully because image quality can be dependent on.

(31-2) WHEN USING BUILT-IN POWER SUPPLY CIRCUIT

- power ON sequence

Reset the IC after supplying the logic power at V_{DD} terminal or after supplying power through voltage common port (V_{EE}) of boosting voltage generation and then operate internal power circuit by command.

And when internal voltage converter is used, reset the IC after supplying the logic power at V_{DD} terminal, and then supply power to V_{LCD} terminal.

You should turn on the display after the output level of internal power module is set.

If you do not keep this sequence, LCD can display wrong data.

- power OFF sequence

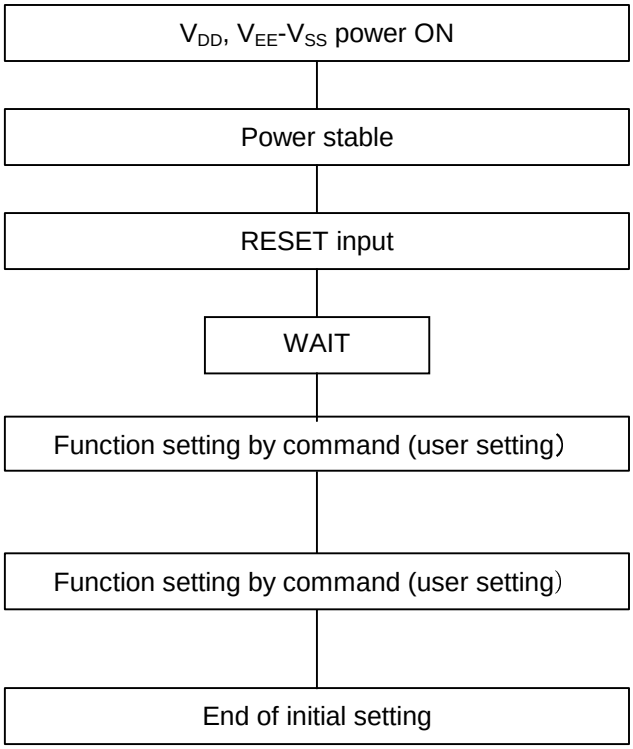
To make off state of LCD driving output, cut the source to voltage common port (V_{EE}) of boosting voltage generation, the logic power at V_{DD} terminal after reset the IC by HALT command.

If V_{EE}, and V_{DD} are supplied from different power source, V_{EE} terminal should be turned on/off during V_{DD} terminal voltage maintain voltage level specified in specification sheet.

Specially, when turn off the power, after cut the source to voltage common port (V_{EE}), and then turn off the logic power at V_{DD} terminal after the voltage levels of V_{EE}, V_{OUT}, V_{LCD}, V_1~V_4 become under LCD on voltage(LCD threshold voltage)level.

(32) COMMAND SETTING EXAMPLE

(32-1) initial setting

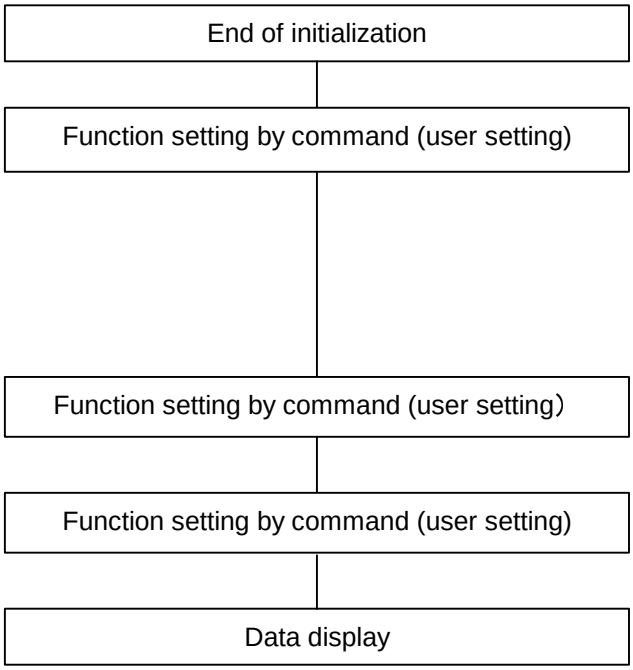


- electric volume code set
- bias ratio set

- power control set
  (DCON="1", AMPON="1")

(notice) If the voltage level of VEE and VDD are different, VDD should be inputted first.

(32-2) DATA DISPLAY

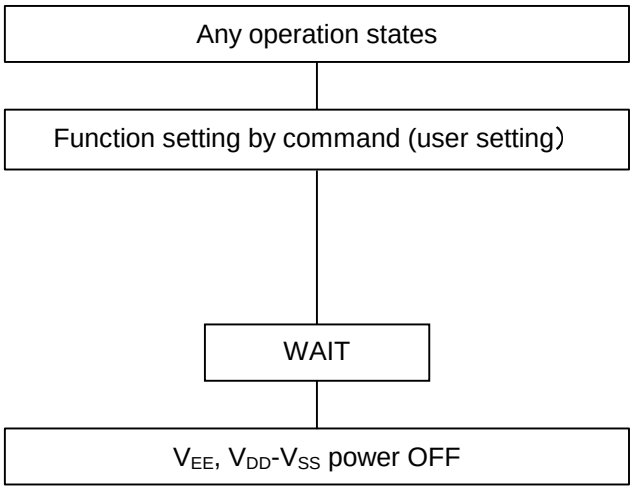


- display start line set
- increment mode set
- X address set
- Y address set

- display data write

- display ON/OFF command set(ON/OFF="1")

(32-3) POWER OFF



- HALT command set or reset operation (all LCD driver output is V_{SS} level)
- Discharge command set (discharge of V_{LCD}, V_1~V_4 capacitor)

Before turning off the power, be sure to execute HALT or RESET command to make LCD driver output OFF state.

And if V_{DD} and V_{EE} have different potential (V_{DD} and V_{EE} are not common), be sure to turn off V_{EE} first during V_{DD} is supplied.

(33) INSTRUCTION

INSTRUCTION TABLE (1)

INSTRUCTION	CODE (80 series I/F)							CODE								FUNCTION
	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
display data write in	0	0	1	0	0/1	0/1	0/1	Write Data								Write in to display RAM
display data read out.	0	0	0	1	0/1	0/1	0/1	Read Data								Read out from display RAM
X address (lower) [0_H]	0	1	1	0	0	0	0	0	0	0	0	AX_3	AX_2	AX_1	AX_0	Display RAM X direction set
X address (upper) [1_H]	0	1	1	0	0	0	0	0	0	0	1	*	AX_6	AX_5	AX_4	Display RAM X direction set
Y address (lower) [2_H]	0	1	1	0	0	0	0	0	0	1	0	AY_3	AY_2	AY_1	AY_0	Display RAM Y direction set
Y address (upper) [3_H]	0	1	1	0	0	0	0	0	0	1	1	*	AY_6	AY_5	AY_4	Display RAM Y direction set
display start line set (lower) [4_H]	0	1	1	0	0	0	0	0	1	0	0	LA_3	LA_2	LA_1	LA_0	RAM Y address setting corresponds to scan start line of common driver.
display start line set (upper) [5_H]	0	1	1	0	0	0	0	0	1	0	1	*	LA_6	LA_5	LA_4	RAM Y address setting corresponds to scan start line of common driver.
N line inversion set (lower) [6_H]	0	1	1	0	0	0	0	0	1	1	0	N_3	N_2	N_1	N_0	quantity setting of line inversion
N line inversion set (upper) [7_H]	0	1	1	0	0	0	0	0	1	1	1	*	N_6	N_5	N_4	quantity setting of line inversion
display control (1) [8_H]	0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALLON	ON/OFF	SHIFT: common shift direction set, MON: BW/gradation display, ALLON: all on , ON/OFF: display ON/OFF control
display control (2) [9_H]	0	1	1	0	0	0	0	1	0	0	1	REV	NLIN	SWAP	REF	REV: display positive / negative, NLIN: n line inversion ON/OFF, SWAP: display data swap, REF: segment positive / negative
increment control [A_H]	0	1	1	0	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI	WIN: window selection, AIM: increment timing selection, AYI:Y increment, AXI:X increment
power control [B_H]	0	1	1	0	0	0	0	1	0	1	1	AMPON	HALT	DCON	ACL	AMPON: internal OP Amp. ON, HALT: power save DCON: boosting circuit ON, ACL: reset
LCD duty set [C_H]	0	1	1	0	0	0	0	1	1	0	0	*	DS_2	DS_1	DS_0	LCD driver duty ratio set
boosting coefficient set [D_H]	0	1	1	0	0	0	0	1	1	0	1	*	VU_2	VU_1	VU_0	Boosting times set
bias ratio set [E_H]	0	1	1	0	0	0	0	1	1	1	0	*	B_2	B_1	B_0	LCD drive bias set
RE register set [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set

*Notice 1) * mark is Don't Care*
Notice 2) [ ] The inner side number is an address for internal register read.
Notice 3) The commands that upper/lower register settings are demanded are effective at the point of commands input. But electric volume is effective after upper and lower register setting.

INSTRUCTION TABLE (2)

INSTRUCTION	CODE (80 series I/F)							CODE								FUNCTION
	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette A_0 set (lower) [0_H]	0	1	1	0	0	0	1	0	0	0	0	PA_{03}	PA_{02}	PA_{01}	PA_{00}	Set value to gradation palette A_0
Gradation palette A_0 set (upper) [1_H]	0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA_{04}	Set value to gradation palette A_0
Gradation palette A_1 set (lower) [2_H]	0	1	1	0	0	0	1	0	0	1	0	PA_{13}	PA_{12}	PA_{11}	PA_{10}	Set value to gradation palette A_1
Gradation palette A_1 set (upper) [3_H]	0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA_{14}	Set value to gradation palette A_1
Gradation palette A_2 set (lower) [4_H]	0	1	1	0	0	0	1	0	1	0	0	PA_{23}	PA_{22}	PA_{21}	PA_{20}	Set value to gradation palette A_2
Gradation palette A_2 set (upper) [5_H]	0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA_{24}	Set value to gradation palette A_2
Gradation palette A_3 set (lower) [6_H]	0	1	1	0	0	0	1	0	1	1	0	PA_{33}	PA_{32}	PA_{31}	PA_{30}	Set value to gradation palette A_3
Gradation palette A_3 set (upper) [7_H]	0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA_{34}	Set value to gradation palette A_3
Gradation palette A_4 set (lower) [8_H]	0	1	1	0	0	0	1	1	0	0	0	PA_{43}	PA_{42}	PA_{41}	PA_{40}	Set value to gradation palette A_4
Gradation palette A_4 set (upper) [9_H]	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PA_{44}	Set value to gradation palette A_4
Gradation palette A_5 set (lower) [A_H]	0	1	1	0	0	0	1	1	0	1	0	PA_{53}	PA_{52}	PA_{51}	PA_{50}	Set value to gradation palette A_5
Gradation palette A_5 set (upper) [B_H]	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PA_{54}	Set value to gradation palette A_5
Gradation palette A_6 set (lower) [C_H]	0	1	1	0	0	0	1	1	1	0	0	PA_{63}	PA_{62}	PA_{61}	PA_{60}	Set value to gradation palette A_6
Gradation palette A_6 set (upper) [D_H]	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PA_{64}	Set value to gradation palette A_6
RE register set [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set

*Notice 1) * mark is Don't Care*
Notice 2) [ ] The inner side number is an address for internal register read.
Notice 3) The commands that upper/lower register settings are demanded are effective at the point of commands input. But electric volume is effective after upper and lower register setting.

INSTRUCTION TABLE (3)

INSTRUCTION	CODE (80 series I/F)							CODE								FUNCTION
	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette A_7 set (lower) [0_H]	0	1	1	0	0	1	0	0	0	0	0	PA_{73}	PA_{72}	PA_{71}	PA_{70}	Set value to gradation palette A_7
Gradation palette A_7 set (upper) [1_H]	0	1	1	0	0	1	0	0	0	0	1	*	*	*	PA_{74}	Set value to gradation palette A_7
Gradation palette B_0 set (lower) [2_H]	0	1	1	0	0	1	0	0	0	1	0	PB_{03}	PB_{02}	PB_{01}	PB_{00}	Set value to gradation palette B_0
Gradation palette B_0 set (upper) [3_H]	0	1	1	0	0	1	0	0	0	1	1	*	*	*	PB_{04}	Set value to gradation palette B_0
Gradation palette B_1 set (lower) [4_H]	0	1	1	0	0	1	0	0	1	0	0	PB_{13}	PB_{12}	PB_{11}	PB_{10}	Set value to gradation palette B_1
Gradation palette B_1 set (upper) [5_H]	0	1	1	0	0	1	0	0	1	0	1	*	*	*	PB_{14}	Set value to gradation palette B_1
Gradation palette B_2 set (lower) [6_H]	0	1	1	0	0	1	0	0	1	1	0	PB_{23}	PB_{22}	PB_{21}	PB_{20}	Set value to gradation palette B_2
Gradation palette B_2 set (upper) [7_H]	0	1	1	0	0	1	0	0	1	1	1	*	*	*	PB_{24}	Set value to gradation palette B_2
Gradation palette B_3 set (lower) [8_H]	0	1	1	0	0	1	0	1	0	0	0	PB_{33}	PB_{32}	PB_{31}	PB_{30}	Set value to gradation palette B_3
Gradation palette B_3 set (upper) [9_H]	0	1	1	0	0	1	0	1	0	0	1	*	*	*	PB_{34}	Set value to gradation palette B_3
Gradation palette B_4 set (lower) [A_H]	0	1	1	0	0	1	0	1	0	1	0	PB_{43}	PB_{42}	PB_{41}	PB_{40}	Set value to gradation palette B_4
Gradation palette B_4 set (upper) [B_H]	0	1	1	0	0	1	0	1	0	1	1	*	*	*	PB_{44}	Set value to gradation palette B_4
Gradation palette B_5 set (lower) [C_H]	0	1	1	0	0	1	0	1	1	0	0	PB_{53}	PB_{52}	PB_{51}	PB_{50}	Set value to gradation palette B_5
Gradation palette B_5 set (upper) [D_H]	0	1	1	0	0	1	0	1	1	0	1	*	*	*	PB_{54}	Set value to gradation palette B_5
RE register set [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set

*Notice 1) * mark is Don't Care*
Notice 2) [ ] The inner side number is an address for internal register read.
Notice 3) The commands that upper/lower register settings are demanded are effective at the point of commands input. But electric volume is effective after upper and lower register setting.

INSTRUCTION TABLE (4)

INSTRUCTION	CODE (80 series I/F)							CODE								FUNCTION
	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette B_6 set (lower) [0_H]	0	1	1	0	0	1	1	0	0	0	0	PB_{63}	PB_{62}	PB_{61}	PB_{60}	Set value to gradation palette B_6
Gradation palette B_6 set (upper) [1_H]	0	1	1	0	0	1	1	0	0	0	1	*	*	*	PB_{64}	Set value to gradation palette B_6
Gradation palette B_7 set (lower) [2_H]	0	1	1	0	0	1	1	0	0	1	0	PB_{73}	PB_{72}	PB_{71}	PB_{70}	Set value to gradation palette B_7
Gradation palette B_7 set (upper) [3_H]	0	1	1	0	0	1	1	0	0	1	1	*	*	*	PB_{74}	Set value to gradation palette B_7
Gradation palette C_0 set (lower) [4_H]	0	1	1	0	0	1	1	0	1	0	0	PC_{03}	PC_{02}	PC_{01}	PC_{00}	Set value to gradation palette C_0
Gradation palette C_0 set (upper) [5_H]	0	1	1	0	0	1	1	0	1	0	1	*	*	*	PC_{04}	Set value to gradation palette C_0
Gradation palette C_1 set (lower) [6_H]	0	1	1	0	0	1	1	0	1	1	0	PC_{13}	PC_{12}	PC_{11}	PC_{10}	Set value to gradation palette C_1
Gradation palette C_1 set (upper) [7_H]	0	1	1	0	0	1	1	0	1	1	1	*	*	*	PC_{14}	Set value to gradation palette C_1
Gradation palette C_2 set (lower) [8_H]	0	1	1	0	0	1	1	1	0	0	0	PC_{23}	PC_{22}	PC_{21}	PC_{20}	Set value to gradation palette C_2
Gradation palette C_2 set (upper) [9_H]	0	1	1	0	0	1	1	1	0	0	1	*	*	*	PC_{24}	Set value to gradation palette C_2
Gradation palette C_3 set (lower) [A_H]	0	1	1	0	0	1	1	1	0	1	0	PC_{33}	PC_{32}	PC_{31}	PC_{30}	Set value to gradation palette C_3
Gradation palette C_3 set (upper) [B_H]	0	1	1	0	0	1	1	1	0	1	1	*	*	*	PC_{34}	Set value to gradation palette C_3
Gradation palette C_4 set (lower) [C_H]	0	1	1	0	0	1	1	1	1	0	0	PC_{43}	PC_{42}	PC_{41}	PC_{40}	Set value to gradation palette C_4
Gradation palette C_4 set (upper) [D_H]	0	1	1	0	0	1	1	1	1	0	1	*	*	*	PC_{44}	Set value to gradation palette C_4
RE register set [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set

*Notice 1) * mark is Don't Care*
Notice 2) [ ] The inner side number is an address for internal register read.
Notice 3) The commands that upper/lower register settings are demanded are effective at the point of commands input. But electric volume is effective after upper and lower register setting.

INSTRUCTION TABLE (5)

INSTRUCTION	CODE (80 series I/F)							CODE								FUNCTION
	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_{3_z}	D_2	D_1	D_0	
Gradation palette C_5 set (lower) [0_H]	0	1	1	0	1	0	0	0	0	0	0	PC_{53}	PC_{52}	PC_{51}	PC_{50}	Set value to gradation palette C_5
Gradation palette C_5 set (upper) [1_H]	0	1	1	0	1	0	0	0	0	0	1	*	*	*	PC_{54}	Set value to gradation palette C_5
Gradation palette C_6 set (lower) [2_H]	0	1	1	0	1	0	0	0	0	1	0	PC_{63}	PC_{62}	PC_{61}	PC_{60}	Set value to gradation palette C_6
Gradation palette C_6 set (upper) [3_H]	0	1	1	0	1	0	0	0	0	1	1	*	*	*	PC_{64}	Set value to gradation palette C_6
Gradation palette C_7 set (lower) [4_H]	0	1	1	0	1	0	0	0	1	0	0	PC_{73}	PC_{72}	PC_{71}	PC_{70}	Set value to gradation palette C_7
Gradation palette C_7 set (upper) [5_H]	0	1	1	0	1	0	0	0	1	0	1	*	*	*	PC_{74}	Set value to gradation palette C_7
Display start command set [6_H]	0	1	1	0	1	0	0	0	1	1	0	*	SC_2	SC_1	SC_0	Common drive scan start line set
Serial extension CS control [7_H]	0	1	1	0	1	0	0	0	1	1	1	*	*	*	EXCS	Serial I/F, extension CS port (EXCS) control
Display selection control [8_H]	0	1	1	0	1	0	0	1	0	0	0	PWM	GLSB	*	*	Gradation display set
RAM data length set [9_H]	0	1	1	0	1	0	0	1	0	0	1	*	*	CKS	WLS	RAM access data length set 8 bit/16 bit selection
Electric volume control (lower) [A_H]	0	1	1	0	1	0	0	1	0	1	0	DV_3	DV_2	DV_1	DV_0	Electric volume level set (lower bit)
Electric volume control (upper) [B_H]	0	1	1	0	1	0	0	1	0	1	1	*	DV_6	DV_5	DV_4	Electric volume level set (upper bit)
Oscillator Rf control [D_H]	0	1	1	0	1	0	0	1	1	0	1	FFL	RF_2	RF_1	RF_0	RF: oscillator feed back resistor set FFL: oscillator frequency control
discharge [E_H]	0	1	1	0	1	0	0	1	1	1	0	*	*	*	DIS	V_{LCD}, V_1~V_4 capacitor discharge
RE register set [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set
Internal register read address set [C_H]	0	1	1	0	1	0	0	1	1	0	0	Register read address				Internal register read out address set
Internal register read	0	1	0	1	0/1	0/1	0/1	*	*	*	*	Read Data				Internal register read out

*Notice 1) * mark is Don't Care*
Notice 2) [ ] The inner side number is an address for internal register read.
Notice 3) The commands that upper/lower register settings are demanded are effective at the point of commands input.
But electric volume is effective after upper and lower register setting.
Notice 4) CKS=0: internal oscillation mode
CKS=1: external oscillation mode
Default CSK=0

INSTRUCTION TABLE (6)

INSTRUCTION	CODE (80 series I/F)							CODE								FUNCTION
	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Window end X address(lower) [0_H]	0	1	1	0	1	0	1	0	0	0	0	EX_3	EX_2	EX_1	EX_0	Window mode X direction end address set
Window end X address(upper) [1_H]	0	1	1	0	1	0	1	0	0	0	1	*	EX_6	EX_5	EX_4	Window mode X direction end address set
Window end Y address(lower) [2_H]	0	1	1	0	1	0	1	0	0	1	0	EY_3	EY_2	EY_1	EY_0	Window mode Y direction end address set
Window end Y address(upper) [3_H]	0	1	1	0	1	0	1	0	0	1	1	*	EY_6	EY_5	EY_4	Window mode Y direction end address set
Line inversion start Address (lower) [4_H]	0	1	1	0	1	0	1	0	1	0	0	LS_3	LS_2	LS_1	LS_0	Line inversion start address set
Line inversion start address (upper) [5_H]	0	1	1	0	1	0	1	0	1	0	1	*	LS_6	LS_5	LS_4	Line inversion start address set
Line inversion end Address (lower) [6_H]	0	1	1	0	1	0	1	0	1	1	0	LE_3	LE_2	LE_1	LE_0	Line inversion end address set
Line inversion end Address (upper) [7_H]	0	1	1	0	1	0	1	0	1	1	1	*	LE_6	LE_5	LE_4	Line inversion end address set
Line inversion control [8_H]	0	1	1	0	1	0	1	1	0	0	0	*	*	BT	LREV	LREV,BT: line inversion display set
Dummy segment driver address set [9_H]	0	1	1	0	1	0	1	1	0	0	1	*	*	*	DMY	Dummy segment driver address selection
PWM mode control [A_H]	0	1	1	0	1	0	1	1	0	1	0	PWMS	PWMA	PWMB	PWMC	PWM mode selection
RE register set [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set

*Notice 1) * mark is Don't Care*
Notice 2) [ ] The inner side number is an address for internal register read.
Notice 3) The commands that upper/lower register settings are demanded are effective at the point of commands input.
But electric volume is effective after upper and lower register setting.

(34) INSTRUCTION DESCRIPTION

As shown in instruction table, HM17CM256 has abundant command set.

All the data code and command code are valid only when the chip select signal $\overline{CS}$ is at "0" state. The left side of the following command code and data table are the setting of 80 series CPU` interface. Do not use undefined command code.

(34-1) Write display data on RAM

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	0	1	0	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display RAM write data							

Writing the 8-bit display RAM data at specified X, Y address.

(34-2) Read display data from RAM

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	0	0	1	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display RAM read data							

Reading out the 8-bit display RAM data from specified X, Y address.
One Dummy read cycle is needed after X, Y address is set.

(34-3) X address register set

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	0	0	0	0	0	AX_3	AX_2	AX_1	AX_0

(reset :AX_3~AX_4=0_H, read address :0_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	0	0	0	0	1	*	AX_6	AX_5	AX_4

*(reset :AX_6~AX_4=0_H, read address :1_H) * : "Don't care"*

Setting the X direction address address set. The lower 4-bits are set first, and then upper 3-bits are set later. Please set from lower bit.

(34-4) Y address register set

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	0	0	0	1	0	AY_3	AY_2	AY_1	AY_0

(reset :AY_3~AY_0=0_H, read address :2_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	0	0	0	1	1	*	AY_6	AY_5	AY_4

*(reset :AY_6~AY_4=0_H, read address :3_H) * : "Don't care"*

Setting the Y address of display RAM. The lower 4-bits are set first, and then upper 3-bits are set later. Please set from lower bit.

00_H~51_H is valid range at Y address(AY_6~AY_0). Do not use 52_H~FF_H range. The Y address(AY_6~AY_0) of 50_H,51_H is used for ICON display data address.

(34-5) Display start line register set

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	LA_3	LA_2	LA_1	LA_0

(reset:LA_3~LA_0=0_H, read address:4_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	LA_6	LA_5	LA_4

*(reset:LA_6~LA_4=0_H, read address:5_H) * : "Don't care"*

Setting the line address of COM_0. The address stored at the start line register becomes display line at COM_0 line of LCD panel.

The display of LCD panel is done from line address value to the direction of increase.

LA_6	LA_5	LA_4	LA_3	LA_2	LA_1	LA_0	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
1	0	0	1	1	1	1	79

(34-6) n line inversion register set

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	N_3	N_2	N_1	N_0

(reset :N_3~N_0=0_H, read address :6_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	N_6	N_5	N_4

*(reset :N_6~N_4=0_H, read address :7_H) * : "Don't care"*

Setting line number to be inversed to register. Setting range is from 2 to 80. N line inversion register can be effective only when N line inversion command NLIN='1".

If NLIN="0", the polarity of LCD driving voltage is inverted by every other frame.

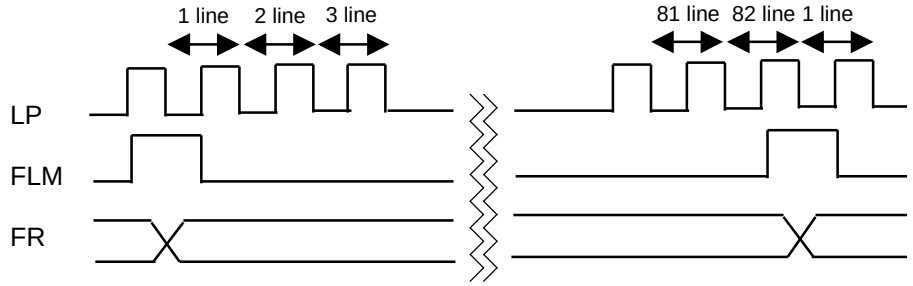
N_6	N_5	N_4	N_3	N_2	N_1	N_0	Inversion line number
0	0	0	0	0	0	0	Forbidden *
0	0	0	0	0	0	1	2
			:				:
1	0	0	1	1	1	1	80

n=N-1

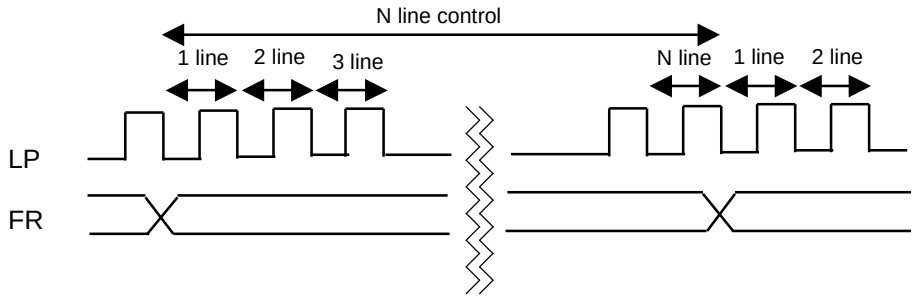
** : N_0~N_6 ="0" is forbidden.*

- Inversion timing

a) when n-line inversion function is OFF(1/82 duty display)



b) when n-line inversion function is ON



(34-7) display control (1) register set

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	SHIFT	MON	ALLON	ON/OFF

(reset :{SHIFT, MON, ALLON, ON/OFF}=0_H, read address : 8_H)

various control setting of display

a) ON/OFF command

Display ON/OFF control

ON/OFF=”0”: display OFF (all ports are V_{SS} level)

ON/OFF=”1”: display ON

b) ALLON command

Setting display data to “1” with independence of RAM data. This command has higher priority than positive display/negative display command. RAM data is not changed.

ALLON=”0”: normal display state

ALLON=”1”: turn on all the pixel

c) MON command

BW display / gradation display selection

MON=”0”: gradation display mode

MON=”1”: BW display mode

d) SHIFT command

Selection of the shift direction of scan data of common driver output

SHIFT=”0”:$COM_0 \rightarrow COM_{79}$ shift

SHIFT=”1”:$COM_{79} \rightarrow COM_0$ shift

(34-8) Display control (2) register set

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	REV	NLIN	SWAP	REF

(reset :{REV, NLIN, SWAP, REF}=0_H, read address :9_H)

various control setting of display

a) REF command

When CPU tries to access display RAM, the relation between X address and write data is changed by command, normal or headfirst.

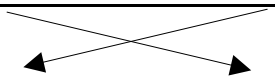
The output sequence of display data to segment driver can be controlled by register setting. The IC can be placed in panel with less constraint at application.

b) SWAP command

When CPU tries to access display RAM, the display data can be swapped.

SWAP="0": Normal state, D_7~D_0 or D_{15}~D_0 are written to the RAM.

SWAP="1": SWAP mode on : The swapped data of D_7~D_0 or D_{15}~D_0 are written to the RAM.

	SWAP="0"	SWAP="1"
Write data	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
		
Internal data	d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	d_0 d_1 d_2 d_3 d_4 d_5 d_6 d_7
		
Read data	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0

c) NLIN command

n line inversion ON/OFF control.

NLIN="0": n line inversion OFF. Polarity signal, FR is inverted every other frame.

NLIN="1": n line inversion ON. The n lines are inverted according to the contents of n line inversion register

d) REV command

The relation between RAM data and display data is defined by this command.

REV="0": The display data are reflected the RAM data until that time.

REV="1": The display data are reflected the opposite data from RAM data.

(34-9) Increment control register set

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	WIN	AIM	AYI	AXI

(reset :{WIN, AIM, AYI, AXI}=0_H, read address :A_H) * : "Don't care"

Sets the display RAM address to increment mode when RAM data is accessed.

Per RAM write or read access, the increment or non-increment settings of X and Y address counter are possible by AIM, AYI, AXI register setting. When accessing consecutive RAM areas by read or write, the address increment operation is possible without setting the read or write address by this register setting.

After setting the auto increment register, the X, Y address should be set lower bits first.

Please revise X, Y address register after increment register setting.

When WIN register is set to "1", the CPU accesses specified area of display RAM. In this case X, Y address should be used with auto increment mode set (AXI="1", AYI="1"). Do not revise X, Y address register when it is not auto increment mode.

WIN="0": normal display RAM access
WIN="1": window area access at display RAM

The window to be accessed is defined by setting the start X, Y address and end X, Y address.

When accessing display with window area mode, please set X, Y start address and then X, Y window end address.

When accessing consecutive RAM area, it is possible to access next location without setting the address by using this command. X, Y address is unknown after auto increment setting. When WIN register is set to "1", the RAM should be accessed after setting start point address and end point address.

And address setting should be done in sequence of start point of X address and Y address, and then end point of X address and Y address after WIN command setting (WIN="1").

The relationship between AIM, AYI, AXI register and X, Y address increment mode is as follow.

AIM	Increment timing selection	Remark
0	Both case of writing in and read out display RAM	①
1	Only when writing in display RAM(read modify)	②

notice①) This mode is valid when read or write is performed on consecutive RAM location.

notice②) This mode is valid when read out consecutive data and modifying the data and then write them in again or read → write per access.

AYI	AXI	Increment timing selection	Remark
0	0	No increment	①
0	1	X address auto increment	②
1	0	Y address auto increment	③
1	1	X, Y address auto increment	④

notice①) Regardless of AIM setting, no auto increment for X and Y address

notice②) According to AIM setting, auto increment only for X address.

And X address is increased as followed loop according to REF register(SEG output direction setting register) value.

∗) Please refer to 「RAM address bitmap」 in 「(10) relation between display RAM and address」

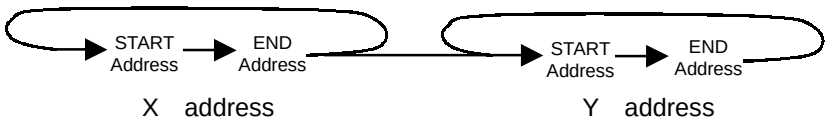
notice③) According to AIM setting, auto increment only for Y address

Y address is increased as followed loop regardless of REF register.

notice④) According to AIM setting, auto increment for X and Y address
X address is increased to Max_H first and then Y address is increased later.
You should set X address, Y address in sequence, anything else is forbidden.

*) Please refer to「RAM address bitmap」in「(10) relation between display RAM and address」

And when X, Y auto increment mode operating, window access is possible. When window mode is selected (WIN ="1"), address is increased as following loop.



a) 8 bit access mode
The increment operating is as above description.

b) 16 bit access mode
Two-byte access is done by single RAM access.
Address is increased after access.
X address is increased as (00_H, 01_H, ···· $3E_H$, $3F_H$) sequence.

(34-10) Power control register set

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	AMPON	HALT	DCON	ACL

(reset :{AMPON, HALT, DCON, ACL}=0_H, read address :B_H)

a) ACL command

This command initializes internal circuit and it is valid only at master operating.

ACL="0": normal state
ACL="1": initialization ON

Just after the execution of ACL command (ACL="1"), D_0 bit is set to 1. But as the initialization process goes on internally, D_0 is reset to "0".

When ACL command is executed, internal reset signal is produced by using local display clock (clock from internal oscillator or from external resistor oscillation mode).

So, after ACL command is executed, it needs to WAIT at least 2 period of the clock for next process beginning.

ACL command is effective only at master mode operation because it uses original oscillator clock.

It is prohibited for slave mode operation to use the internal oscillator or external oscillator.

So, ACL command is impossible at slave mode. Please reset the slave device at $\overline{RES}$ terminal, when needed.

b) DCON command

ON/OFF the internal voltage boosting circuit.

DCON="0": boosting circuit OFF
DCON="1": boosting circuit ON

c) HALT command

Power save mode ON/OFF control

HALT="0": normal state
HALT="1": power save state

The power consumption is decreased near static current at power save mode.

States of each sub-block in power save mode are as follow.

- Oscillator, built-in power supply block stop.
- Stop driving LCD panel, segment drive, the outputs of common driver are all set to V_{SS} level.
- Clock input from OSC_1 port is disabled.
- Display RAM data are conserved.
- Operational modes are preserved as those before power save command was executed.
- V_{LCD}, $V_1 \sim V_4$ become high impedance state.

Make display OFF state before power save mode by HALT command.

And when returning from power save mode, you should display ON after oscillator, power circuit is activated stably.

After display OFF and HALT command, if the display is turned ON before oscillator and power circuit is not activated stably, wrong display can be appeared.

d) AMPON command

ON/OFF the internal OP. amplifier circuit of power block (voltage regulator block, electric volume, voltage converting circuit).

AMPON="0": internal power circuit OP. Amplifier OFF
AMPON="1": internal power circuit OP. Amplifier ON

(34-11) LCD duty set

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	*	DS_2	DS_1	DS_0

*(reset :{DS_2, DS_1, DS_0}=0_H, read address :C_H) *:"Don't care"*

LCD display duty setting

DS_2	DS_1	DS_0	duty
0	0	0	Y direction 80 dot width display, 1/82 duty
0	0	1	Y direction 75 dot width display, 1/77 duty
0	1	0	Y direction 64 dot width display, 1/66 duty
0	1	1	Y direction 45 dot width display, 1/47 duty
1	0	0	Y direction 30 dot width display, 1/32 duty
1	0	1	Y direction 15 dot width display, 1/17 duty
1	1	0	Y direction 36 dot width display, 1/38 duty
1	1	1	Y direction 24 dot width display, 1/26 duty

Partial display is possible by setting duty operation.

(34-12) Boosting coefficient setting

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	VU_2	VU_1	VU_0

*(reset :{VU_2~VU_0}=0_H, read address :D_H) * : "Don't care"*

coefficient setting of boosting circuit

VU_2	VU_1	VU_0	Boosting multiple
0	0	0	No boosting *
0	0	1	2 times boosting operation
0	1	0	3 times boosting operation
0	1	1	4 times boosting operation
1	0	0	5 times boosting operation
1	0	1	6 times boosting operation
1	1	0	7 times boosting operation
1	1	1	forbidden

*V_{REG} amplifier gain is 1.

(34-13) Bias setting register

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	*	B_2	B_1	B_0

*(reset :{B_2~B_0}=0_H, read address : E_H) * : "Don't care"*

The bias ratio is selected by this register. 1/10, 1/9, 1/8, 1/7, 1/6, 1/5 biases can be selected by B_2, B_1 and B_0 register.

B_2	B_1	B_0	bias
0	0	0	Operating under 1/9 bias
0	0	1	Operating under 1/8 bias
0	1	0	Operating under 1/7 bias
0	1	1	Operating under 1/6 bias
1	0	0	Operating under 1/5 bias
1	0	1	Operating under 1/10 bias
1	1	0	forbidden
1	1	1	forbidden

(34-14) RE flag state register setting.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	1	TST_0	RE_2	RE_1	RE_0

(reset :{TST_0, RE_2, RE_1, RE_0}=0_H, read address :F_H)

Setting the register of command extension register(RE_2, RE_1, RE_0). When accessing command register, the extension register corresponding flag should be set first, and then access it. The TST_0 register is that for test, and so please set to "0".

(34-15) Gradation palette register setting

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	0	0	0	PA_{03}	PA_{02}	PA_{01}	PA_{00}

(read address :0_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA_{04}

*(read address :1_H) *:"Don't care"*
(reset :PA_{04}~PA_{00}="00000")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	0	1	0	PA_{13}	PA_{12}	PA_{11}	PA_{10}

(read address :2_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA_{14}

*(read address :3_H) * : "Don't care"*
(reset :PA_{14}~PA_{10}="00101")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	1	0	0	PA_{23}	PA_{22}	PA_{21}	PA_{20}

(read address :4_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA_{24}

*(read address:5_H) * : "Don't care"*
(reset :PA_{24}~PA_{20}="01010")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	1	1	0	PA_{33}	PA_{32}	PA_{31}	PA_{30}

(read address : 6_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA_{34}

*(read address : 7_H) * : "Don't care"*
(reset : PA_{34}~PA_{30}="01110")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	1	0	0	0	PA_{43}	PA_{42}	PA_{41}	PA_{40}

(read address :8_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PA_{44}

*(read address :9_H) * : "Don't care"*
(reset :PA_{44}~PA_{40}="10001")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PA_{53}	PA_{52}	PA_{51}	PA_{50}

(read address :A_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PA_{54}

*(read address :B_H) * : "Don't care"*
(reset :PA_{54}~PA_{50}="10101")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PA_{63}	PA_{62}	PA_{61}	PA_{60}

(read address :C_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PA_{64}

*(read address :D_H) * : "Don't care"*
(reset :PA_{64}~PA_{60}="11010")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PA_{73}	PA_{72}	PA_{71}	PA_{70}

(read address :0_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PA_{74}

*(read address :1_H) * : "Don't care"*
(reset :PA_{74}~PA_{70}="11111")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PB_{03}	PB_{02}	PB_{01}	PB_{00}

(read address :2_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PB_{04}

*(read address :3_H) * : "Don't care"*
(reset :PB_{04}~PB_{00}="00000")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PB_{13}	PB_{12}	PB_{11}	PB_{10}

(read address :4_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PB_{14}

*(read address :5_H) * : "Don't care"*
(reset :PB_{14}~PB_{10}="00101")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	PB_{23}	PB_{22}	PB_{21}	PB_{20}

(read address :6_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	PB_{24}

*(read address :7_H) * : "Don't care"*
(reset :PB_{24}~PB_{20}="01010")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PB_{33}	PB_{32}	PB_{31}	PB_{30}

(read address :8_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PB_{34}

*(read address :9_H) * : "Don't care"*
(reset :PB_{34}~PB_{30}="01110")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PB_{43}	PB_{42}	PB_{41}	PB_{40}

(read address :A_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PB_{44}

*(read address :B_H) * : "Don't care"*
(reset :PB_{44}~PB_{40}="10001")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PB_{53}	PB_{52}	PB_{51}	PB_{50}

(read address :C_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PB_{54}

*(read address :D_H) * : "Don't care"*
(reset :PB_{54}~PB_{50}="10101")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PB_{63}	PB_{62}	PB_{61}	PB_{60}

(read address :0_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PB_{64}

*(read address :1_H) * : "Don't care"*
(reset :PB_{64}~PB_{60}="11010")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PB_{73}	PB_{72}	PB_{71}	PB_{70}

(read address :2_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PB_{74}

*(read address :3_H) * : "Don't care"*
(reset :PB_{74}~PB_{70}="11111")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PC_{03}	PC_{02}	PC_{01}	PC_{00}

(read address :4_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PC_{04}

*(read address :5_H) * : "Don't care"*
(reset :PC_{04}~PC_{00}="00000")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	PC_{13}	PC_{12}	PC_{11}	PC_{10}

(read address :6_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	PC_{14}

*(read address :7_H) * : "Don't care"*
(reset :PC_{14}~PC_{10}="00101")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PC_{23}	PC_{22}	PC_{21}	PC_{20}

(read address :8_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PC_{24}

*(read address :9_H) * : "Don't care"*
(reset :PC_{24}~PC_{20}="01010")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PC_{33}	PC_{32}	PC_{31}	PC_{30}

(read address :A_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PC_{34}

*(read address :B_H) * : "Don't care"*
(reset :PC_{34}~PC_{30}="01110")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PC_{43}	PC_{42}	PC_{41}	PC_{40}

(read address :C_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PC_{44}

*(read address :D_H) * : "Don't care"*
(reset :PC_{44}~PC_{40}="10001")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PC_{53}	PC_{52}	PC_{51}	PC_{50}

(read address :0_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PC_{54}

*(read address :1_H) * : "Don't care"*
(reset :PC_{54}~PC_{50}="10101")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PC_{63}	PC_{62}	PC_{61}	PC_{60}

(read address :2_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PC_{64}

*(read address :3_H) * : "Don't care"*
(reset :PC_{64}~PC_{60}="11010")

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PC_{73}	PC_{72}	PC_{71}	PC_{70}

(read address :4_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PC_{74}

*(read address :5_H) * : "Don't care"*
(reset :PC_{74}~PC_{70}="11111")

Setting each gradation palette. The gradation level is selected among 32 level.

GRADATION LEVEL TABLE

(palette Aj, palette Bj, palette Cj (j=0~7) 3 kinds)

Palette value	Gradation level	Remarks	Palette value	Gradation level	remarks
0 0 0 0 0	0	Initial value of palette 0	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Initial value of palette 4
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31		1 0 0 1 1	19/31	
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Initial value of palette 1	1 0 1 0 1	21/31	Initial value of palette 5
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31		1 0 1 1 1	23/31	
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31	Initial value of palette 2	1 1 0 1 0	26/31	Initial value of palette 6
0 1 0 1 1	11/31		1 1 0 1 1	27/31	
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31	Initial value of palette 3	1 1 1 1 0	30/31	
0 1 1 1 1	15/31		1 1 1 1 1	31/31	Initial value of palette 7

(34-16) Display start command set

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	*	SC_2	SC_1	SC_0

*(reset :{SC_2, SC_1, SC_0}=0_H, read address :6_H) * : "Don't care"*

Setting the scan start output of common driver.

SC_2	SC_1	SC_0	SHIFT=0 starting point of COM.	SHIFT=1 starting point of COM.
0	0	0	COM_0~	COM_{79}~
0	0	1	COM_{15}~	COM_{64}~
0	1	0	COM_{30}~	COM_{49}~
0	1	1	COM_{45}~	COM_{34}~
1	0	0	COM_{60}~	COM_{19}~
1	0	1	COM_{75}~	COM_4~
1	1	0	forbidden	forbidden
1	1	1	forbidden	forbidden

SHIFT=0:COM increasing direction scanning
SHIFT=1:COM decreasing direction scanning

(34-17) Serial extension CS control

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	EXCS

*(reset :{EXCS}=1_H, read address :7_H) * : "Don't care"*

Controlling the output of extension CS at serial interface application.
EXCS pin is I/O pin and used as output at master mode device thus can be controlled.
EXCS="0":EXCS pin output is set to "L".
EXCS="1":EXCS pin output is set to "H".

(34-18) display selection control

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PWM	GLSB	*	*

*(reset :{PWM, GLSB}=0_H, read address :8_H) * : "Don't care"*

a) GLSB command
The segment driver outputs corresponding to 4 gradation display actually uses 3 bit data to select 4 gradation levels out of 8 gradation levels, 2 bit data out of RAM area and 1 bit out of Gradation LBS.
This command sets the supplement 1 bit Gradation LSB (GLSB) register.
GLSB="0": Set the LSB of segment driver corresponding to 4-gradataion display to "0".
GLSB="1": Set the LSB of segment driver corresponding to 4 gradataion display to "1".

b) PWM command
Selection gradation display mode.
PWM="0": Gradation mode is selected variable 8 gradation among 32 levels.
PWM="1": Fixed 8 gradation display mode.

(34-19) RAM data length setting

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	CKS	WLS

*(reset :{WLS}=0_H, read address :9_H) * : "Don't care"*

WLS: Selection 8 bit access or 16 bit access at RAM access. Access with 16 bits data length is effective only at RAM access. The other accesses are 8 bits access (command access).

WLS="0": RAM access is done by 8 bits data length.

WLS="1": RAM access is done by 16 bits data length

CKS: Selection the oscillator.

CKS="0": internal oscillation mode (default).

Internal oscillation mode should be used under condition of OSC_1 and OSC_2 open.

CKS="1": external oscillation mode.

External oscillation mode should be used under the condition of clock input by OSC_1 port or resistor connection between OSC_1 and OSC_2 port.

(34-20) Electric volume registers setting.

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	DV_3	DV_2	DV_1	DV_0

(read address :A_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	DV_6	DV_5	DV_4

*(read address :B_H) * : "Don't care"*

(reset :DV_6~DV_0=00_H)

Setting the electric volume code. The voltage range is divided into 127 levels by this register

DV_6	DV_5	DV_4	DV_3	DV_2	DV_1	DV_0	Output voltage
0	0	0	0	0	0	0	low
0	0	0	0	0	0	1	:
			:				:
1	1	1	1	1	1	0	:
1	1	1	1	1	1	1	high

The output voltage of V_{REG} is determined by Eq. ①.

$$V_{REG} = V_{REF} \times N \quad \cdots\cdots ①$$

(N: booster coefficient)

N=1 under the condition of boosting operation is not valid (booster coefficient register, VU=0_H).

The LCD driving voltage V_{LCD} is decided by V_{REG} level or electric volume value (Eq. ②).

$$V_{LCD} = 0.5 \times V_{REG} + M \times (V_{REG} - 0.5V_{REG}) / 127 \quad \cdots\cdots ②$$

(M : DV_6~DV_0 register value)

To prevent over voltage from being generated by electric volume setting, when the register value is set to upper side of electric volume, voltage level is not changed immediately.

When the register value is set to lower side of electric volume, the voltage level is changed instantly.

(34-21) Oscillator circuit Rf control

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	FFL	Rf_2	Rf_1	Rf_0

(reset : {FFL, Rf_2, Rf_1, Rf_0}=0_H, read address : D_H)

The feedback resistance of oscillator circuit can be changed by setting this register.

The frame frequency is changed according to the frequency of oscillator, and the oscillation frequency is determined by the resistor value.

When you set the frame rate, please check the state of LCD display.

Rf_2	Rf_1	Rf_0	Feedback resistance size
0	0	0	Reference value
0	0	1	0.8 x reference value
0	1	0	0.9 x reference value
0	1	1	1.1 x reference value
1	0	0	1.2 x reference value
1	0	1	forbidden
1	1	0	forbidden
1	1	1	forbidden

FFL command : Setting oscillator frequency (frame frequency f_{FLM}). (refer to DC characteristic)

FFL=0 : normal oscillator frequency (set frame frequency, f_{FLM} to 73Hz(Typ))

FFL=1 : high speed oscillator frequency (set frame frequency, f_{FLM} to 150Hz(Typ))

* The value of typical frame frequency f_{FLM}Typ is under following condition.

- Display mode : variable gradation display
- 1/82 Duty
- {Rf_2, Rf_1, Rf_0}=0_H

(34-22) Discharge control

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	*	*	*	DIS

*(reset : {DIS}=0_H, read address : E_H) * : "Don't care"*

The capacitors connected between V_{LCD}~V_4 and V_{SS} can be discharged by this control. Please refer to capacitor setting example.

DIS="0" : discharge stop

DIS="1" : start discharge

(34-23) Set read address of internal register

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	RA_3	RA_2	RA_1	RA_0

(reset :{RA_3, RA_2, RA_1, RA_0}=B_H)

Before executing the internal register data read command the address of register should be specified first. For example, when display control (1) is being read out, { RA_3, RA_2, RA_1, RA_0 } = 8_H should be specified first.

Because selected register is corresponded with RE flag, please set RE flag first and then read out the register.

Refer to the command function description and the lists of commands for the address of each register.

(34-24) Internal register data read

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
*	*	*	*	Internal register data read			

** : "Don't care"*

This command is used to read out internal register data. Before executing this command, RE flag and the address for internal register to read should be set first.

(34-25) Window end X address set

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	EX_3	EX_2	EX_1	EX_0

(reset :{EX_3~EX_0}=0_H, read address :0_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	EX_6	EX_5	EX_4

*(reset :{EX_6~EX_4}=0_H, read address :1_H) * : "Don't care"*

When the window area of RAM is specified(WIN="1") to access, the end X address of the window is set by this command. The lower 4 bits of address should be set first and then upper 3 bits are set later

(34-26) Window end Y address set

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	EY_3	EY_2	EY_1	EY_0

(reset :{EY_3~EY_0}=0_H, read address :2_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	EY_6	EY_5	EY_4

*(reset :{EY_6~EY_4}=0_H, read address :3_H) * : "Don't care"*

When window area of RAM is specified(WIN="1") to access , the end Y address of the window is set by this command. The lower 4 bits of address should be set first and then upper 3 bits are set later.

(34-27) Line inversion start address set

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	LS_3	LS_2	LS_1	LS_0

(reset :{LS_3~LS_0}=0_H, read address :4_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	LS_6	LS_5	LS_4

*(reset :{LS_6~LS_4}=0_H, read address :5_H) * : "Don't care"*

When the start address of negative display is set on, it is set by this command. The lower 4 bits of address should be set first and then upper 3 bits are set later. The possible range is LS=00_H~$4F_H$.
The other values are forbidden. Please set the value under the condition, LS≤LE.

(34-28) Line inversion end address set

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	LE_3	LE_2	LE_1	LE_0

(reset :{LE_3~LE_0}=0_H, read address :6_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	LE_6	LE_5	LE_4

*(reset :{LE_6~LE_4}=0_H, read address :7_H) * : "Don't care"*

When the end address of negative display is set on, it is set by this command. The lower 4 bits of address should be set first and then upper 3 bits are set later.
The possible range is LS=00_H~$4F_H$. The other values are forbidden. Please set the value under the condition, LS≤LE.

(34-29) Line inversion control

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	*	*	BT	LREV

*(reset :{PSC, BT, LREV}=0_H, read address :8_H) * : "Don't care"*

Setting the status of line inversion display tone.
LREV command : line inversion display ON/OFF setting.
LREV="0": normal display
LREV="1": line inversion display ON. The area specified by line inversion start/stop address is blinked.
The blink type display is controlled by BT command.

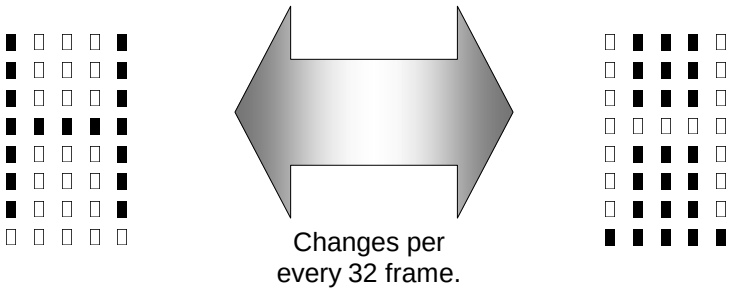
When line inversion display is ON(LREV="1"), line inversion start address(LSi) and line inversion stop address(LEi) should be set as following condition.

$$LSi \leq LEi \quad - (1)$$

And following condition is forbidden.

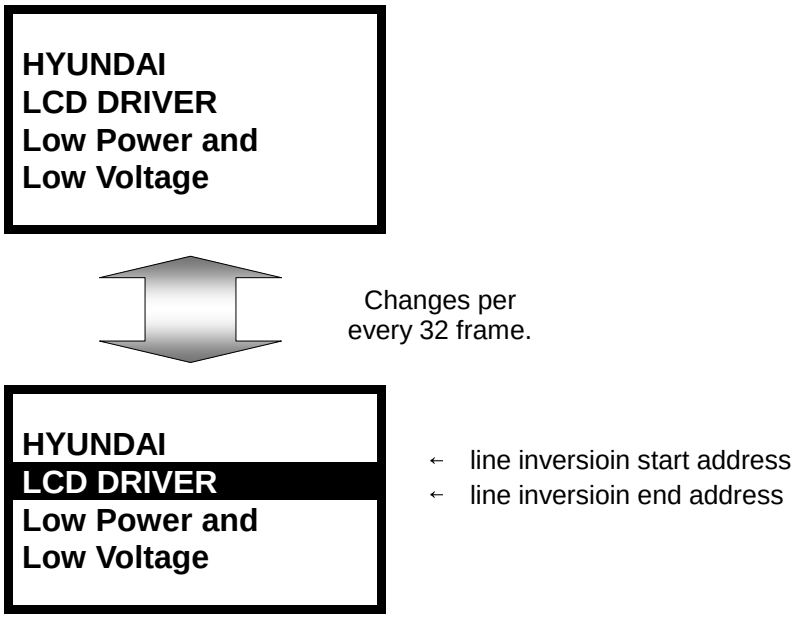
$$LEi < LSi \quad - (2)$$

BT command : inversion timing selection at line inversion display
BT="0": Negative tone display in specified area
BT="1": The image of specified area is blinked by every 32 frame.



Display example (BT="1")

And be cautious that LREV and BT commands have no influence on dummy segment driver circuit. And the image selected by $COMI_0$, $COMI_1$ is excluded.



Line inversion display example (LREV="1",BT="1")

(34-30) Dummy segment driver address selection (Refer to dummy segment drive related description.)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	DMY

*(reset :{DMY}=0_H, read address :8_H) * : "Don't care"*

When data is to be written to dummy segment driver, this register is active (DMY="1").
DMY="0": normal display RAM access
DMY="1": display data access to dummy segment driver

Normal segment drivers acquire display data from display RAM, but dummy segment drivers acquire display data from corresponding register not from display RAM. The capacity of register is 4 bytes. That is correspond to $SEGSA_0$~$SEGSA_3$、$SEGSB_0$~$SEGSB_3$、$SEGSC_0$~$SEGSC_3$ output.

When accessing with DMY = "1", address setting is valid by only X address. There is 4 byte capacity, and so 00_H, 01_H, 02_H, 03_H is valid at 8 bits mode and 00_H, 01_H is valid at 16 bits mode. There is no

relation with Y address setting value.
To access with DMY = “1”, register data write-in is possible with increment mode.

(34-31) PWM mode control

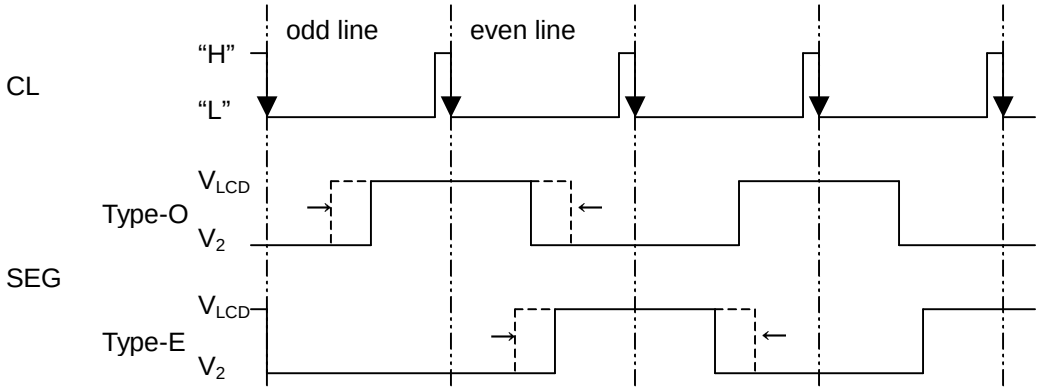
$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PWMS	PWMA	PWMB	PWMC

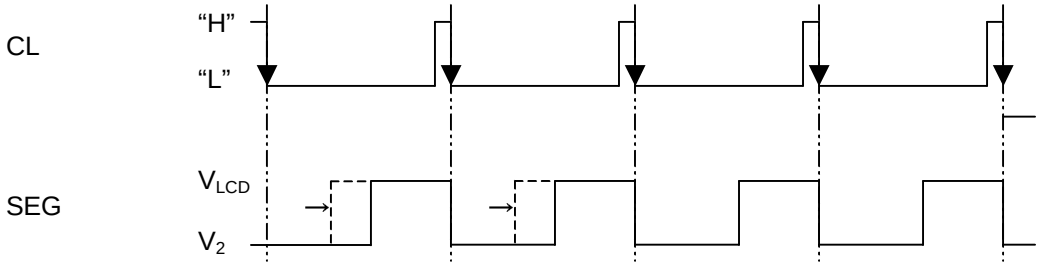
*(reset :{PWMS, PWMA, PWMB, PWMC}=0_H, read address :8_H) * : “Don’t care”*

PWM mode selection. (Refer to following wave diagram.)
PWMS=”0”: Selection PWM type1.
PWMA, PWMB, PWMC=”0” : PWM type1-O is selectable for each A, B, C data.
PWMA, PWMB, PWMC=”1” : PWM type1-E is selectable for each A, B, C data.
PWMS=”1”: Selection PWM type2.

a) PWM type1 (PWMS=”0”)



b) PWM type2 (PWMS=”1”)



(35) Relation between each setting and COM / display RAM

The COM port number corresponds to Y address of display RAM by SHIFT command, LCD duty command, common display start position command and display start line setting command.

- When display start address was set to “0”.

  According to LCD duty and display start common line address, the port of COM line and display RAM address (MY) is changed by 15 line unit.

  When SHIFT register is set to “0” common line shift to upward direction, and when the value is “1”, common line shift to downward direction. When display start address (LA_6~LA_0) is set to “0”, the “MY” corresponds to starting position is “0”. The MY shift upward direction as display goes on.

  In any case, $COMI_0$=MY80, $COMI_1$=MY81 .

- When display start line was set except for “0”

  According to LCD duty and display start common line address, the port of COM line and display RAM address, MY is changed by 15 line unit.

  When SHIFT register is set to “0” common line shift to upward direction, and when the value is “1”, common line shift to downward direction. When display start address (LA_6~LA_0) is set to except for “0”, the “MY” corresponds to starting position is shift by the amount of set value. The MY shift upward direction as display goes on but MY is set to “0” after MY=79.

  In any case, $COMI_0$=MY80, $COMI_1$=MY81 .

① display start line set to "0" , 1/82 duty by DS_2~DS_0 register

SHIFT set value			SHIFT="0" (common forward scan)						SHIFT="1" (common backward scan)					
DS_2	DS_1	DS_0	"000" (1/82 duty)						"000" (1/82 duty)					
SC_2	SC_1	SC_0	"000"	"001"	"010"	"011"	"100"	"101"	"000"	"001"	"010"	"011"	"100"	"101"
LA_6	·····	LA_0	"0000000" (display start point 0)						"0000000" (display start point 0)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	
COM_0	0	65	50	35	20	5	79	64	49	34	19	4	
COM_1													
COM_2													
COM_3													
COM_4												0	
COM_5												79	
COM_6													
COM_7													
COM_8													
COM_9													
COM_{10}													
COM_{11}													
COM_{12}													
COM_{13}													
COM_{14}		79											
COM_{15}		0											
COM_{16}													
COM_{17}													
COM_{18}													
COM_{19}											0		
COM_{20}											79		
COM_{21}													
COM_{22}													
COM_{23}													
COM_{24}													
COM_{25}													
COM_{26}													
COM_{27}													
COM_{28}													
COM_{29}			79										
COM_{30}			0										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}										0			
COM_{35}										79			
COM_{36}													
COM_{37}													
COM_{38}													
COM_{39}													
COM_{40}													
COM_{41}													
COM_{42}													
COM_{43}													
COM_{44}				79									
COM_{45}				0									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}									0				
COM_{50}									79				
COM_{51}													
COM_{52}													
COM_{53}													
COM_{54}													
COM_{55}													
COM_{56}													
COM_{57}													
COM_{58}													
COM_{59}					79								
COM_{60}					0								
COM_{61}													
COM_{62}													
COM_{63}													
COM_{64}								0					
COM_{65}								79					
COM_{66}													
COM_{67}													
COM_{68}													
COM_{69}													
COM_{70}													
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}						79							
COM_{75}						0							
COM_{76}													
COM_{77}													
COM_{78}													
COM_{79}	79	64	49	34	19	4	0	65	50	35	20	5	
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	

The number on the table means MY (Y direction shift address).
The COM electrodes without MY number are driving with non-selection level signal.
The ▭ Marked line is display start line.

② display start line set to “0” , 1/77 duty by DS_2~DS_0 register

SHIFT set value			SHIFT=“0” (common forward scan)						SHIFT=“1” (common backward scan)					
DS_2	DS_1	DS_0	“001” (1/77 duty)						“001” (1/77 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000000” (display start point 0)						“0000000” (display start point 0)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	0	65	50	35	20	5		64	49	34	19	4	
COM_1													
COM_2													
COM_3													
COM_4												0	
COM_5							74						
COM_6													
COM_7													
COM_8													
COM_9		74											
COM_{10}												74	
COM_{11}													
COM_{12}													
COM_{13}													
COM_{14}													
COM_{15}		0											
COM_{16}													
COM_{17}													
COM_{18}													
COM_{19}											0		
COM_{20}													
COM_{21}													
COM_{22}													
COM_{23}													
COM_{24}				74									
COM_{25}											74		
COM_{26}													
COM_{27}													
COM_{28}													
COM_{29}													
COM_{30}				0									
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}										0			
COM_{35}													
COM_{36}													
COM_{37}													
COM_{38}													
COM_{39}					74								
COM_{40}										74			
COM_{41}													
COM_{42}													
COM_{43}													
COM_{44}													
COM_{45}					0								
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											0		
COM_{50}													
COM_{51}													
COM_{52}													
COM_{53}													
COM_{54}						74							
COM_{55}											74		
COM_{56}													
COM_{57}													
COM_{58}													
COM_{59}													
COM_{60}						0							
COM_{61}													
COM_{62}													
COM_{63}													
COM_{64}								0					
COM_{65}													
COM_{66}													
COM_{67}													
COM_{68}													
COM_{69}						74							
COM_{70}								74					
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}	74												
COM_{75}						0							
COM_{76}													
COM_{77}													
COM_{78}													
COM_{79}		64	49	34	19	4	0	65	50	35	20	5	
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
The COM electrodes without MY number are driving with non-selection level signal.
The ▭ Marked line is display start line.

③ display start line set to “0” , 1/66 duty by DS_2~DS_0 register

SHIFT set value			SHIFT=”0” (common forward scan)						SHIFT=”1” (common backward scan)					
DS_2	DS_1	DS_0	“010” (1/66 duty)						“010” (1/66 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000000” (display start point 0)						“0000000” (display start point 0)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	0		50	35	20	5			49	34	19	4	
COM_1								63					
COM_2													
COM_3													
COM_4												0	
COM_5													
COM_6													
COM_7													
COM_8													
COM_9													
COM_{10}													
COM_{11}													
COM_{12}													
COM_{13}			63										
COM_{14}													
COM_{15}		0											
COM_{16}								63					
COM_{17}													
COM_{18}													
COM_{19}											0		
COM_{20}													
COM_{21}												63	
COM_{22}													
COM_{23}													
COM_{24}													
COM_{25}													
COM_{26}													
COM_{27}													
COM_{28}				63									
COM_{29}													
COM_{30}			0										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}											0		
COM_{35}													
COM_{36}												63	
COM_{37}													
COM_{38}													
COM_{39}													
COM_{40}													
COM_{41}													
COM_{42}													
COM_{43}					63								
COM_{44}													
COM_{45}				0									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											0		
COM_{50}													
COM_{51}												63	
COM_{52}													
COM_{53}													
COM_{54}													
COM_{55}													
COM_{56}													
COM_{57}													
COM_{58}							63						
COM_{59}													
COM_{60}						0							
COM_{61}													
COM_{62}													
COM_{63}	63												
COM_{64}										0			
COM_{65}													
COM_{66}											63		
COM_{67}													
COM_{68}													
COM_{69}													
COM_{70}													
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}													
COM_{75}							0						
COM_{76}													
COM_{77}													
COM_{78}		63											
COM_{79}			49	34	19	4	0		50	35	20	5	
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	

The number on the table means MY (Y direction shift address).
The COM electrodes without MY number are driving with non-selection level signal.
The ▭ Marked line is display start line.

④ display start line set to “0” , 1/47 duty by DS_2~DS_0 register

SHIFT set value			SHIFT=”0” (common forward scan)						SHIFT=”1” (common backward scan)					
DS_2	DS_1	DS_0	“011” (1/47 duty)						“011” (1/47 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000000” (display start point 0)						“0000000” (display start point 0)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	0			35	20	5					34	19	4
COM_1													
COM_2													
COM_3													
COM_4													0
COM_5											44		
COM_6													
COM_7													
COM_8													
COM_9				44									
COM_{10}													
COM_{11}													
COM_{12}													
COM_{13}													
COM_{14}													
COM_{15}		0											
COM_{16}													
COM_{17}													
COM_{18}													
COM_{19}												0	
COM_{20}										44			
COM_{21}													
COM_{22}													
COM_{23}													
COM_{24}					44								
COM_{25}													
COM_{26}													
COM_{27}													
COM_{28}													
COM_{29}													
COM_{30}			0										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}												0	
COM_{35}									44				
COM_{36}													
COM_{37}													
COM_{38}													
COM_{39}						44							
COM_{40}													44
COM_{41}													
COM_{42}													
COM_{43}													
COM_{44}	44												
COM_{45}				0									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											0		
COM_{50}													
COM_{51}													
COM_{52}													
COM_{53}													
COM_{54}													
COM_{55}												44	
COM_{56}													
COM_{57}													
COM_{58}													
COM_{59}		44											
COM_{60}						0							
COM_{61}													
COM_{62}													
COM_{63}													
COM_{64}										0			
COM_{65}													
COM_{66}													
COM_{67}													
COM_{68}													
COM_{69}													
COM_{70}												44	
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}			44										
COM_{75}							0						
COM_{76}													
COM_{77}													
COM_{78}													
COM_{79}				34	19	4	0				35	20	5
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
The COM electrodes without MY number are driving with non-selection level signal.
The ▭ Marked line is display start line.

⑤ display start line set to “0” , 1/32 duty by DS_2~DS_0 register

SHIFT set value			SHIFT=”0” (common forward scan)						SHIFT=”1” (common back scan)					
DS_2	DS_1	DS_0	“100” (1/32 duty)						“100” (1/32 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000000” (display start point 0)						“0000000” (display start point 0)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	0				20	5					19	4
COM_1												
COM_2												
COM_3												
COM_4												0
COM_5										29		
COM_6												
COM_7												
COM_8												
COM_9					29							
COM_{10}												
COM_{11}												
COM_{12}												
COM_{13}												
COM_{14}												
COM_{15}		0										
COM_{16}												
COM_{17}												
COM_{18}												
COM_{19}											0	
COM_{20}										29		
COM_{21}												
COM_{22}												
COM_{23}												
COM_{24}						29						
COM_{25}												
COM_{26}												
COM_{27}												
COM_{28}												
COM_{29}	29											
COM_{30}			0									
COM_{31}												
COM_{32}												
COM_{33}												
COM_{34}											0	
COM_{35}									29			
COM_{36}												
COM_{37}												
COM_{38}												
COM_{39}												
COM_{40}												
COM_{41}												
COM_{42}												
COM_{43}												
COM_{44}		29										
COM_{45}				0								
COM_{46}												
COM_{47}												
COM_{48}												
COM_{49}										0		
COM_{50}								29				
COM_{51}												
COM_{52}												
COM_{53}												
COM_{54}												
COM_{55}												29
COM_{56}												
COM_{57}												
COM_{58}												
COM_{59}			29									
COM_{60}					0							
COM_{61}												
COM_{62}												
COM_{63}												
COM_{64}									0			
COM_{65}												
COM_{66}												
COM_{67}												
COM_{68}												
COM_{69}												
COM_{70}											29	
COM_{71}												
COM_{72}												
COM_{73}												
COM_{74}				29								
COM_{75}						0						
COM_{76}												
COM_{77}												
COM_{78}												
COM_{79}					19	4	0				20	5
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
The COM electrodes without MY number are driving with non-selection level signal.
The ▭ Marked line is display start line.

⑥ display start line set to “0” , 1/17 duty by DS_2~DS_0 register

SHIFT set value			SHIFT=”0” (common forward scan)						SHIFT=”1” (common backward scan)					
DS_2	DS_1	DS_0	“101” (1/17 duty)						“101” (1/17 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000000” (display start point 0)						“0000000” (display start point 0)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	0					5							4
COM_1													
COM_2													
COM_3													
COM_4													0
COM_5												14	
COM_6													
COM_7													
COM_8													
COM_9						14							
COM_{10}													
COM_{11}													
COM_{12}													
COM_{13}													
COM_{14}	14												
COM_{15}		0											
COM_{16}													
COM_{17}													
COM_{18}													
COM_{19}												0	
COM_{20}												14	
COM_{21}													
COM_{22}													
COM_{23}													
COM_{24}													
COM_{25}													
COM_{26}													
COM_{27}													
COM_{28}													
COM_{29}		14											
COM_{30}			0										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}												0	
COM_{35}											14		
COM_{36}													
COM_{37}													
COM_{38}													
COM_{39}													
COM_{40}													
COM_{41}													
COM_{42}													
COM_{43}													
COM_{44}			14										
COM_{45}				0									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											0		
COM_{50}										14			
COM_{51}													
COM_{52}													
COM_{53}													
COM_{54}													
COM_{55}													
COM_{56}													
COM_{57}													
COM_{58}													
COM_{59}				14									
COM_{60}					0								
COM_{61}													
COM_{62}													
COM_{63}													
COM_{64}										0			
COM_{65}									14				
COM_{66}													
COM_{67}													
COM_{68}													
COM_{69}													
COM_{70}													14
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}					14								
COM_{75}						0							
COM_{76}													
COM_{77}													
COM_{78}													
COM_{79}						4	0						5
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
The COM electrodes without MY number are driving with non-selection level signal.
The ▭ Marked line is display start line.

⑦ display start line set to “0” , 1/38 duty by DS_2~DS_0 register

SHIFT set value			SHIFT=”0” (common forward scan)						SHIFT=”1” (common backward scan)					
DS_2	DS_1	DS_0	“110” (1/38 duty)						“110” (1/38 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000000” (display start point 0)						“0000000” (display start point 0)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	0			35	20	5				34	19	4	
COM_1													
COM_2													
COM_3													
COM_4												0	
COM_5													
COM_6													
COM_7													
COM_8													
COM_9													
COM_{10}													
COM_{11}													
COM_{12}													
COM_{13}													
COM_{14}											35		
COM_{15}		0			35								
COM_{16}													
COM_{17}													
COM_{18}													
COM_{19}												0	
COM_{20}													
COM_{21}													
COM_{22}													
COM_{23}													
COM_{24}													
COM_{25}													
COM_{26}													
COM_{27}													
COM_{28}													
COM_{29}										35			
COM_{30}			0			35							
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}												0	
COM_{35}	35												
COM_{36}													
COM_{37}													
COM_{38}													
COM_{39}													
COM_{40}													
COM_{41}													
COM_{42}													
COM_{43}													
COM_{44}									35				
COM_{45}				0									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											0		35
COM_{50}		35											
COM_{51}													
COM_{52}													
COM_{53}													
COM_{54}													
COM_{55}													
COM_{56}													
COM_{57}													
COM_{58}													
COM_{59}													
COM_{60}						0							
COM_{61}													
COM_{62}													
COM_{63}													
COM_{64}										0		35	
COM_{65}			35										
COM_{66}													
COM_{67}													
COM_{68}													
COM_{69}													
COM_{70}													
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}													
COM_{75}							0						
COM_{76}													
COM_{77}													
COM_{78}													
COM_{79}				34	19	4	0			35	20	5	
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
The COM electrodes without MY number are driving with non-selection level signal.
The ▭ Marked line is display start line.

⑧ display start line set to “0” , 1/26 duty by DS_2~DS_0 register

SHIFT set value			SHIFT=”0” (common forward scan)						SHIFT=”1” (common backward scan)					
DS_2	DS_1	DS_0	“111” (1/26 duty)						“111” (1/26 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000000” (display start point 0)						“0000000” (display start point 0)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	0				20	5						19	4
COM_1													
COM_2													
COM_3					23								
COM_4													0
COM_5													
COM_6													
COM_7													
COM_8													
COM_9													
COM_{10}													
COM_{11}												23	
COM_{12}													
COM_{13}													
COM_{14}													
COM_{15}		0											
COM_{16}													
COM_{17}													
COM_{18}						23							
COM_{19}												0	
COM_{20}													
COM_{21}													
COM_{22}													
COM_{23}	23												
COM_{24}													
COM_{25}													
COM_{26}											23		
COM_{27}													
COM_{28}													
COM_{29}													
COM_{30}			0										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}												0	
COM_{35}													
COM_{36}													
COM_{37}													
COM_{38}		23											
COM_{39}													
COM_{40}													
COM_{41}										23			
COM_{42}													
COM_{43}													
COM_{44}													
COM_{45}				0									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											0		
COM_{50}													
COM_{51}													
COM_{52}													
COM_{53}			23										
COM_{54}													
COM_{55}													
COM_{56}									23				
COM_{57}													
COM_{58}													
COM_{59}													
COM_{60}						0							
COM_{61}													23
COM_{62}													
COM_{63}													
COM_{64}										0			
COM_{65}													
COM_{66}													
COM_{67}													
COM_{68}				23									
COM_{69}													
COM_{70}													
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}													
COM_{75}							0						
COM_{76}												23	
COM_{77}													
COM_{78}													
COM_{79}						19	4		0			20	5
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
The COM electrodes without MY number are driving with non-selection level signal.
The ▭ Marked line is display start line.

⑨ display start line set to “5” , 1/82 duty by DS_2~DS_0 register

SHIFT set value			SHIFT=”0” (common forward scan)						SHIFT=”1” (common backward scan)					
DS_2	DS_1	DS_0	“000” (1/82 duty)						“000” (1/82 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000101” (display start point 5)						“0000101” (display start point 5)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	5	70	55	40	25	10	4	69	54	39	24	9		
COM_1														
COM_2														
COM_3														
COM_4							0					5		
COM_5							79							
COM_6														
COM_7														
COM_8														
COM_9		79										0		
COM_{10}		0										79		
COM_{11}														
COM_{12}														
COM_{13}														
COM_{14}														
COM_{15}		5												
COM_{16}														
COM_{17}														
COM_{18}														
COM_{19}											5			
COM_{20}														
COM_{21}														
COM_{22}														
COM_{23}														
COM_{24}			79								0			
COM_{25}			0								79			
COM_{26}														
COM_{27}														
COM_{28}														
COM_{29}														
COM_{30}			5											
COM_{31}														
COM_{32}														
COM_{33}														
COM_{34}										5				
COM_{35}														
COM_{36}														
COM_{37}														
COM_{38}														
COM_{39}				79						0				
COM_{40}				0						79				
COM_{41}														
COM_{42}														
COM_{43}														
COM_{44}														
COM_{45}				5										
COM_{46}														
COM_{47}														
COM_{48}														
COM_{49}											5			
COM_{50}														
COM_{51}														
COM_{52}														
COM_{53}														
COM_{54}						79					0			
COM_{55}						0					79			
COM_{56}														
COM_{57}														
COM_{58}														
COM_{59}														
COM_{60}						5								
COM_{61}														
COM_{62}														
COM_{63}														
COM_{64}										5				
COM_{65}														
COM_{66}														
COM_{67}														
COM_{68}														
COM_{69}							79			0				
COM_{70}							0			79				
COM_{71}														
COM_{72}														
COM_{73}														
COM_{74}	79													
COM_{75}	0						5							
COM_{76}														
COM_{77}														
COM_{78}														
COM_{79}	4	69	54	39	24	9	5	70	55	40	25	10		
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81		

The number on the table means MY (Y direction shift address).
The COM electrodes without MY number are driving with non-selection level signal.
The ▭ Marked line is display start line.

⑩ display start line set to “5” , 1/77 duty by DS_2~DS_0 register

SHIFT set value			SHIFT=”0” (common forward scan)						SHIFT=”1” (common backward scan)					
DS_2	DS_1	DS_0	“001” (1/77 duty)						“001” (1/77 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000101” (display start point 5)						“0000101” (display start point 5)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	5	70	55	40	25	10		69	54	39	24	9		
COM_1														
COM_2														
COM_3														
COM_4													5	
COM_5							79							
COM_6														
COM_7														
COM_8														
COM_9		79												
COM_{10}													79	
COM_{11}														
COM_{12}														
COM_{13}														
COM_{14}														
COM_{15}		5												
COM_{16}														
COM_{17}														
COM_{18}														
COM_{19}												5		
COM_{20}														
COM_{21}														
COM_{22}														
COM_{23}														
COM_{24}				79										
COM_{25}												79		
COM_{26}														
COM_{27}														
COM_{28}														
COM_{29}														
COM_{30}				5										
COM_{31}														
COM_{32}														
COM_{33}														
COM_{34}											5			
COM_{35}														
COM_{36}														
COM_{37}														
COM_{38}														
COM_{39}					79									
COM_{40}											79			
COM_{41}														
COM_{42}														
COM_{43}														
COM_{44}														
COM_{45}					5									
COM_{46}														
COM_{47}														
COM_{48}														
COM_{49}											5			
COM_{50}														
COM_{51}														
COM_{52}														
COM_{53}														
COM_{54}						79								
COM_{55}											79			
COM_{56}														
COM_{57}														
COM_{58}														
COM_{59}														
COM_{60}						5								
COM_{61}														
COM_{62}														
COM_{63}														
COM_{64}										5				
COM_{65}														
COM_{66}														
COM_{67}														
COM_{68}														
COM_{69}							79							
COM_{70}										79				
COM_{71}														
COM_{72}														
COM_{73}														
COM_{74}	79													
COM_{75}							5							
COM_{76}														
COM_{77}														
COM_{78}														
COM_{79}		69	54	39	24	9	5	70	55	40	25	10		
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
The COM electrodes without MY number are driving with non-selection level signal.
The ▭ Marked line is display start line.

⑪ display start line set to “5” , 1/66 duty by DS_2~DS_0 register

SHIFT set value			SHIFT=”0” (common forward scan)						SHIFT=”1” (common backward scan)					
DS_2	DS_1	DS_0	“010” (1/66 duty)						“010” (1/66 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000101” (display start point 5)						“0000101” (display start point 5)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	5		55	40	25	10					54	39	24	9
COM_1										68				
COM_2														
COM_3														
COM_4														5
COM_5														
COM_6														
COM_7														
COM_8														
COM_9														
COM_{10}														
COM_{11}														
COM_{12}														
COM_{13}			68											
COM_{14}														
COM_{15}		5												
COM_{16}									68					
COM_{17}														
COM_{18}														
COM_{19}													5	
COM_{20}														
COM_{21}														68
COM_{22}														
COM_{23}														
COM_{24}														
COM_{25}														
COM_{26}														
COM_{27}														
COM_{28}				68										
COM_{29}														
COM_{30}			5											
COM_{31}														
COM_{32}														
COM_{33}														
COM_{34}												5		
COM_{35}														
COM_{36}													68	
COM_{37}														
COM_{38}														
COM_{39}														
COM_{40}														
COM_{41}														
COM_{42}														
COM_{43}						68								
COM_{44}														
COM_{45}				5										
COM_{46}														
COM_{47}														
COM_{48}														
COM_{49}											5			
COM_{50}														
COM_{51}												68		
COM_{52}														
COM_{53}														
COM_{54}														
COM_{55}														
COM_{56}														
COM_{57}														
COM_{58}							68							
COM_{59}														
COM_{60}						5								
COM_{61}														
COM_{62}														
COM_{63}	68													
COM_{64}										5				
COM_{65}														
COM_{66}											68			
COM_{67}														
COM_{68}														
COM_{69}														
COM_{70}														
COM_{71}														
COM_{72}														
COM_{73}														
COM_{74}														
COM_{75}							5							
COM_{76}														
COM_{77}														
COM_{78}		68												
COM_{79}			54	39	24	9	5				55	40	25	10
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
The COM electrodes without MY number are driving with non-selection level signal.
The ▭ Marked line is display start line.

⑫ display start line set to “5” , 1/47 duty by DS_2~DS_0 register

SHIFT set value			SHIFT=”0” (common forward scan)						SHIFT=”1” (common backward scan)					
DS_2	DS_1	DS_0	“011” (1/47 duty)						“011” (1/47 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000101” (display start point 5)						“0000101” (display start point 5)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	5			40	25	10					39	24	9	
COM_1														
COM_2														
COM_3														
COM_4													5	
COM_5											49			
COM_6														
COM_7														
COM_8														
COM_9				49										
COM_{10}														
COM_{11}														
COM_{12}														
COM_{13}														
COM_{14}														
COM_{15}		5												
COM_{16}														
COM_{17}														
COM_{18}														
COM_{19}													5	
COM_{20}										49				
COM_{21}														
COM_{22}														
COM_{23}														
COM_{24}					49									
COM_{25}														
COM_{26}														
COM_{27}														
COM_{28}														
COM_{29}														
COM_{30}			5											
COM_{31}														
COM_{32}														
COM_{33}														
COM_{34}												5		
COM_{35}									49					
COM_{36}														
COM_{37}														
COM_{38}														
COM_{39}							49							
COM_{40}														49
COM_{41}														
COM_{42}														
COM_{43}														
COM_{44}	49													
COM_{45}				5										
COM_{46}														
COM_{47}														
COM_{48}														
COM_{49}											5			
COM_{50}														
COM_{51}														
COM_{52}														
COM_{53}														
COM_{54}														
COM_{55}													49	
COM_{56}														
COM_{57}														
COM_{58}														
COM_{59}		49												
COM_{60}						5								
COM_{61}														
COM_{62}														
COM_{63}														
COM_{64}										5				
COM_{65}														
COM_{66}														
COM_{67}														
COM_{68}														
COM_{69}														
COM_{70}												49		
COM_{71}														
COM_{72}														
COM_{73}														
COM_{74}			49											
COM_{75}							5							
COM_{76}														
COM_{77}														
COM_{78}														
COM_{79}				39	24	9		5				40	25	10
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
The COM electrodes without MY number are driving with non-selection level signal.
The ▭ Marked line is display start line.

⑬ display start line set to “5” , 1/32 duty by DS_2~DS_0 register

SHIFT set value			SHIFT=”0” (common forward scan)						SHIFT=”1” (common backward scan)					
DS_2	DS_1	DS_0	“100” (1/32 duty)						“100” (1/32 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000101” (display start point 5)						“0000101” (display start point 5)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	5				25	10						24	9
COM_1													
COM_2													
COM_3													
COM_4													5
COM_5												34	
COM_6													
COM_7													
COM_8													
COM_9					34								
COM_{10}													
COM_{11}													
COM_{12}													
COM_{13}													
COM_{14}													
COM_{15}		5											
COM_{16}													
COM_{17}													
COM_{18}													
COM_{19}												5	
COM_{20}											34		
COM_{21}													
COM_{22}													
COM_{23}													
COM_{24}						34							
COM_{25}													
COM_{26}													
COM_{27}													
COM_{28}													
COM_{29}	34												
COM_{30}			5										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}												5	
COM_{35}										34			
COM_{36}													
COM_{37}													
COM_{38}													
COM_{39}													
COM_{40}													
COM_{41}													
COM_{42}													
COM_{43}													
COM_{44}		34											
COM_{45}				5									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											5		
COM_{50}									34				
COM_{51}													
COM_{52}													
COM_{53}													
COM_{54}													
COM_{55}													34
COM_{56}													
COM_{57}													
COM_{58}													
COM_{59}			34										
COM_{60}						5							
COM_{61}													
COM_{62}													
COM_{63}													
COM_{64}										5			
COM_{65}													
COM_{66}													
COM_{67}													
COM_{68}													
COM_{69}													
COM_{70}													34
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}				34									
COM_{75}						5							
COM_{76}													
COM_{77}													
COM_{78}													
COM_{79}					24	9	5					25	10
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
The COM electrodes without MY number are driving with non-selection level signal.
The ▭ Marked line is display start line.

⑭ display start line set to “5” , 1/17 duty by DS_2~DS_0 register

SHIFT set value			SHIFT=”0” (common forward scan)						SHIFT=”1” (common backward scan)					
DS_2	DS_1	DS_0	“101” (1/17 duty)						“101” (1/17 duty)					
SC_2	SC1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000101” (display start point 5)						“0000101” (display start point 5)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	5					10							9
COM_1													
COM_2													
COM_3													
COM_4													5
COM_5												19	
COM_6													
COM_7													
COM_8													
COM_9						19							
COM_{10}													
COM_{11}													
COM_{12}													
COM_{13}													
COM_{14}	19												
COM_{15}		5											
COM_{16}													
COM_{17}													
COM_{18}													
COM_{19}												5	
COM_{20}												19	
COM_{21}													
COM_{22}													
COM_{23}													
COM_{24}													
COM_{25}													
COM_{26}													
COM_{27}													
COM_{28}													
COM_{29}		19											
COM_{30}			5										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}												5	
COM_{35}											19		
COM_{36}													
COM_{37}													
COM_{38}													
COM_{39}													
COM_{40}													
COM_{41}													
COM_{42}													
COM_{43}													
COM_{44}			19										
COM_{45}				5									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											5		
COM_{50}										19			
COM_{51}													
COM_{52}													
COM_{53}													
COM_{54}													
COM_{55}													
COM_{56}													
COM_{57}													
COM_{58}													
COM_{59}				19									
COM_{60}					5								
COM_{61}													
COM_{62}													
COM_{63}													
COM_{64}										5			
COM_{65}									19				
COM_{66}													
COM_{67}													
COM_{68}													
COM_{69}													
COM_{70}													19
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}					19								
COM_{75}						5							
COM_{76}													
COM_{77}													
COM_{78}													
COM_{79}						9		5					10
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
The COM electrodes without MY number are driving with non-selection level signal.
The ▭ Marked line is display start line.

⑮ display start line set to “5” , 1/38 duty by DS_2~DS_0 register

SHIFT set value			SHIFT=”0” (common forward scan)						SHIFT=”1” (common backward scan)					
DS_2	DS_1	DS_0	“110” (1/38 duty)						“110” (1/38 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000101” (display start point 5)						“0000101” (display start point 5)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	5			40	25	10				39	24	9	
COM_1													
COM_2													
COM_3													
COM_4												5	
COM_5													
COM_6													
COM_7													
COM_8													
COM_9													
COM_{10}													
COM_{11}													
COM_{12}													
COM_{13}													
COM_{14}											40		
COM_{15}		5			40								
COM_{16}													
COM_{17}													
COM_{18}													
COM_{19}												5	
COM_{20}													
COM_{21}													
COM_{22}													
COM_{23}													
COM_{24}													
COM_{25}													
COM_{26}													
COM_{27}													
COM_{28}													
COM_{29}										40			
COM_{30}			5			40							
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}												5	
COM_{35}	40												
COM_{36}													
COM_{37}													
COM_{38}													
COM_{39}													
COM_{40}													
COM_{41}													
COM_{42}													
COM_{43}													
COM_{44}									40				
COM_{45}				5									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											5		40
COM_{50}		40											
COM_{51}													
COM_{52}													
COM_{53}													
COM_{54}													
COM_{55}													
COM_{56}													
COM_{57}													
COM_{58}													
COM_{59}													
COM_{60}						5							
COM_{61}													
COM_{62}													
COM_{63}													
COM_{64}										5		40	
COM_{65}			40										
COM_{66}													
COM_{67}													
COM_{68}													
COM_{69}													
COM_{70}													
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}													
COM_{75}							5						
COM_{76}													
COM_{77}													
COM_{78}													
COM_{79}				39	24	9	5			40	25	10	
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
The COM electrodes without MY number are driving with non-selection level signal.
The ▭ Marked line is display start line.

⑯ display start line set to “5” , 1/26 duty by DS_2~DS_0 register

SHIFT set value			SHIFT=”0” (common forward scan)						SHIFT=”1” (common backward scan)					
DS_2	DS_1	DS_0	“111” (1/26 duty)						“111” (1/26 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000101” (display start point 5)						“0000101” (display start point 5)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	5				25	10					24	9	
COM_1													
COM_2													
COM_3					28								
COM_4												5	
COM_5													
COM_6													
COM_7													
COM_8													
COM_9													
COM_{10}													
COM_{11}											28		
COM_{12}													
COM_{13}													
COM_{14}													
COM_{15}		5											
COM_{16}													
COM_{17}													
COM_{18}						28							
COM_{19}											5		
COM_{20}													
COM_{21}													
COM_{22}													
COM_{23}	28												
COM_{24}													
COM_{25}													
COM_{26}											28		
COM_{27}													
COM_{28}													
COM_{29}													
COM_{30}			5										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}											5		
COM_{35}													
COM_{36}													
COM_{37}													
COM_{38}		28											
COM_{39}													
COM_{40}													
COM_{41}										28			
COM_{42}													
COM_{43}													
COM_{44}													
COM_{45}				5									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											5		
COM_{50}													
COM_{51}													
COM_{52}													
COM_{53}			28										
COM_{54}													
COM_{55}													
COM_{56}									28				
COM_{57}													
COM_{58}													
COM_{59}													
COM_{60}					5								
COM_{61}													28
COM_{62}													
COM_{63}													
COM_{64}										5			
COM_{65}													
COM_{66}													
COM_{67}													
COM_{68}				28									
COM_{69}													
COM_{70}													
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}													
COM_{75}						5							
COM_{76}												28	
COM_{77}													
COM_{78}													
COM_{79}					24	9	5				25	10	
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	

The number on the table means MY (Y direction shift address).
The COM electrodes without MY number are driving with non-selection level signal.
The ▭ Marked line is display start line.

■ ABSOLUTE MAXIMUM RATING

ITEM	SYMBOL	CONDITION	PORT	RATINGS	UNIT
supply voltage (1)	V_{DD}	V_{SS}(0V) reference Ta = +25°C	V_{DD}	-0.3 ~ +4.0	V
supply voltage (2)	V_{EE}		V_{EE}	-0.3 ~ +4.0	V
supply voltage (3)	V_{OUT}		V_{OUT}	-0.3 ~ +20.0	V
supply voltage (4)	V_{REG}		V_{REG}	-0.3 ~ +20.0	V
supply voltage (5)	V_{LCD}		V_{LCD}	-0.3 ~ +20.0	V
supply voltage (6)	V_1, V_2, V_3, V_4		V_1, V_2, V_3, V_4	-0.3 ~ V_{LCD} + 0.3	V
input voltage	V_I		*1	-0.3 ~ V_{DD} + 0.3	V
Storage temperature	T_{stg}			-45 ~ +125	°C

*1 D_0~D_{15}, $\overline{CS}$, RS, M/S, $\overline{RD}$, $\overline{WR}$, OSC_1, LP, FLM, FR, CLK, $\overline{RES}$, TEST port

■ RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	PORT	MIN	TYP	MAX	UNIT	REMARK
supply voltage	V_{DD1}	V_{DD}	1.7		3.3	V	*1
	V_{DD2}		2.4		3.3	V	*2
	V_{EE}	V_{EE}	2.4		3.3	V	*3
Recommended operating voltage	V_{LCD}	V_{LCD}	5		18.0	V	*4
	V_{OUT}	V_{OUT}			18.0	V	
	V_{REG}	V_{REG}			V_{OUT} x 0.9	V	
	V_{REF}	V_{REF}	2.1		3.3	V	*5
Operation temperature	T_{opr}		-30		85	°C	

*1 The case when internal reference voltage generation circuit (V_{BA} output) is not used.
The voltage compare to V_{SS} port.

*2 The case when internal reference voltage generation circuit (V_{BA} output) is used.
The voltage compare to V_{SS} port.

*3 When the boosting circuit is used, supply voltage V_{EE} should be used within the limit.
When driving LCD panel by use of internal boosting circuit, it is possible to short V_{DD} and V_{EE}.

*4 Please keep the relation, $V_{SS} < V_4 < V_3 < V_2 < V_1 < V_{LCD} \leq V_{OUT}$.

*5 When the internal voltage regulator circuit is used, reference voltage V_{REF} should be used within the limit.
Please keep the relation $V_{REF} \leq V_{EE}$.

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics 1

Unless otherwise noted V_{SS} = 0V, V_{DD} = +1.7~+3.3V, Ta = -30~+85°C

ITEM	SYMBOL	CONDITION		MIN	TYP	MAX	UNIT	PORT
High level input voltage	V_{IH}			0.8 V_{DD}		V_{DD}	V	*1
Low level input voltage	V_{IL}			0		0.22 V_{DD}	V	*1
High level output voltage	V_{OH1}	I_{OH} = -0.4mA		V_{DD} - 0.4			V	*2
Low level output voltage	V_{OL1}	I_{OL} = 0.4mA				0.4	V	*2
High level output voltage	V_{OH2}	I_{OH} = -0.1mA		V_{DD} - 0.4			V	*3
Low level output voltage	V_{OL2}	I_{OL} = 0.1mA				0.4	V	*3
Input leakage current	IL_I	V_I = V_{SS} or V_{DD}		-10		10	µA	*4
Output leakage current	IL_O	V_I = V_{SS} or V_{DD}		-10		10	µA	*5
LCD driver output ON resistance	R_{ON1}	$\|\Delta V_{ON}\|$ = 0.5V	V_{LCD} = 10V		1	2	kΩ	*6
			V_{LCD} = 6V		2	4		
Static current	I_{STB}	$\overline{CS}$=V_{DD}, Ta=25°C	V_{DD} = 3V			15	µA	*7
Oscillator frequency	f_{OSC1}	V_{DD} = 3V Ta = 25°C	FFL = "0" (normal mode)	TBD	372	TBD	kHz	*8
	f_{OSC2}				84			*9
	f_{OSC3}				12			*10
	f_{OSC4}		FFL = "1" (high speed mode)	TBD	762.6	TBD		*8
	f_{OSC5}				172.2			*9
	f_{OSC6}				24.6			*10
oscillator frequency by External resistor	fr_1	Rf=6.2kΩ		TBD	775.2	TBD	kHz	
	fr_2	Rf=20kΩ			373.9			
	fr_3	Rf=51kΩ			167.8			
	fr_4	Rf=110kΩ			84.3			
	fr_5	Rf=390kΩ			25.8			
	fr_6	Rf=820kΩ			12.6			
Boosting output voltage	V_{OUT}	N x boosting (N=2~7) RL = 30kΩ (between V_{OUT} ,V_{SS})		N * V_{EE} * 0.95			V	*11
Current consumption (1)	I_{DD1}	V_{DD} = 2.5V 7 x boosting (all ON)	FFL = "0"		TBD	TBD	µA	*12
Current consumption (2)	I_{DD2}		FFL = "1"		TBD	TBD		
Current consumption (3)	I_{DD3}	V_{DD} = 2.5V 7x boosting(cross check)	FFL = "0"		TBD	TBD		
Current consumption (4)	I_{DD4}		FFL = "1"		TBD	TBD		
Current consumption (5)	I_{DD5}	V_{DD} = 3.0V 6 x boosting (all ON)	FFL = "0"		TBD	TBD		
Current consumption (6)	I_{DD6}		FFL = "1"		TBD	TBD		
Current consumption (7)	I_{DD7}	V_{DD} = 3.0V 6x boosting(cross check)	FFL = "0"		TBD	TBD		
Current consumption (8)	I_{DD8}		FFL = "1"		TBD	TBD		
Current consumption (9)	I_{DD9}	V_{DD} = 3.0V 5 x boosting (all ON)	FFL = "0"		TBD	TBD		
Current consumption (10)	I_{DD10}		FFL = "1"		TBD	TBD		
Current consumption (11)	I_{DD11}	V_{DD} = 3.0V 5x boosting(cross check)	FFL = "0"		TBD	TBD		
Current consumption (12)	I_{DD12}		FFL = "1"		TBD	TBD		
Current consumption (13)	I_{DD13}	V_{DD} = 3.0V 4 x boosting (all ON)	FFL = "0"		TBD	TBD		
Current consumption (14)	I_{DD14}		FFL = "1"		TBD	TBD		
Current consumption (15)	I_{DD15}	V_{DD} = 3.0V 4x boosting(cross check)	FFL = "0"		TBD	TBD		
Current consumption (16)	I_{DD16}		FFL = "1"		TBD	TBD		
V_{BA} output voltage	V_{BA}	V_{EE} = 2.4~3.3V		TBD	0.9 V_{EE}	TBD	V	*13
V_{REG} output voltage	V_{REG}	V_{EE} = 2.4~3.3V V_{REF} = 0.9 x V_{EE} N x boosting (N=2~7)		TBD	(V_{REF} x N)	TBD	V	*14

■ ELECTRICAL CHARACTERISTICS

- DC Characteristics 1

Unless otherwise noted V_{SS} = 0V, V_{DD} = +1.7~+3.3V, Ta = -30~+85°C

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	PORT
Output voltage	V_{LCD}	TBD	TBD	TBD	TBD	V	
	V_1	TBD	TBD	TBD	TBD	V	
	V_2	TBD	TBD	TBD	TBD	V	
	V_3	TBD	TBD	TBD	TBD	V	
	V_4	TBD	TBD	TBD	TBD	V	

- Oscillator frequency,f_{OSC} at each mode, relation external clock frequency,f_{CK} to LCD frame frequency,f_{FLM}

ITEM	Used clock	Display mode	Display duty (1/D)			PORT
			1/82, 1/77, 1/66	1/47, 1/38, 1/32, 1/26	1/17	
Using internal oscillator circuit	f_{OSC}	Variable gradation display	f_{OSC} / (62*D)	f_{OSC} / (62*D*2)	f_{OSC} / (62*D*4)	FLM
		Fixed gradation display	f_{OSC} / (14*D)	f_{OSC} / (14*D*2)	f_{OSC} / (14*D*4)	
		BW display	f_{OSC} / (2*D)	f_{OSC} / (2*D*2)	f_{OSC} / (2*D*4)	
Input external clock	f_{CK}	Variable gradation display	f_{CK} / (62*D)	f_{CK} / (62*D*2)	f_{CK} / (62*D*4)	
		Fixed gradation display	f_{CK} / (14*D)	f_{CK} / (14*D*2)	f_{CK} / (14*D*4)	
		BW display	f_{CK} / (2*D)	f_{CK} / (2*D*2)	f_{CK} / (2*D*4)	

Applied port (* Remark Solves)

*1 D_0~D_{15}, $\overline{CS}$, RS, M/S, $\overline{RD}$, $\overline{WR}$, P/S, SEL68, CLK, CL, FLM, FR, $\overline{RES}$ ports

*2 D_0~D_{15} ports

*3 CL, FLM, FR, CLK ports

*4 $\overline{CS}$, RS, M/S, SEL68, $\overline{RD}$, $\overline{WR}$, P/S, $\overline{RES}$, OSC_1 ports

*5 applicable at D_0~D_{15}, CL, FLM, FR, CLK = high impedance state

*6 $SEGA_0$~$SEGA_{127}$, $SEGB_0$~$SEGB_{127}$, $SEGC_0$~$SEGC_{127}$, COM_0~COM_{79}, $COMI_0$, $COMI_1$ ports
resistance when being supplied 0.5V between each output ports and power port ($V_{LCD,}$ $V_{1,}$ $V_{2,}$ $V_{3,}$ V_4)
applicable under bias ratio = 1/9

*7 V_{DD} ports
V_{DD} current when source clock is stopped, chip selection ($\overline{CS}$=V_{DD}) is non-selection state and no load.

*8 oscillator frequency when internal oscillator circuit is used (gradation display mode).
applicable under Rf register of oscillator circuit, {Rf_2, Rf_1, Rf_0} = “000”

*9 oscillator frequency when internal oscillator circuit is used (fixed gradation display mode).
applicable under Rf register of oscillator circuit, {Rf_2, Rf_1, Rf_0} = “000”

*10 oscillator frequency when internal oscillator circuit is used (BW display mode).
applicable under Rf register of oscillator circuit, {Rf_2, Rf_1, Rf_0} = “000”

*11 V_{OUT} port
N x boosting (N=2~7). applicable under internal oscillator circuit and internal power circuit are ON state
V_{EE} = 2.4~3.3V, electric volume is MAX(“1111111”).
bias = 1/5~1/10, 1/82 duty, no load at LCD driver port.
RL = 30kΩ(between V_{OUT} ,V_{SS}), CA_1= CA_2=1.0μF, CA_3=0.1μF, DCON=“1”, AMPON=“1”

*12 applicable under internal oscillator circuit and internal power circuit are ON state and no access from CPU.
electric volume is “1111111”.
Display is all ON and cross check pattern display (variable gradation display mode), and no load at LCD driver port.
Test condition : V_{DD}=V_{EE}=V_{REF}, CA_1=CA_2=1.0μF, CA_3=0.1μF, DCON=“1”, AMPON=“1”, NLIN=”0”, 1/82 duty.

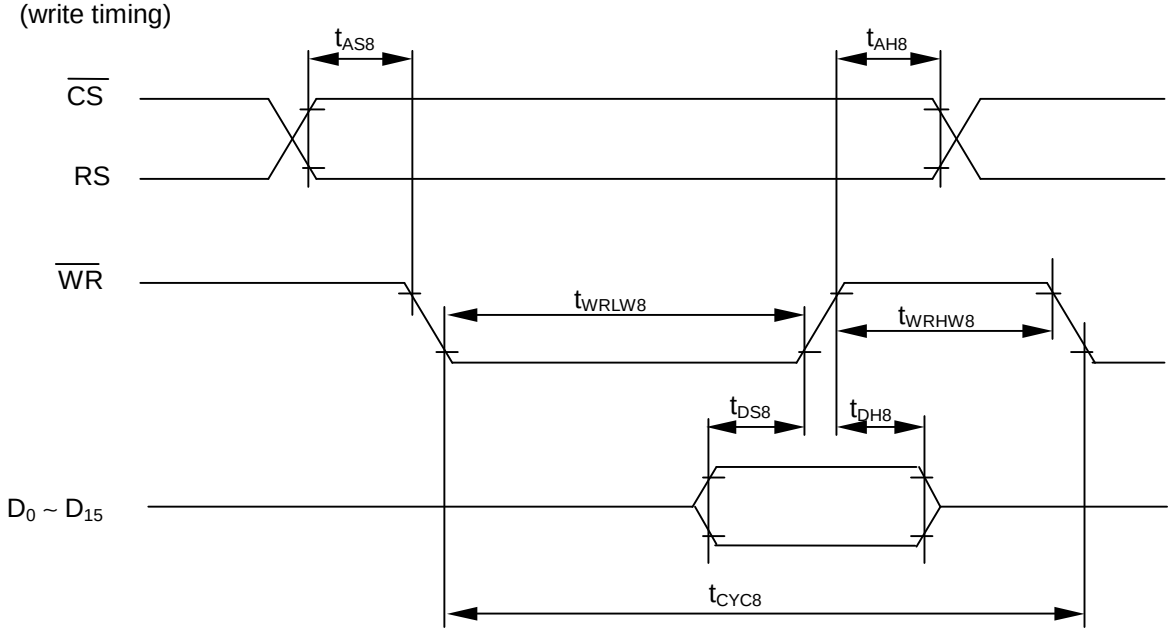
*13 V_{REG} output voltage when V_{BA} output is connected to V_{REF} input, V_{REG} gain is N=1.

*14 V_{REG} port
V_{EE}= 2.4~3.3V, V_{REF}= 0.9 V_{EE}, bias= 1/5~1/10, 1/82 duty, electric volume is “1111111”。
Cross hatch state and no load at LCD driver port.
Boosting coefficient N is 2~7 times
Test condition : CA_1=CA_2=1.0μF, CA_3=0.1μF, DCON=“1”, AMPON=“1”, NLIN=”0”。

■ AC CHARACTERISTICS

- SYSTEM BUS READ / WRITE TIMING (80 series CPU interface)

(write timing)



(V_{DD}=2.7~3.3V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH8} t_{AS8}		TBD TBD		ns ns	$\overline{CS}$ RS
System cycle timing Write "L" pulse width Write "H" pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		TBD TBD TBD		ns ns ns	$\overline{WR}$
Data setup timing Data hold timing	t_{DS8} t_{DH8}		TBD TBD		ns ns	D_0 ~ D_{15}

(V_{DD}=2.4~2.7V, Ta=-30~+85°C)

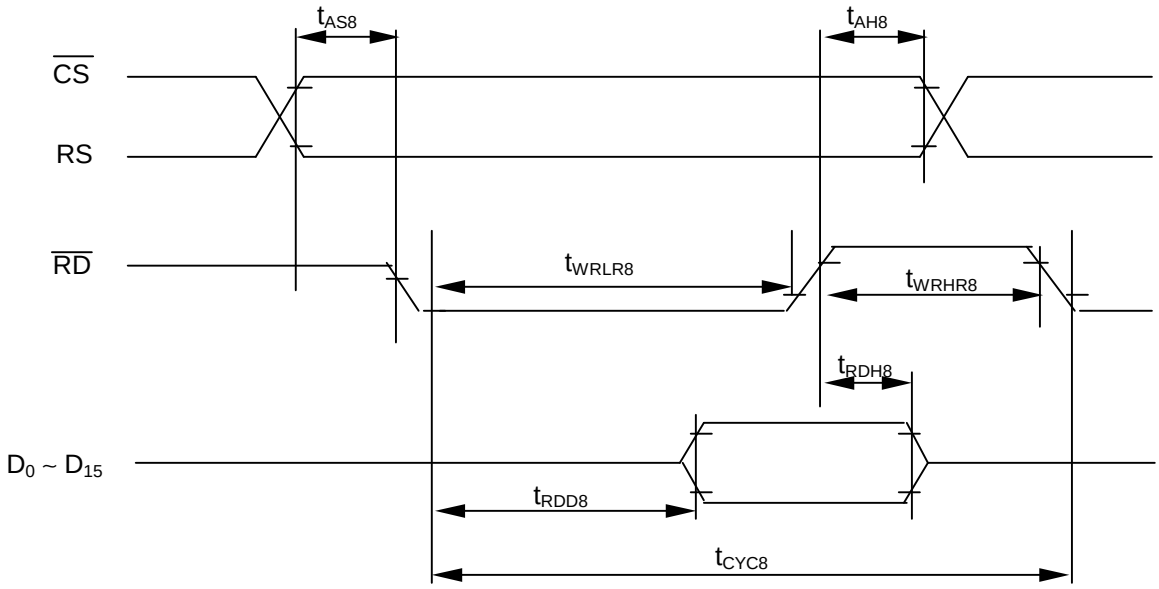
ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH8} t_{AS8}		TBD TBD		ns ns	$\overline{CS}$ RS
System cycle timing Write "L" pulse width Write "H" pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		TBD TBD TBD		ns ns ns	$\overline{WR}$
Data setup timing Data hold timing	t_{DS8} t_{DH8}		TBD TBD		ns ns	D_0 ~ D_{15}

(V_{DD}=1.7~2.4V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH8} t_{AS8}		TBD TBD		ns ns	$\overline{CS}$ RS
System cycle timing Write "L" pulse width Write "H" pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		TBD TBD TBD		ns ns ns	$\overline{WR}$
Data setup timing Data hold timing	t_{DS8} t_{DH8}		TBD TBD		ns ns	D_0 ~ D_{15}

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

(read timing)



(V_{DD}=2.7~3.3V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH8} t_{AS8}		TBD TBD		ns ns	$\overline{CS}$ RS
System cycle timing Write "L" pulse width Write "H" pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		TBD TBD TBD		ns ns ns	$\overline{RD}$
Data setup timing Data hold timing	t_{DS8} t_{DH8}		 TBD	TBD	ns ns	D_0 ~ D_{15}

(V_{DD}=2.4~2.7V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH8} t_{AS8}		TBD TBD		ns ns	$\overline{CS}$ RS
System cycle timing Write "L" pulse width Write "H" pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		TBD TBD TBD		ns ns ns	$\overline{RD}$
Data setup timing Data hold timing	t_{DS8} t_{DH8}		 TBD	TBD	ns ns	D_0 ~ D_{15}

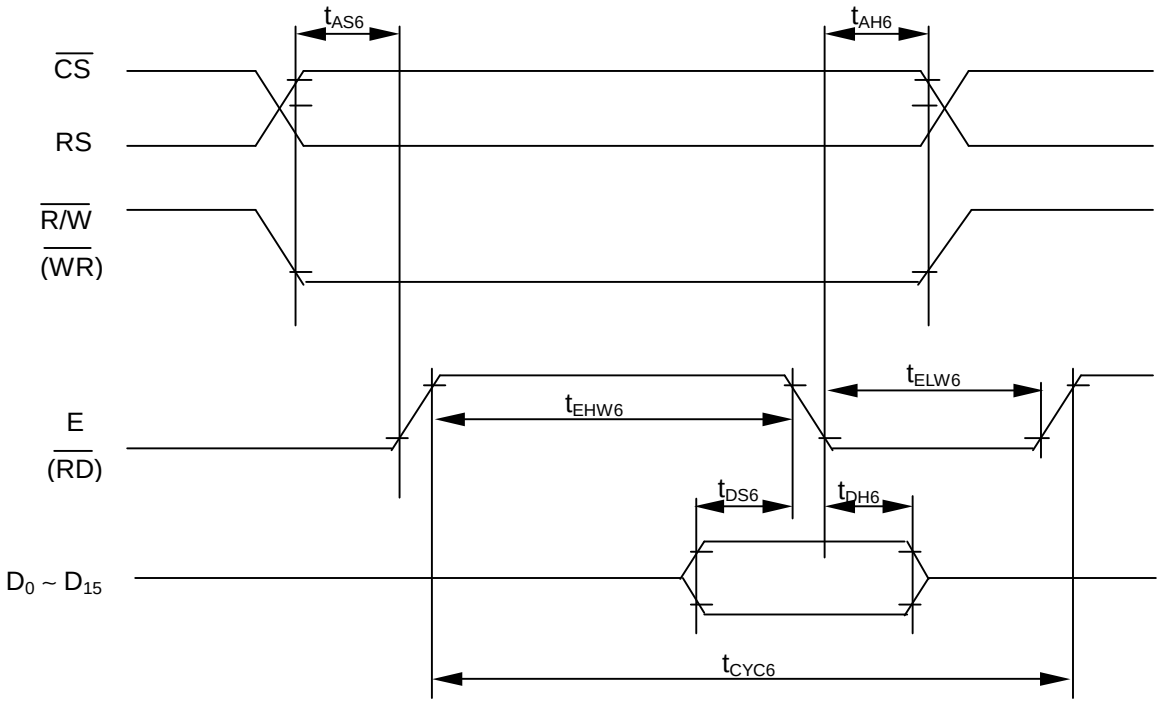
(V_{DD}=1.7~2.4V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH8} t_{AS8}		TBD TBD		ns ns	$\overline{CS}$ RS
System cycle timing Write "L" pulse width Write "H" pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		TBD TBD TBD		ns ns ns	$\overline{RD}$
Data setup timing Data hold timing	t_{DS8} t_{DH8}		 TBD	TBD	ns ns	D_0 ~ D_{15}

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

- SYSTEM BUS READ / WRITE TIMING (68 series CPU interface)

(write timing)



(V_{DD}=2.7~3.3V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH6} t_{AS6}		TBD TBD		ns ns	$\overline{CS}$ RS
System cycle timing Enable "L" pulse width Enable "H" pulse width	t_{CYC6} t_{ELW6} t_{EHW6}		TBD TBD TBD		ns ns ns	$\overline{E}$
Data setup timing Data hold timing	t_{DS6} t_{DH6}		TBD TBD		ns ns	D_0 ~ D_{15}

(V_{DD}=2.4~2.7V, Ta=-30~+85°C)

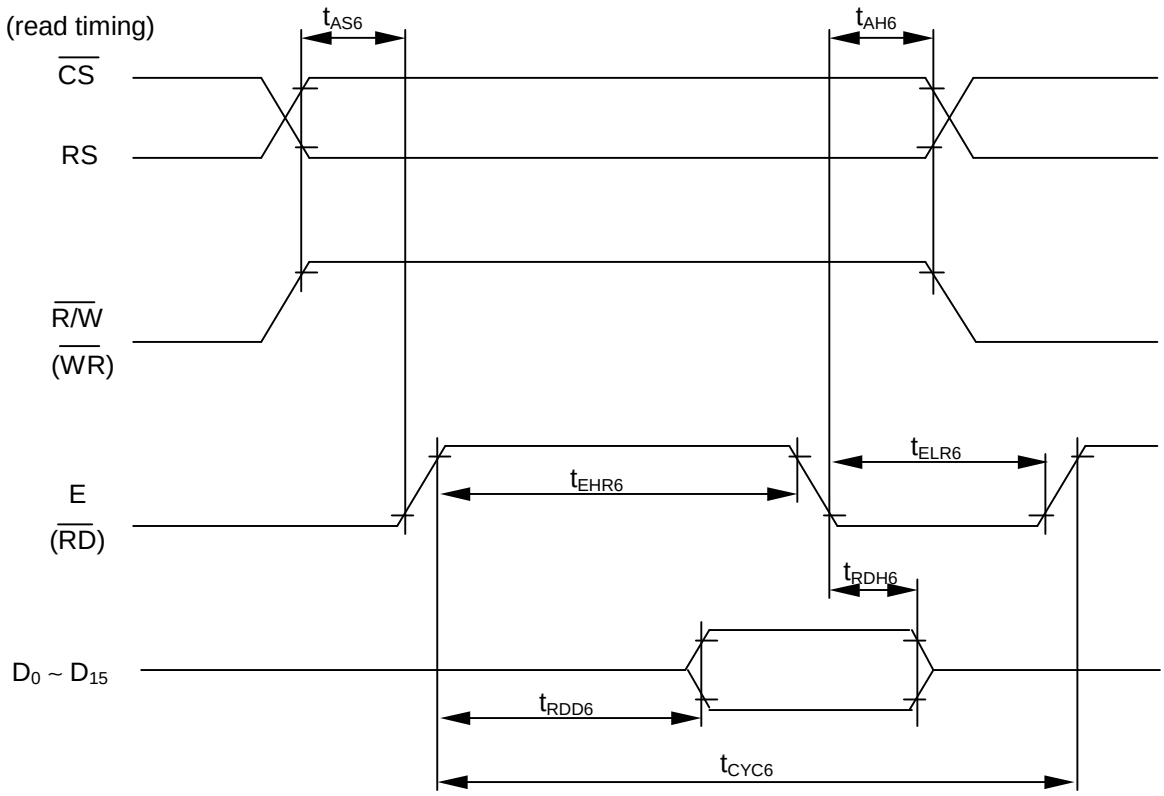
ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH6} t_{AS6}		TBD TBD		ns ns	$\overline{CS}$ RS
System cycle timing Enable "L" pulse width Enable "H" pulse width	t_{CYC6} t_{ELW6} t_{EHW8}		TBD TBD TBD		ns ns ns	$\overline{E}$
Data setup timing Data hold timing	t_{DS6} t_{DH6}		TBD TBD		ns ns	D_0 ~ D_{15}

(V_{DD}=1.7~2.4V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH6} t_{AS6}		TBD TBD		ns ns	$\overline{CS}$ RS
System cycle timing Enable "L" pulse width Enable "H" pulse width	t_{CYC6} t_{ELW6} t_{EHW6}		TBD TBD TBD		ns ns ns	$\overline{E}$
Data setup timing Data hold timing	t_{DS6} t_{DH6}		TBD TBD		ns ns	D_0 ~ D_{15}

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

(read timing)



(V_{DD}=2.7~3.3V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH6} t_{AS6}		TBD TBD		ns ns	$\overline{CS}$ RS
System cycle timing Enable "L" pulse width Enable "H" pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		TBD TBD TBD		ns ns ns	$\overline{E}$
Data setup timing Data hold timing	t_{DS6} t_{DH6}		 TBD	TBD	ns ns	D_0 ~ D_{15}

(V_{DD}=2.4~2.7V, Ta=-30~+85°C)

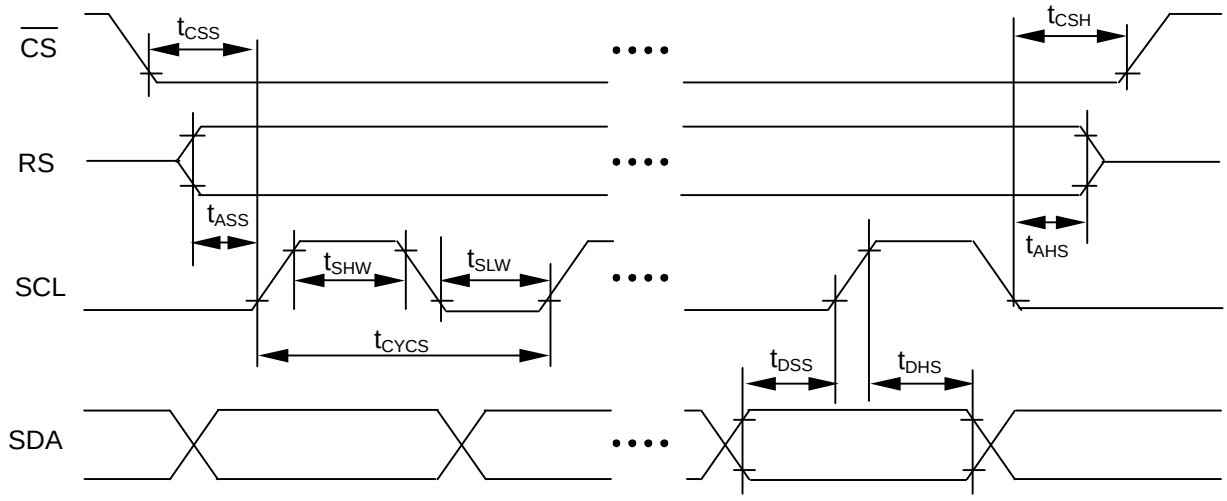
ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH6} t_{AS6}		TBD TBD		ns ns	$\overline{CS}$ RS
System cycle timing Enable "L" pulse width Enable "H" pulse width	t_{CYC6} t_{ELR6} t_{EHR8}		TBD TBD TBD		ns ns ns	$\overline{E}$
Data setup timing Data hold timing	t_{DS6} t_{DH6}		 TBD	TBD	ns ns	D_0 ~ D_{15}

(V_{DD}=1.7~2.4V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH6} t_{AS6}		TBD TBD		ns ns	$\overline{CS}$ RS
System cycle timing Enable "L" pulse width Enable "H" pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		TBD TBD TBD		ns ns ns	$\overline{E}$
Data setup timing Data hold timing	t_{DS6} t_{DH6}		TBD TBD		ns ns	D_0 ~ D_{15}

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

- SERIAL INTERFACE TIMING



(V_{DD}=2.7~3.3V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Serial clock cycle SCL "H" pulse width SCL "L" pulse width	t_{CYCS} t_{SHW} t_{SLW}		TBD TBD TBD		ns ns ns	SCL
Address setup timing Address hold timing	t_{ASS} t_{AHS}		TBD TBD		ns ns	RS
Data setup timing Data hold timing	t_{DSS} t_{DHS}		TBD TBD		ns ns	SDA
$\overline{CS}$ – SCL timing $\overline{CS}$ hold timing	t_{CSS} t_{CSH}		TBD TBD		ns ns	$\overline{CS}$

(V_{DD}=2.4~2.7V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Serial clock cycle SCL "H" pulse width SCL "L" pulse width	t_{CYCS} t_{SHW} t_{SLW}		TBD TBD TBD		ns ns ns	SCL
Address setup timing Address hold timing	t_{ASS} t_{AHS}		TBD TBD		ns ns	RS
Data setup timing Data hold timing	t_{DSS} t_{DHS}		TBD TBD		ns ns	SDA
$\overline{CS}$ – SCL timing $\overline{CS}$ hold timing	t_{CSS} t_{CSH}		TBD TBD		ns ns	$\overline{CS}$

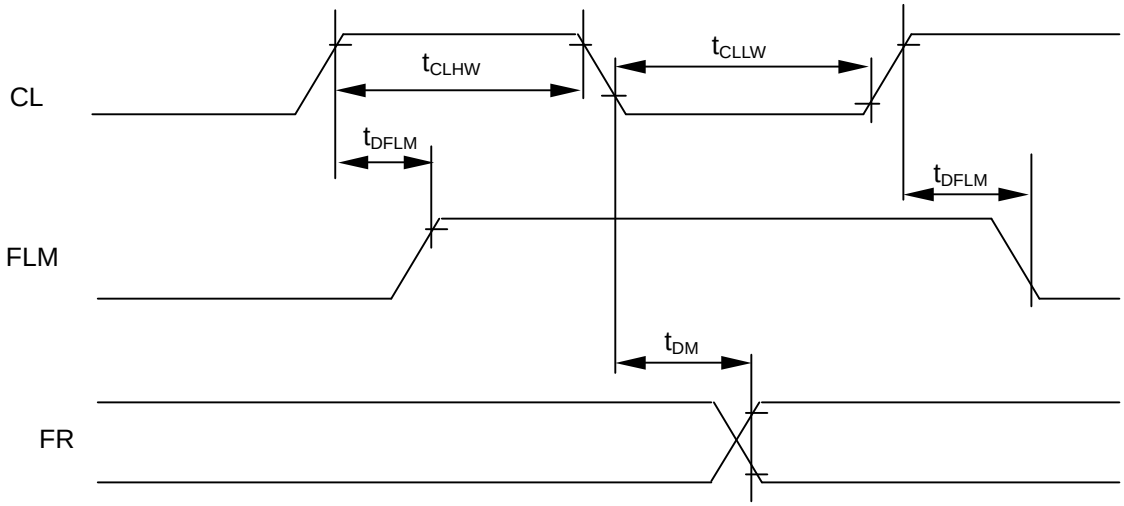
notice) All timing reference is 20% and 80% of V_{DD} and 80%.

(V_{DD}=1.7~2.4V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Serial clock cycle	t_{CYCS}		TBD		ns	SCL
SCL "H" pulse width	t_{SHW}		TBD		ns	
SCL "L" pulse width	t_{SLW}		TBD		ns	
Address setup timing	t_{ASS}		TBD		ns	RS
Address hold timing	t_{AHS}		TBD		ns	
Data setup timing	t_{DSS}		TBD		ns	SDA
Data hold timing	t_{DHS}		TBD		ns	
$\overline{CS}$ – SCL timing	t_{CSS}		TBD		ns	$\overline{CS}$
$\overline{CS}$ hold timing	t_{CSH}		TBD		ns	

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

- DISPLAY CONTROL TIMING



INPUT TIMING (slave mode) (V_{DD}=2.4~3.3V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
CL "H" pulse width CL "L" pulse width	t_{CLHW} t_{CLLW}		80 80		µs µs	CL
FLM delay time	t_{DFLM}		-1.0	1.0	µs	FLM
FR delay time	t_{FR}		-1.0	1.0	µs	FR

INPUT TIMING (slave mode) (V_{DD}=1.7~2.4V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
CL "H" pulse width CL "L" pulse width	t_{CLHW} t_{CLLW}		80 80		µs µs	CL
FLM delay time	t_{DFLM}		-1.0	1.0	µs	FLM
FR delay time	t_{FR}		-1.0	1.0	µs	CL

OUTPUT TIMING (master mode) (V_{DD}=2.4~3.3V, Ta=-30~+85°C)

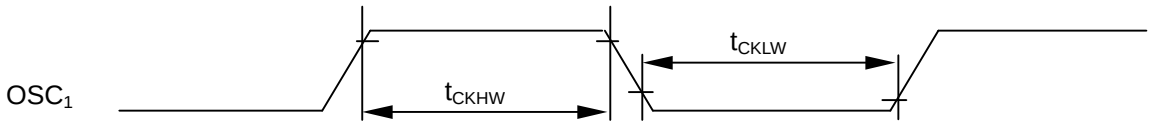
ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
FLM delay time	t_{DFLM}	CL=15pF	10	500	ns	FLM
FR delay time	t_{FR}		10	500	ns	FR

OUTPUT TIMING (master mode) (V_{DD}=1.7~2.4V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
FLM delay time	t_{DFLM}	CL=15pF	10	1000	ns	FLM
FR delay time	t_{FR}		10	1000	ns	FR

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

- SOURCE CLOCK INPUT TIMING



(V_{DD}=2.4~3.3V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
OSC_1 "H" pulse width (1)	t_{CKHW1}		TBD	TBD	µs	OSC_1
OSC_1 "L" pulse width (1)	t_{CKLW1}		TBD	TBD	µs	∗1
OSC_1 "H" pulse width (2)	t_{CKHW2}		TBD	TBD	µs	OSC_1
OSC_1 "L" pulse width (2)	t_{CKLW2}		TBD	TBD	µs	∗2
OSC_1 "H" pulse width (3)	t_{CKHW3}		TBD	TBD	µs	OSC_1
OSC_1 "L" pulse width (3)	t_{CKLW3}		TBD	TBD	µs	∗3

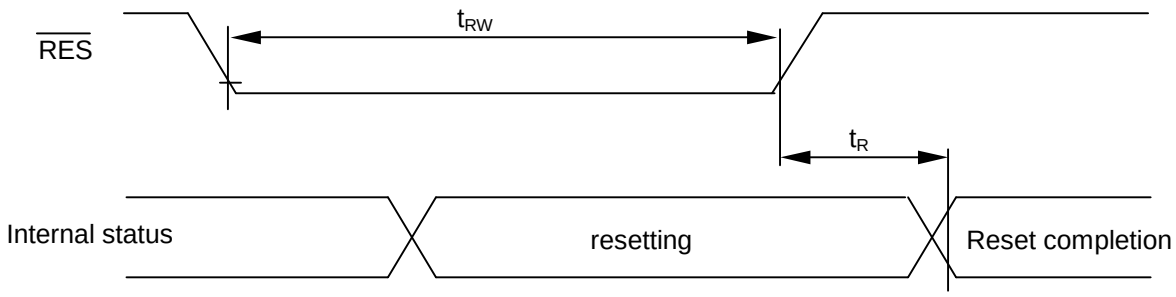
(V_{DD}=1.7~2.4V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
OSC_1 "H" pulse width (1)	t_{CKHW1}		TBD	TBD	µs	OSC_1
OSC_1 "L" pulse width (1)	t_{CKLW1}		TBD	TBD	µs	∗1
OSC_1 "H" pulse width (2)	t_{CKHW2}		TBD	TBD	µs	OSC_1
OSC_1 "L" pulse width (2)	t_{CKLW2}		TBD	TBD	µs	∗2
OSC_1 "H" pulse width (3)	t_{CKHW3}		TBD	TBD	µs	OSC_1
OSC_1 "L" pulse width (3)	t_{CKLW3}		TBD	TBD	µs	∗3

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

∗1 applicable under gradation display , MON="0", PWM="0"
∗2 applicable under fixed gradation display , MON="0",PWM="1"
∗3 applicable under BW display , MON="1"

- RESET INPUT TIMING



(V_{DD}=2.4~3.3V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Reset time	t_R			1.0	μs	
$\overline{RES}$ "L" pulse width	t_{RW}		10.0		μs	$\overline{RES}$

(V_{DD}=1.7~2.4V, Ta=-30~+85°C)

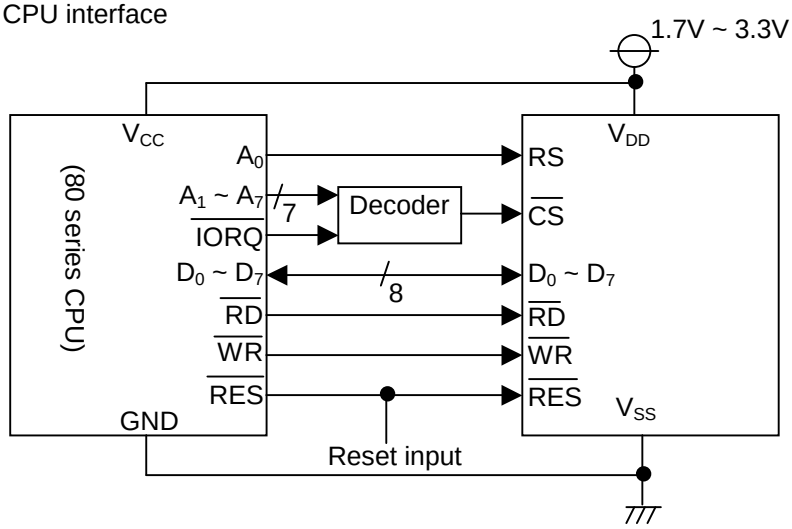
ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Reset time	t_R			1.5	μs	
$\overline{RES}$ "L" pulse width	t_{RW}		10.0		μs	$\overline{RES}$

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

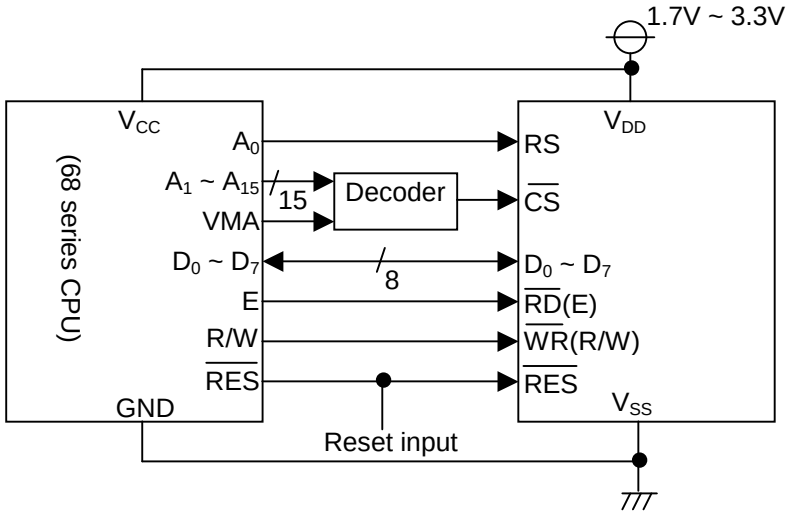
■ APPLICATION EXAMPLE（*reference*）

(1) connection with CPU

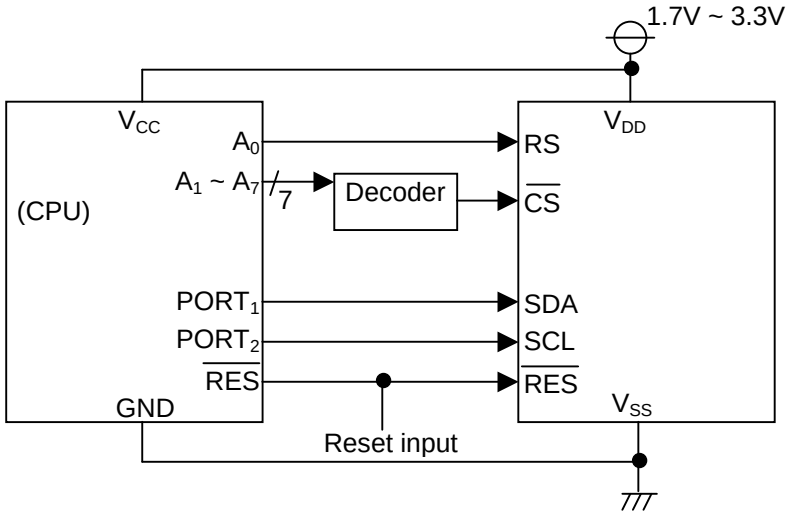
a) 80 series CPU interface



b) 68 series CPU interface



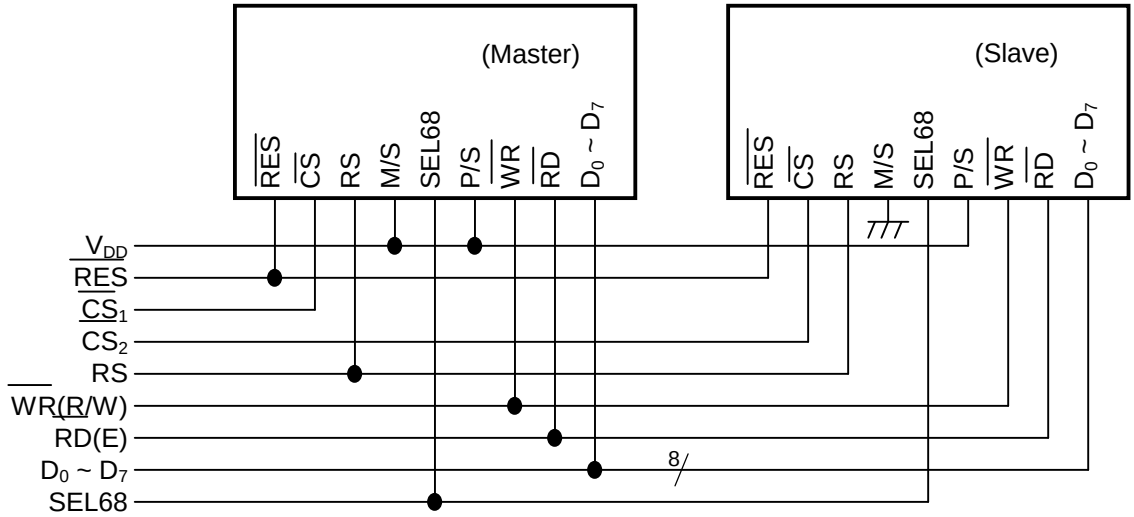
c) CPU connection with serial interface



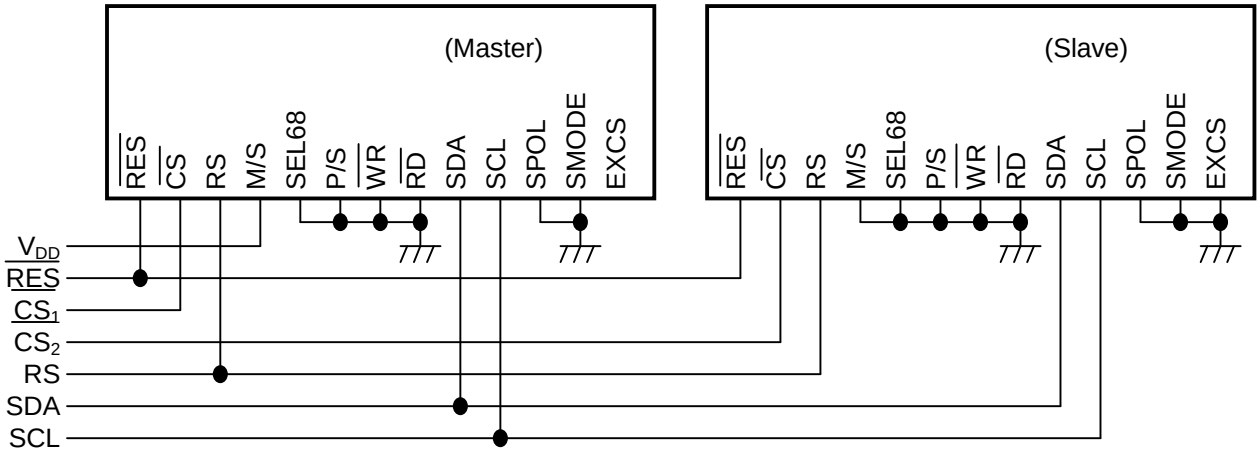
(2) MULTI CHIP INTERFACE

a) connection example of input interface

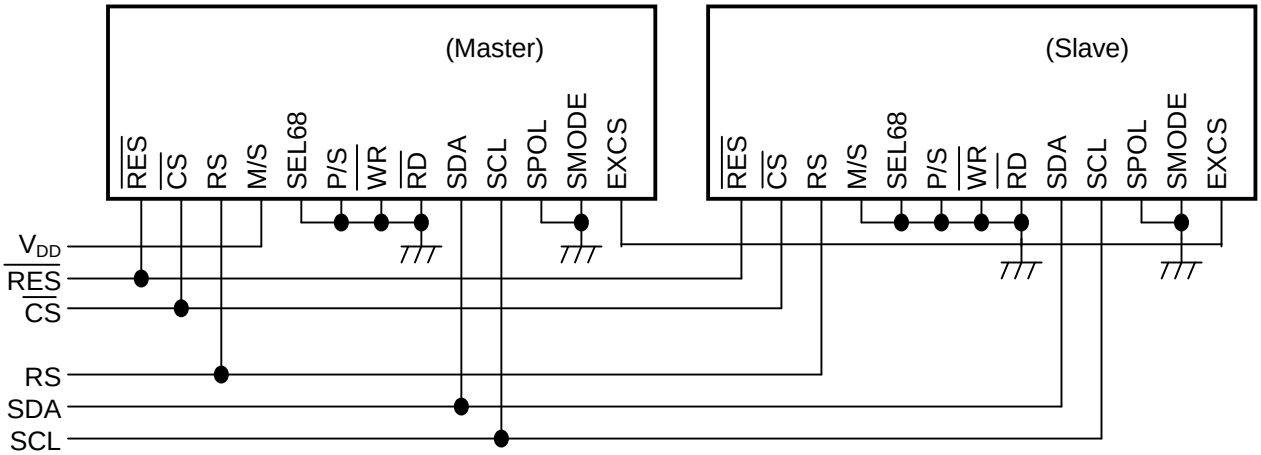
(parallel interface)



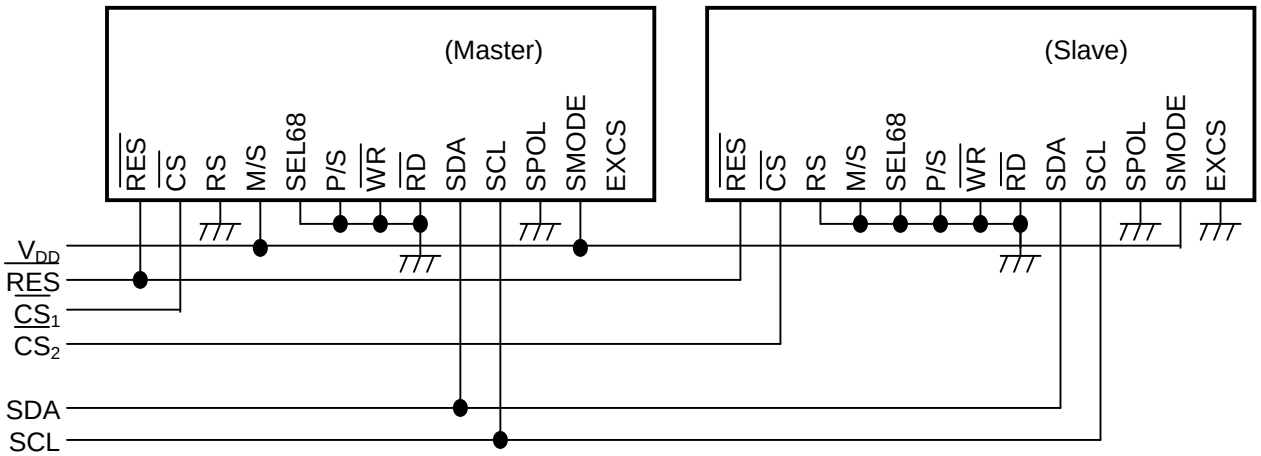
(4-line type serial interface)



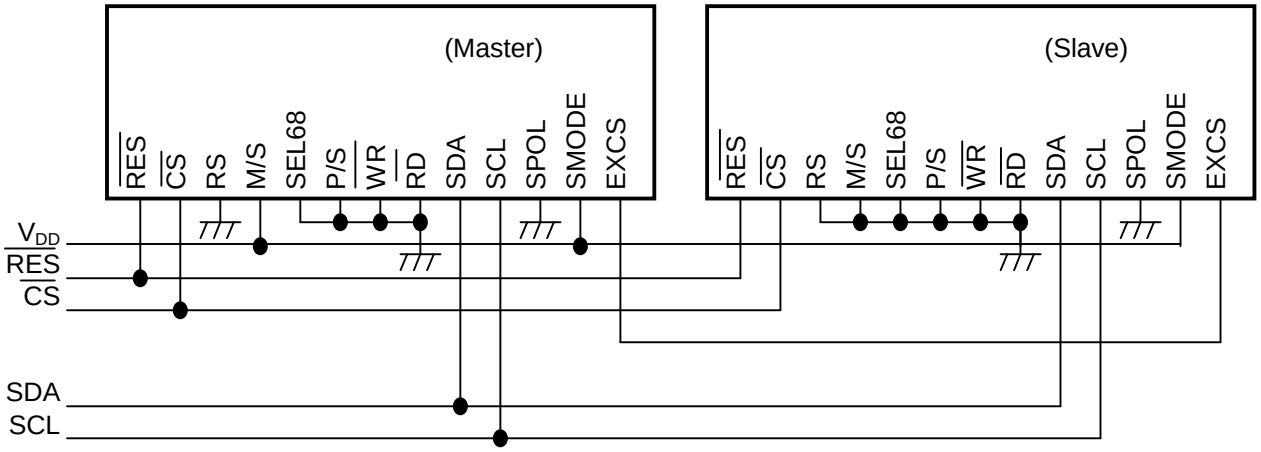
(4-line type serial interface, $\overline{CS_1}$ common)



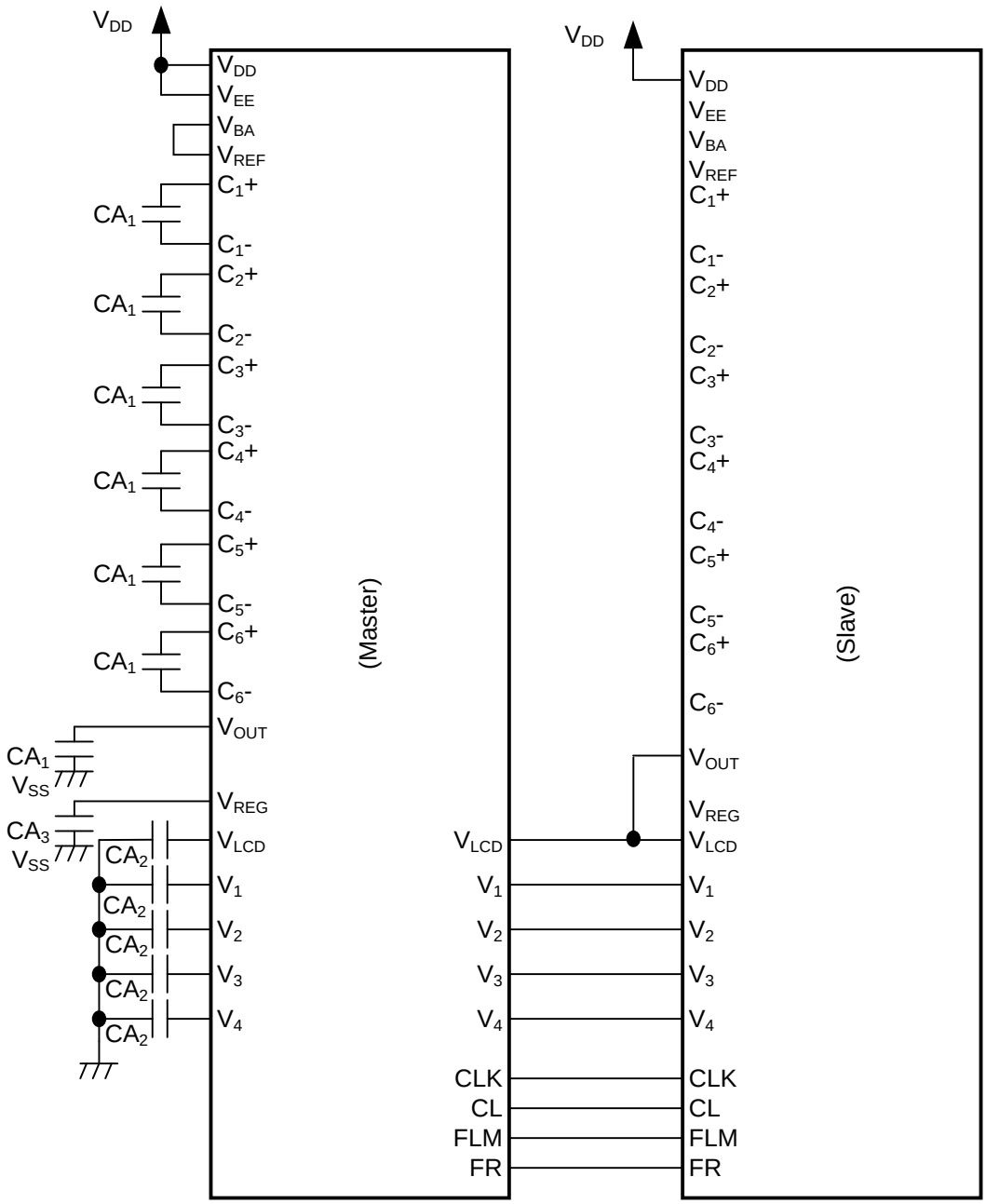
(3-line type serial interface)



(3-line type serial interface, $\overline{CS_1}$ common)



a) connection example of power supply



Be cautious of using as following description when LCD panel is connected with master/slave structure.

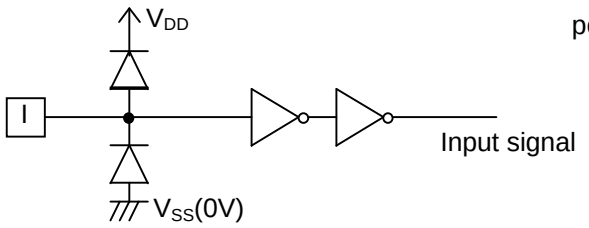
1) Display timing is controlled by master chip. The CL, FLM, FR, CLK signals are stopped when master chip is display OFF. When you are going to OFF the display, please OFF the display of slave chip first before master chip display is OFF.
2) Boosting circuit and voltage converting circuit is OFF after execution HALT command at master chip, then LCD driving output is V_{SS} level and so display is OFF. And Voltage common is stopped. Because the voltage common of slave chip is stopped, please run slave chip display OFF first and then run master chip HALT command.
3) The electric volume setting is valid at master chip only(at upper structure).
4) To protect that V_{OUT} is being floated, please connect V_{OUT} with V_{LCD} voltage level.
5) Please use under condition that OSC_1 and OSC_2 port of slave chip is OFF.

- Typical characteristic

ITEM	CONDITION	MIN	TYP	MAX	UNIT
Basic delay time of gate	Ta=+25°C, V_{SS}=0V, V_{DD}=3.0V		10		ns

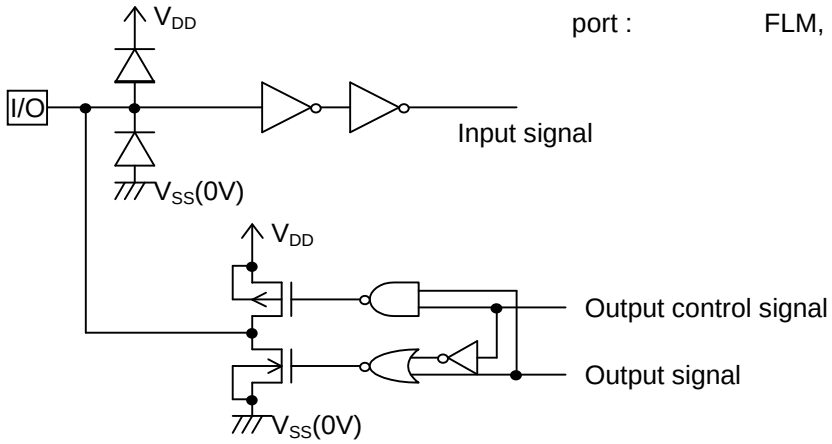
- IN/OUTPUT CIRCUIT STRUCTURE

(a) input circuit 1



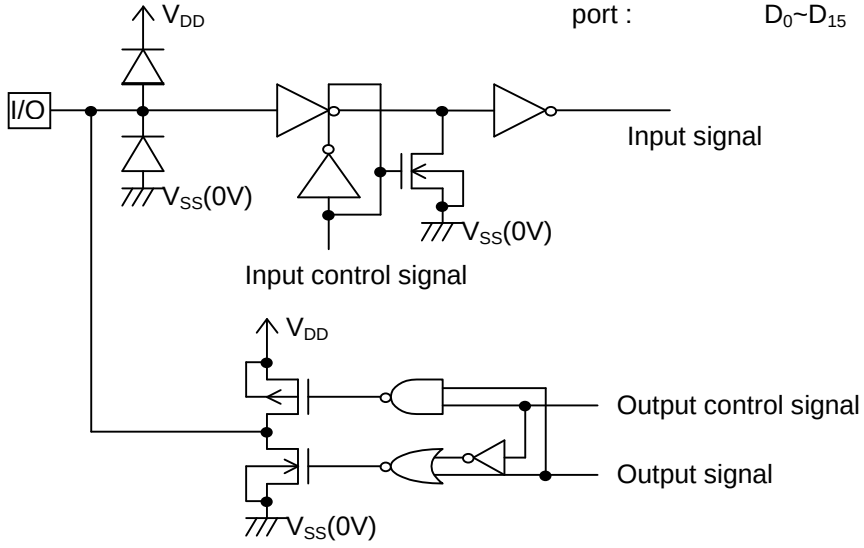
port : $\overline{CS}$, RS, $\overline{RD}$, $\overline{WR}$, SEL68, M/S
P/S, $\overline{RES}$

(b-1) in/out circuit 1



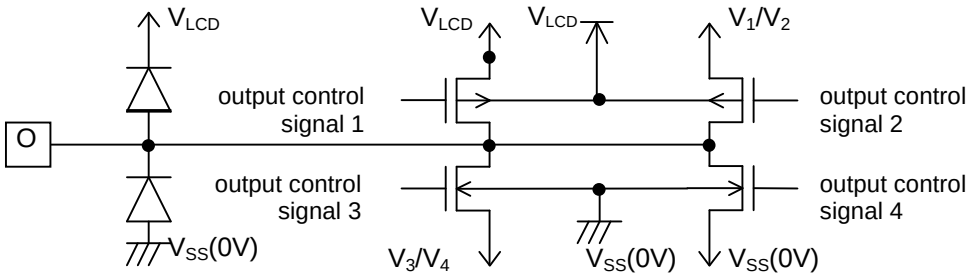
port : FLM, LP, FR, CLK

(b-2) in/out circuit 2



port : D_0~D_{15}

(c) LCD driver output circuit



Port : $SEGA_0$~$SEGA_{127}$
$SEGB_0$~$SEGB_{127}$
$SEGC_0$~$SEGC_{127}$
COM_0~COM_{79}
$COMI_0$, $COMI_1$
$SEGSA_0$, $SEGSR_1$
$SEGSB_0$, $SEGSB_1$
$SEGSC_0$, $SEGSC_1$

<precautions>

The details of this specification was written sincerely, but it is not a letter of guarantee of legal. Especially, the application circuit is just for reference.

This specification do not guarantee that we did not use others patent or intellectural property.