

HSP061-2

2-line ESD protection for high speed lines

Features

- Flow-through routing to keep signal integrity
- Ultralarge bandwidth: 6 GHz
- Ultralow capacitance: 0.6 pF
- Low leakage current: 100 nA at 25 °C
- Extended operating junction temperature range: -40 °C to 150 °C
- RoHS compliant

Benefits

- High ESD robustness of the equipment
- Suitable for high density boards

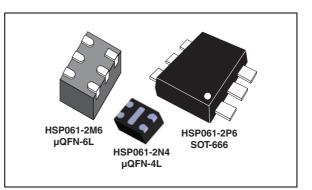
Complies with following standards

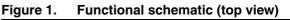
- MIL-STD 883G Method 3015-7 Class 3B:
 8 kV
- IEC 61000-4-2 level 4:
 - 15 kV (air discharge)
 - 8 kV (contact discharge)

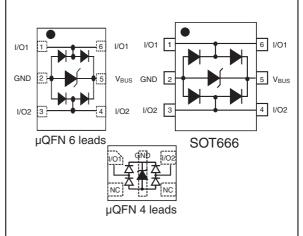
Applications

The HSP061-2 series is designed to protect against electrostatic discharge on sub micron technology circuits driving:

- HDMI 1.3 and 1.4
- Digital Video Interface
- Display Port
- USB 3.0
- Serial ATA
- Ethernet
- HMI







Description

The HSP061-2 is a 2-channel ESD array with a rail to rail architecture designed specifically for the protection of high speed differential lines.

The ultralow variation of the capacitance ensures very low influence on signal-skew. The large bandwidth makes it compatible with 5 Gbps.

The HSP061-2P6 is housed in SOT-666. The HSP061-2M6 is packaged in μ QFN-6L (1.45 x 1.0 mm) with a 500 μ m pitch. The HSP061-2N4 is packaged in μ QFN-4L (1.0 x 0.8 mm) with a 400 μ m pitch.

1 Characteristics

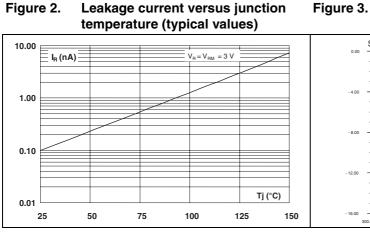
Symbol	Parameter			Unit	
V	Peak pulse voltage	IEC 61000-4-2 contact discharge	8	kV	
V _{PP}	reak puise voltage	IEC 61000-4-2 air discharge	15	κv	
I _{pp}	Repetitive peak pulse current (8/20	3	А		
Тj	Operating junction temperature range		-40 to +150	°C	
T _{stg}	Storage temperature range	-65 to +150	°C		
TL	Maximum lead temperature for sold	260	°C		

Table 1.Absolute maximum ratings Tamb = 25 °C

Table 2.Electrical characteristics $T_{amb} = 25 \ ^{\circ}C$

Symbol	Parameter	Test co	Min.	Тур.	Max.	Unit	
V _{BR}	Breakdown voltage	I _R = 1 mA		6			V
I _{RM}	Leakage current	$V_{RM} = 3 V$			100	nA	
V _{CL}	Clamping voltage	IEC 61000-4-2, - (I _{PP} = 30 A), me		18		V	
C _{I/O - GND}	Capacitance (input/output to ground)	$V_{I/O} = 0 V, F = 20$ $V_{OSC} = 30 mV$		0.6	0.85	pF	
$\Delta C_{I/O - GND}$	Capacitance variation (input/output to ground)	$V_{I/O} = 0 V F = 20$ $V_{OSC} = 30 mV$		0.03	0.13	pF	
f _C	Cut-off frequency	-3 dB	HSP061-2M6, HSP061-2P6		5.5		GHz
-			HSP061-2N4		6		







S21 (dB)

0 -1 -2 -3 -4 -5 -6 -7 -8 -9

-10

300k 1M 3M 101

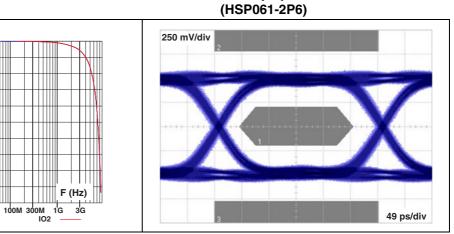
Figure 5. Eye diagram - HDMI mask at 3.4 Gbps per channel⁽¹⁾

S21 attenuation measurement (HSP061-2P6, HSP061-2M6)

> F(Hz)

> > 1 1 1 1 1

30



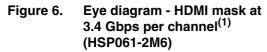
S21(db)

0.0

8.00

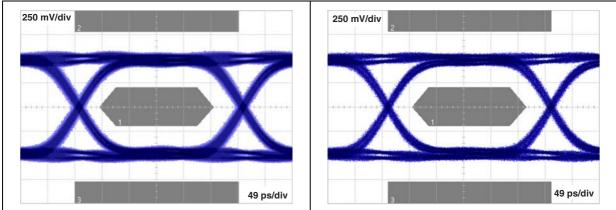
12.00

1. HDMI specification conditions. This information can be provided for other applications. Please contact your local ST office.

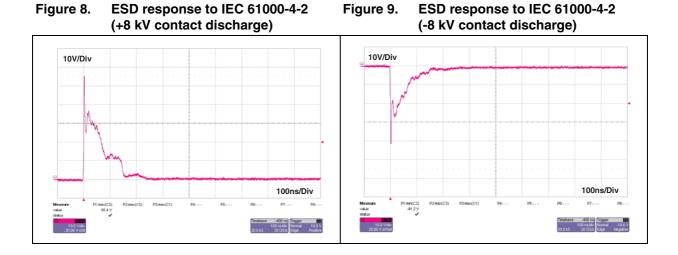


10M 30M



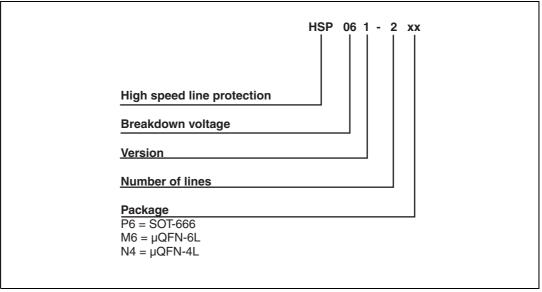






2 Ordering information scheme

Figure 10. Ordering information scheme





3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: <u>www.st.com</u>. ECOPACK[®] is an ST trademark.

Table 3. SOT-666 dimensions

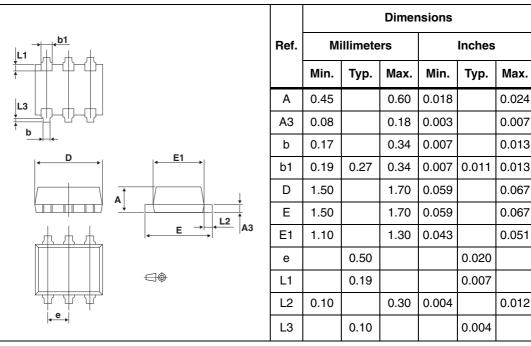


Figure 11. Footprint recommendations I dimensions in mm (inches)

Figure 12. Marking

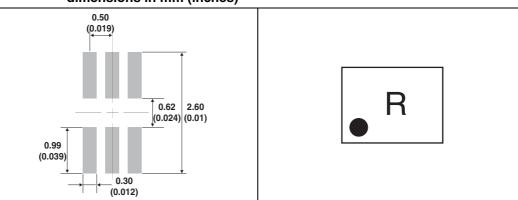
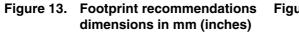
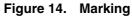


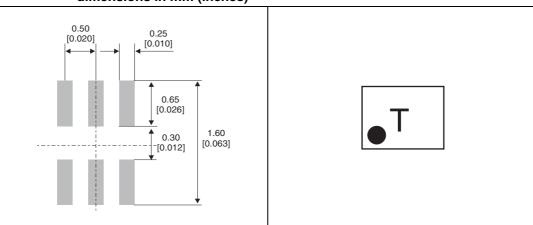


Table 4. µQFN 1.45X1.00 6L dimensions							
		Dimensions					
	Ref.	Millimeters		Inches			
<u></u> k		Min.	Тур.	Max.	Min.	Тур.	Max.
→ ←	Α	0.50	0.55	0.60	0.020	0.022	0.024
€	A1	0.00	0.02	0.05	0.000	0.001	0.002
	b	0.18	0.25	0.30	0.007	0.010	0.012
	D		1.45			0.057	
	Е		1.00			0.039	
	е		0.50			0.020	
	К	0.20			0.008		
¥	L	0.30	0.35	0.40	0.012	0.014	0.016

Table 4. µQFN 1.45x1.00 6L dimensions







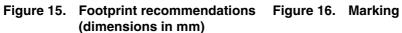
Note:

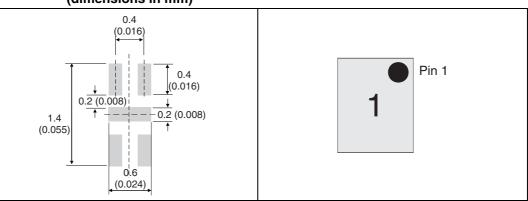
Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.



•		Dimensions					
	Ref.	Millimeters			Inches		
Side A		Min.	Тур.	Max.	Min.	Тур.	Max.
	Α	0.45	0.50	0.55	0.018	0.020	0.022
A1	A1	0.00	0.02	0.05	0.000	0.001	0.002
Bottom	b	0.15	0.20	0.25	0.006	0.008	0.010
	D	0.75	0.80	0.85	0.030	0.031	0.033
	D2	0.55	0.6	0.65	0.022	0.024	0.026
E + E2	е	0.35	0.40	0.45	0.014	0.016	0.018
	Е	0.95	1.00	1.05	0.037	0.039	0.041
→ b +	E2	0.15	0.20	0.25	0.006	0.008	0.010
	k	0.17	0.20	0.23	0.007	0.008	0.009
	L	0.15	0.20	0.25	0.006	0.008	0.010

Table 5. µQFN-4L dimensions





Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

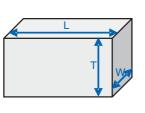


4 **Recommendation on PCB assembly**

4.1 Stencil opening design

- 1. General recommendation on stencil opening design
 - a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 17. Stencil opening dimensions



b) General design rule

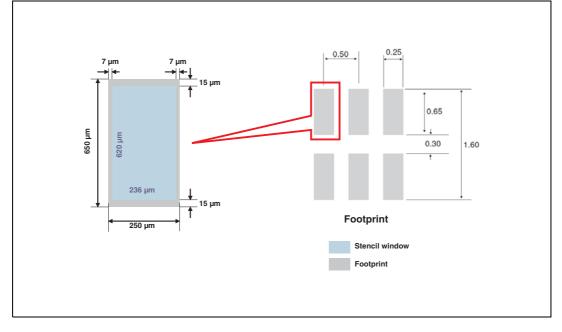
Stencil thickness (T) = 75 ~ 125 μ m

Aspect Ratio =
$$\frac{W}{T} \ge 1.5$$

Aspect Area =
$$\frac{L \times W}{2T(L+W)} \ge 0.66$$

- 2. Reference design
 - a) Stencil opening thickness: 100 µm
 - b) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 18. Recommended stencil window position for µQFN-6L





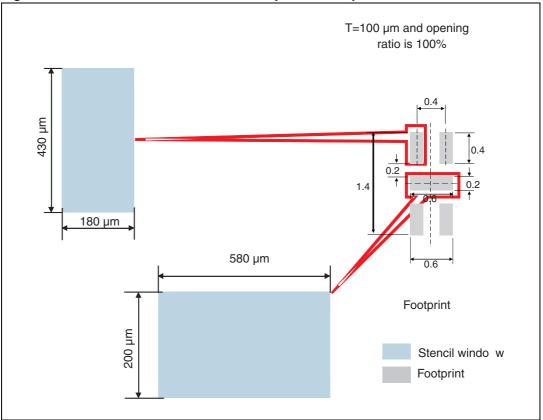


Figure 19. Recommended stencil window position for µQFN-4L

4.2 Solder paste

- 1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
- 2. "No clean" solder paste is recommended.
- 3. Offers a high tack force to resist component movement during high speed.
- 4. Solder paste with fine particles: powder particle size is 20-45 $\mu m.$

4.3 Placement

- 1. Manual positioning is not recommended.
- 2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
- 3. Standard tolerance of \pm 0.05 mm is recommended.



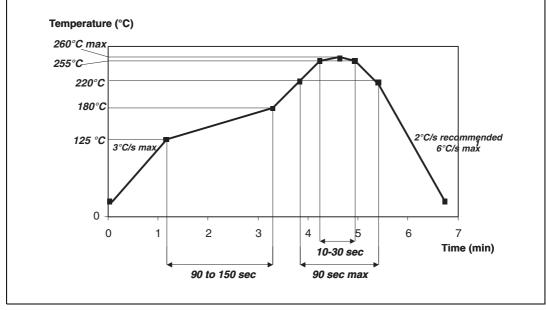
- 4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
- 5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
- 6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

- 1. To control the solder paste amount, the closed via is recommended instead of open vias.
- 2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 **Reflow profile**





Note: Minimize air convection currents in the reflow oven to avoid component movement.



5 Ordering information

Table 6. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
HSP061-2P6	R	SOT-666	2.85 mg	3000	Tape and reel (7")
HSP061-2M6	T ⁽¹⁾	µQFN-6L	2.3 mg	3000	Tape and reel (7")
HSP061-2N4	1 ⁽¹⁾	µQFN-4L	1.17 mg	10000	Tape and reel (7")

1. The marking can be rotated by multiple of 90° to differentiate assembly location

6 Revision history

Table 7.Document revision history

Date	Revision	Changes
07-Feb-2012	1	Initial release.



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