RAM Mapping 64 ×16 LCD Controller for I/O μC

Features

- Operating voltage: 2.7V~5.2V
- External Crystal 32.768kHz oscillator
- 1/5 bias, 1/16 duty, frame frequency is 64Hz
- Max. 64×16 patterns, 16 commons, 64 segments
- Built-in internal resistor type bias generator
- 3-wire serial interface
- 8 kinds of time base/WDT selection
- Time base or WDT overflow output
- Built-in LCD display RAM
- R/W address auto increment
- Two selectable buzzer frequencies (2kHz/4kHz)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- VLCD pin to adjust LCD operating voltage

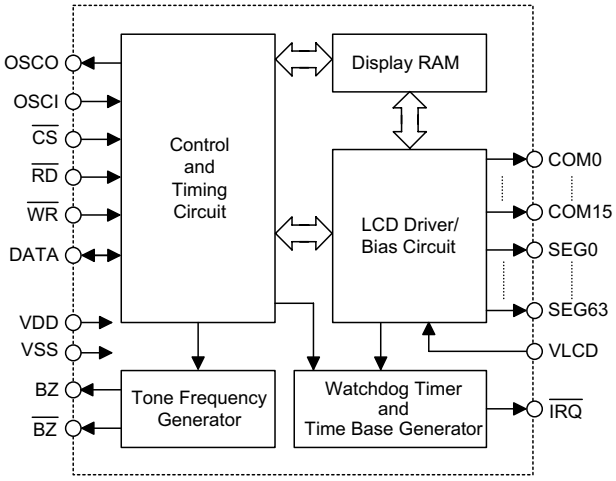
General Description

HT16270 is a peripheral device specially designed for I/O type μC used to expand the display capability. The max. display segment of the device are 1024 patterns (64×16). It also supports serial interface, buzzer sound, watchdog timer or time base timer functions. The HT16270 is a memory mapping and multi-function LCD controller. The software configuration feature of the HT16270 make it suitable for multiple LCD applications including LCD modules and display subsystems. Only three lines are required for the interface between the host controller and the HT16270. The HT162X series have many kinds of products that match various applications.

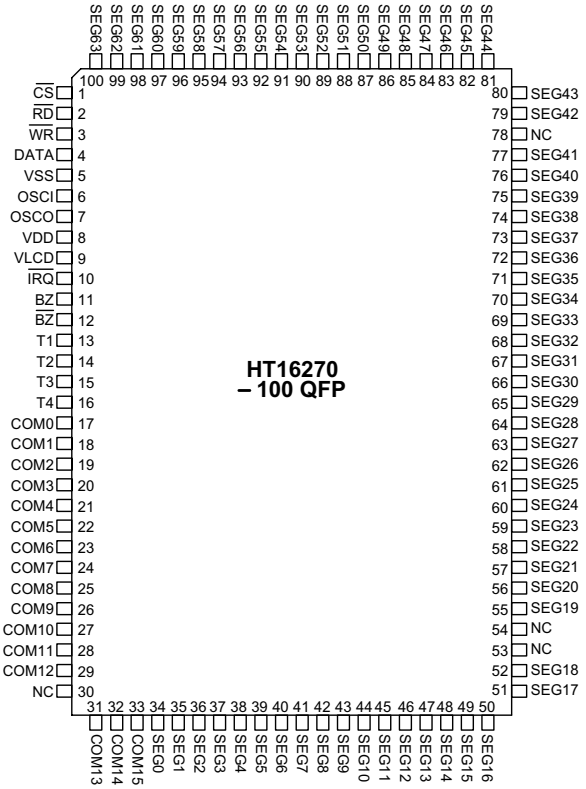
Selection Table

HT162X	HT1620	HT1621	HT1622	HT16220	HT1623	HT1625	HT1626	HT1627	HT16270
COM	4	4	8	8	8	8	16	16	**16**
SEG	32	32	32	32	48	64	48	64	**64**
Built-in Osc.		√	√		√	√	√	√	
Crystal Osc.	√	√		√	√	√	√		√

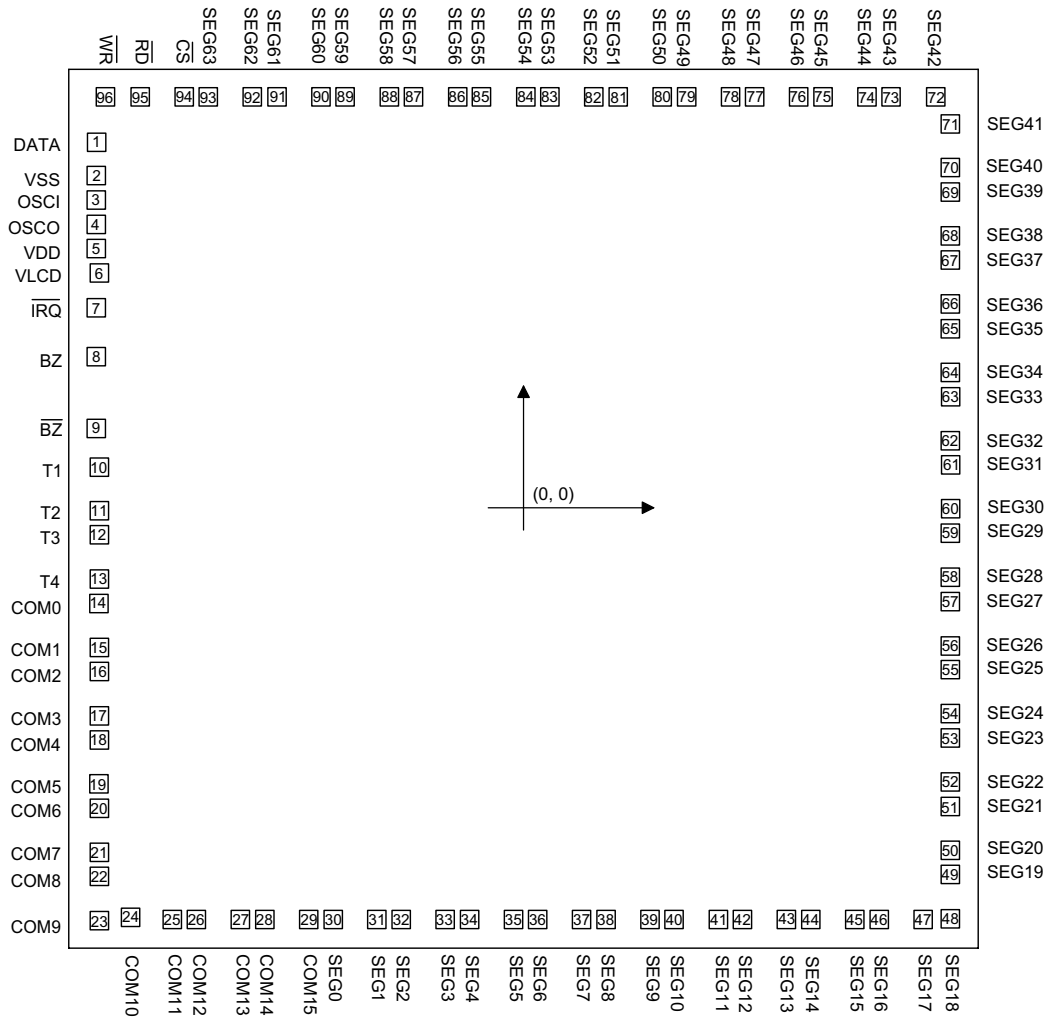
Block Diagram



Pin Assignment



Pad Assignment



Chip size: 245 × 237 (mil)^2

* The IC substrate should be connected to VDD in the PCB layout artwork.

Pad Coordinates

Unit: mil

Pad No.	X	Y	Pad No.	X	Y
1	–116.57	99.90	49	116.15	–99.79
2	–116.68	90.80	50	116.15	–93.16
3	–116.72	84.15	51	116.19	–81.18
4	–116.72	77.50	52	116.19	–74.54
5	–116.72	70.90	53	116.15	–62.58
6	–115.93	64.25	54	116.19	–55.93
7	–116.72	54.75	55	116.19	–43.94
8	–116.72	41.45	56	116.19	–37.40
9	–116.72	21.85	57	116.19	–25.37
10	–115.94	11.39	58	116.19	–18.70
11	–115.94	–0.60	59	116.19	–6.72
12	–115.94	–7.18	60	116.24	–0.09
13	–115.90	–19.21	61	116.24	11.90
14	–115.97	–25.85	62	116.19	18.49
15	–115.93	–37.85	63	116.24	30.51
16	–115.93	–44.45	64	116.19	37.10
17	–115.93	–56.45	65	116.19	49.09
18	–115.93	–63.05	66	116.15	55.76
19	–115.97	–75.05	67	116.15	67.75
20	–115.93	–81.70	68	116.19	74.38
21	–115.93	–93.65	69	116.15	86.36
22	–115.94	–100.30	70	116.19	93.03
23	–115.94	–112.37	71	116.11	104.85
24	–108.08	–112.07	72	112.20	112.24
25	–96.03	–112.05	73	100.04	112.24
26	–89.43	–112.05	74	93.42	112.24
27	–77.43	–112.05	75	81.43	112.24
28	–70.82	–112.05	76	74.80	112.24
29	–58.83	–112.05	77	62.77	112.24
30	–52.17	–112.05	78	56.23	112.24
31	–40.22	–112.05	79	44.20	112.24
32	–33.58	–112.05	80	37.57	112.24
33	–21.58	–112.00	81	25.63	112.24
34	–14.98	–112.05	82	18.95	112.24
35	–2.97	–112.00	83	6.97	112.24
36	3.67	–112.05	84	0.38	112.24
37	15.63	–112.05	85	–11.65	112.24
38	22.27	–112.05	86	–18.23	112.20
39	34.28	–112.05	87	–30.22	112.24
40	40.88	–112.05	88	–36.89	112.24
41	52.88	–112.05	89	–48.92	112.24
42	59.47	–112.05	90	–55.51	112.24
43	71.47	–112.00	91	–67.45	112.29
44	78.13	–112.00	92	–74.12	112.24
45	90.07	–112.05	93	–86.15	112.24
46	96.72	–112.05	94	–92.72	112.25
47	108.72	–112.00	95	–104.72	112.25
48	116.19	–111.82	96	–114.22	112.25

Pad Description

Pad No.	Pad Name	I/O	Description
1	DATA	I/O	Serial data input/output with pull-high resistor
2	VSS	—	Negative power supply, ground
3	OSCI	I	Crystal oscillator input pin
4	OSCO	O	Crystal oscillato output pin
5	VDD	—	Positive power supply
6	VLCD	I	LCD operating voltage input pad.
7	$\overline{IRQ}$	O	Time base or watchdog timer overflow flag, NMOS open drain output
8, 9	BZ, $\overline{BZ}$	O	2kHz or 4kHz tone frequency output pair (Tristate output buffer)
10~13	T1~T4	I	Not connected
14~29	COM0~COM15	O	LCD common outputs
30~93	SEG0~SEG63	O	LCD segment outputs
94	$\overline{CS}$	I	Chip selection input with pull-high resistor. When the $\overline{CS}$ is logic high, the data and command read from or write to the HT16270 are disabled. The serial interface circuit is also reset. But if the $\overline{CS}$ is at logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the HT16270 are all enabled.
95	$\overline{RD}$	I	READ clock input with pull-high resistor. Data in the RAM of the HT16270 are clocked out on the rising edge of the $\overline{RD}$ signal. The clocked out data will appear on the data line. The host controller can use the next falling edge to latch the clocked out data.
96	$\overline{WR}$	I	WRITE clock input with pull-high resistor. Data on the DATA line are latched into the HT16270 on the rising edge of the $\overline{WR}$ signal.

Absolute Maximum Ratings

Supply Voltage .....–0.3V to 5.5V

Input Voltage.....V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature.....–50°C to 125°C

Operating Temperature .....–25°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.7	—	5.2	V
I_{DD1}	Operating Current	3V	No load/LCD ON Crystal oscillator	—	30	75	μA
		5V		—	50	125	μA
I_{DD2}	Operating Current	3V	No load/LCD OFF Crystal oscillator	—	5	25	μA
		5V		—	10	45	μA
I_{STB}	Standby Current	3V	No load Power down mode	—	2	14	μA
		5V		—	4	28	μA
V_{IL}	Input Low Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0	—	0.6	V
		5V		0	—	1.0	V
V_{IH}	Input High Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	2.4	—	3	V
		5V		4.0	—	5	V
I_{OL1}	BZ, $\overline{BZ}$, $\overline{IRQ}$	3V	V_{OL}=0.3V	0.9	1.8	—	mA
		5V	V_{OL}=0.5V	1.7	3	—	mA
I_{OH1}	BZ, $\overline{BZ}$	3V	V_{OH}=2.7V	–0.9	–1.8	—	mA
		5V	V_{OH}=4.5V	–1.7	–3	—	mA
I_{OL2}	DATA	3V	V_{OL}=0.3V	0.9	1.8	—	mA
		5V	V_{OL}=0.5V	1.7	3	—	mA
I_{OH2}	DATA	3V	V_{OH}=2.7V	–0.9	–1.8	—	mA
		5V	V_{OH}=4.5V	–1.7	–3	—	mA
I_{OL3}	LCD Common Sink Current	3V	V_{OL}=0.3V	80	160	—	μA
		5V	V_{OL}=0.5V	180	360	—	μA
I_{OH3}	LCD Common Source Current	3V	V_{OH}=2.7V	–40	–80	—	μA
		5V	V_{OH}=4.5V	–90	–180	—	μA
I_{OL4}	LCD Segment Sink Current	3V	V_{OL}=0.3V	50	100	—	μA
		5V	V_{OL}=0.5V	120	240	—	μA
I_{OH4}	LCD Segment Source Current	3V	V_{OH}=2.7V	–30	–60	—	μA
		5V	V_{OH}=4.5V	–70	–140	—	μA
R_{PH}	Pull-high Resistor	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	100	200	300	kΩ
		5V		50	100	150	kΩ

A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS}	System Clock	3V	Crystal oscillator	—	32	—	kHz
		5V		—	32	—	kHz
f_{LCD}	LCD Frame Frequency	3V	Crystal oscillator	—	64	—	Hz
		5V		—	64	—	Hz
t_{COM}	LCD Common Period	—	n: Number of COM	—	n/f_{LCD}	—	sec
f_{CLK1}	Serial Data Clock ($\overline{WR}$ Pin)	3V	Duty cycle 50%	—	—	150	kHz
		5V		—	—	300	kHz
f_{CLK2}	Serial Data Clock ($\overline{RD}$ Pin)	3V	Duty cycle 50%	—	—	75	kHz
		5V		—	—	150	kHz
t_{CS}	Serial Interface Reset Pulse Width (Figure 3)	—	$\overline{CS}$	—	250	—	ns
t_{CLK}	$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	3.34	—	—	μs
			Read mode	6.67	—	—	
		5V	Write mode	1.67	—	—	μs
			Read mode	3.34	—	—	
t_r, t_f	Rise/Fall Time Serial Data Clock Width (Figure 1)	3V	—	—	120	—	ns
		5V					
t_{su}	Setup Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	3V	—	—	120	—	ns
		5V					
t_h	Hold Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	3V	—	—	120	—	ns
		5V					
t_{su1}	Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	3V	—	—	100	—	ns
		5V					
t_{h1}	Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	3V	—	—	100	—	ns
		5V					

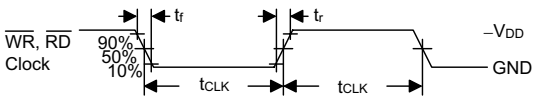


Figure 1

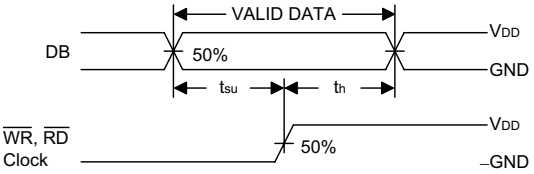


Figure 2

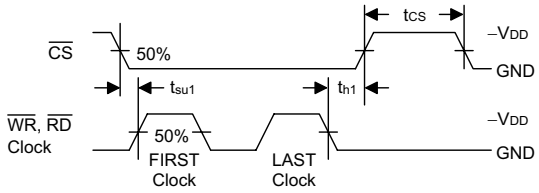


Figure 3

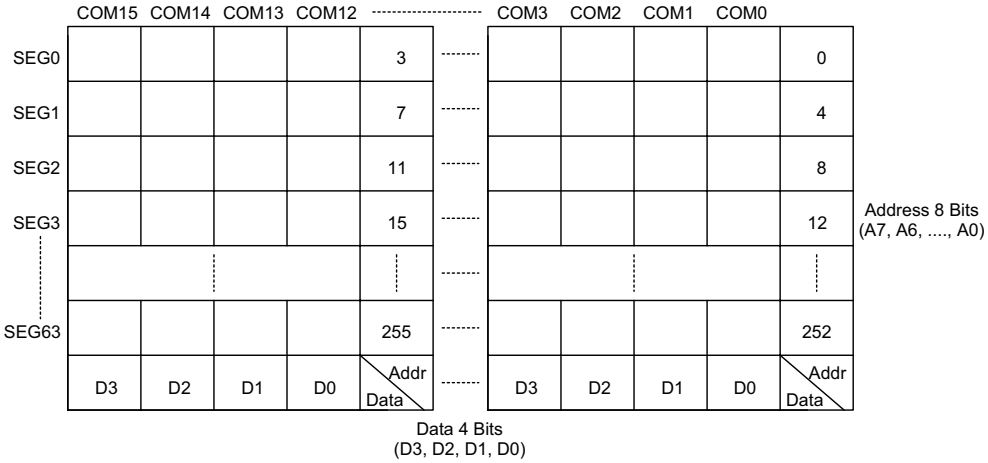
Functional Description

Display memory – RAM structure

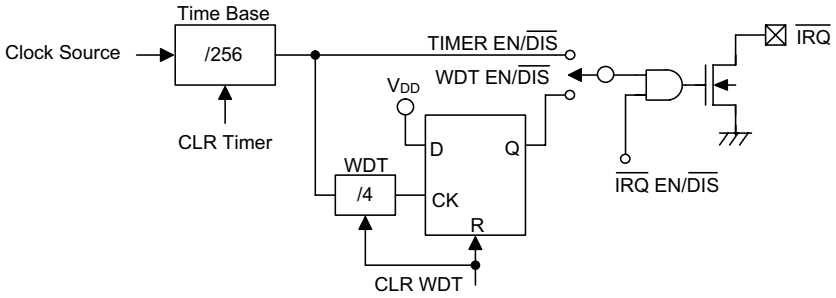
The static display RAM is organized into 256×4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.

Time base and watchdog timer – WDT

The time base generator and WDT share the same divided (/256) counter. TIMER DIS/EN/CLR, WDT DIS/EN/CLR and $\overline{IRQ}$ EN/DIS are independent from each other. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will remain at logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued.



RAM mapping



Timer and WDT configurations

If an external clock is selected as the source of system frequency, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.

Buzzer tone output

A simple tone generator is implemented in the HT16270. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$ which are used to generate a single tone.

Command format

The HT16270 can be configured by the software setting. There are two mode commands to configure the HT16270 resource and to transfer the LCD display data.

The following are the data mode ID and the command mode ID:

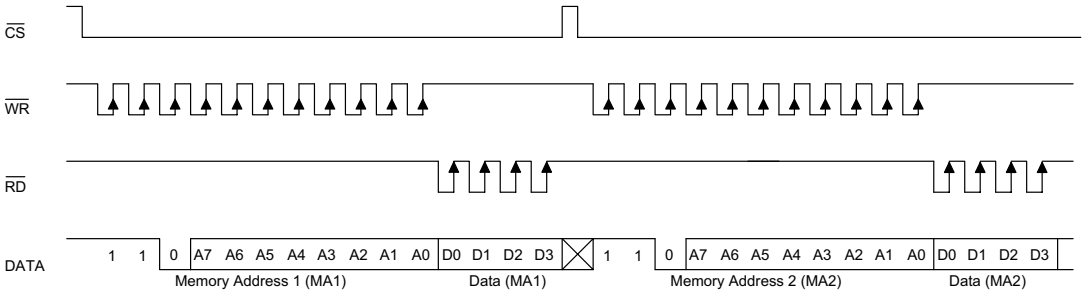
Operation	Mode	ID
READ	Data	1 1 0
WRITE	Data	1 0 1
READ-MODIFY-WRITE	Data	1 0 1
COMMAND	Command	1 0 0

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the $\overline{CS}$ pin should be set to "1" and the previous operation mode will be reset also. The $\overline{CS}$ pin returns to "0", a new operation mode ID should be issued first.

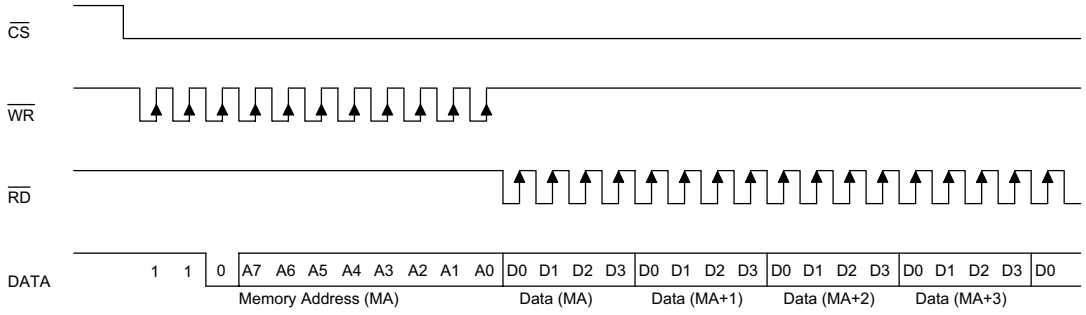
Name	Command Code	Function
TONE OFF	0000-1000-X	Turn-off tone output
TONE 4K	010X-XXXX-X	Turn-on tone output, tone frequency is 4kHz
TONE 2K	0110-XXXX-X	Turn-on tone output, tone frequency is 2kHz

Timing Diagrams

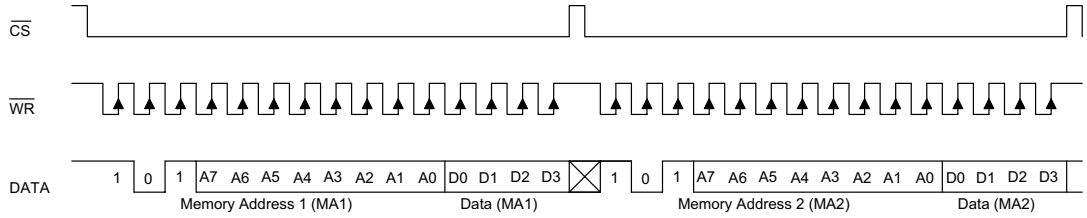
READ mode (command code : 1 1 0)



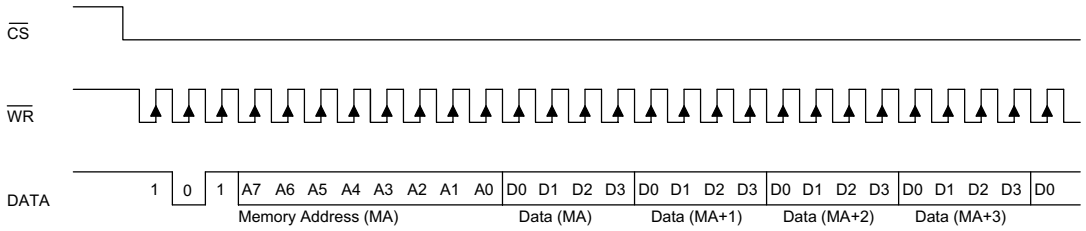
READ mode (successive address reading)



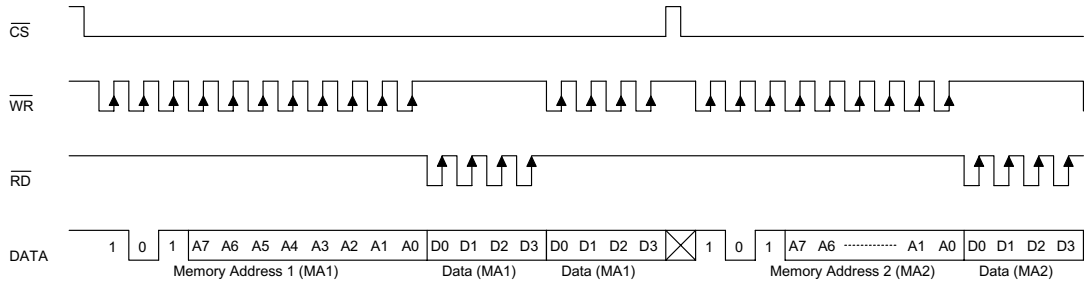
WRITE mode (command code : 1 0 1)



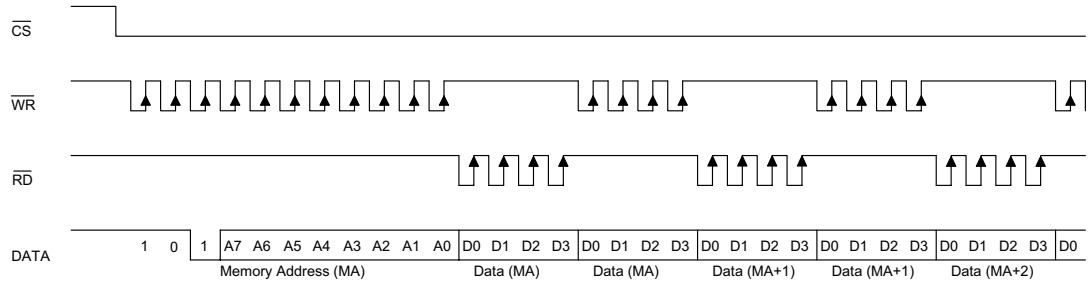
WRITE mode (successive address writing)



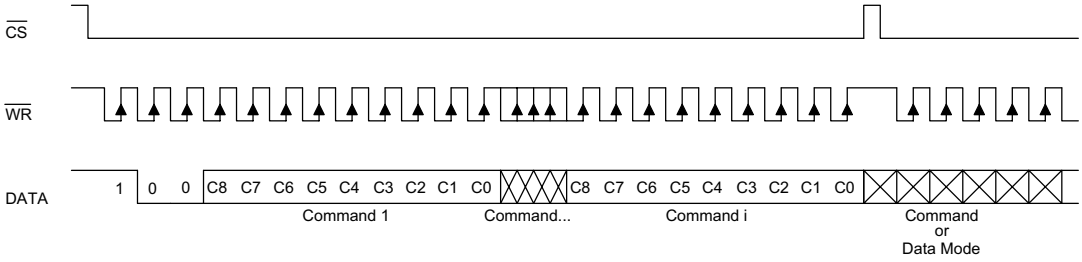
READ-MODIFY-WRITE mode (command code : 1 0 1)



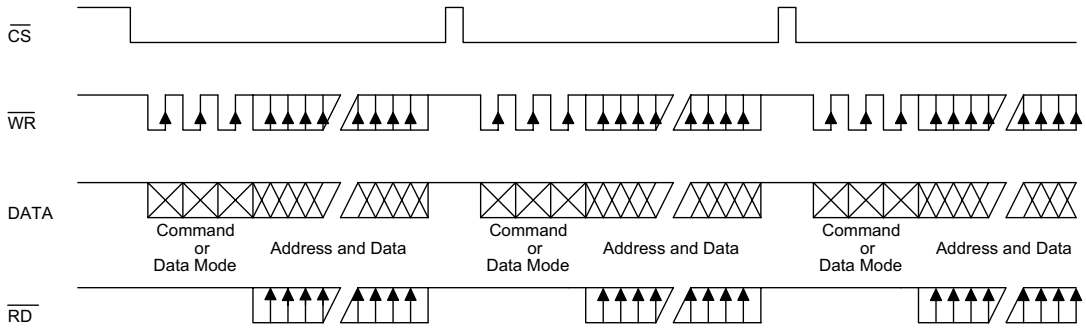
READ-MODIFY-WRITE mode (successive address accessing)



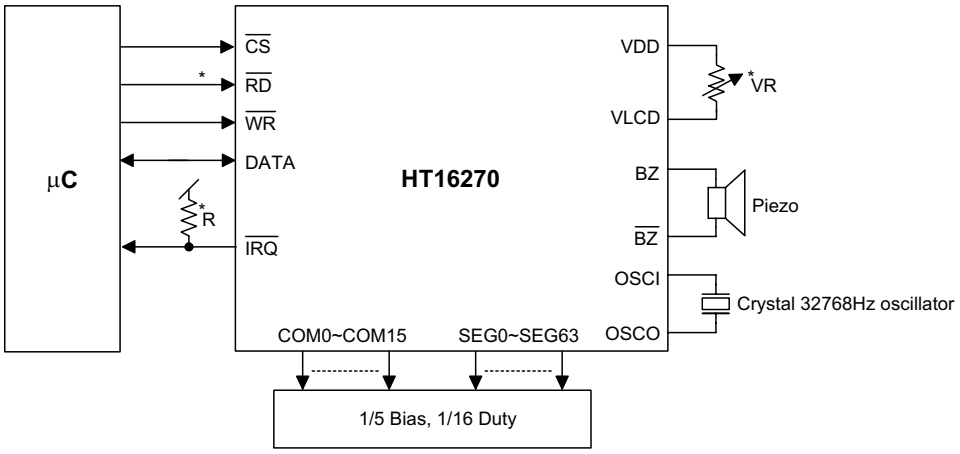
Command mode (command code : 1 0 0)



Mode (data and command mode)



Application Circuits



*Note: The connection of $\overline{IRQ}$ and $\overline{RD}$ pin can be selected depending on the requirement of the μC.
The voltage applied to V_{LCD} pin must be lower than V_{DD}.
Adjust VR to fit LCD display, at V_{DD}=5V, V_{LCD}=4V, VR=15kΩ±20%.
Adjust R (external pull-high resistance) to fit user's time base clock.

Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	**1 1 0**	A7A6A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	**1 0 1**	A7A6A5A4A3A2A1A0 D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	**1 0 1**	A7A6A5A4A3A2A1A0 D0D1D2D3	D	Read and Write data to the RAM	
SYS DIS	**1 0 0**	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	**1 0 0**	0000-0001-X	C	Turn on system oscillator	
LCD OFF	**1 0 0**	0000-0010-X	C	Turn off LCD display	Yes
LCD ON	**1 0 0**	0000-0011-X	C	Turn on LCD display	
TIMER DIS	**1 0 0**	0000-0100-X	C	Disable time base output	Yes
WDT DIS	**1 0 0**	0000-0101-X	C	Disable WDT time-out flag output	Yes
TIMER EN	**1 0 0**	0000-0110-X	C	Enable time base output	
WDT EN	**1 0 0**	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	**1 0 0**	0000-1000-X	C	Turn off tone outputs	Yes
CLR TIMER	**1 0 0**	0000-1101-X	C	Clear the contents of the time base generator	
CLR WDT	**1 0 0**	0000-1111-X	C	Clear the contents of the WDT stage	
TONE 4K	**1 0 0**	010X-XXXX-X	C	Tone frequency output: 4kHz	
TONE 2K	**1 0 0**	0110-XXXX-X	C	Tone frequency output: 2kHz	
$\overline{\text{IRQ}}$ DIS	**1 0 0**	100X-0XXX-X	C	Disable $\overline{\text{IRQ}}$ output	Yes
$\overline{\text{IRQ}}$ EN	**1 0 0**	100X-1XXX-X	C	Enable $\overline{\text{IRQ}}$ output	
F1	**1 0 0**	101X-0000-X	C	Time base clock output: 1Hz The WDT time-out flag after: 4s	
F2	**1 0 0**	101X-0001-X	C	Time base clock output: 2Hz The WDT time-out flag after: 2s	
F4	**1 0 0**	101X-0010-X	C	Time base clock output: 4Hz The WDT time-out flag after: 1s	
F8	**1 0 0**	101X-0011-X	C	Time base clock output: 8Hz The WDT time-out flag after: 1/2 s	
F16	**1 0 0**	101X-0100-X	C	Time base clock output: 16Hz The WDT time-out flag after: 1/4 s	

Name	ID	Command Code	D/C	Function	Def.
F32	**1 0 0**	101X-0101-X	C	Time base clock output: 32Hz The WDT time-out flag after: 1/8 s	
F64	**1 0 0**	101X-0110-X	C	Time base clock output: 64Hz The WDT time-out flag after: 1/16 s	
F128	**1 0 0**	101X-0111-X	C	Time base clock output: 128Hz The WDT time-out flag after: 1/32 s	Yes
TEST	**1 0 0**	1110-0000-X	C	Test mode, user don't use.	
NORMAL	**1 0 0**	1110-0011-X	C	Normal mode	Yes

Note: X : Don't care

A7~A0 : RAM address

D3~D0 : RAM data

D/C : Data/Command mode

Def. : Power on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base/WDT clock frequency can be derived from a 32.768kHz crystal oscillator or an external 32kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HT16270 after power on reset, for power on reset may fail, which in turn leads to malfunctioning of the HT16270.

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