



## Frequency Generator for CD-ROM Systems

### General Description

The ICS9120-48 is a high performance frequency generator designed to support digital compact disk drive systems. It offers all clock frequencies required for the servo and decoder sections of these devices. These frequencies are synthesized from a single 16.9344 MHz on-chip oscillator.

High accuracy, low jitter PLLs meet the 150 ppm frequency tolerance required by these systems. Fast output clock edge rates minimize board induced jitter.

Unlike competitive devices, the ICS9120-48 operates over the entire 3.0-5.5V range.

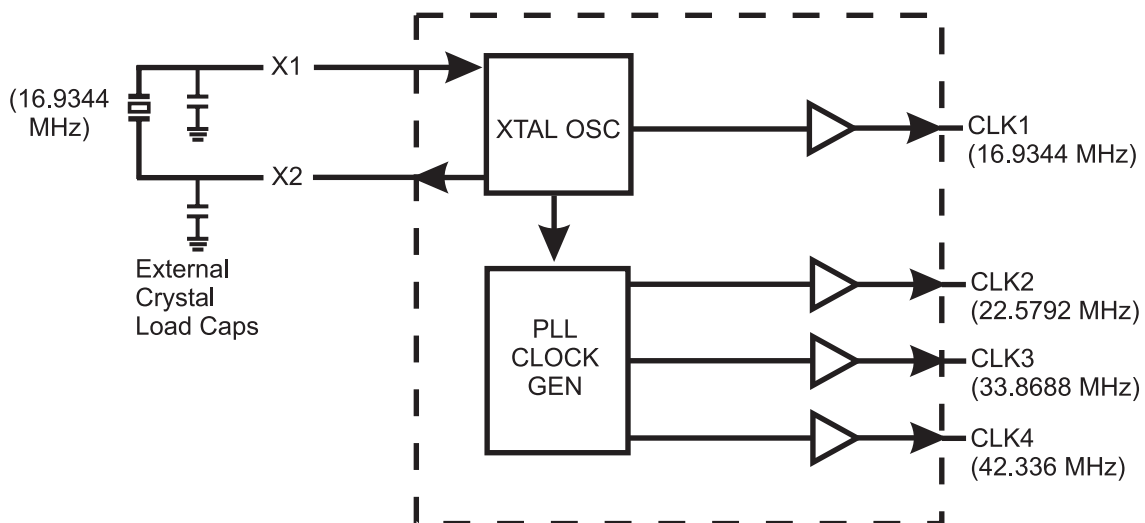
### Features

- Generates the output clock frequencies required by CD-ROM drive systems
- Single 16.9344 MHz crystal or system clock reference
- 100ps one sigma jitter
- Output rise/fall times less than 2.0ns (at 5V VDD)
- On-chip loop filter components
- 3.0V-5.5V supply range
- 150 ppm output frequency accuracy
- 8-pin, 150-mil SOIC

### Applications

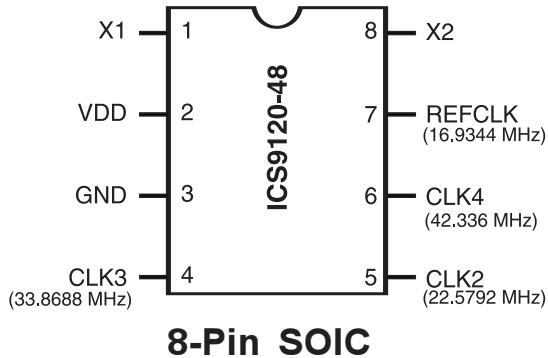
- Specifically designed to support CD-ROM drive requirements of multimedia applications

### Block Diagram





## Pin Configuration



## External Components/Crystal Selection

The ICS9120-48 incorporates a crystal oscillator circuit designed to provide 50% duty cycle over a range of operating conditions, including the addition of external crystal load capacitors to pins X1 and X2. A parallel resonant 16.9344 MHz, 12pF load crystal is recommended. A series resonant crystal or a parallel resonant crystal specifying a different load can be used, but either will result in frequencies which are slightly (up to 0.06%) different from the ideal.

The crystal load capacitance can be increased by adding a capacitor to each of the X1 and X2 pins and ground. This enables the use of a crystal specifying a load greater than 12pF without changing the output frequency.

Duty cycle is also maintained when using an external clock source (connected to X1, X2 left unconnected) as long as the external clock has good duty cycle.

## Pin Descriptions for ICS9120-48

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	X1	Input	Crystal or external clock source. Has feedback bias for crystal.
2	VDD	Power	+Power supply input.
3	GND	Power	Ground return for Pin 2.
4	CLK3	Output	33.8688 MHz target output clock.
5	CLK2	Output	22.5792 MHz target output clock.
6	CLK4	Output	42.336 MHz target output clock.
7	CLK1	Output	16.9344 MHz reference clock buffered output.
8	X2	Output	Crystal output drive (leave this pin unconnected when using an external clock).



## Absolute Maximum Ratings

AVDD, VDD referenced to GND ..... 7V  
 Operating temperature under bias ..... 0°C to +70°C  
 Storage temperature ..... -65°C to +150°C  
 Voltage on I/O pins referenced to GND ..... GND -0.5V to VDD +0.5V  
 Power dissipation ..... 0.5 Watts

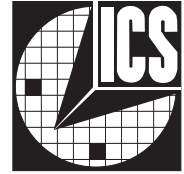
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Electrical Characteristics at 5 V

V<sub>DD</sub> = +4.5 to +5.5 V, T<sub>A</sub> = 0 to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V <sub>IL</sub>		-	-	0.8	V
Input High Voltage	V <sub>IH</sub>		2.0	-	-	V
Input Low Current	I <sub>IL</sub>	V <sub>IN</sub> =0V	-18.0	-8.3	-	µA
Input High Current	I <sub>IH</sub>	V <sub>IN</sub> =V <sub>DD</sub>	-	-	5.0	µA
Output Low Voltage	V <sub>OL</sub> *	I <sub>OL</sub> =+10mA	-	0.15	0.4	V
Output High Voltage	V <sub>OH</sub> *	I <sub>OH</sub> =-30mA	2.4	3.7	-	V
Output Low Current	I <sub>OL</sub> *	V <sub>OL</sub> =0.8V	25.0	45.0	-	mA
Output High Current	I <sub>OH</sub> *	V <sub>OH</sub> =2.4V	-	-53.0	-35.0	mA
Supply Current	I <sub>DD</sub> *	Unloaded	-	30.0	70.0	mA
Pull-up Resistor Value	R <sub>pu</sub> *		-	400.0	800.0	k ohm
AC Characteristics						
Rise Time	T <sub>r</sub> *	15pF load 0.8 to 2.0V	-	0.8	2.0	ns
Fall Time	T <sub>f</sub> *	15pF load 2.0 to 0.8V	-	0.6	1.5	ns
Rise Time	T <sub>r</sub> *	15pF load 20% to 80%	-	1.7	2.5	ns
Fall Time	T <sub>f</sub> *	15pF load 80% to 20%	-	1.1	2.0	ns
Duty Cycle	D <sub>t</sub> *	15pF load @ 50% of V <sub>DD</sub> ; Except REFCLK	45.0	50.0	55.0	%
Duty Cycle	D <sub>t</sub> *	15pF load @ 50% of V <sub>DD</sub> ; REFCLK only	40.0	55.0	60.0	%
Jitter, One Sigma	T <sub>jis</sub> *	For all frequencies except REFCLK	-	130.0	180.0	ps
Jitter, Absolute	T <sub>jab</sub> *	For all frequencies except REFCLK	-400.0	350.0	400.0	ps
Jitter, One Sigma	T <sub>jis</sub> *	REFCLK only	-	150.0	200.0	ps
Jitter Absolute	T <sub>jab</sub> *	REFCLK only	-700.0	400.0	700.0	ns
Input Frequency Range	F <sub>i</sub> *		11.0	14.0	17.0	MHz
Output Frequency Range	F <sub>o</sub> *		14.0	-	52.0	MHz
Power-up Time	T <sub>pu</sub> *	0 to 40.3 MHz	-	5.5	12.0	ms
Crystal Input Capacitance	C <sub>inx</sub> *	X1 (Pin 1), X2 (Pin 8)	-	5	-	pF

\*Parameter is guaranteed by design and characterization. Not 100% tested in production.

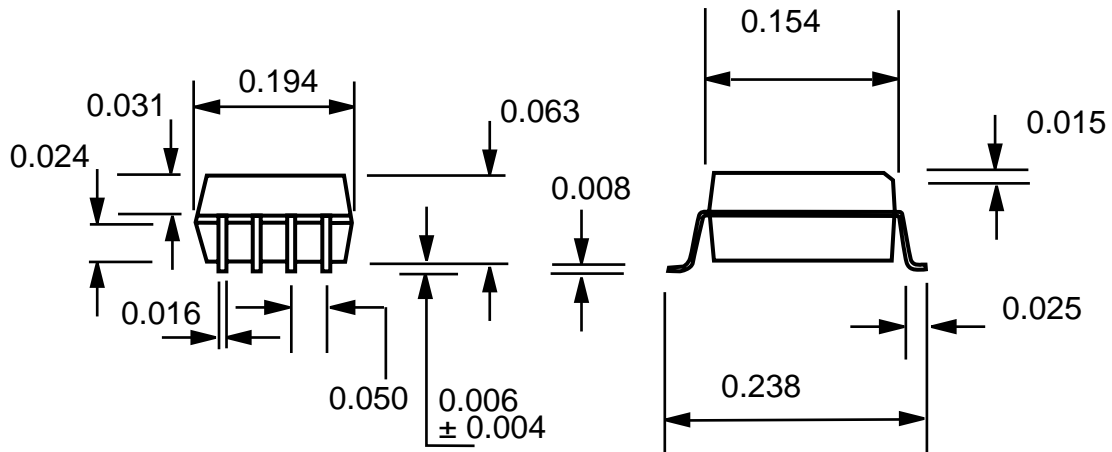


## Electrical Characteristics at 3.3 V

$V_{DD} = +3.0$  to  $+3.7V$ ,  $T_A = 0^{\circ}C$ - $70^{\circ}C$  unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	$V_{IL}$		-	-	$0.2V_{DD}$	V
Input High Voltage	$V_{IH}$		$0.7V_{DD}$	-	-	V
Input Low Current	$I_{IL}$	$V_{IN}=0V$	-8.0	-3.6	-	$\mu A$
Input High Current	$I_{IH}$	$V_{IN}=V_{DD}$	-	-	5.0	$\mu A$
Output Low Voltage	$V_{OL}^*$	$I_{OL}=6.0mA$	-	$0.05V_{DD}$	0.1	V
Output High Voltage	$V_{OH}^*$	$I_{OH}=4.0mA$	$0.85V_{DD}$	$0.94V_{DD}$	-	V
Output Low Current	$I_{OL}^*$	$V_{OL}=0.2V_{DD}$	15.0	24.0	-	mA
Output High Current	$I_{OH}^*$	$V_{OH}=0.7V_{DD}$	-	-13.0	-8.0	mA
Supply Current	$I_{DD}^*$	Unloaded	-	23.0	45.0	mA
AC Characteristics						
Rise Time	$T_r^*$	15pF load 0.8 to 2.0V	-	2.2	3.5	ns
Fall Time	$T_f^*$	15pF load 2.0 to 0.8V	-	1.2	2.0	ns
Rise Time	$T_r^*$	15pF load 20% to 80%	-	2.5	3.5	ns
Fall Time	$T_f^*$	15pF load 80% to 20%	-	1.4	2.5	ns
Duty Cycle	$D_t^*$	15pF load @ 50% of $V_{DD}$ ; Except REFCLK	45.0	50.0	55.0	%
Duty Cycle	$D_t^*$	15pF load @ 50% of $V_{DD}$ ; REFCLK only	40.0	45.0	65.0	%
Jitter, One Sigma	$T_{jis}^*$	For all frequencies except REFCLK	-	130.0	200	ps
Jitter Absolute	$T_{jab}^*$	For all frequencies except REFCLK	-500.0	400.0	500.0	ps
Jitter, One Sigma	$T_{jis}^*$	REFCLK only	-	170.0	250.0	ps
Jitter, Absolute	$T_{jab}^*$	REFCLK only	-500.0	300.0	500.0	ns
Input Frequency Range	$F_i^*$		11.0	14.3	17.0	MHz
Output Frequency Range	$F_o^*$		14.0	-	42.0	MHz
Power-up Time	$T_{pu}^*$	0 to 33.8 MHz	-	5.5	12.0	ms
Crystal Input Capacitance	$C_{inx}^*$	X1 (Pin 1), X2 (Pin 8)	-	5	-	pF

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**8-Pin SOIC Package**

### Ordering Information

ICS9120M-48

Example:

**ICS XXXX M-PPP**

