Integrated Circuit Systems, Inc.

ICS9148-47

Pentium/Pro™ System Clock Chip

General Description

The **ICS9148-47** is part of a reduced pin count two-chip clock solution for designs using an Intel BX style chipset. Companion SDRAM buffers are ICS9179-11 and –12.

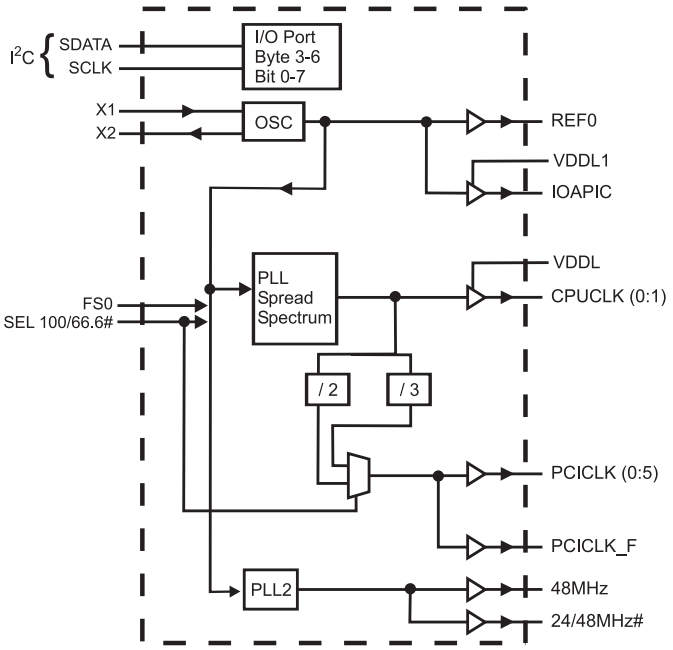
There are two PLLs, with the first PLL capable of spread spectrum operation. Spread spectrum typically reduces system EMI by 8-10dB. The second PLL provides support for USB (48MHz) and 24MHz requirements. CPU frequencies up to 100MHz are supported.

The I^2C interface allows stop clock programming, frequency selection, and spread spectrum operation to be programmed. Clock outputs include two CPU (2.5V or 3.3V), seven PCI (3.3V), one REF (3.3V), one IOAPIC (2.5V or 3.3V), one 48MHz, and one selectable 48/24MHz.

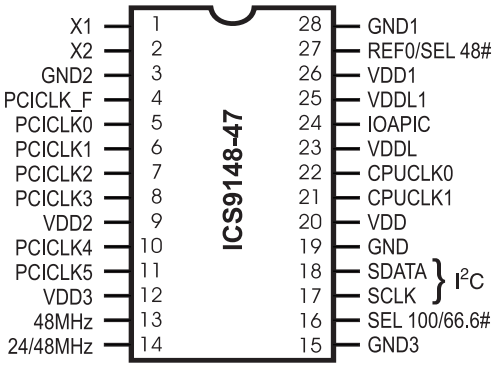
Features

- Generates system clocks for CPU, PCI, IOAPIC , 14.314 MHz, 48 and 24MHz.
- Supports single or dual processor systems
- Skew from CPU (earlier) to PCI clock 1 to 4ns
- Separate 2.5V and 3.3V supply pins
- 2.5V outputs: CPU, IOAPIC
- 3.3V outputs: PCI, REF
- No power supply sequence requirements
- 28 pin SOIC
- Spread Sectrum operation optional for PLL1
- CPU frequencies to 100MHz are supported.

Block Diagram



Pin Configuration



28 pin SOIC

Power Groups

VDD = Supply for PLL core
VDD1 = REF0, X1, X2
VDD2 = PCICLK_F, PCICLK (0:5)
VDD3 = 48MHz
VDDL = CPUCLK (0:1)
VDDL1=IOAPIC

Ground Groups

GND = Ground Source Core
GND1 = REF0, X1, X2
GND2 = PCICLK_F, PCICLK (0:5)
GND3=48MHz
GNDL = CPUCLK (0:1)

Pentium is a trademark on Intel Corporation.

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	X1	IN	XTAL_IN 14.318MHz Crystal input, has internal 33pF load cap and feed back resistor from X2
2	X2	OUT	XTAL_OUT Crystal output, has internal load cap 33pF
3	GND2	PWR	Ground for PCI outputs
4	PCICLK_F	OUT	Free Running PCI output
5, 6, 7, 8, 10, 11	PCICLK (0:5)	OUT	PCI clock outputs. TTL compatible 3.3V
6, 9	VDD2	PWR	Power for PCICLK outputs, nominally 3.3V
12	VDD3	PWR	Poer for 48MHz
13	48MHz	OUT	Fixed CLK output @ 48MHz
14	24/48MHz	OUT	Fixed CLK output; 24MHz if pin 27 =1 at power up, 48MHz if pin 27=0 at power up.
15	GND3	PWR	Ground for 48MHz
16	SEL100/66.6#	IN	Select pin for enabling 100MHz or 66.6MHz H=100MHz, L=66.6MHz (PCI always synchronous 33.3MHz)
17	SCLK	IN	Clock input for I^2C input
18	SDATA	IN	Data input for I^2C input
19	GND	PWR	Ground for CPUCLK (0:1)
20	VDD	PWR	Power for PLL core
21, 22	CPUCLK (1:0)	OUT	CPU and Host clock outputs nominally 2.5V
23	VDDL	PWR	Power for CPU outputs, nominally 2.5V
24	IOAPIC	OUT	IOAPIC clock output 14.318MHz.
25	VDDL	PWR	Power for IOAPIC
26	VDD1	PWR	Power for REF outputs.
27	REF0/SEL 48#	OUT/IN	14.318MHz clock output/Latched input at power up. When low, pin 14 is 48MHz.
28	GND1	PWR	Ground for REF outputs, X1, X2.

General I^2C serial interface information

The information in this section assumes familiarity with I^2C programming. For more information, contact ICS for an I^2C programming application note.

How to Write:

- Send the address $D2_{(H)}$.
- Send two additional dummy bytes, a command code and byte count.
- Send the desired number of data bytes.

See the diagram below:

Clock Generator Address (7 bits)	ACK	+ 8 bits dummy command code	ACK	+ 8 bits dummy Byte count	ACK	Data Byte 1	ACK	Data Byte N	ACK
A(6:0) & R/W#									
$D2_{(H)}$									

Note that the acknowledge bit is sent by the clock chip, and pulls the data line low. There is no minimum of data bytes that must be sent.

How to Read:

- Send the address $D3_{(H)}$.
- Send the byte count in binary coded decimal
- Read back the desired number of data bytes

See the diagram below:

Clock Generator Address (7 bits)	ACK	Byte Count	ACK	Data Byte 1	ACK	Data Byte N
A(6:0) & R/W#						
D3(H)						

The following specifications should be observed:
1. Operating voltage for I^2C pins is 3.3V
2. Maximum data transfer rate (SCLK) is 100K bits/sec.

Serial Bitmap

Byte 3: Functionality & Frequency Select & Spread Slect Register

Bit	Description				PWD
7	(Reserved)				0
6:4	Bit 654	CPU	PCI	Spread Percentage	
	000	68.5	34.25	±0.5% Center	0
	001	75.0	37.5	±0.5% Center	
	010	83.3	41.6	±0.5% Center	
	011	66.6	33.3	±0.5% Center	
	100	103	34.3	±0.5% Center	
	101	112	37.3	±0.5% Center	
	110	133.3	44.43	±0.5% Center	
	111	100	33.33	±0.5% Center	
3	0 - Frequency is selected by hardware select SEL100/66.6# 1 - Frequency is selected by 6:4 above				0
2	(Reserved)				
10	00 - Normal operation 01 - Test mode 10 - Spread sprectrum ON 11 - Tristate all outputs				00

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 4:

Bit	Pin#	Pin Name	PWD	Description	
				Bit Value = 0	Bit Value = 1
7	-	-	-	(Reserved)	(Reserved)
6	-	-	-	(Reserved)	(Reserved)
5	-	-	-	(Reserved)	(Reserved)
4	-	-	-	(Reserved)	(Reserved)
3	-	-	-	(Reserved)	(Reserved)
2	21	CPUCLK1	1	Disabled (low)	Enabled
1	-	-	0	(Reserved)	(Reserved)
0	22	CPUCLK0	1	(Disabled) (low)	Enabled

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Note: PWD = Power-Up Default

Byte 5:

Bit	Pin#	Pin Name	PWD	Description	
				Bit Value = 0	Bit Value = 1
7	4	PCICLK_F	1	Disabled (low)	Enabled
6	11	PCICLK5	1	Disabled (low)	Enabled
5	10	PCICLK4	1	Disabled (low)	Enabled
4	-	-	0	(Reserved)	(Reserved)
3	8	PCICLK3	1	Disabled (low)	Enabled
2	7	PCICLK2	1	Disabled (low)	Enabled
1	6	PCICLK1	1	Disabled (low)	Enabled
0	5	PCICLK0	1	Disabled (low)	Enabled

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 6:

Bit	Pin#	Pin Name	PWD	Description	
				Bit Value = 0	Bit Value = 1
7	-	-	0	(Reserved)	(Reserved)
6	-	-	0	(Reserved)	(Reserved)
5	24	IOAPIC	1	Disabled (low)	Enabled
4	-	-	0	(Reserved)	(Reserved)
3	-	-	0	(Reserved)	(Reserved)
2	-	-	0	(Reserved)	(Reserved)
1	27	REF0	1	(Disabled) (low)	Enabled
0	27	REF0	1	(Disabled) (low)	Enabled

Notes:
1 = Enabled; 0 = Disabled, outputs held low

For pin 27, there are 2 output stages together for 1 pin. These 2 latches must be both 0 or 1 simultaneously or there will be a short to ground if one is disabled and the other is running.

Absolute Maximum Ratings

Supply Voltage . . . . . 7.0 V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}		0.1	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating Supply Current	$I_{DD3.3OP66}$	C_L = 0 pF; Select @ 66MHz		60	170	mA
	$I_{DD3.3OP100}$	C_L = 0 pF; Select @ 100MHz		66	170	
Power Down Supply Current	$I_{DD3.3PD}$	C_L = 0 pF; With input address to Vdd or GND		3	650	µA
Input frequency	F_i	V_{DD} = 3.3 V;		14.318		MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	ms
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.		5		ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$T_{AGP-PCI1}$	V_T = 1.5 V;	1	3.5	4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5OP66}$	C_L = 0 pF; Select @ 66.8 MHz		16	72	mA
	$I_{DD2.5OP100}$	C_L = 0 pF; Select @ 100 MHz		23	100	mA
Power Down Supply Current	$I_{DD2.5PD}$	C_L = 0 pF; With input address to Vdd or GND		10	100	µA
Skew[1]	$t_{CPU-AGP}$		0	0.5	1	ns
	$t_{CPU-PCI2}$	V_T = 1.5 V; V_{TL} = 1.25 V	1	2.6	4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2	2.3		V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA		0.2	0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V		-41	-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19	37		mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.25	1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1	1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	48	55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V		30	175	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$[1]	V_T = 1.25 V		150	250	ps
Jitter, One Sigma	t_{j1s2B}[1]	V_T = 1.25 V		40	150	ps
Jitter, Absolute	t_{jabs2B}[1]	V_T = 1.25 V	-250	140	+250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.4	3.1		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.1	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-62	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	16	57		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.5	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.1	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	50	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V		140	500	ps
Jitter, One Sigma[1]	t_{j1s1}	V_T = 1.5 V		17	150	ps
Jitter, Absolute[1]	t_{jabs1}	V_T = 1.5 V	-500	70	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH4B}	I_{OH} = -18 mA	2	2.2		V
Output Low Voltage	V_{OL4B}	I_{OL} = 18 mA		0.33	0.4	V
Output High Current	I_{OH4B}	V_{OH} = 1.7 V		-41	-28	mA
Output Low Current	I_{OL4B}	V_{OL} = 0.7 V	29	37		mA
Rise Time[1]	T_{r4B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.3	1.6	ns
Fall Time[1]	T_{f4B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.1	1.6	ns
Duty Cycle[1]	D_{t4B}	V_T = 1.25 V	45	54	55	%
Skew[1]	t_{sk4B}[1]	V_T = 1.25 V		60	250	ps
Jitter, One Sigma[1]	T_{j1s4B}	V_T = 1.25 V		1	3	%
Jitter, Absolute[1]	T_{jabs4B}	V_T = 1.25 V	-5		5	%

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 48, 24 MHz

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.6	3		V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA		0.14	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-44	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	42		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.2	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.2	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	52	55	%
Jitter, One Sigma[1]	t_{j1s5}	V_T = 1.5 V		1	3	%
Jitter, Absolute[1]	t_{jabs5}	V_T = 1.5 V		3	5	%

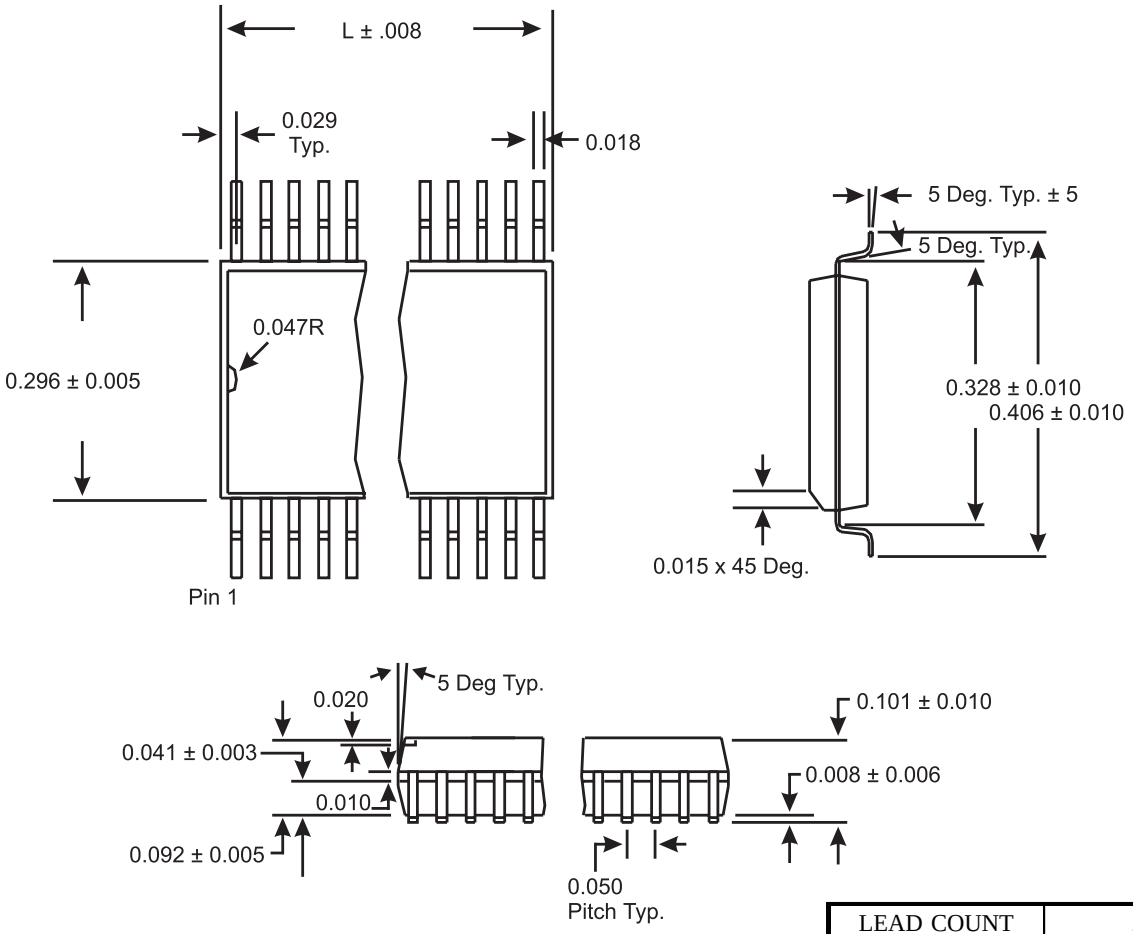
[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.6	3.1		V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA		0.17	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-44	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	29	42		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.4	2	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.1	2	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	47	54	57	%
Jitter, One Sigma[1]	t_{j1s5}	V_T = 1.5 V		1	3	%
Jitter, Absolute[1]	t_{jabs5}	V_T = 1.5 V		3	5	%

[1]Guaranteed by design, not 100% tested in production.



LEAD COUNT	28L
DIMENSION L	0.704

SOIC Package

Ordering Information

ICS9148M-47

Example:

ICS XXXX M - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device