

# Pentium/Pro™ System Clock Chip

## General Description

The ICS9148-60 is part of a reduced pin count two-chip clock solution for designs using an Intel BX style chipset. Companion SDRAM buffers are ICS9179-11 and -12.

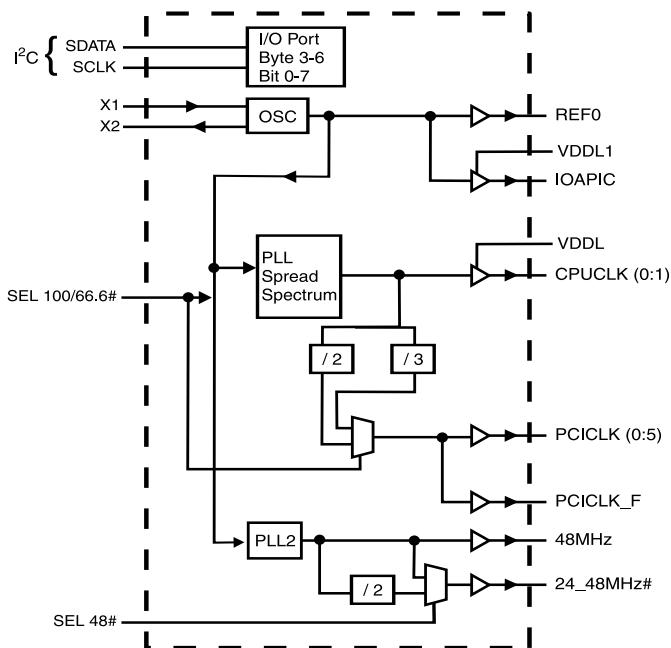
There are two PLLs, with the first PLL capable of spread spectrum operation. Spread spectrum typically reduces system EMI by 8-10dB. The second PLL provides support for USB (48MHz) and 24MHz requirements. CPU frequencies up to 100MHz are supported.

The I<sup>2</sup>C interface allows stop clock programming, frequency selection, and spread spectrum operation to be programmed. Clock outputs include two CPU (2.5V or 3.3V), seven PCI (3.3V), one REF (3.3V), one IOAPIC (2.5V or 3.3V), one 48MHz, and one selectable 48\_24MHz.

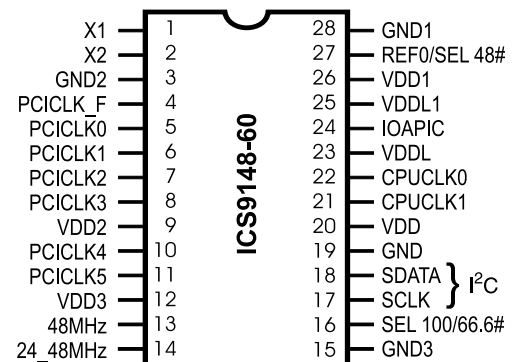
## Features

- Generates system clocks for CPU, PCI, IOAPIC, 14.314 MHz, 48 and 24MHz.
- Supports single or dual processor systems
- Skew from CPU (earlier) to PCI clock 1 to 4ns
- Separate 2.5V and 3.3V supply pins
- 2.5V outputs: CPU, IOAPIC
- 3.3V outputs: PCI, REF
- No power supply sequence requirements
- 28 pin SOIC and SSOP
- Spread Spectrum operation optional for PLL1
- CPU frequencies to 100MHz are supported.

## Block Diagram



## Pin Configuration



## 28 pin SOIC and SSOP

## Power Groups

VDD = Supply for PLL core  
 VDD1 = REF0, X1, X2  
 VDD2 = PCICLK\_F, PCICLK (0:5)  
 VDD3 = 48MHz  
 VDDL = CPUCLK (0:1)  
 VDDL1 = IOAPIC

## Ground Groups

GND = Ground Source Core  
 GND1 = REF0, X1, X2  
 GND2 = PCICLK\_F, PCICLK (0:5)  
 GND3 = 48MHz  
 GNDL = CPUCLK (0:1)

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## Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	X1	IN	XTAL_IN 14.318MHz Crystal input, has internal 33pF load cap and feed back resistor from X2
2	X2	OUT	XTAL_OUT Crystal output, has internal load cap 33pF
3	GND2	PWR	Ground for PCI outputs
4	PCICLK_F	OUT	Free Running PCI output
5, 6, 7, 8, 10, 11	PCICLK (0:5)	OUT	PCI clock outputs. TTL compatible 3.3V
6, 9	VDD2	PWR	Power for PCICLK outputs, nominally 3.3V
12	VDD3	PWR	Power for 48MHz
13	48MHz	OUT	Fixed CLK output @ 48MHz
14	24_48MHz	OUT	Fixed CLK output; 24MHz if pin 27 =1 at power up, 48MHz if pin 27=0 at power up.
15	GND3	PWR	Ground for 48MHz
16	SEL100/66.6#	IN	Select pin for enabling 100MHz or 66.6MHz H=100MHz, L=66.6MHz (PCI always synchronous 33.3MHz)
17	SCLK	IN	Clock input for I <sup>2</sup> C input
18	SDATA	IN	Data input for I <sup>2</sup> C input
19	GND	PWR	Ground for CPUCLK (0:1)
20	VDD	PWR	Power for PLL core
21, 22	CPUCLK (1:0)	OUT	CPU and Host clock outputs nominally 2.5V
23	VDDL	PWR	Power for CPU outputs, nominally 2.5V
24	IOAPIC	OUT	IOAPIC clock output 14.318MHz.
25	VDDL	PWR	Power for IOAPIC
26	VDD1	PWR	Power for REF outputs.
27	REF0	OUT	14.318MHz clock .
	SEL48#	IN	Output/Latched input at power up. When low, pin 14 is 48MHz
28	GND1	PWR	Ground for REF outputs, X1, X2.



## General I<sup>2</sup>C serial interface information

The information in this section assumes familiarity with I<sup>2</sup>C programming.  
For more information, contact ICS for an I<sup>2</sup>C programming application note.

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will **acknowledge** each byte *one at a time*.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D2 <sub>(H)</sub>	
	<b>ACK</b>
Dummy Command Code	
	<b>ACK</b>
Dummy Byte Count	
	<b>ACK</b>
Byte 0	
	<b>ACK</b>
Byte 1	
	<b>ACK</b>
Byte 2	
	<b>ACK</b>
Byte 3	
	<b>ACK</b>
Byte 4	
	<b>ACK</b>
Byte 5	
	<b>ACK</b>
Byte 6	
	<b>ACK</b>
Stop Bit	

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3<sub>(H)</sub>
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 6**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D3 <sub>(H)</sub>	
	<b>ACK</b>
	<b>Byte Count</b>
ACK	
	<b>Byte 0</b>
ACK	
	<b>Byte 1</b>
ACK	
	<b>Byte 2</b>
ACK	
	<b>Byte 3</b>
ACK	
	<b>Byte 4</b>
ACK	
	<b>Byte 5</b>
ACK	
	<b>Byte 6</b>
ACK	
Stop Bit	

### Notes:

1. The ICS clock generator is a slave/receiver, I<sup>2</sup>C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I<sup>2</sup>C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



## Serial Bitmap

### Byte 3: Functionality & Frequency Select & Spread Slect Register

Bit	Description			PWD
7	0: Center Spread ( $\pm 0.25$ ) 1: Down Spread (0 to $-0.6\%$ )			0
6:4	Bit 654	CPU	PCI	0
	000	68.5	34.25	
	001	75.0	37.5	
	010	83.3	41.6	
	011	66.6	33.3	
	100	103	34.3	
	101	112	37.3	
	110	133.3	44.43	
	111	100	33.33	
3	0 - Frequency is selected by hardware select SEL100/66.6# 1 - Frequency is selected by 6:4 above			0
2	(Reserved)			
10	00 - Normal operation 01 - Test mode 10 - Spread spectrum ON 11 - Tristate all outputs			00

Notes: 1 = Enabled; 0 = Disabled, outputs held low

### Byte 4:

Bit	Pin#	Pin Name	PWD	Description	
				Bit Value = 0	Bit Value = 1
7	-	-	-	(Reserved)	(Reserved)
6	-	-	-	(Reserved)	(Reserved)
5	-	-	-	(Reserved)	(Reserved)
4	-	-	-	(Reserved)	(Reserved)
3	-	-	-	(Reserved)	(Reserved)
2	21	CPUCLK1	1	Disabled (low)	Enabled
1	-	-	0	(Reserved)	(Reserved)
0	22	CPUCLK0	1	(Disabled) (low)	Enabled

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Note: PWD = Power-Up Default

### Byte 5:

Bit	Pin#	Pin Name	PWD	Description	
				Bit Value = 0	Bit Value = 1
7	4	PCICLK_F	1	Disabled (low)	Enabled
6	11	PCICLK5	1	Disabled (low)	Enabled
5	10	PCICLK4	1	Disabled (low)	Enabled
4	-	-	0	(Reserved)	(Reserved)
3	8	PCICLK3	1	Disabled (low)	Enabled
2	7	PCICLK2	1	Disabled (low)	Enabled
1	6	PCICLK1	1	Disabled (low)	Enabled
0	5	PCICLK0	1	Disabled (low)	Enabled

Notes: 1 = Enabled; 0 = Disabled, outputs held low

### Byte 6:

Bit	Pin#	Pin Name	PWD	Description	
				Bit Value = 0	Bit Value = 1
7	-	-	0	(Reserved)	(Reserved)
6	-	-	0	(Reserved)	(Reserved)
5	24	IOAPIC	1	Disabled (low)	Enabled
4	-	-	0	(Reserved)	(Reserved)
3	-	-	0	(Reserved)	(Reserved)
2	-	-	0	(Reserved)	(Reserved)
1	27	REF0	1	(Disabled) (low)	Enabled
0	27	REF0	1	(Disabled) (low)	Enabled

Notes:

1 = Enabled; 0 = Disabled, outputs held low

For pin 27, there are 2 output stages together for 1 pin. These 2 latches must be both 0 or 1 simultaneously or there will be a short to ground if one is disabled and the other is running.



### Absolute Maximum Ratings

Supply Voltage ..... 7.0 V  
 Logic Inputs ..... GND–0.5 V to V<sub>DD</sub>+0.5 V  
 Ambient Operating Temperature ..... 0°C to +70°C  
 Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Electrical Characteristics - Input/Supply/Common Output Parameters

T<sub>A</sub> = 0 - 70C; Supply Voltage V<sub>DD</sub> = V<sub>DDL</sub> = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V <sub>IH</sub>		2		V <sub>DD</sub> +0.3	V
Input Low Voltage	V <sub>IL</sub>		V <sub>SS</sub> -0.3		0.8	V
Input High Current	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>DD</sub>		0.1	5	μA
Input Low Current	I <sub>IL1</sub>	V <sub>IN</sub> = 0 V; Inputs with no pull-up resistors	-5	2.0		μA
Input Low Current	I <sub>IL2</sub>	V <sub>IN</sub> = 0 V; Inputs with pull-up resistors	-200	-100		μA
Operating Supply Current	I <sub>DD3.3OP66</sub>	C <sub>L</sub> = 0 pF; Select @ 66MHz		60	170	mA
	I <sub>DD3.3OP100</sub>	C <sub>L</sub> = 0 pF; Select @ 100MHz		66	170	mA
Power Down Supply Current	I <sub>DD3.3PD</sub>	C <sub>L</sub> = 0 pF; With input address to V <sub>DD</sub> or GND		3	650	μA
Input frequency	F <sub>i</sub>	V <sub>DD</sub> = 3.3 V;		14.318		MHz
Input Capacitance <sup>1</sup>	C <sub>IN</sub>	Logic Inputs			5	pF
	C <sub>INX</sub>	X1 & X2 pins	27	36	45	pF
Transition Time <sup>1</sup>	T <sub>trans</sub>	To 1st crossing of target Freq.			3	ms
Settling Time <sup>1</sup>	T <sub>s</sub>	From 1st crossing to 1% target Freq.		5		ms
Clk Stabilization <sup>1</sup>	T <sub>STAB</sub>	From V <sub>DD</sub> = 3.3 V to 1% target Freq.			3	ms
Skew <sup>1</sup>	T <sub>AGP-PCI1</sub>	V <sub>T</sub> = 1.5 V;	1	3.5	4	ns

<sup>1</sup>Guaranteed by design, not 100% tested in production.

### Electrical Characteristics - Input/Supply/Common Output Parameters

T<sub>A</sub> = 0 - 70C; Supply Voltage V<sub>DD</sub> = 3.3 V +/-5%, V<sub>DDL</sub> = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	I <sub>DD2.5OP66</sub>	C <sub>L</sub> = 0 pF; Select @ 66.8 MHz		16	72	mA
	I <sub>DD2.5OP100</sub>	C <sub>L</sub> = 0 pF; Select @ 100 MHz		23	100	mA
Power Down Supply Current	I <sub>DD2.5PD</sub>	C <sub>L</sub> = 0 pF; With input address to V <sub>DD</sub> or GND		10	100	μA
Skew <sup>1</sup>	t <sub>CPU-AGP</sub>		0	0.5	1	ns
	t <sub>CPU-PCI2</sub>	V <sub>T</sub> = 1.5 V; V <sub>TL</sub> = 1.25 V	1	2.6	4	ns

<sup>1</sup>Guaranteed by design, not 100% tested in production.



## Electrical Characteristics - CPUCLK

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3 \text{ V} \pm 5\%$ ,  $V_{DDL} = 2.5 \text{ V} \pm 5\%$ ;  $C_L = 20 \text{ pF}$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	$V_{OH2B}$	$I_{OH} = -12.0 \text{ mA}$	2	2.3		V
Output Low Voltage	$V_{OL2B}$	$I_{OL} = 12 \text{ mA}$		0.2	0.4	V
Output High Current	$I_{OH2B}$	$V_{OH} = 1.7 \text{ V}$		-41	-19	mA
Output Low Current	$I_{OL2B}$	$V_{OL} = 0.7 \text{ V}$	19	37		mA
Rise Time	$t_{r2B}^1$	$V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.0 \text{ V}$		1.25	1.6	ns
Fall Time	$t_{f2B}^1$	$V_{OH} = 2.0 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$		1	1.6	ns
Duty Cycle	$d_{t2B}^1$	$V_T = 1.25 \text{ V}$	45	48	55	%
Skew	$t_{sk2B}^1$	$V_T = 1.25 \text{ V}$		30	175	ps
Jitter, Cycle-to-cycle	$t_{jvc-cyc2B}^1$	$V_T = 1.25 \text{ V}$		150	250	ps
Jitter, One Sigma	$t_{j1s2B}^1$	$V_T = 1.25 \text{ V}$		40	150	ps
Jitter, Absolute	$t_{jabs2B}^1$	$V_T = 1.25 \text{ V}$	-250	140	+250	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - PCICLK

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 30 \text{ pF}$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	$V_{OH1}$	$I_{OH} = -11 \text{ mA}$	2.4	3.1		V
Output Low Voltage	$V_{OL1}$	$I_{OL} = 9.4 \text{ mA}$		0.1	0.4	V
Output High Current	$I_{OH1}$	$V_{OH} = 2.0 \text{ V}$		-62	-22	mA
Output Low Current	$I_{OL1}$	$V_{OL} = 0.8 \text{ V}$	16	57		mA
Rise Time <sup>1</sup>	$t_{r1}$	$V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.4 \text{ V}$		1.5	2	ns
Fall Time <sup>1</sup>	$t_{f1}$	$V_{OH} = 2.4 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$		1.1	2	ns
Duty Cycle <sup>1</sup>	$d_{t1}$	$V_T = 1.5 \text{ V}$	45	50	55	%
Skew <sup>1</sup>	$t_{sk1}$	$V_T = 1.5 \text{ V}$		140	500	ps
Jitter, One Sigma <sup>1</sup>	$t_{j1s1}$	$V_T = 1.5 \text{ V}$		17	150	ps
Jitter, Absolute <sup>1</sup>	$t_{jabs1}$	$V_T = 1.5 \text{ V}$	-500	70	500	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.

**Electrical Characteristics - IOAPIC**

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ,  $V_{DDL} = 2.5\text{ V} \pm 5\%$ ;  $C_L = 20\text{ pF}$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	$V_{OH4B}$	$I_{OH} = -18\text{ mA}$	2	2.2		V
Output Low Voltage	$V_{OL4B}$	$I_{OL} = 18\text{ mA}$		0.33	0.4	V
Output High Current	$I_{OH4B}$	$V_{OH} = 1.7\text{ V}$		-41	-28	mA
Output Low Current	$I_{OL4B}$	$V_{OL} = 0.7\text{ V}$	29	37		mA
Rise Time <sup>1</sup>	$T_{r4B}$	$V_{OL} = 0.4\text{ V}$ , $V_{OH} = 2.0\text{ V}$		1.3	1.6	ns
Fall Time <sup>1</sup>	$T_{f4B}$	$V_{OH} = 2.0\text{ V}$ , $V_{OL} = 0.4\text{ V}$		1.1	1.6	ns
Duty Cycle <sup>1</sup>	$D_{t4B}$	$V_T = 1.25\text{ V}$	45	54	55	%
Skew <sup>1</sup>	$t_{sk4B}$ <sup>1</sup>	$V_T = 1.25\text{ V}$		60	250	ps
Jitter, One Sigma <sup>1</sup>	$T_{j1s4B}$	$V_T = 1.25\text{ V}$		1	3	%
Jitter, Absolute <sup>1</sup>	$T_{jabs4B}$	$V_T = 1.25\text{ V}$	-5		5	%

<sup>1</sup>Guaranteed by design, not 100% tested in production.

**Electrical Characteristics - REF**

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 20\text{ pF}$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	$V_{OH5}$	$I_{OH} = -12\text{ mA}$	2.6	3.1		V
Output Low Voltage	$V_{OL5}$	$I_{OL} = 9\text{ mA}$		0.17	0.4	V
Output High Current	$I_{OH5}$	$V_{OH} = 2.0\text{ V}$		-44	-22	mA
Output Low Current	$I_{OL5}$	$V_{OL} = 0.8\text{ V}$	29	42		mA
Rise Time <sup>1</sup>	$t_{r5}$	$V_{OL} = 0.4\text{ V}$ , $V_{OH} = 2.4\text{ V}$		1.4	2	ns
Fall Time <sup>1</sup>	$t_{f5}$	$V_{OH} = 2.4\text{ V}$ , $V_{OL} = 0.4\text{ V}$		1.1	2	ns
Duty Cycle <sup>1</sup>	$d_{t5}$	$V_T = 1.5\text{ V}$	47	54	57	%
Jitter, One Sigma <sup>1</sup>	$t_{j1s5}$	$V_T = 1.5\text{ V}$		1	3	%
Jitter, Absolute <sup>1</sup>	$t_{jabs5}$	$V_T = 1.5\text{ V}$		3	5	%

<sup>1</sup>Guaranteed by design, not 100% tested in production.

# ICS9148-60



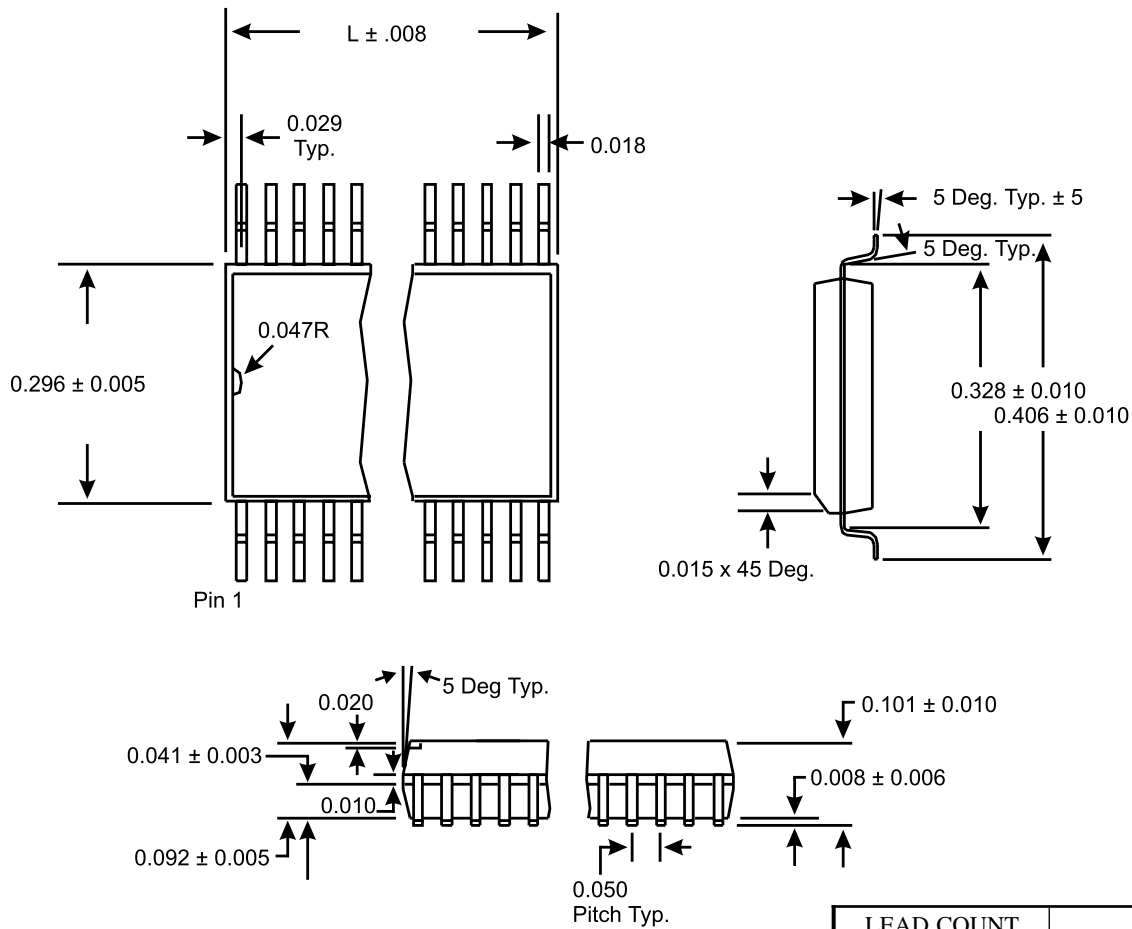
## Electrical Characteristics - 48, 24 MHz

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 20\text{ pF}$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	$V_{OH5}$	$I_{OH} = -12\text{ mA}$	2.6	3		V
Output Low Voltage	$V_{OL5}$	$I_{OL} = 9\text{ mA}$		0.14	0.4	V
Output High Current	$I_{OH5}$	$V_{OH} = 2.0\text{ V}$		-44	-22	mA
Output Low Current	$I_{OL5}$	$V_{OL} = 0.8\text{ V}$	16	42		mA
Rise Time <sup>1</sup>	$t_{r5}$	$V_{OL} = 0.4\text{ V}, V_{OH} = 2.4\text{ V}$		1.2	4	ns
Fall Time <sup>1</sup>	$t_{f5}$	$V_{OH} = 2.4\text{ V}, V_{OL} = 0.4\text{ V}$		1.2	4	ns
Duty Cycle <sup>1</sup>	$d_{t5}$	$V_T = 1.5\text{ V}$	45	52	55	%
Jitter, One Sigma <sup>1</sup>	$t_{j1s5}$	$V_T = 1.5\text{ V}$		1	3	%
Jitter, Absolute <sup>1</sup>	$t_{jabs5}$	$V_T = 1.5\text{ V}$		3	5	%

<sup>1</sup>Guaranteed by design, not 100% tested in production.





**SOIC Package**

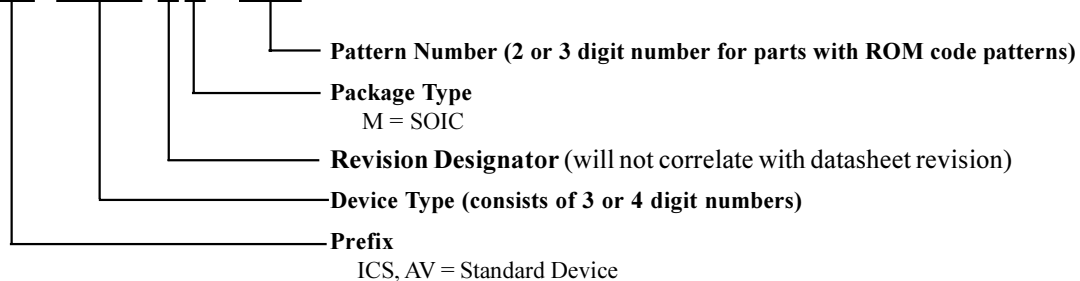
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DIMENSION L	0.704

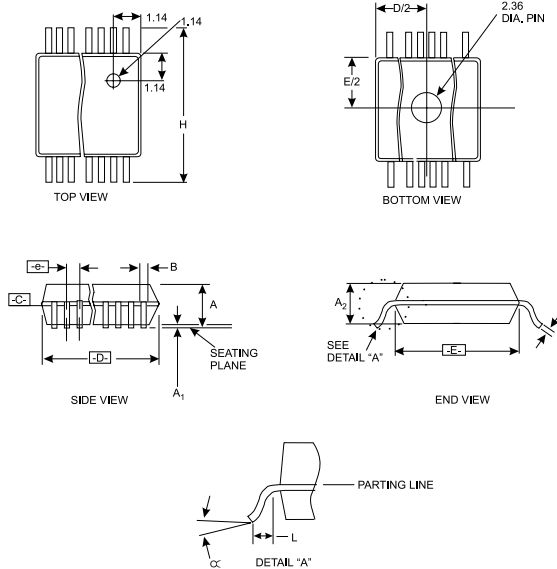
**Ordering Information**

**ICS9148yM-60**

Example:

**ICS XXXX y M - PPP**





SYMBOL	COMMON DIMENSIONS			VARIATIONS	D		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	0.068	0.073	0.078	14	0.239	0.244	0.249
A1	0.002	0.005	0.008	16	0.239	0.244	0.249
A2	0.066	0.068	0.070	20	0.278	0.284	0.289
b	0.010	0.012	0.015	24	0.318	0.323	0.328
c	0.004	0.006	0.008	28	0.397	0.402	0.407
D	See Variations			30	0.397	0.402	0.407
E	0.205	0.209	0.212	<b>SSOP Package</b> Dimensions in inches			
e	0.0256 BSC						
H	0.301	0.307	0.311				
L	0.025	0.030	0.037				
N	See Variations						
$\infty$	0°	4°	8°				

## Ordering Information

ICS9148yF-60

Example:

ICS XXXX y F - PPP

