



AMD-K7™ System Clock Chip

Recommended Application:

AMD-K7 (AMD 750, Irongate Chipset)

Output Features:

- 3 differential pair open drain CPU clocks (1.5V external pull-up; up to 150MHz achievable through I²C)
- 2 - AGPCLK @ 3.3V
- 8 - PCI @3.3V, including 1 free running
- 1 - 48MHz @ 3.3V
- 1 - 24/48MHz @ 3.3V
- 2- REF @3.3V, 14.318MHz.

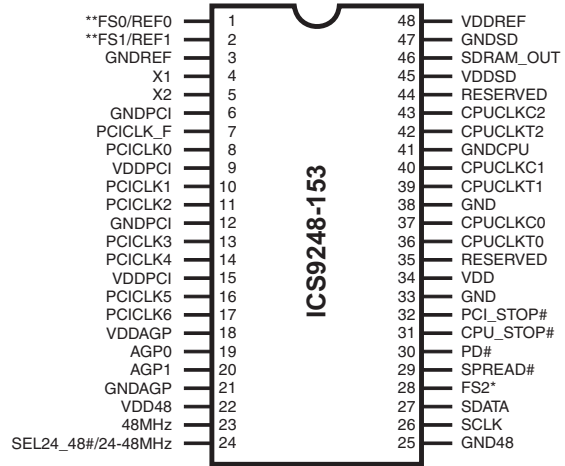
Features:

- Up to 150MHz frequency support
- Support power management: CPU, PCI, stop and Power down Mode from I²C programming.
- Spread spectrum for EMI control +/-0.25% center spread
- Uses external 14.318MHz crystal
- FS pins for frequency select

Key Specifications:

- CPU – CPU: <200ps
- AGP-AGP: <250ps
- PCI – PCI: <500ps
- CPU - SDRAM_OUT: 1250psl
- CPU-AGP: 1250psl

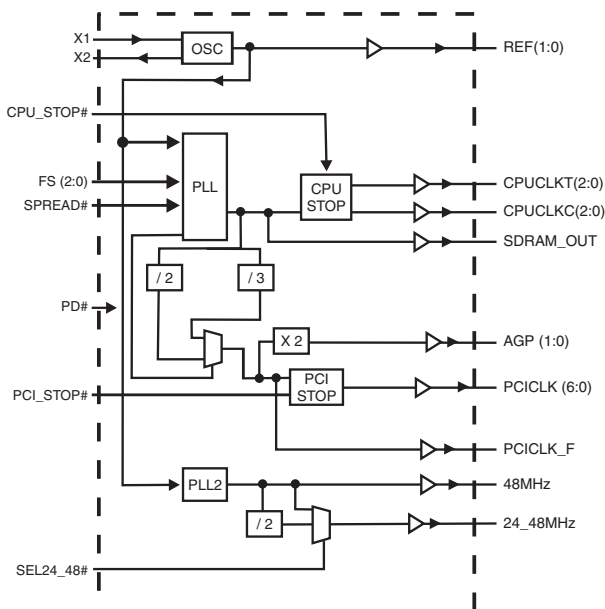
Pin Configuration



48-Pin 300mil SSOP

- * Internal 120K pullup resistor on indicated inputs
- ** Internal 240K pullup resistor on indicated inputs

Block Diagram



Functionality

| FS2 | FS1 | FS0 | CPU, SDRAM | PCI | AGP |
|-----|-----|-----|------------|-------|-------|
| 0 | 0 | 0 | 133.33 | 33.33 | 66.67 |
| 0 | 0 | 1 | 95 | 31.67 | 63.33 |
| 0 | 1 | 0 | 100.99 | 33.66 | 67.33 |
| 0 | 1 | 1 | 115 | 38.33 | 76.67 |
| 1 | 0 | 0 | 100.7 | 33.57 | 67.13 |
| 1 | 0 | 1 | 103 | 34.33 | 68.67 |
| 1 | 1 | 0 | 105 | 35.00 | 70.00 |
| 1 | 1 | 1 | 110 | 36.67 | 73.33 |

Power Groups

VDD48, GND48 = 48MHz, PLL2
 VDDREF, GNDREF= REF, X1, X2
 VDD, GND = PLL Core



Pin Descriptions

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|---------------------------------|---------------|------|---|
| 2,1 | FS (1:0) | IN | Frequency Select pins, has pull-up to VDD |
| | REF (1:0) | OUT | 14.318MHz clock output |
| 3, 6, 21, 25, 33, 38, 41, 47 | GND | PWR | Ground |
| 4 | X1 | IN | XTAL_IN 14.318MHz Crystal input, has internal 33pF load cap and feed back resistor from X2 |
| 5 | X2 | OUT | XTAL_OUT Crystal output, has internal load cap 33pF |
| 7 | PCICLK_F | OUT | Free Running PCI output. Not affected by the PCI_STOP# input. |
| 17, 16, 14, 13, 11, 10, 8 | PCICLK (6:0) | OUT | PCI clock outputs. TTL compatible 3.3V |
| 9, 15 | VDDPCI | PWR | Power for PCICLK outputs, nominally 3.3V |
| 18 | VDDAGP | PWR | Power for AGP outputs, nominally 3.3V |
| 20, 19 | AGP (1:0) | OUT | AGP outputs defined as 2X PCI. These may not be stopped. |
| 34 | VDD | PWR | Isolated power for core, nominally 3.3V |
| 22 | VDD48 | PWR | Power for 48MHz and 24MHz outputs nominally 3.3V |
| 23 | 48MHz | OUT | 48MHz output |
| 24 | SEL24-48# | IN | Selects 24 or 48MHz output for pin 24 Low = 48MHz High = 24MHz |
| | 24-48MHz | OUT | Fixed clock out selectable through SEL24-48# |
| 26 | SCLK | IN | Clock pin of I ² C circuitry 5V tolerant |
| 27 | SDATA | I/O | Data pin for I ² C circuitry 5V tolerant |
| 28 | FS2 | IN | Frequency Select pin, has pull-up to VDD |
| 29 | SPREAD# | IN | Enables Spread Spectrum feature when LOW. Center spread of +/- 0.25%. |
| 30 | PD# | IN | Powers down chip, active low. Internal PLL & all outputs are disabled. |
| 31 | CPU_STOP# | IN | Halts CPUCLKs. CPUCLKT is driven LOW whereas CPUCLKC is driven HIGH when this pin is asserted (Active LOW). |
| 32 | PCI_STOP# | IN | Halts PCI Bus at logic "0" level when driven low. PCICLK_F is not affected by this pin |
| 46 | SDRAM_OUT | OUT | Reference clock for SDRAM zero delay buffer |
| 35, 44 | RESERVED | N/C | Future CPU power rail |
| 42, 39, 36 | CPUCLKT (2:0) | OUT | "True" clocks of differential pair CPU outputs. These open drain outputs need an external 1.5V pull-up. |
| 43, 40, 37 | CPUCLKC (2:0) | OUT | "Complementary" clocks of differential pair CPU output. These open drain outputs need an external 1.5V pull_up. |
| 45 | VDDSD | PWR | Power for SDRAM_OUT pin. Nominally 3.3V |
| 48 | VDDREF | PWR | Power for REF, X1, X2, nominally 3.3V |



I²C Command Bitmaps

Byte 6: SDRAM Clock & Generator Mode Control Register

| Bit | Description | | | | | | | | PWD |
|-----|---|-------|--------------|--------------|--------------|---------------|-------|-------|----------------|
| 7 | Spread Spectrum enable (+/- 0.25% center spread) 0=OFF 1=ON | | | | | | | | 0 |
| 6:2 | Bit 3 | Bit 2 | FS2 Bit 6 | FS1 Bit 5 | FS0 Bit 4 | CPU, SDRAM | PCI | AGP | 01000 Note1 |
| | 0 | 0 | 0 | 0 | 0 | 133.33 | 33.33 | 66.67 | |
| | 0 | 0 | 0 | 0 | 1 | 95 | 31.67 | 63.33 | |
| | 0 | 0 | 0 | 1 | 0 | 100.99 | 33.66 | 67.33 | |
| | 0 | 0 | 0 | 1 | 1 | 115 | 38.33 | 76.67 | |
| | 0 | 0 | 1 | 0 | 0 | 100.7 | 33.57 | 67.13 | |
| | 0 | 0 | 1 | 0 | 1 | 103 | 34.33 | 68.67 | |
| | 0 | 0 | 1 | 1 | 0 | 105 | 35.00 | 70.00 | |
| | 0 | 0 | 1 | 1 | 1 | 110 | 36.67 | 73.33 | |
| | 0 | 1 | 0 | 0 | 0 | 102 | 34.00 | 68.00 | |
| | 0 | 1 | 0 | 0 | 1 | 104 | 34.67 | 69.33 | |
| | 0 | 1 | 0 | 1 | 0 | 106 | 35.33 | 70.67 | |
| | 0 | 1 | 0 | 1 | 1 | 107 | 35.67 | 71.33 | |
| | 0 | 1 | 1 | 0 | 0 | 108 | 36.00 | 72.00 | |
| | 0 | 1 | 1 | 0 | 1 | 109 | 36.33 | 72.67 | |
| | 0 | 1 | 1 | 1 | 0 | 90 | 30.00 | 60.00 | |
| | 0 | 1 | 1 | 1 | 1 | 111 | 37.00 | 74.00 | |
| | 1 | 0 | 0 | 0 | 0 | 112 | 37.33 | 74.67 | |
| | 1 | 0 | 0 | 0 | 1 | 113 | 37.67 | 75.33 | |
| | 1 | 0 | 0 | 1 | 0 | 114 | 38.00 | 76.00 | |
| | 1 | 0 | 0 | 1 | 1 | 116 | 38.67 | 77.33 | |
| | 1 | 0 | 1 | 0 | 0 | 117 | 39.00 | 78.00 | |
| | 1 | 0 | 1 | 0 | 1 | 118 | 39.33 | 78.67 | |
| | 1 | 0 | 1 | 1 | 0 | 119 | 39.67 | 79.33 | |
| | 1 | 0 | 1 | 1 | 1 | 120 | 30.00 | 60.00 | |
| | 1 | 1 | 0 | 0 | 0 | 142 | 35.50 | 71.00 | |
| | 1 | 1 | 0 | 0 | 1 | 144 | 36.00 | 72.00 | |
| | 1 | 1 | 0 | 1 | 0 | 146 | 36.50 | 73.00 | |
| 1 | 1 | 0 | 1 | 1 | 138 | 34.50 | 69.00 | | |
| 1 | 1 | 1 | 0 | 0 | 136 | 34.00 | 68.00 | | |
| 1 | 1 | 1 | 0 | 1 | 135 | 33.75 | 67.50 | | |
| 1 | 1 | 1 | 1 | 0 | 140 | 35.00 | 70.00 | | |
| 1 | 1 | 1 | 1 | 1 | 150 | 37.50 | 75.00 | | |
| 1 | 0 - Frequency is selected by hardware select, latched input; Spread controlled by pin 29 1 - Frequency is selected by Bit (6:2); Spread controlled by Bit 7 | | | | | | | | 0 |
| 0 | 0 - SDRAM_OUT Disable 1 - SDRAM_OUT Enable | | | | | | | | 1 |

Notes:

1. Default at power-up will be latched logic inputs to define frequency, as displayed by Bit 1.
2. PWD = Power-Up Default



I²C Command Bitmaps

Byte 4: Clock Control Register

| Bit | Pin# | Default | Description |
|-----|--------|---------|--|
| 7 | 1 | 1 | REF0 enable |
| 6 | 24 | 1 | 24MHz/48MHz enable |
| 5 | 23 | 1 | 48MHz enable |
| 4 | 20 | 1 | AGP1 enable |
| 3 | 19 | 1 | AGP0 enable |
| 2 | 42, 43 | 1 | CPUCLK2 enable (both of differential pair, True" and "Complimentary" |
| 1 | 39, 40 | 1 | CPUCLK1 enable (both of differential pair, True" and "Complimentary" |
| 0 | 36, 37 | 1 | CPUCLK0 enable (both of differential pair, True" and "Complimentary" |

Notes: A value of '1' is enable, '0' is disable

Byte 5: PCI Clock Control Register

| Bit | Pin# | Default | Description |
|-----|------|---------|----------------|
| 7 | 2 | 1 | REF1 enable |
| 6 | 17 | 1 | PCICLK6 enable |
| 5 | 16 | 1 | PCICLK5 enable |
| 4 | 14 | 1 | PCICLK4 enable |
| 3 | 13 | 1 | PCICLK3 enable |
| 2 | 11 | 1 | PCICLK2 enable |
| 1 | 10 | 1 | PCICLK1 enable |
| 0 | 8 | 1 | PCICLK0 enable |

Notes: A value of '1' is enable, '0' is disable



Absolute Maximum Ratings

Supply Voltage 5.5 V
 Logic Inputs GND -0.5 V to V_{DD} +0.5 V
 Ambient Operating Temperature 0°C to +70°C
 Storage Temperature -65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-------------------------|--|----------------------|--------|----------------------|-------|
| Input High Voltage | V _{IH} | | 2 | | V _{DD} +0.3 | V |
| Input Low Voltage | V _{IL} | | V _{SS} -0.3 | | 0.8 | V |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | | | 5 | μA |
| Input Low Current | I _{IL1} | V _{IN} = 0V; Inputs with no pull-up resistors | -5 | | | μA |
| Input Low Current | I _{IL2} | V _{IN} = 0V; Inputs with pull-up resistors | -200 | | | μA |
| Operating Supply Current | I _{DD3.3OP100} | C _L = 0 pF; Select @ 100 MHz | | | 180 | mA |
| | I _{DD3.3OP133} | C _L = 0 pF; Select @ 133 MHz | | | 180 | mA |
| Powerdown Current | I _{DD3.3PD} | C _L = 0 pF; Input address to VDD or GND | | | 600 | μA |
| Input Frequency | F _i | V _{DD} = 3.3 V | 12 | 14.318 | 16 | MHz |
| Input Capacitance ¹ | C _{IN} | Logic Inputs | | | 5 | pF |
| | C _{INX} | X1 & X2 pins | 27 | | 45 | pF |
| Clk Stabilization ¹ | T _{STAB} | From V _{DD} = 3.3 V to 1% target frequency | | | 3 | ms |
| Skew ¹ | T _{CPU-SDRAM} | V _T = 50%, CPU=100MHz | -250 | -210 | | ps |
| | T _{CPU-AGP} | V _T = 50%, CPU=100MHz | -250 | 0 | | ps |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - USB, REF

$T_A = 0 - 70^\circ \text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $C_L = 20 \text{ pF}$ (unless otherwise stated).

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|---------------------------------|---|-----|------|------|-------|
| Output High Voltage | V_{OH5} | $I_{OH} = -12 \text{ mA}$ | 2.4 | | | V |
| Output Low Voltage | V_{OL5} | $I_{OL} = 9 \text{ mA}$ | | | 0.4 | V |
| Output High Current | I_{OH5} | $V_{OH} = 2.0 \text{ V}$ | | | -22 | mA |
| Output Low Current | I_{OL5} | $V_{OL} = 0.8 \text{ V}$ | 16 | | | mA |
| Rise Time | t_{r5}^1 | $V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.4 \text{ V}$ | | 2.28 | 4 | ns |
| Fall Time | t_{f5}^1 | $V_{OH} = 2.4 \text{ V}$, $V_{OL} = 0.4 \text{ V}$ | | 2.28 | 4 | ns |
| Duty Cycle | d_5^1 | $V_T = 50\%$ | 45 | 52.5 | 55 | % |
| Jitter, Cycle-to-Cycle, REF | $t_{j\text{cyc-cyc5, REF}}^1$ | $V_T = 50\%$ | | 402 | 1000 | ps |
| Jitter, Cycle-to-Cycle, fixed clock | $t_{j\text{cyc-cyc5, fixed}}^1$ | $V_T = 50\%$ | | 248 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK (Open Drain)

$T_A = 0 - 70^\circ \text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $C_L = 20 \text{ pF}$ (unless otherwise stated).

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|---------------------------|--|------|------|---------------------------------------|----------|
| Output Impedance | Z_O^1 | $V_O = V_X$ | | | 60 | Ω |
| Output High Voltage | V_{OH2B} | Termination to $V_{\text{pull-up (external)}}$ | 1 | | 1.2 | V |
| Output Low Voltage | V_{OL2B} | Termination to $V_{\text{pull-up (external)}}$ | | | 0.4 | V |
| Output Low Current | I_{OL2B} | $V_{OL} = 0.3 \text{ V}$ | 18 | | | mA |
| Rise Time | t_{r2B}^1 | $V_{OL} = 20\%$, $V_{OH} = 80\%$ | | 2.4 | 2.6 | ns |
| Fall Time | t_{f2B}^1 | $V_{OH} = 80\%$, $V_{OL} = 20\%$ | | 1.2 | 2.6 | ns |
| Duty Cycle | d_{t2B}^1 | $V_T = 50\%$ | 42 | 45.4 | 52 | % |
| Differential Voltage-AC | V_{DIF}^1 | Note 2 | 0.4 | 1.03 | $V_{\text{pull-up (external)}} + 0.6$ | V |
| Differential Voltage-DC | V_{DIF}^1 | Note 2 | 0.2 | | $V_{\text{pull-up (external)}} + 0.6$ | V |
| Differential Crossover Voltage | V_X^1 | Note 3 | 400 | 412 | 950 | mV |
| Skew | t_{sk2B}^1 | $V_T = 50\%$ | | 55 | 200 | ps |
| Jitter, Absolute | t_{jabs2B}^1 | $V_T = 50\%$ | -250 | 120 | +250 | ps |
| Jitter, Cycle-to-cycle | $t_{j\text{cyc-cyc2B}}^1$ | $V_T = V_X$ | | 99 | 250 | ps |

Notes:

- 1 - Guaranteed by design, not 100% tested in production.
- 2 - V_{DIF} specifies the minimum input differential voltages ($V_{TR} - V_{CP}$) required for switching, where V_{TR} is the "true" input level and V_{CP} is the "complement" input level.
- 3 - $V_{\text{pull-up(external)}} = 1.5\text{V}$, $\text{Min} = (V_{\text{pull-up(external)}}/2) - 150\text{mV}$; $\text{Max} = (V_{\text{pull-up(external)}}/2) + 150\text{mV}$



Electrical Characteristics - PCICLK

T_A = 0 - 70° C; V_{DD} = 3.3 V +/- 5%, C_L = 30 pF (unless otherwise stated).

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|-----------------------------------|--|-----|------|-----|-------|
| Output High Voltage | V _{OH1} | I _{OH} = -11 mA | 2.6 | | | V |
| Output Low Voltage | V _{OL1} | I _{OL} = 9.4 mA | | | 0.4 | V |
| Output High Current | I _{OH1} | V _{OH} = 2.0 V | | | -16 | mA |
| Output Low Current | I _{OL1} | V _{OL} = 0.8 V | 19 | | | mA |
| Rise Time | t _{r1} ¹ | V _{OL} = 0.4 V, V _{OH} = 2.4 V | | 1.56 | 2 | ns |
| Fall Time | t _{f1} ¹ | V _{OH} = 2.4V, V _{OL} = 0.4 V | | 1.56 | 2 | ns |
| Duty Cycle | d _u ¹ | V _T = 50% | 45 | 51.3 | 55 | % |
| Skew (window) | t _{sk1} ¹ | V _T = 50% | | 320 | 500 | ps |
| Jitter, Cycle-to-Cycle | t _{jyc-cyc} ¹ | V _T = 50% | | 88 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK_F

T_A = 0 - 70° C; V_{DD} = 3.3 V +/- 5%, C_L = 30 pF (unless otherwise stated).

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|-----------------------------------|--|-----|------|-----|-------|
| Output High Voltage | V _{OH1} | I _{OH} = -11 mA | 2.6 | | | V |
| Output Low Voltage | V _{OL1} | I _{OL} = 9.4 mA | | | 0.4 | V |
| Output High Current | I _{OH1} | V _{OH} = 2.0 V | | | -12 | mA |
| Output Low Current | I _{OL1} | V _{OL} = 0.8 V | 12 | | | mA |
| Rise Time | t _{r1} ¹ | V _{OL} = 0.4 V, V _{OH} = 2.4 V | | 1.56 | 2 | ns |
| Fall Time | t _{f1} ¹ | V _{OH} = 2.4V, V _{OL} = 0.4 V | | 1.56 | 2 | ns |
| Duty Cycle | d _u ¹ | V _T = 50% | 45 | 51.3 | 55 | % |
| Jitter, Cycle-to-Cycle | t _{jyc-cyc} ¹ | V _T = 50% | | 88 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - AGP

$T_A = 0 - 70^\circ \text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$, $C_L = 20 \text{ pF}$ (unless otherwise stated).

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|-------------------|---|-----|------|-----|-------|
| Output High Voltage | V_{OH4B} | $I_{OH} = -18 \text{ mA}$ | 2 | | | V |
| Output Low Voltage | V_{OL4B} | $I_{OL} = 18 \text{ mA}$ | | | 0.4 | V |
| Output High Current | I_{OH4B} | $V_{OH} = 2.0 \text{ V}$ | | | -19 | mA |
| Output Low Current | I_{OL4B} | $V_{OL} = 0.8 \text{ V}$ | 19 | | | mA |
| Rise Time | t_{r4B}^1 | $V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.4 \text{ V}$ | | 1.27 | 2 | ns |
| Fall Time | t_{f4B}^1 | $V_{OH} = 2.4 \text{ V}$, $V_{OL} = 0.4 \text{ V}$ | | 1.10 | 2 | ns |
| Duty Cycle | d_{t4B}^1 | $V_T = 50\%$ | 45 | 50.6 | 55 | % |
| Skew (window) | t_{sk4B}^1 | $V_T = 50\%$ | | 30 | 250 | ps |
| Jitter, Cycle-to-Cycle | $t_{jyc-cyc4B}^1$ | $V_T = 50\%$ | | 272 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM_OUT

$T_A = 0 - 70^\circ \text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$, $C_L = 30 \text{ pF}$ (unless otherwise stated).

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|------------------|---|-----|------|-----|-------|
| Output High Voltage | V_{OH3} | $I_{OH} = -11 \text{ mA}$ | 2 | | | V |
| Output Low Voltage | V_{OL3} | $I_{OL} = 11 \text{ mA}$ | | | 0.4 | V |
| Output High Current | I_{OH3} | $V_{OH} = 2.0 \text{ V}$ | | | -12 | mA |
| Output Low Current | I_{OL3} | $V_{OL} = 0.8 \text{ V}$ | 12 | | | mA |
| Rise Time | t_{r3}^1 | $V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.4 \text{ V}$ | | 0.90 | 2.2 | ns |
| Fall Time | t_{f3}^1 | $V_{OH} = 2.4 \text{ V}$, $V_{OL} = 0.4 \text{ V}$ | | 0.77 | 2.2 | ns |
| Duty Cycle | d_{t3}^1 | $V_T = 50\%$ | 45 | 52 | 55 | % |
| Jitter, Cycle-to-Cycle | $t_{jyc-cyc3}^1$ | $V_T = 50\%$ | | 89 | 250 | ps |

¹Guaranteed by design, not 100% tested in production.



General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will **acknowledge** each byte **one at a time**.
- Controller (host) sends a Stop bit

| How to Write: | |
|---------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D2 _(H) | |
| | ACK |
| Dummy Command Code | |
| | ACK |
| Dummy Byte Count | |
| | ACK |
| Byte 0 | |
| | ACK |
| Byte 1 | |
| | ACK |
| Byte 2 | |
| | ACK |
| Byte 3 | |
| | ACK |
| Byte 4 | |
| | ACK |
| Byte 5 | |
| | ACK |
| Stop Bit | |

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 5**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

| How to Read: | |
|---------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D3 _(H) | |
| | ACK |
| | Byte Count |
| ACK | |
| | Byte 0 |
| ACK | |
| | Byte 1 |
| ACK | |
| | Byte 2 |
| ACK | |
| | Byte 3 |
| ACK | |
| | Byte 4 |
| ACK | |
| | Byte 5 |
| ACK | |
| Stop Bit | |

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9248-153 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

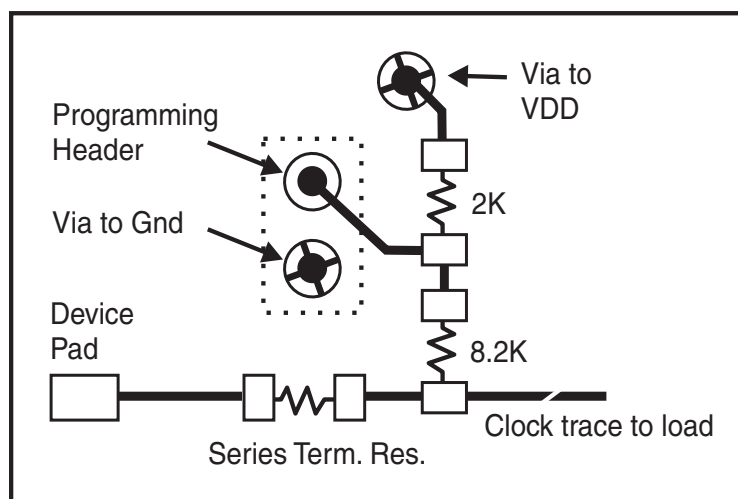


Fig. 1



General Description

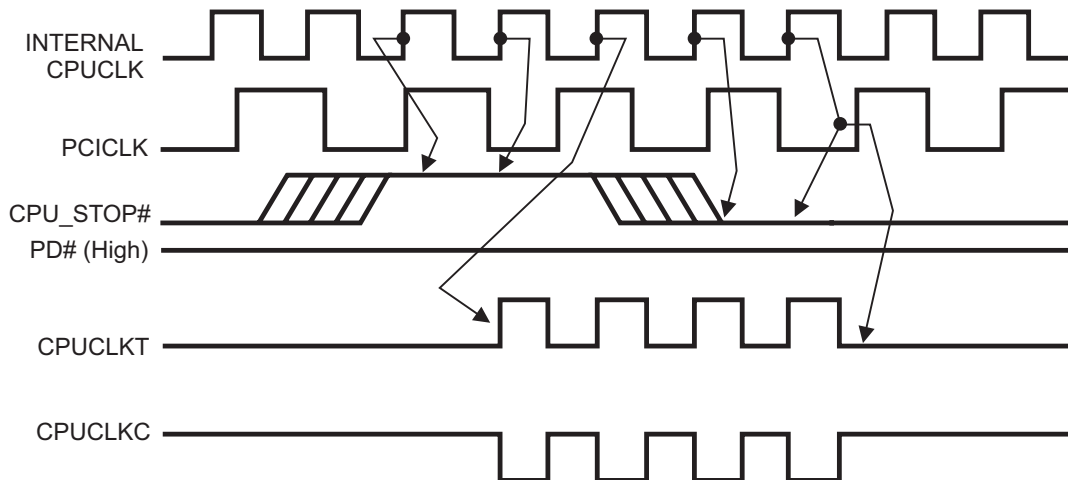
The **ICS9248-153** is a main clock synthesizer chip for AMD-K7 based systems. This provides all clocks required for such a system when used with a Zero Delay Buffer Chip such as the ICS9179-06.

Spread spectrum may be enabled through I²C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9248-153 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I²C interface allows changing functions, stop clock programming and frequency selection.

CPU_STOP# Timing Diagram

CPU_STOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the **ICS9248-153**. All other clocks will continue to run while the CPUCLKs clocks are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.



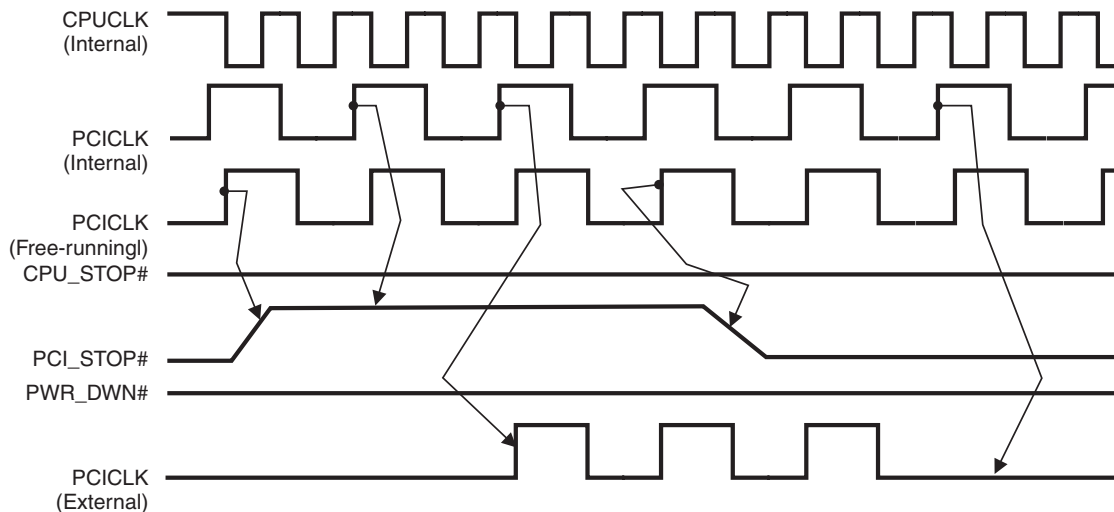
Notes:

1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS9248-153**.
3. All other clocks continue to run undisturbed.
4. PD# and PCI_STOP# are shown in a high (true) state.



PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9248-153**. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI_STOP# is synchronized by the **ICS9248-153** internally. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:

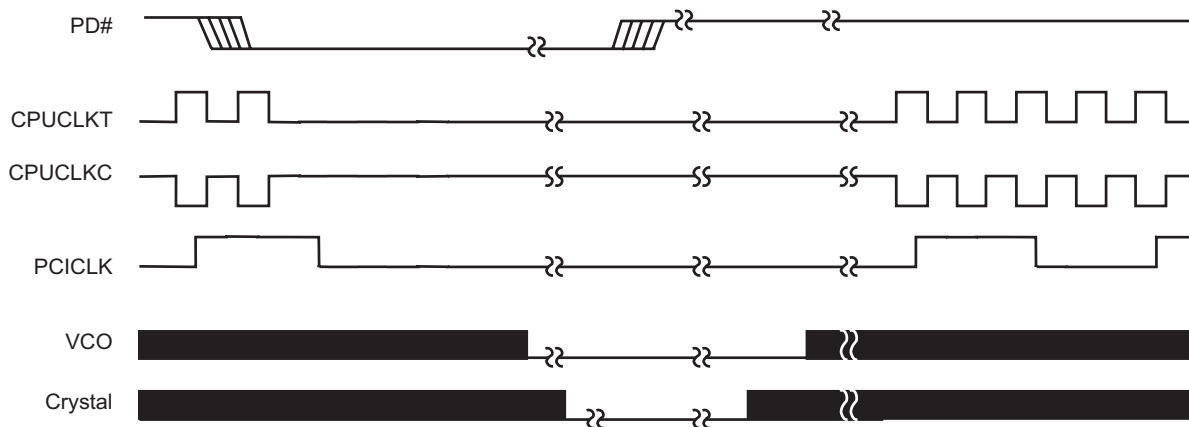
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248.
3. All other clocks continue to run undisturbed.
4. PD# and CPU_STOP# are shown in a high (true) state.



PD# Timing Diagram

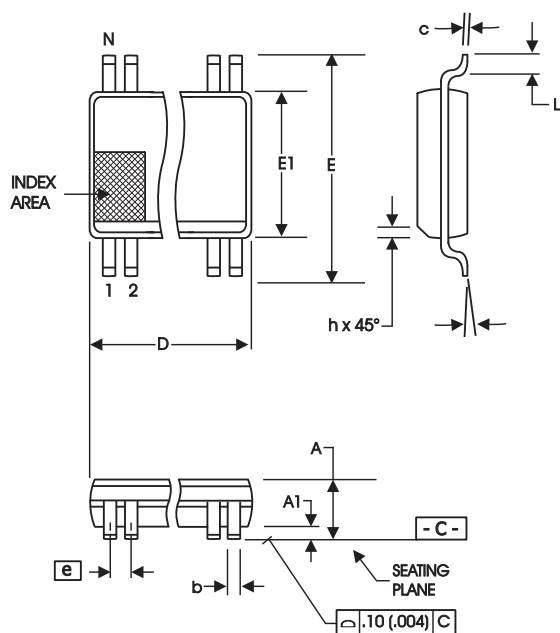
The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248-153 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.



300 mil SSOP Package

| SYMBOL | In Millimeters | | In Inches | |
|----------|-------------------|-------------------|-------------------|-------------------|
| | COMMON DIMENSIONS | COMMON DIMENSIONS | COMMON DIMENSIONS | COMMON DIMENSIONS |
| A | 2.41 | 2.80 | .095 | .110 |
| A1 | 0.20 | 0.40 | .008 | .016 |
| b | 0.20 | 0.34 | .008 | .0135 |
| c | 0.13 | 0.25 | .005 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 10.03 | 10.68 | .395 | .420 |
| E1 | 7.40 | 7.60 | .291 | .299 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| h | 0.38 | 0.64 | .015 | .025 |
| L | 0.50 | 1.02 | .020 | .040 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |

VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| 48 | 15.75 | 16.00 | .620 | .630 |

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS9248yF-153-T

Example:

ICS XXXX y F - PPP - T

